Practical Homework set 3

(These problems should be done individually, not with project partner)

Due –As indicated on Canvas

I: Getting Started with the Altera Cyclone V SoC and Linux

1. If you have not already done this, download and install the Quartus FPGA development software. Follow the directions in the **"DE1-SoC Getting Started Guide"** from Terasic on Canvas starting with section 2.3 on page 7. This document is on Canvas.

2. Follow the instructions in chapter 3 of the guide to setup and test the DE1-SoC board.

3. Follow the instructions in chapter 4 of the guide to create an FPGA image for the DE1-SoC board and test it.

4. Follow the instructions in chapter 5 of the guide to create a Linux SD card image for the DE1-SoC board and test it using a USB serial port connection. You will need to provide an **8GB microSD card** for this part.

5. Follow the instructions in chapter 6 of the guide to create a Linux LXDE Boot SD card image for the DE1-SoC board and test it using a VGA monitor. You should get Linux images from Canvas or from https://www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=205&No=836&PartNo=4#contents .

*********You may use monitors in the lab for this purpose or one of you own. **VGA cables or adapters may be required.** They are available in a lab cabinet, ask the TAs for access. You will need to provide an **8 GB microSD card** for this part of the project. You may reuse the one from step 4********.*

6. Answer these questions:

a. In #2, did your LED turn on? Show a picture to verify.

b. In #3, Estimate the % utilization of the FPGA logic.

c. Record your observations of the board behavior once the FPGA is programmed in #3. Does it behave as you expected?

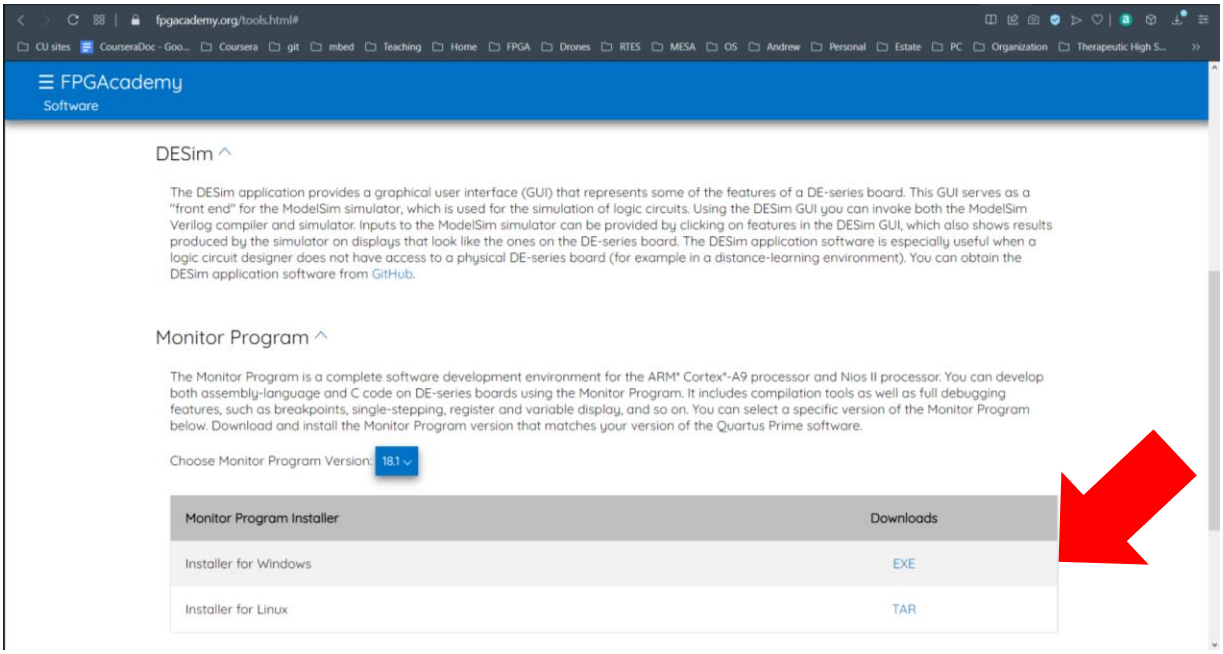
d. The main traditional connection to a Linux System is through a terminal. Where you able to get a terminal connected? If so, list the directories found in root.

e. In step 5, were you able to find the mp4 video and play it?

II: Embedded Development on an SoC

(**Start Early)

1. Download and install the Altera Monitor Program, an alternative to the EDS suite should you have licensing problems, found here: https://www.intel.com/content/www/us/en/programmable/support/training/university/materials-software.html#Monitor-Program or https://fpgacademy.org/tools.html and download the University program installer towards the bottom of the page:



2. Download and follow the directions in the lab1.pdf found in Canvas. Also download the source files found in lab1_design_files.zip.

3. How is this development process different from software development on a standard ARM Microprocessor?

4. When you stop the program, what value is in the program counter?

Grading Rubric

1) - [10 points]
    [2 pt] a, b
    [4 pt] c,d
    [4 pt] e
    Screenshots for all observations

2) - [10 points]
    [4 pt] Code
    [4 pt] Implementation
    [2 pt] Observations
    Screenshots for all observations