Q1)
Using the equation shown in figure 1, I calculated the MTBF as:

A) MTBF = e^(C2*Tmet)/(C1*f_d*f_c)
= e^(1.57x10^10 * 0) / (9.11x10^-12 * 10 MHz * 50 MHz)
= 1/(4555)
= 219.5x10^-6
B) MTBF = e^(C2*Tmet)/(C1*f_d*f_c)
= e^(1.57x10^10 * 0) / (9.11x10^-12 * 1 MHz * 10 MHz)
= 1/(91.1)
= 11.0x10^-3

Q2)

A) I used the same counter.v file from the project 3, lab 5 section and I wrapped a top level module around it. I was then able to create constraints on my design, and I set the clock frequency to 50 MHz and the input/output delay to 1 ns. This resulted in an fMax of 403.877, as shown in figure 2. I ran a timing simulation, as shown in figure 3. The timing simulation showed that there were no glitches between 0 and 64 on a 50 MHz clock.
B) Using a for loop and some synthesis directives, I was able to create the chain of inverters for the clock.
C) The fMax for this design was 134.698 MHz, which is significantly lower than the 403 MHz that was observed earlier. Clearly adding in clock skew required the clock frequency to go down, since there is now a longer critical path, meaning that it can't run as quickly. This fMax is shown in figure 4. When running a simulation, many glitches were observed, as shown in figure 5. I counted a total of 33 glitches. A zoomed in screenshot of an individual glitch is shown in figure 6.

Q3)

A) In order to compute the values for the setup required and arrival time, I needed to use SmartTime maximum delay analysis so that I could see the routing delays for the various signals. In looking at the path for the most significant digit, I was able to find the different delays that are used to compute the data arrival time, as shown in figure 7. Adding all of these delays up resulted in a data arrival time of 5.904ns. A similar process was performed for the required time, and the least significant bit. Here are the results:
MSB arrival time: 5.904ns (fig 7)
MSB required time: 22.296ns (fig 8)
LSB arrival time: 5.531 ns (fig 9)
LSB required time: 22.144 (fig 10)

For the hold time, I looked at the SmartTime minimum delay analysis to find the different delays. The results are listed below:
MSB arrival time: 2.111ns (fig 11)
MSB required time: 1.581ns (fig 12)
LSB arrival time: 2.048 ns (fig 13)

LSB required time: 1.589 (fig 14)

B) Running SmartTime results in an fMax of 240.848 MHz, as shown in figure 15.
C) To increase the fMax, I can change some of the constraints, which would result in a better frequency. I lowered the input delay and increased output delay to help with this. I also removed any unnecessary paths in the design to minimize potentially slow critical paths. This design work as a whole resulted in a new fMax of 338.066 MHz, as shown in figure 16.

Like other FPGA manufacturers, to absorb the fixed value the of e^{Tco} term, Microsemi simplifies EQ 20-9 on page 412 to the following form:

$$MTBF = e^{C2 * Tmet} / (C1 \times f_d \times f_c)$$

EQ 20-10

where C2 is a constant inversely proportional to the metastability decay constant, and C1 is the proportionality constant, which is similar to aperture.

Fig 1. A screenshot from the ProASIC user manual showing the equation for MTBF.

Clock Domain	Period (ns)	Frequency (MHz)	Required Period (ns)	Required Frequency (MHz)	External Setup (ns)	Max Clock-To-Out (ns)
clk	2.476	403.877	20.000	50.000	N/A	8.408

Fig 2. A screenshot of Libera showing the maximum clock frequency.

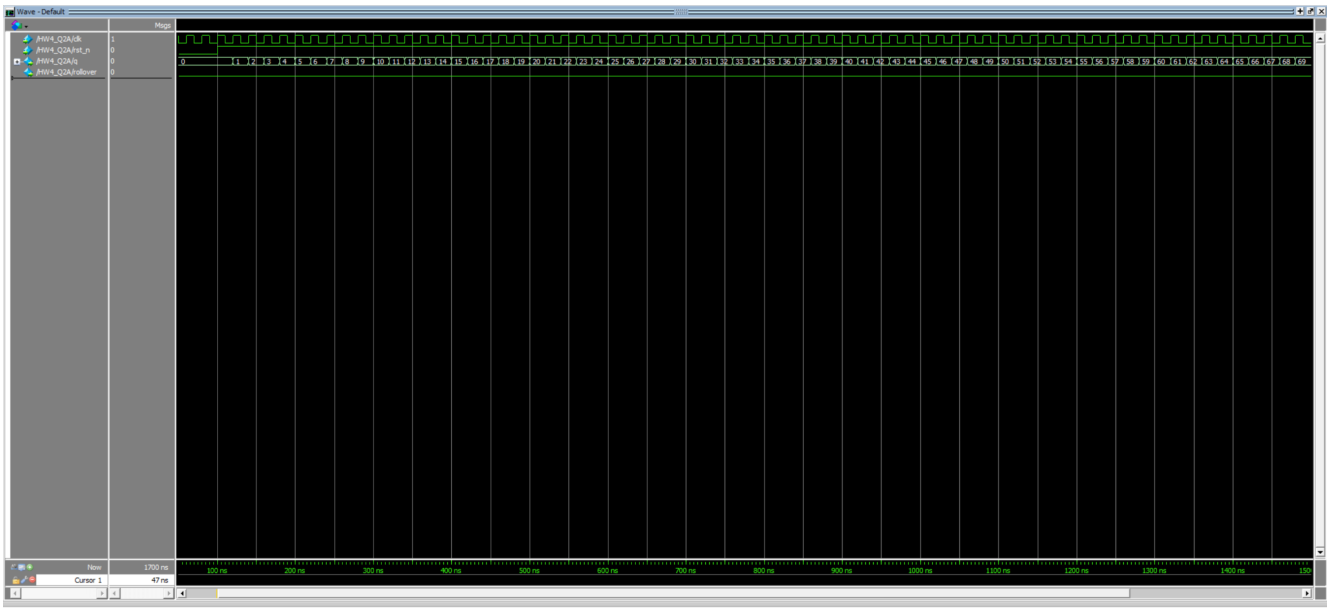

Fig 3. A timing simulation of the design counting up to 64.

Clock Domain	Period (ns)	Frequency (MHz)	Required Period (ns)	Required Frequency (MHz)	External Setup (ns)	Max Clock-To-Out (ns)
clk	7.424	134.698	N/A	N/A	N/A	8.518

Fig 4. A screenshot showing the fMax for a design with skewed clocks.

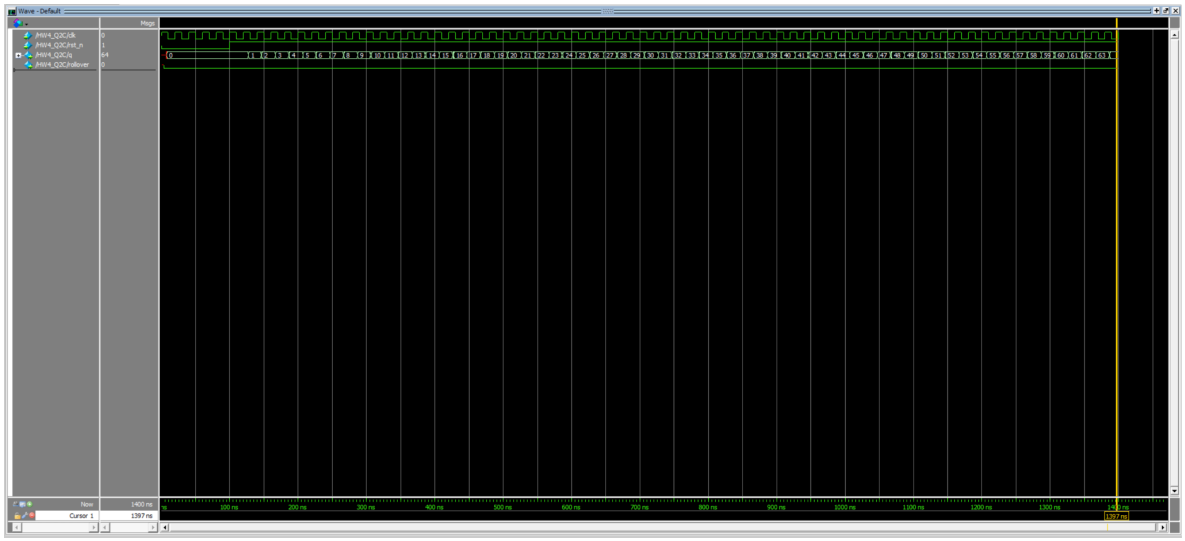

Fig 5. A screenshot of the skewed design in modelsim counting up to 64.

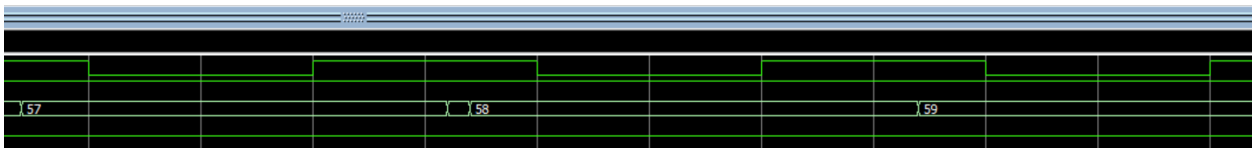

Fig 6. A screenshot showing a single glitch between 57 and 58 (briefly went to 59).

Data_arrival_time_calculation							
clk					0.000	0.000	
clk	Clock source			+	0.000	0.000	r
clk_ibuf/U0/U_IOPAD:PAD	net	clk		+	0.000	0.000	r
clk_ibuf/U0/U_IOPAD:Y	cell		ADLIB:IOPAD_IN	+	1.273	1.273	2 r
clk_ibuf_RNIVTI2:An	net	clk_ibuf_Z		+	0.054	1.327	f
clk_ibuf_RNIVTI2:YSn	cell		ADLIB:GB	+	0.085	1.412	5 f
clk_ibuf_RNIVTI2/U0_RGB1_RGB1:An	net	clk_ibuf_RNIVTI2/U0_YNn_GSouth		+	0.288	1.700	f
clk_ibuf_RNIVTI2/U0_RGB1_RGB1:YL	cell		ADLIB:RGB	+	0.251	1.951	20 r
Q[22]:CLK	net	clk_ibuf_RNIVTI2/U0_RGB1_RGB1_rgbl_net_1		+	0.496	2.447	r
Q[22]:Q	cell		ADLIB:SLE	+	0.108	2.555	3 f
Rollover5_13:A	net	q_c[22]		+	0.612	3.167	f
Rollover5_13:Y	cell		ADLIB:CFG4	+	0.179	3.346	1 f
Rollover5_21:C	net	Rollover5_13_Z		+	0.630	3.976	f
Rollover5_21:Y	cell		ADLIB:CFG4	+	0.179	4.155	1 f
Rollover5:C	net	Rollover5_21_Z		+	0.224	4.379	f
Rollover5:Y	cell		ADLIB:CFG3	+	0.198	4.577	1 f
Rollover:Dn	net	Rollover5_Z		+	1.327	5.904	r
data arrival time						5.904	

Fig 7. All of the delays provided by SmartTime for the MSB arrival setup time.

Data_required_time_calculation							
clk	Clock Constraint				20.000	20.000	
clk	Clock source			+	0.000	20.000	r
clk_ibuf/U0/U_IOPAD:PAD	net	clk		+	0.000	20.000	r
clk_ibuf/U0/U_IOPAD:Y	cell		ADLIB:IOPAD_IN	+	1.273	21.273	2 r
clk_ibuf_RNIVTI2:An	net	clk_ibuf_Z		+	0.054	21.327	f
clk_ibuf_RNIVTI2:YSn	cell		ADLIB:GB	+	0.085	21.412	5 f
clk_ibuf_RNIVTI2/U0_RGB1_RGB3:An	net	clk_ibuf_RNIVTI2/U0_YNn_GSouth		+	0.289	21.701	f
clk_ibuf_RNIVTI2/U0_RGB1_RGB3:YL	cell		ADLIB:RGB	+	0.251	21.952	1 r
Rollover:CLK	net	clk_ibuf_RNIVTI2/U0_RGB1_RGB3_rgbl_net_1		+	0.503	22.455	r
Rollover:Dn	Library setup time		ADLIB:IOOEFF	-	0.159	22.296	
data required time						22.296	

Fig 8. All of the delays provided by SmartTime for the MSB required setup time.

Data_arrival_time_calculation							
clk					0.000	0.000	
clk	Clock source			+	0.000	0.000	r
clk_ibuf/U0/U_IOPAD:PAD	net	clk		+	0.000	0.000	r
clk_ibuf/U0/U_IOPAD:Y	cell		ADLIB:IOPAD_IN	+	1.273	1.273	2 r
clk_ibuf_RNIVTI2:An	net	clk_ibuf_Z		+	0.054	1.327	f
clk_ibuf_RNIVTI2:YSn	cell		ADLIB:GB	+	0.085	1.412	5 f
clk_ibuf_RNIVTI2/U0_RGB1_RGB2:An	net	clk_ibuf_RNIVTI2/U0_YNn_GSouth		+	0.289	1.701	f
clk_ibuf_RNIVTI2/U0_RGB1_RGB2:YL	cell		ADLIB:RGB	+	0.251	1.952	1 r
Q[0]:CLK	net	clk_ibuf_RNIVTI2/U0_RGB1_RGB2_rgbl_net_1		+	0.460	2.412	r
Q[0]:Q	cell		ADLIB:SLE	+	0.110	2.522	4 f
Q_s_1:B	net	q_c[0]		+	0.665	3.187	f
Q_s_1:P	cell		ADLIB:ARI1_CC	+	0.200	3.387	1 f
Q_s_1_CC_0:P[0]	net	NET_CC_CONFIG3		+	0.000	3.387	f
Q_s_1_CC_0:CO	cell		ADLIB:CC_CONFIG	+	0.573	3.960	1 r
Q_s_1_CC_1:CI	net	CI_TO_CO2		+	0.000	3.960	r
Q_s_1_CC_1:CC[11]	cell		ADLIB:CC_CONFIG	+	0.401	4.361	1 r
Q_s[23]:CC	net	NET_CC_CONFIG74		+	0.000	4.361	r
Q_s[23]:S	cell		ADLIB:ARI1_CC	+	0.066	4.427	1 r
Q[23]:D	net	Q_s_Z[23]		+	1.104	5.531	r
data arrival time						5.531	

Fig 9. All of the delays provided by SmartTime for the LSB arrival setup time.

Data_required_time_calculation							
clk	Clock Constraint				20.000	20.000	
clk	Clock source			+	0.000	20.000	r
clk_ibuf/U0/U_IOPAD:PAD	net	clk		+	0.000	20.000	r
clk_ibuf/U0/U_IOPAD:Y	cell		ADLIB:IOPAD_IN	+	1.273	21.273	2 r
clk_ibuf_RNIVTI2:An	net	clk_ibuf_Z		+	0.054	21.327	f
clk_ibuf_RNIVTI2:YSn	cell		ADLIB:GB	+	0.085	21.412	5 f
clk_ibuf_RNIVTI2/U0_RGB1_RGB0:An	net	clk_ibuf_RNIVTI2/U0_YNn_GSouth		+	0.287	21.699	f
clk_ibuf_RNIVTI2/U0_RGB1_RGB0:YL	cell		ADLIB:RGB	+	0.251	21.950	1 r
Q[23]:CLK	net	clk_ibuf_RNIVTI2/U0_RGB1_RGB0_rgbl_net_1		+	0.448	22.398	r
Q[23]:D	Library setup time		ADLIB:SLE	-	0.254	22.144	
data required time						22.144	

Fig 10. All of the delays provided by SmartTime for the LSB required setup time.

Data_arrival_time_calculation							
clk					0.000	0.000	
clk	Clock source			+	0.000	0.000	r
clk_ibuf/U0/U_IOPAD:PAD	net	clk		+	0.000	0.000	r
clk_ibuf/U0/U_IOPAD:Y	cell		ADLIB:IOPAD_IN	+	0.796	0.796	2 r
clk_ibuf_RNIVTI2:An	net	clk_ibuf_Z		+	0.036	0.832	f
clk_ibuf_RNIVTI2:YSn	cell		ADLIB:GB	+	0.057	0.889	5 f
clk_ibuf_RNIVTI2/U0_RGB1_RGB1:An	net	clk_ibuf_RNIVTI2/U0_YNn_GSouth		+	0.192	1.081	f
clk_ibuf_RNIVTI2/U0_RGB1_RGB1:YL	cell		ADLIB:RGB	+	0.168	1.249	20 r
Q[22]:CLK	net	clk_ibuf_RNIVTI2/U0_RGB1_RGB1_rgbl_net_1		+	0.332	1.581	r
Q[22]:Q	cell		ADLIB:SLE	+	0.072	1.653	3 f
Q_cry[22]:B	net	q_c[22]		+	0.225	1.878	f
Q_cry[22]:S	cell		ADLIB:ARI1_CC	+	0.181	2.059	1 r
Q[22]:D	net	Q_s[22]		+	0.052	2.111	r
data arrival time						2.111	

Fig 11. All of the delays provided by SmartTime for the MSB arrival hold time.

Data_required_time_calculation							
clk	Clock Constraint				0.000	0.000	
clk	Clock source			+	0.000	0.000	r
clk_ibuf/U0/U_IOPAD:PAD	net	clk		+	0.000	0.000	r
clk_ibuf/U0/U_IOPAD:Y	cell		ADLIB:IOPAD_IN	+	0.796	0.796	2 r
clk_ibuf_RNIVTI2:An	net	clk_ibuf_Z		+	0.036	0.832	f
clk_ibuf_RNIVTI2:YSn	cell		ADLIB:GB	+	0.057	0.889	5 f
clk_ibuf_RNIVTI2/U0_RGB1_RGB1:An	net	clk_ibuf_RNIVTI2/U0_YNn_GSouth		+	0.192	1.081	f
clk_ibuf_RNIVTI2/U0_RGB1_RGB1:YL	cell		ADLIB:RGB	+	0.168	1.249	20 r
Q[22]:CLK	net	clk_ibuf_RNIVTI2/U0_RGB1_RGB1_rgbl_net_1		+	0.332	1.581	r
Q[22]:D	Library hold time		ADLIB:SLE	+	0.000	1.581	
data required time						1.581	

Fig 12. All of the delays provided by SmartTime for the MSB required hold time.

Data_arrival_time_calculation							
clk					0.000	0.000	
clk	Clock source			+	0.000	0.000	r
clk_ibuf/U0/U_IOPAD:PAD	net	clk		+	0.000	0.000	r
clk_ibuf/U0/U_IOPAD:Y	cell		ADLIB:IOPAD_IN	+	0.796	0.796	2 r
clk_ibuf_RNIVTI2:An	net	clk_ibuf_Z		+	0.036	0.832	f
clk_ibuf_RNIVTI2:YSn	cell		ADLIB:GB	+	0.057	0.889	5 f
clk_ibuf_RNIVTI2/U0_RGB1_RGB1:An	net	clk_ibuf_RNIVTI2/U0_YNn_GSouth		+	0.192	1.081	f
clk_ibuf_RNIVTI2/U0_RGB1_RGB1:YL	cell		ADLIB:RGB	+	0.168	1.249	20 r
Q[1]:CLK	net	clk_ibuf_RNIVTI2/U0_RGB1_RGB1_rgbl_net_1		+	0.340	1.589	r
Q[1]:Q	cell		ADLIB:SLE	+	0.058	1.647	3 r
Q_cry[1]:B	net	q_c[1]		+	0.036	1.683	r
Q_cry[1]:S	cell		ADLIB:ARI1_CC	+	0.315	1.998	1 r
Q[1]:D	net	Q_s[1]		+	0.050	2.048	r
data arrival time						2.048	

Fig 13. All of the delays provided by SmartTime for the LSB arrival hold time.

Data_required_time_calculation							
clk	Clock Constraint				0.000	0.000	
clk	Clock source			+	0.000	0.000	r
clk_ibuf/U0/U_IOPAD:PAD	net	clk		+	0.000	0.000	r
clk_ibuf/U0/U_IOPAD:Y	cell		ADLIB:IOPAD_IN	+	0.796	0.796	2 r
clk_ibuf_RNIVTI2:An	net	clk_ibuf_Z		+	0.036	0.832	f
clk_ibuf_RNIVTI2:YSn	cell		ADLIB:GB	+	0.057	0.889	5 f
clk_ibuf_RNIVTI2/U0_RGB1_RGB1:An	net	clk_ibuf_RNIVTI2/U0_YNn_GSouth		+	0.192	1.081	f
clk_ibuf_RNIVTI2/U0_RGB1_RGB1:YL	cell		ADLIB:RGB	+	0.168	1.249	20 r
Q[1]:CLK	net	clk_ibuf_RNIVTI2/U0_RGB1_RGB1_rgbl_net_1		+	0.340	1.589	r
Q[1]:D	Library hold time		ADLIB:SLE	+	0.000	1.589	
data required time						1.589	

Fig 14. All of the delays provided by SmartTime for the LSB required hold time.

Clock Details Summary

Clock Domain	Period (ns)	Frequency (MHz)	Required Period (ns)	Required Frequency (MHz)	External Setup (ns)	External Hold (ns)	Min Clock-To-Out (ns)	Max Clock-To-Out (ns)
clk	4.152	240.848	20.000	50.000	N/A	N/A	3.051	7.964

Fig 15. SmartTime fMax summary.

Clock Details Summary

Clock Domain	Period (ns)	Frequency (MHz)	Required Period (ns)	Required Frequency (MHz)	External Setup (ns)	External Hold (ns)	Min Clock-To-Out (ns)	Max Clock-To-Out (ns)
clk	2.958	338.066	20.000	50.000	N/A	N/A	4.145	8.555

Fig 16. Improved design fMax summary.