

# SMARTTIME TUTORIAL GUIDE

2021/02/19 REVISION 1.0

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## INTRODUCTION

This lab exercise gives you the opportunity to practice timing closure using the SmartTime Static Timing Analyzer (STA). It is a port from the ProASIC3 version of this tutorial to the SmartFusion2.

### LEARNING OBJECTIVES

For this project, the objective is for students to:

- Become familiar with the Microsemi FPGA development flow and use of the SmartTime STA
- Appreciate the capabilities of the Microsemi SmartFusion2 System on a chip
- Learn how to create hardware using the SmartDesign design tool.
- Learn to evaluate system timing using SmartTime.

Many actions described in the tutorials can be performed from the menus or in the SmartTime Toolbar. The table below lists all the SmartTime Toolbar actions.



Table 1 · SmartTime Toolbar

Icon	Description
	Commits the changes
	Prints the contents of the constraints editor
	Copies data to the clipboard
	Pastes data from the clipboard
	Modifies the selected object from the constraints editor
	Deletes the selected object from the constraints editor
	Undoes previous changes
	Redoes previous changes
	Opens the maximum delay analysis view
	Opens the minimum delay analysis view
	Opens the manage clock domains manager
	Opens the path set manager
	Recalculates all
	Opens the constraints editor
	Opens the add clock constraint dialog box
	Opens the add generated clock constraint dialog box
	Opens the set input delay clock constraint dialog box
	Opens the set output delay clock constraint dialog box



Icon	Description
	Opens the set false path constraint dialog box
	Opens the set maximum delay constraint dialog box
	Opens the set minimum delay constraint dialog box
	Opens the set multicycle constraint dialog box
	Opens the set clock source latency dialog box
	Opens the set constraint to disable timing arcs dialog box
	Opens the set clock-to-clock uncertainty constraint dialog box
	Checks timing constraints
	Opens the constraint wizard

## I. 32-BIT SHIFT REGISTER

This tutorial section describes how to enter a clock constraint for the 32-bit shift register shown in the figure below. You will use the SmartTime Constraints Editor and perform post-layout timing analysis using the SmartTime Timing Analyzer.

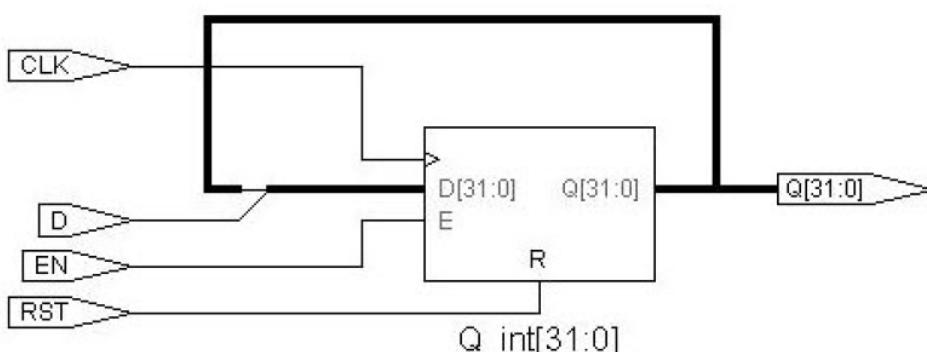


Figure 1 · 32-Bit Shift Registers





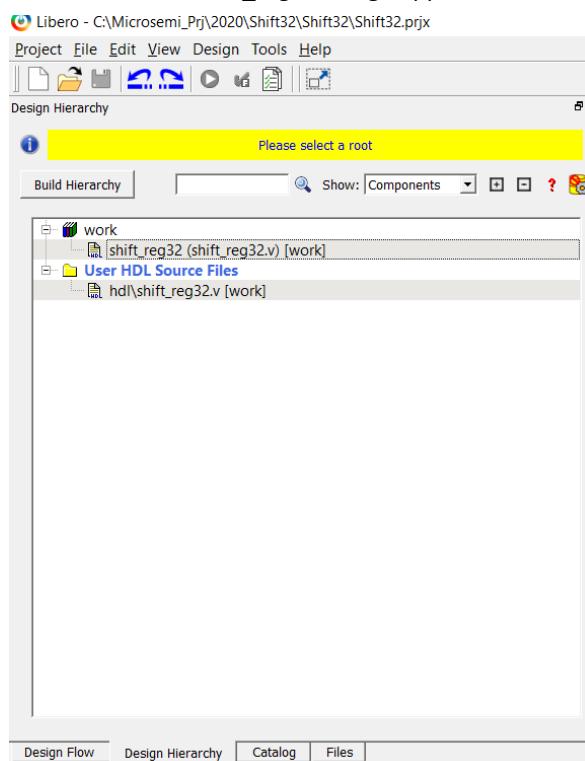
## SETUP

### To set up your project:

1. Invoke Libero SoC. From the **Project** menu, choose **New Project**.
2. Enter Shift32 for your new project name and browse to a folder for your project location. Enter the following values for the project settings:

- Language: Verilog
- Family: SmartFusion2
- Package: 144 TQFP
- Speed: STD
- Die: M2S010
- Temperature Range: COM
- I/O: LVCMOS 2.5v
- PLL Supply Voltage: 2.5
- VDD supply ramp time: 100 ms.
- Design Templates: None
- HDL Source File: Import shift\_reg32.v from the file provided

Confirm that the shift\_reg32 design appears in the Design Hierarchy window as shown:



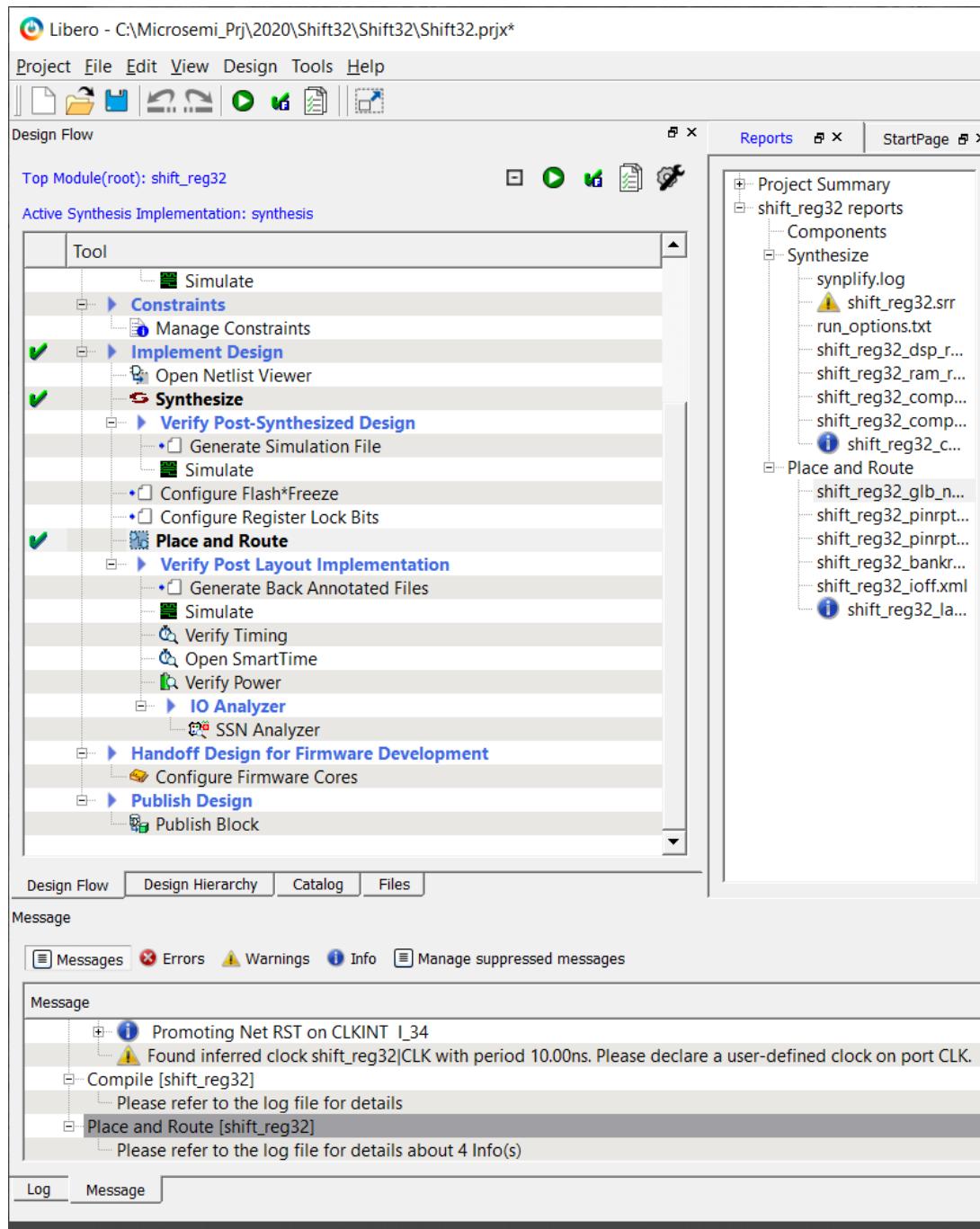
You may have to click on the “Build Hierarchy” button, and then right click on the shift\_reg32 file to set it as root.





Save the Project.

3. In the Design Flow window, double-click **Synthesize** to run Synplify Pro with default settings. A green check marks appears next to Synthesize when Synthesis is successful (as shown in the figure below).
4. Double-click **Place and Route** in the Design Flow window to run Compile with default settings. A green check mark appears next to Compile when it completes successfully (as shown in the figure below).





## CREATE A PIN ASSIGNMENT

5. In the **Design Flow window** double-click **Manage Constraints** and then select the first tab, **I/O Attributes** tab followed by Edit-> Edit with I/O Advisor to open the I/O Advisor (as shown in the figure below).

The screenshot shows the IOAdvisor interface with the following details:

- Left Panel:** Shows the navigation tree with "IO Attributes" selected under "I/O Attributes". Other options include "Output Load", "Output Drive & Slew Rate", and "ODT & Schmitt Trigger".
- Operating Mode:** Power: ACTIVE
- Operating Conditions:** Timing: WORST, Power: TYPICAL
- Total Power:** Initial: 0.00uW, Current: 0.00uW, Saving: 0.00%
- Table:** Adjust ODT and Schmitt Trigger
 

Port Name	Status	Port	Direction	Bank	IO Standard	State	Schmitt Trigger
1	CLK	Input	Bank7-MSIO	LVCMS25	Initial Current Suggested	Off Off --	
2	D	Input	Bank0-DDRIO	LVCMS25	Initial Current Suggested	Off Off --	
3	EN	Input	Bank0-DDRIO	LVCMS25	Initial Current Suggested	Off Off --	
4	RST	Input	Bank4-MSIO	LVCMS25	Initial Current Suggested	Off Off --	
- Buttons:** Set Schmitt Trigger, Set ODT Static, Set ODT Impedance, Apply Suggestion, Restore Initial Value, Select: All / None
- Message:** How the suggested values are computed?
- Bottom:** Fam:SmartFusion2 | Die:M2S010 | Pkg:144 TQ | Speed: STD

6. Click File-> Save and File -> Exit.  
 7. Verify the I/O Pin assignments. In the Constraints Manager, again select I/O Attributes and Edit with I/O Editor. The ports should be assigned pin numbers as shown below:

The screenshot shows the I/O Editor interface with the following details:

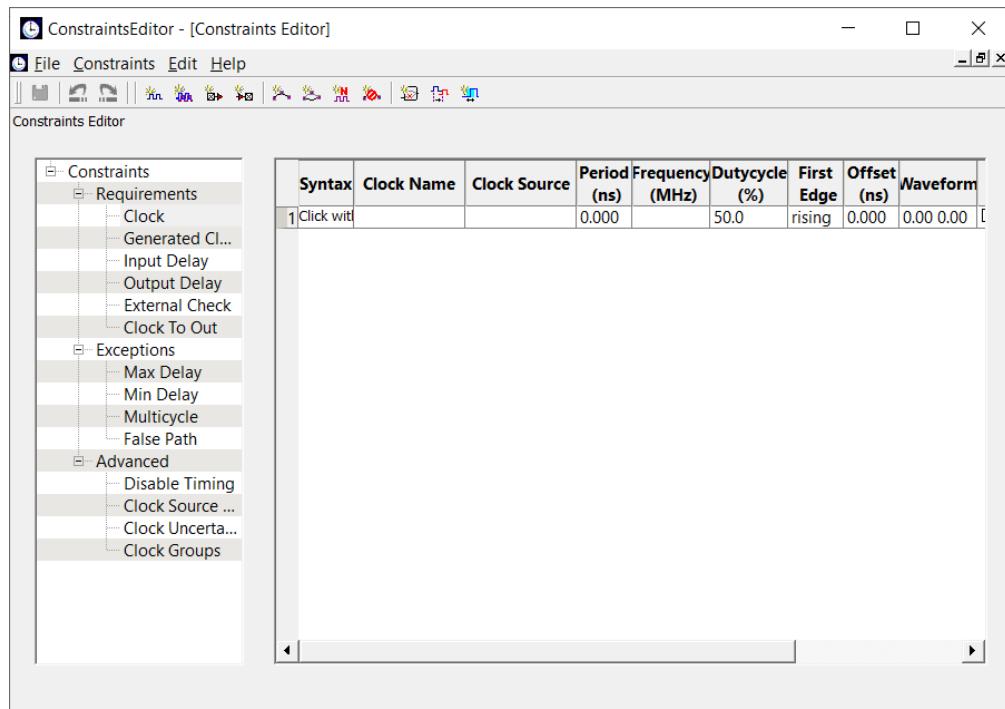
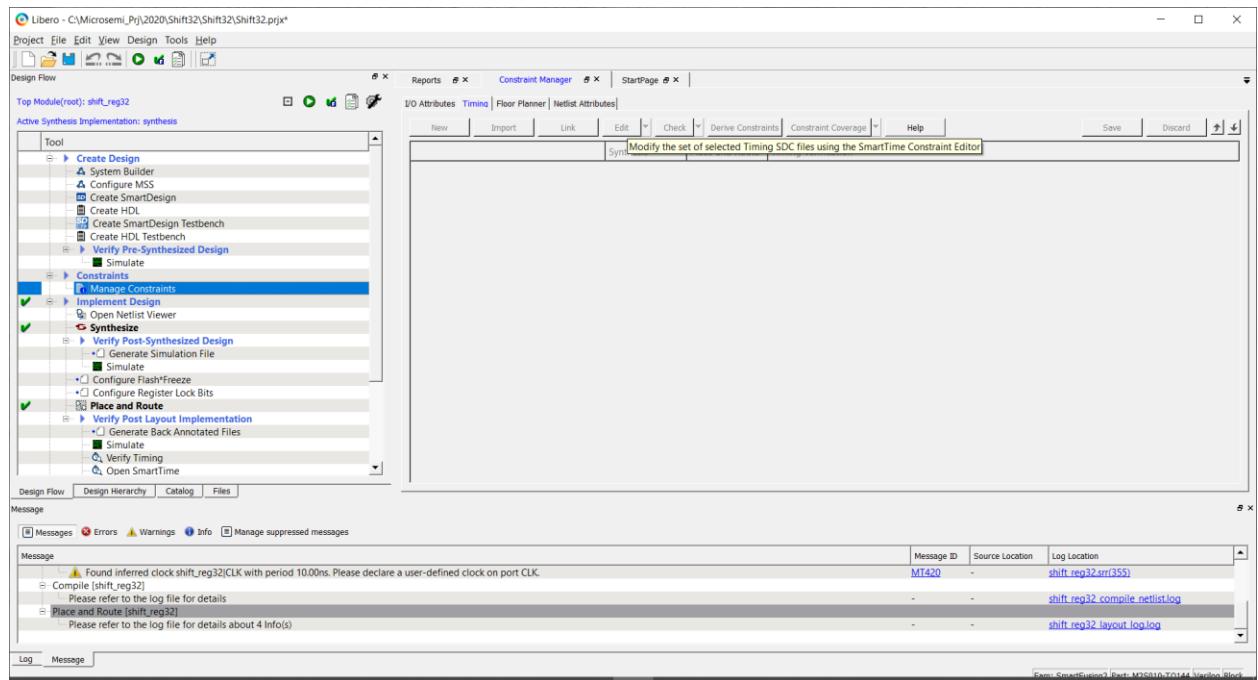
- Main Object Browser:** Shows a tree view of ports: I/O Ports, CLK, D, EN, RST.
- Table:** Port View (active)
 

Port Name	Direction	I/O Standard	Pin Number	Locked	Macro Cell	Rank Name	I/O state in Flash/Freeze mode	Register Pull	I/O available
1 CLK	INPUT	LVCMS25	20		INBUF	Bank7	TRISTATE	None	
2 D	INPUT	LVCMS25	116		INBUF	Bank0	TRISTATE	None	
3 EN	INPUT	LVCMS25	135		INBUF	Bank0	TRISTATE	None	
4 Q[0]	OUTPUT	LVCMS25	118		OUTBUF	Bank0	TRISTATE	None	
5 Q[1]	OUTPUT	LVCMS25	115		OUTBUF	Bank0	TRISTATE	None	
7 Q[2]	OUTPUT	LVCMS25	15		OUTBUF	Bank7	TRISTATE	None	
8 Q[3]	OUTPUT	LVCMS25	19		OUTBUF	Bank7	TRISTATE	None	
9 Q[4]	OUTPUT	LVCMS25	144		OUTBUF	Bank0	TRISTATE	None	
10 Q[5]	OUTPUT	LVCMS25	127		OUTBUF	Bank0	TRISTATE	None	
11 Q[6]	OUTPUT	LVCMS25	125		OUTBUF	Bank0	TRISTATE	None	
12 Q[7]	OUTPUT	LVCMS25	124		OUTBUF	Bank0	TRISTATE	None	
13 Q[8]	OUTPUT	LVCMS25	111		OUTBUF	Bank0	TRISTATE	None	
14 Q[9]	OUTPUT	LVCMS25	112		OUTBUF	Bank0	TRISTATE	None	
15 Q[10]	OUTPUT	LVCMS25	142		OUTBUF	Bank0	TRISTATE	None	
16 Q[11]	OUTPUT	LVCMS25	1		OUTBUF	Bank7	TRISTATE	None	
17 Q[12]	OUTPUT	LVCMS25	13		OUTBUF	Bank7	TRISTATE	None	
18 Q[13]	OUTPUT	LVCMS25	16		OUTBUF	Bank7	TRISTATE	None	
19 Q[14]	OUTPUT	LVCMS25	7		OUTBUF	Bank7	TRISTATE	None	
20 Q[15]	OUTPUT	LVCMS25	14		OUTBUF	Bank7	TRISTATE	None	
21 Q[16]	OUTPUT	LVCMS25	9		OUTBUF	Bank7	TRISTATE	None	
22 Q[17]	OUTPUT	LVCMS25	8		OUTBUF	Bank7	TRISTATE	None	
23 Q[18]	OUTPUT	LVCMS25	131		OUTBUF	Bank0	TRISTATE	None	
24 Q[19]	OUTPUT	LVCMS25	130		OUTBUF	Bank0	TRISTATE	None	
25 Q[20]	OUTPUT	LVCMS25	143		OUTBUF	Bank0	TRISTATE	None	
26 Q[21]	OUTPUT	LVCMS25	3		OUTBUF	Bank7	TRISTATE	None	
27 Q[22]	OUTPUT	LVCMS25	4		OUTBUF	Bank7	TRISTATE	None	
28 Q[23]	OUTPUT	LVCMS25	136		OUTBUF	Bank0	TRISTATE	None	
29 Q[24]	OUTPUT	LVCMS25	141		OUTBUF	Bank0	TRISTATE	None	
30 Q[25]	OUTPUT	LVCMS25	117		OUTBUF	Bank0	TRISTATE	None	
31 Q[26]	OUTPUT	LVCMS25	123		OUTBUF	Bank0	TRISTATE	None	
32 Q[27]	OUTPUT	LVCMS25	2		OUTBUF	Bank7	TRISTATE	None	
33 Q[28]	OUTPUT	LVCMS25	134		OUTBUF	Bank0	TRISTATE	None	
- Properties:** Shows various settings like Netlist View Settings, Device Settings, Design Settings, Region Settings, etc.
- Display Options:** Shows theme, package view settings, device settings, design settings, net settings, region settings, device, titles, modules, banks, design, macros, regions.
- Bottom:** World View, Log, Messages, Info, Log Message, Fam: SmartFusion2 | Die: M2S010 | Pkg: 144 TQ



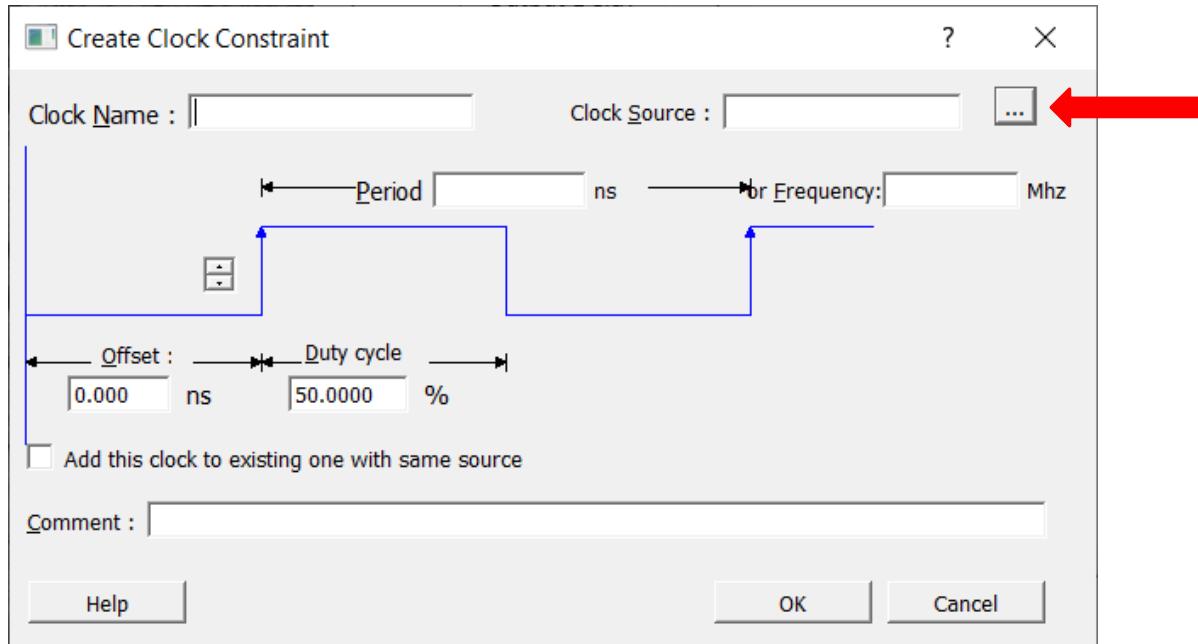
## ADD A CLOCK CONSTRAINT

8. In the **Design Flow window** double-click **Manage Constraints** and then select the **Timing** tab followed by **Edit > Edit Place and Route Timing Constraints** to open the Constraints Editor (as shown in the figure below). Continue in the Constraints Editor.

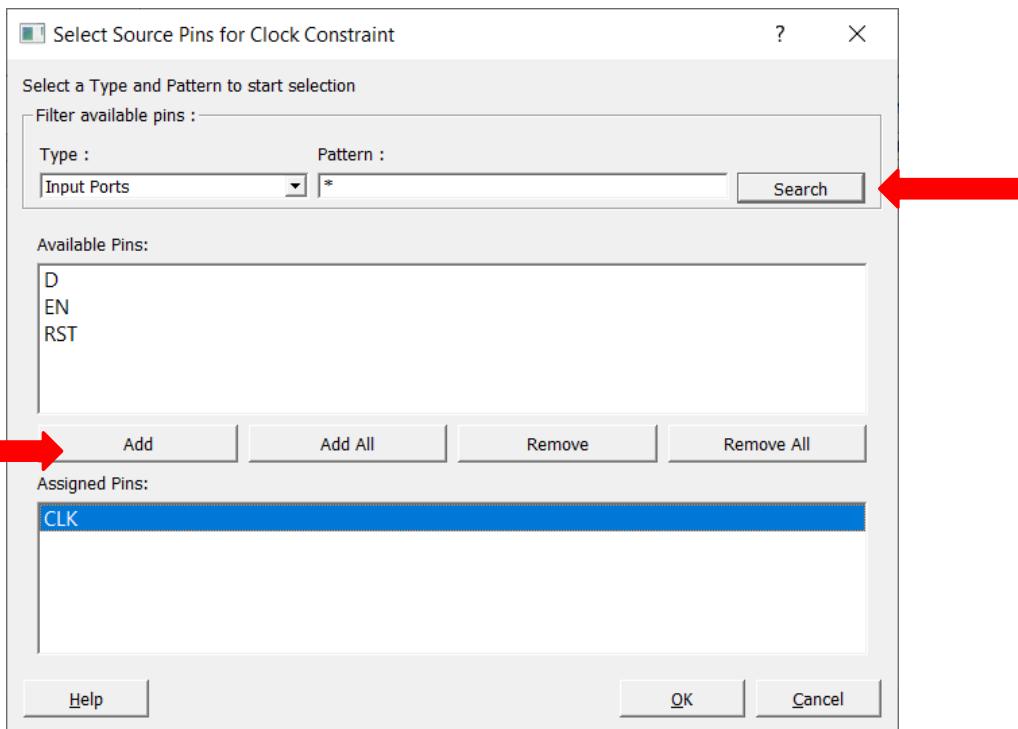




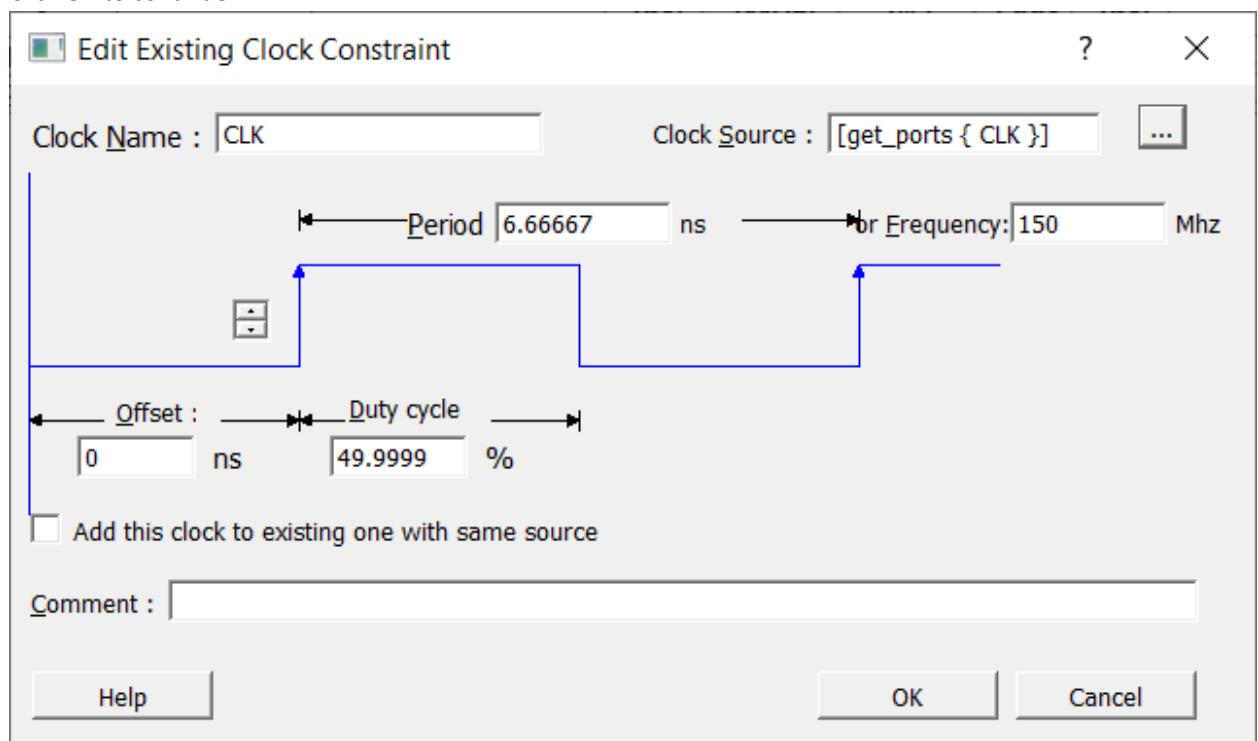
9. From the top menu, choose **Constraints > Clock** to open the Create Clock Constraint Editor, as shown in the figure below. You could also do this by double clicking in the first row of the Constraint Editor spreadsheet.



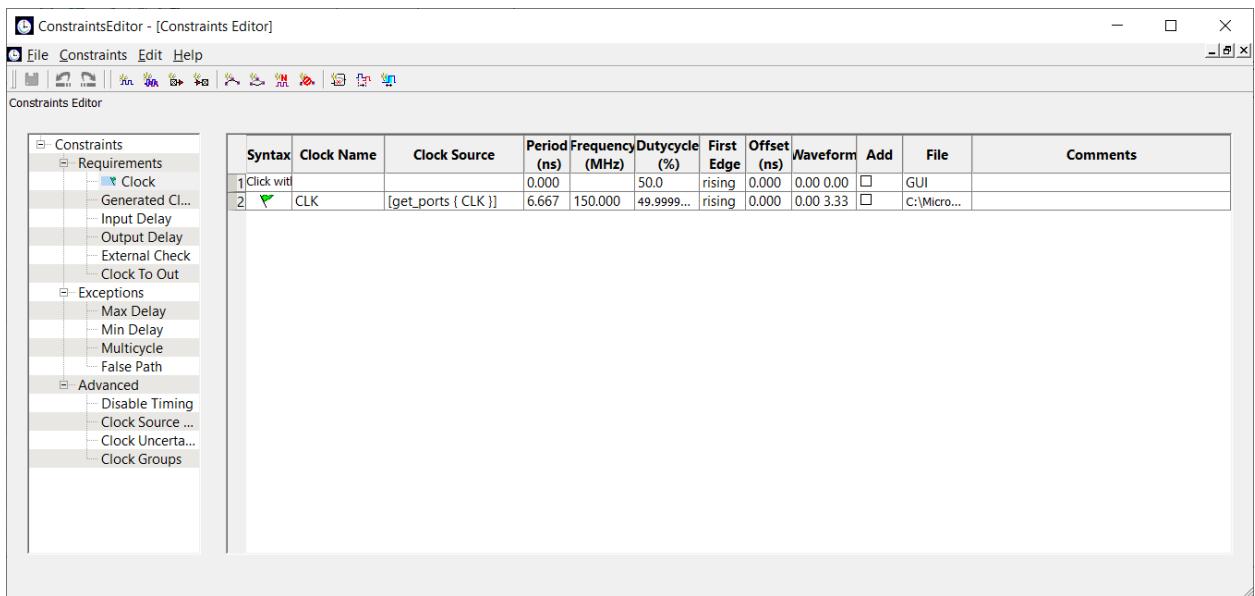
10. Set the **Clock Name** to **CLK** and the **Frequency** to **150 MHz** (as shown in the figure below) and leave all other values at the default setting. Click the ... box to the right of the Clock Source box to add the clock source. In the Select Source Pins for Clock Constraint dialog box, click on Search, and then select CLK. Click Add and then OK.



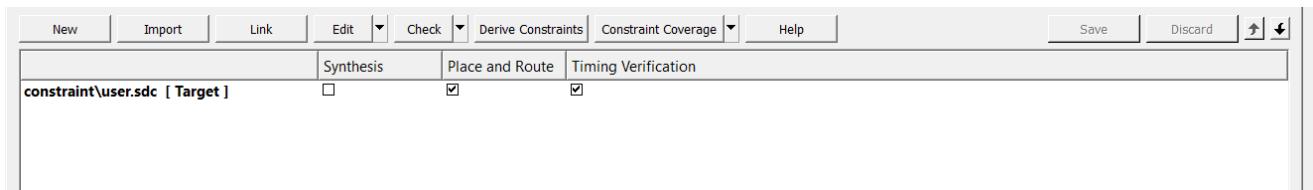
Click **OK** to continue.



11. The clock constraint appears in the SmartTime Constraints Editor (as shown in the figure below).

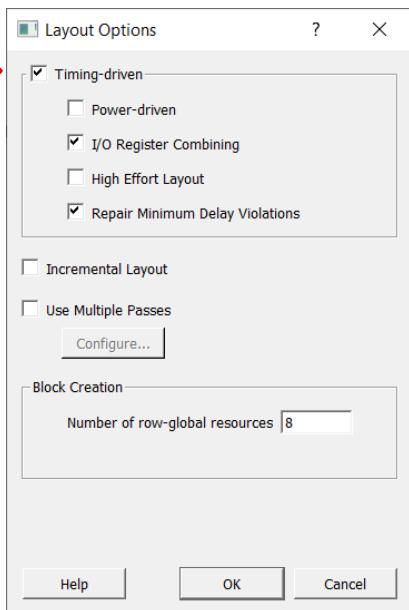


12. From the **File** menu, choose **Save** (was Commit) to save the constraints. Then Select File -> Exit.
13. Looking again at the Constraint Manager tab, make sure the Place and Route and Timing Verification boxes are checked:



## PERFORM TIMING-DRIVEN PLACE AND ROUTE

1. Right-click on **Place and Route** and select **Configure Options**. The Layout options dialog box should appear. Confirm that the Timing-Drive box is checked and click OK:



## 2. Run Place and Route.

### PERFORM MAXIMUM DELAY ANALYSIS

The SmartTime Maximum Delay Analysis window displays the design maximum operating frequency and lists any setup violations.

#### **To perform Maximum Delay Analysis:**

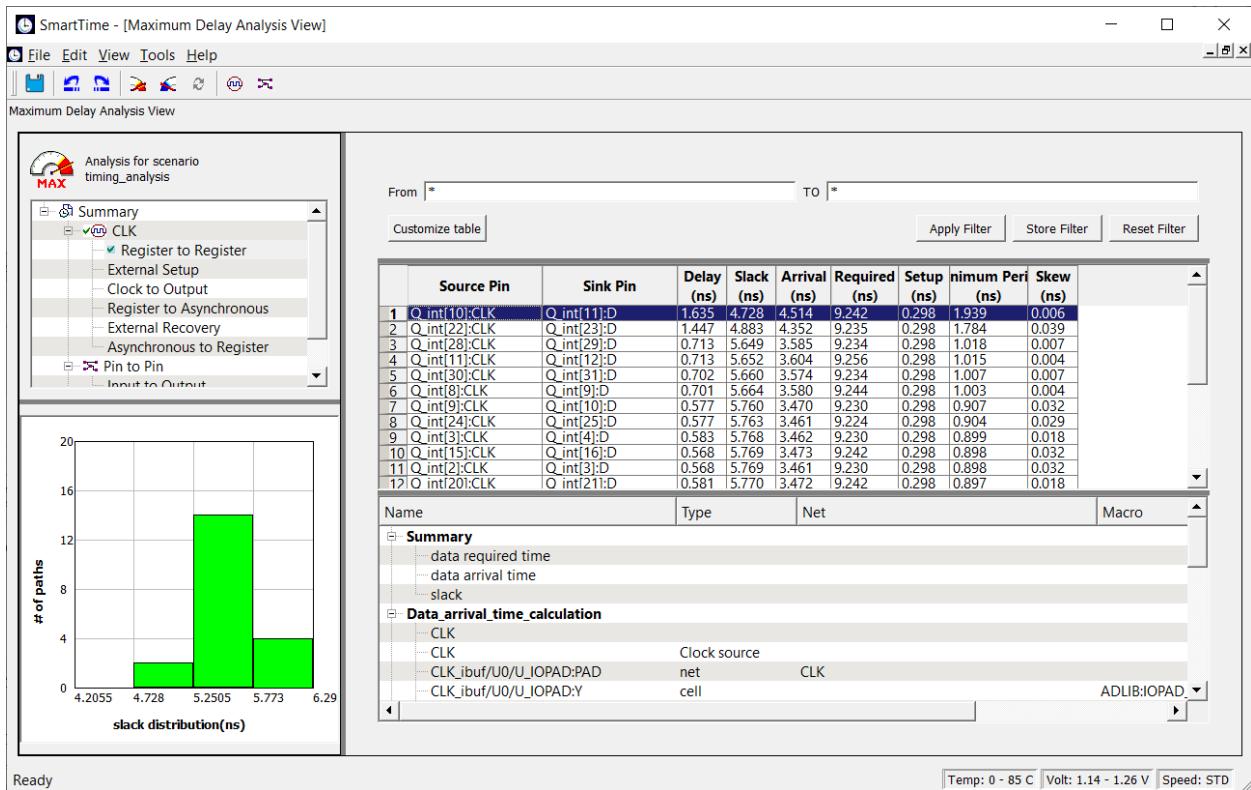
1. Double-Click the **Open SmartTime** button below Place and Route in the Design Flow to open SmartTime. The Maximum Delay analysis window appears (as shown in the figure below). A green check next to the clock name indicates there are no timing violations for that clock domain. The Summary page displays a summary of the clock domain timing performance.

The Maximum Delay Analysis Summary displays the:

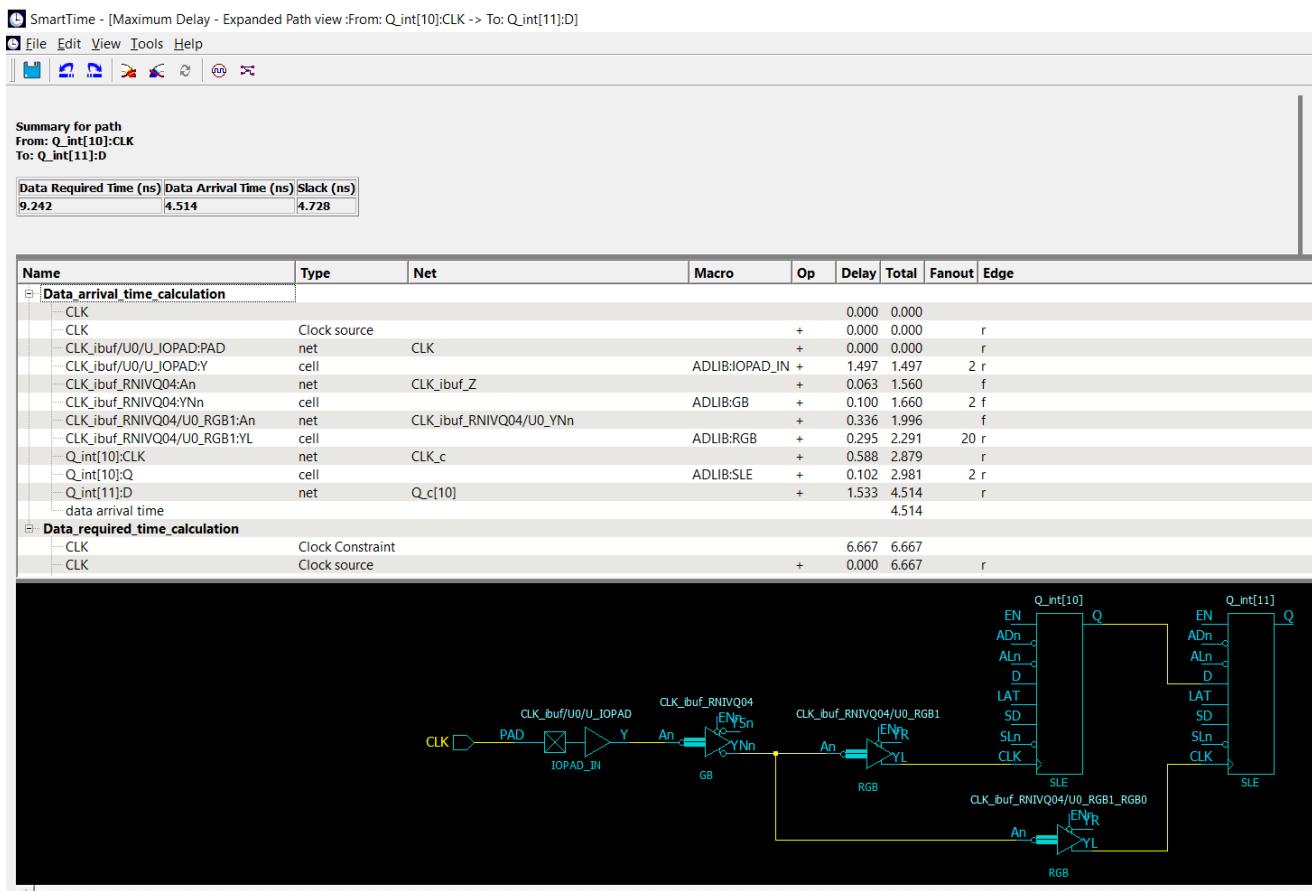
- Maximum operating frequency for the design
- External setup and hold requirements
- Maximum and minimum clock-to-out times.

2. In this example, from the CLK summary you can see the maximum clock frequency for CLK is likely over 500 MHz. The Register to Register summary shows the margin or slack for each path. If the values are all positive then there is no setup timing violations.





3. In the Register to Register display, double-click a path row to open the **Expanded Path Window**. The window shows a calculation of the data arrival and required times along with a schematic of the path (as shown in the figure below). It includes all gate and routing propagation delays.



### PERFORM MINIMUM DELAY ANALYSIS

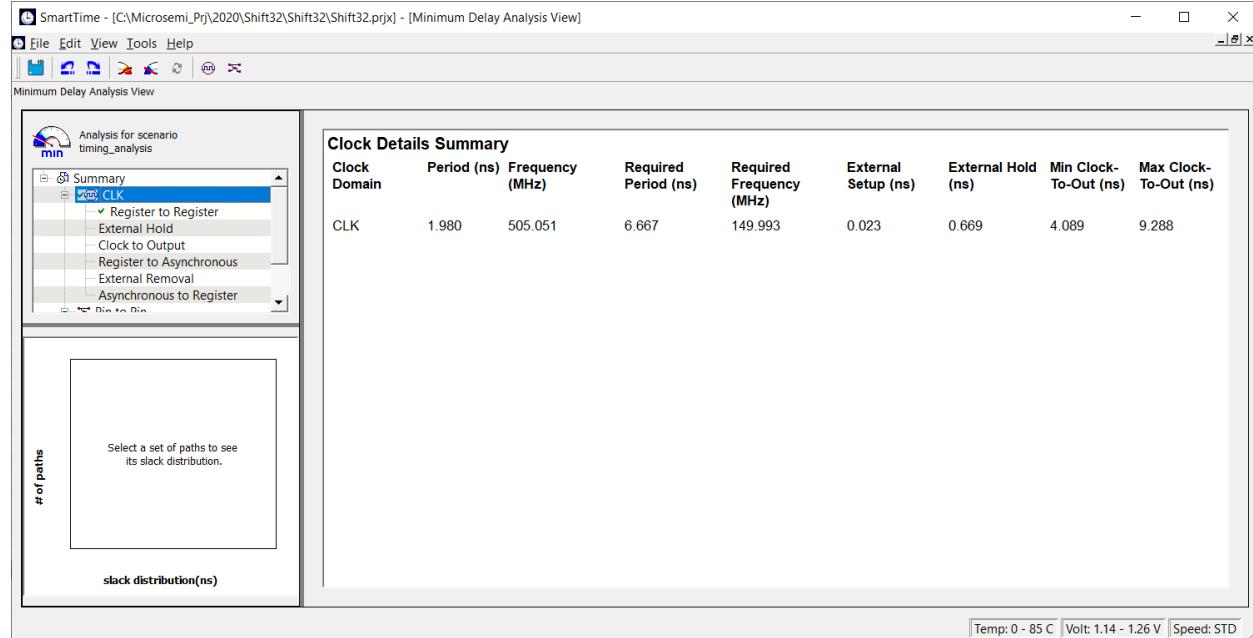
The SmartTime Minimum Delay Analysis window identifies any hold violations that exist in the design.

#### To perform Minimum Delay Analysis:

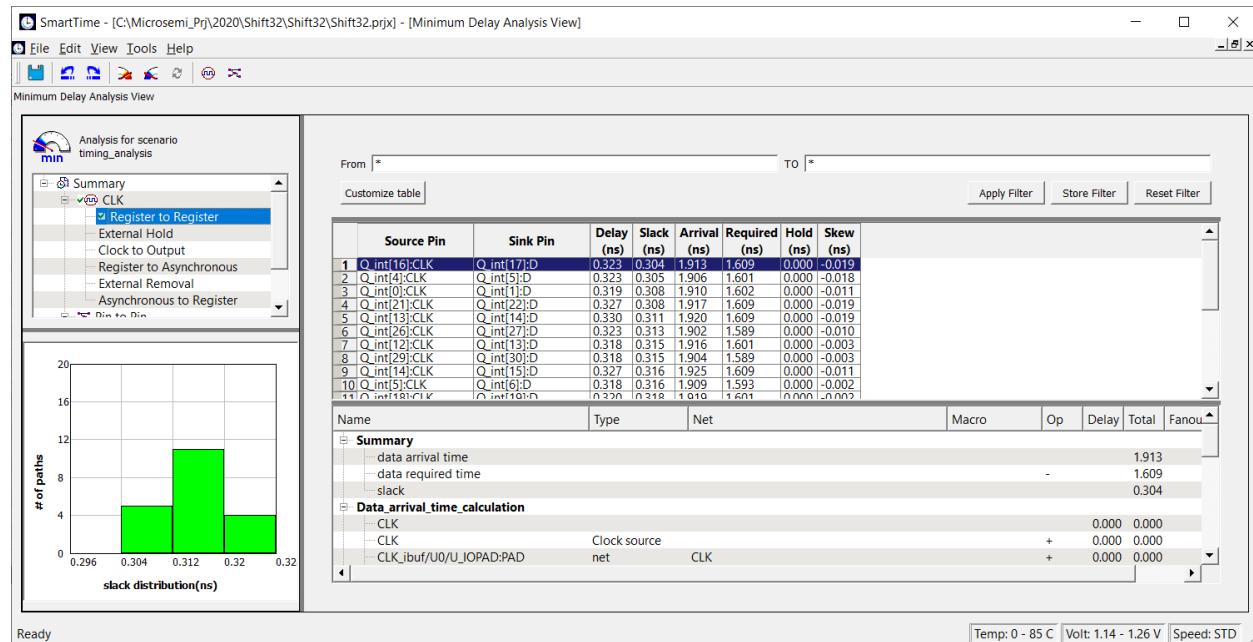
1. From the SmartTime Tools menu, choose **Timing Analyzer > Minimum Delay Analysis**. The Minimum Delay Analysis window appears, as shown in the figure below.



2. Click the + next to CLK to expand the list and display Register to Register, External Hold, Clock to Output, Register to Asynchronous, External Removal and Asynchronous to Reset path sets.



3. Click **Register to Register** to display the reg to reg paths. The window displays a list of register to register paths and detailed timing analysis for the selected path. Note that all slack value are positive, indicating that there are no hold time violations.



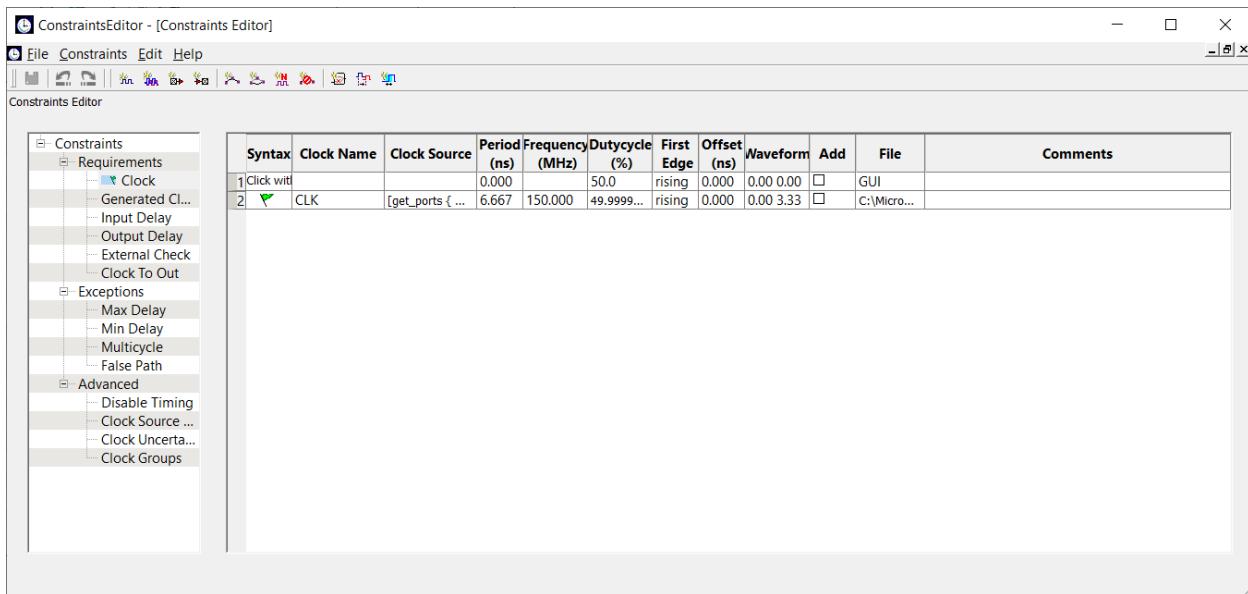
4. Click to select the first path and observe the hold analysis calculation details, as shown in the figure below.



## CHANGING CONSTRAINTS AND OBSERVING CHANGED RESULTS

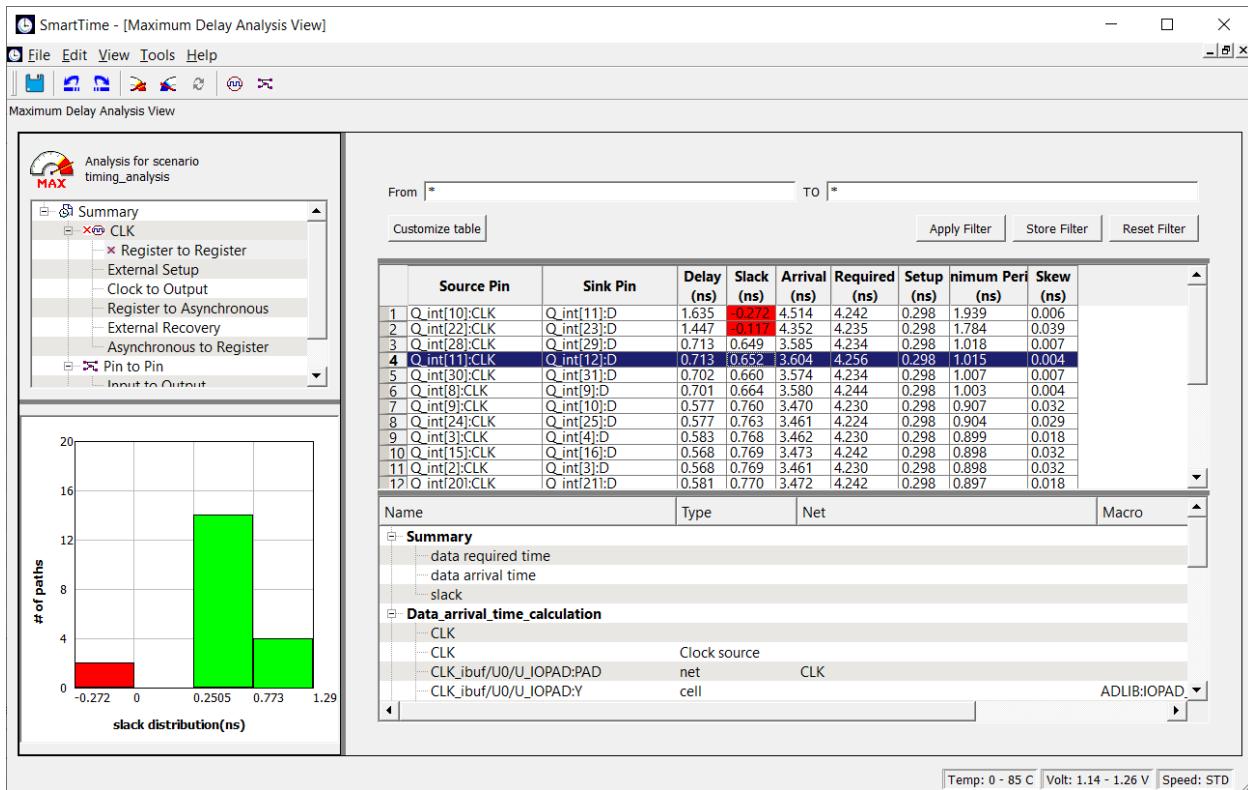
You can use SmartTime to adjust constraints and view the results in your design. The object is to use the constraints to influence the routing to achieve the best Fmax. However, if you over-constrain the design by too much, the Fmax may actually go down. Best performance usually comes from getting the constraint close to the best possible outcome. To make constraint changes:

1. Open the SmartTime Constraints Editor by clicking on the constraints manager in the design flow. The Constraints Editor displays the clock constraint at 150 MHz that you entered earlier, as shown in the figure below.



2. Double-click the CLK constraint row to open the Edit Clock Constraint dialog box. Change the clock constraint from **150 MHz** to **600 MHz** and click **OK** to continue. Click File-> Save and File-> Exit to close the Constraint Editor.
3. Right click on SmartTime in the design flow and select **Open Interactively** to Open SmartTime. From the **View** menu, choose **Recalculate All** to recalculate the delays using your new clock constraint. If Recalculate All is greyed out, then the new delays were automatically calculated.
4. From the **Tools** menu, choose **Timing Analyzer > Maximum Delay Analysis View** to view the max delay analysis.
5. Expand the **CLK** in the Maximum Delay Analysis window. Click **Register to Register** to observe the timing information. Note that the negative slack (timing violations) are shown in red (as shown in the figure below).



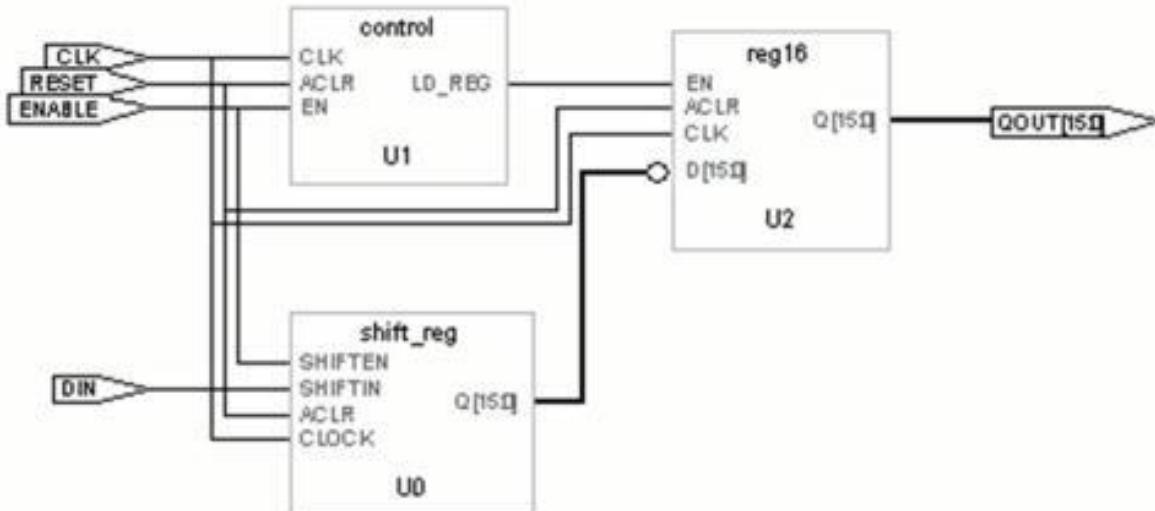


6. Close SmartTime. Click **No** when prompted to commit your unsaved edits.

## II. DUAL CLOCK EDGE DESIGN

This example analyzes SmartTime reports that include both rising and falling edges of a clock in the same design. The design (as shown in the figure below) consists of a 16-bit serial-in parallel-out (SIPO) shift register, a control block and a 16-bit output register. The control block enables the output register after 16 bits of data have been shifted in. The shift register and the control block are clocked on the rising edge of the clock. The output register is clocked on the falling edge of the clock.

You will import the shifter.v HDL file and enter a clock constraint of 100 MHz. After routing the design you will analyze the timing to determine the maximum operating frequency and export a timing report.



## SET UP YOUR EXAMPLE DESIGN PROJECT

1. Invoke Libero SoC. From the **Project** menu, choose **New Project**.
2. Enter Shifter for your new project name and browse to a folder for your project location. Enter the following values for the project settings:

- Language: Verilog
- Family: SmartFusion2
- Package: 144 TQFP
- Speed: STD
- Die: M2S010
- Temperature Range: COM
- I/O: LVCMOS 2.5v
- PLL Supply Voltage: 2.5
- VDD supply ramp time: 100 ms.
- Design Templates: None
- HDL Source File: Import Shifter.v from the file provided

Confirm that the Shifter design appears in the Design Hierarchy window

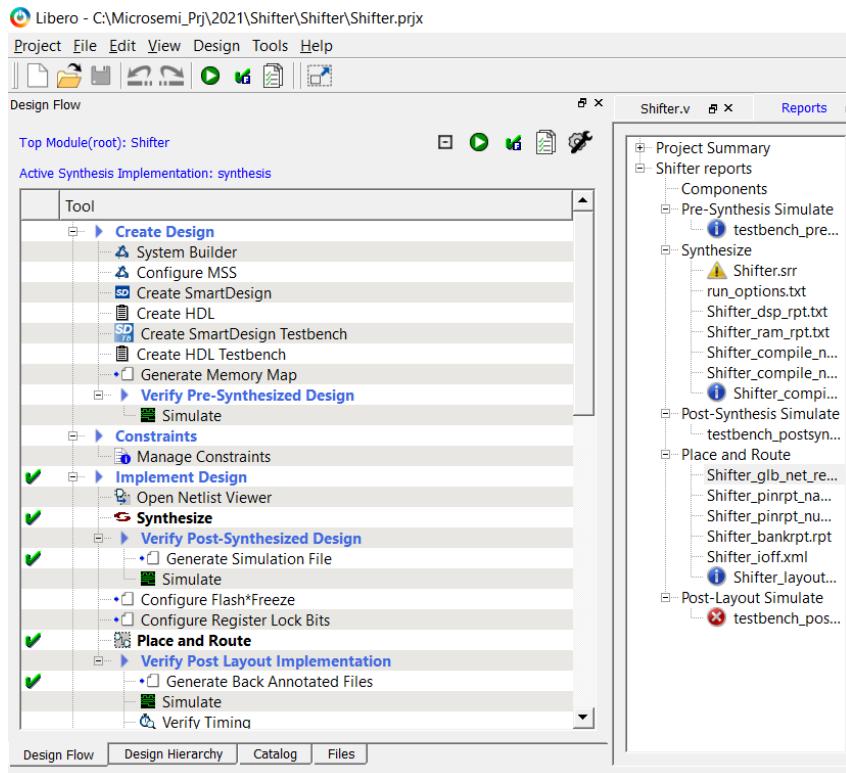
You may have to click on the “Build Hierarchy” button, and then right click on the Shifter file to set it as root.

Save the Project.





3. In the Design Flow window, double-click **Synthesize** to run Synplify Pro with default settings. A green check marks appears next to Synthesize when Synthesis is successful (as shown in the figure below).
4. Double-click **Place and Route** in the Design Flow window to run Compile with default settings. A green check mark appears next to Compile when it completes successfully (as shown in the figure below).



## CREATE A PIN ASSIGNMENT

1. In the **Design Flow window** double-click **Manage Constraints** and then select the first tab, **I/O Attributes** tab followed by Edit-> Edit with I/O Advisor to open the I/O Advisor (as shown in the figure below).



IOAdvisor

File Edit View Help

IO Attributes

Output Load  
Output Drive & S  
ODT & Schmitt T

Summary

Operating Mode:  
Power: ACTIVE

Operating Conditions:  
Timing: WORST  
Power: TYPICAL

Total Power:  
Initial: 0.00uW  
Current: 0.00uW  
Saving: 0.00%

Adjust ODT and Schmitt Trigger

Port Name	Status	Port	Direction	Bank	IO Standard	State	Schmitt Trigger
1 Din	Initial	Din	Input	Bank2-MSIO	LVCMS25	Off	Off
2 clk	Current	clk	Input	Bank7-MSIO	LVCMS25	Off	--
3 enable	Suggested	enable	Input	Bank2-MSIO	LVCMS25	--	--
4 reset	Initial	reset	Input	Bank4-MSIO	LVCMS25	Off	Off

Set Schmitt Trigger | Set ODT Static | Set ODT Impedance | Apply Suggestion | Restore Initial Value | Select: All | None | How the suggested values are computed?

Fam:SmartFusion2 | Die:M2S010 | Pkg:144 TQ | Speed: STD

Ready

2. Click File-> Save and File -> Exit.
3. Verify the I/O Pin assignments. In the Constraints Manager, again select I/O Attributes and Edit with I/O Editor. The ports should be assigned pin numbers similar to those shown below:

Port View [active]	Pin View	Package View	Floorplanner View	Netlist Viewer - Hier	Netlist Viewer - Flat				
Port Name	Direction	I/O Standard	Pin Number	Locked	Macro Cell	Rank Name	I/O state in Flash*Freeze mode	Resistor Pull	I/O available
1 clk	INPUT	LVCMS25	20	<input type="checkbox"/>	INBUF	Bank7	TRISTATE	None	
2 Din	INPUT	LVCMS25	87	<input type="checkbox"/>	INBUF	Bank2	TRISTATE	None	
3 enable	INPUT	LVCMS25	88	<input type="checkbox"/>	INBUF	Bank2	TRISTATE	None	
4 Qout	OUTPUT	LVCMS25		<input type="checkbox"/>	OUTBUF		TRISTATE	None	
5 Qout[0]	OUTPUT	LVCMS25	58	<input type="checkbox"/>	OUTBUF	Bank4	TRISTATE	None	
6 Qout[1]	OUTPUT	LVCMS25	64	<input type="checkbox"/>	OUTBUF	Bank4	TRISTATE	None	
7 Qout[2]	OUTPUT	LVCMS25	67	<input type="checkbox"/>	OUTBUF	Bank4	TRISTATE	None	
8 Qout[3]	OUTPUT	LVCMS25	85	<input type="checkbox"/>	OUTBUF	Bank2	TRISTATE	None	
9 Qout[4]	OUTPUT	LVCMS25	61	<input type="checkbox"/>	OUTBUF	Bank4	TRISTATE	None	
10 Qout[5]	OUTPUT	LVCMS25	82	<input type="checkbox"/>	OUTBUF	Bank2	TRISTATE	None	
11 Qout[6]	OUTPUT	LVCMS25	53	<input type="checkbox"/>	OUTBUF	Bank4	TRISTATE	None	
12 Qout[7]	OUTPUT	LVCMS25	81	<input type="checkbox"/>	OUTBUF	Bank2	TRISTATE	None	
13 Qout[8]	OUTPUT	LVCMS25	92	<input type="checkbox"/>	OUTBUF	Bank2	TRISTATE	None	
14 Qout[9]	OUTPUT	LVCMS25	89	<input type="checkbox"/>	OUTBUF	Bank2	TRISTATE	None	
15 Qout[10]	OUTPUT	LVCMS25	52	<input type="checkbox"/>	OUTBUF	Bank4	TRISTATE	None	
16 Qout[11]	OUTPUT	LVCMS25	60	<input type="checkbox"/>	OUTBUF	Bank4	TRISTATE	None	
17 Qout[12]	OUTPUT	LVCMS25	63	<input type="checkbox"/>	OUTBUF	Bank4	TRISTATE	None	
18 Qout[13]	OUTPUT	LVCMS25	66	<input type="checkbox"/>	OUTBUF	Bank4	TRISTATE	None	
19 Qout[14]	OUTPUT	LVCMS25	55	<input type="checkbox"/>	OUTBUF	Bank4	TRISTATE	None	
20 Qout[15]	OUTPUT	LVCMS25	83	<input type="checkbox"/>	OUTBUF	Bank2	TRISTATE	None	
21 reset	INPUT	LVCMS25	56	<input type="checkbox"/>	INBUF	Bank4	TRISTATE	None	

Log

Messages Errors Warnings Info

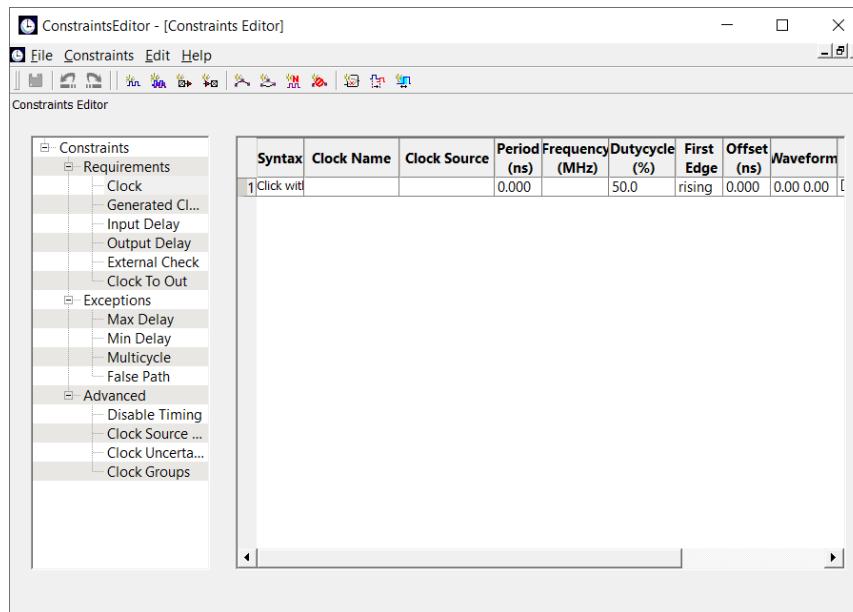
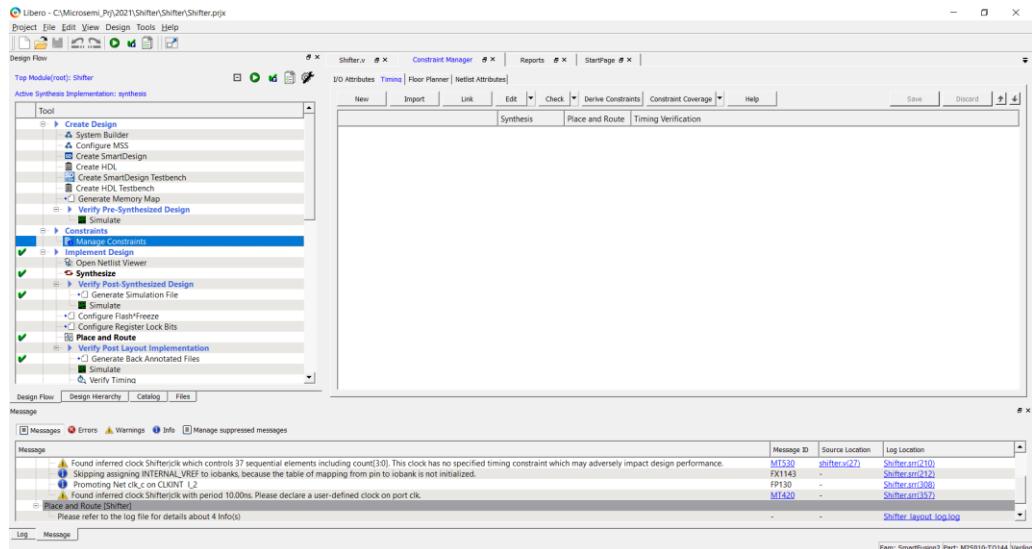
INFO: Reading User PDC file C:/Microsemi\_Prj/2021/Shifter/Shifter/designer/Shifter/Shifter.nmatinit.pdc. 0 error(s) and 0 war

Log Message



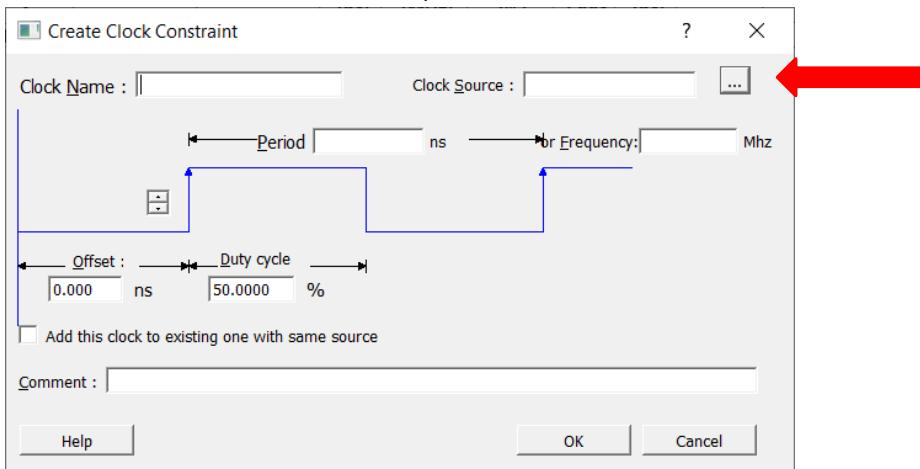
## ADD A CLOCK CONSTRAINT

- In the **Design Flow window** double-click **Manage Constraints** and then select the **Timing** tab followed by **Edit->Edit Place and Route Timing Constraints** to open the Constraints Editor (as shown in the figure below). Continue in the Constraints Editor.

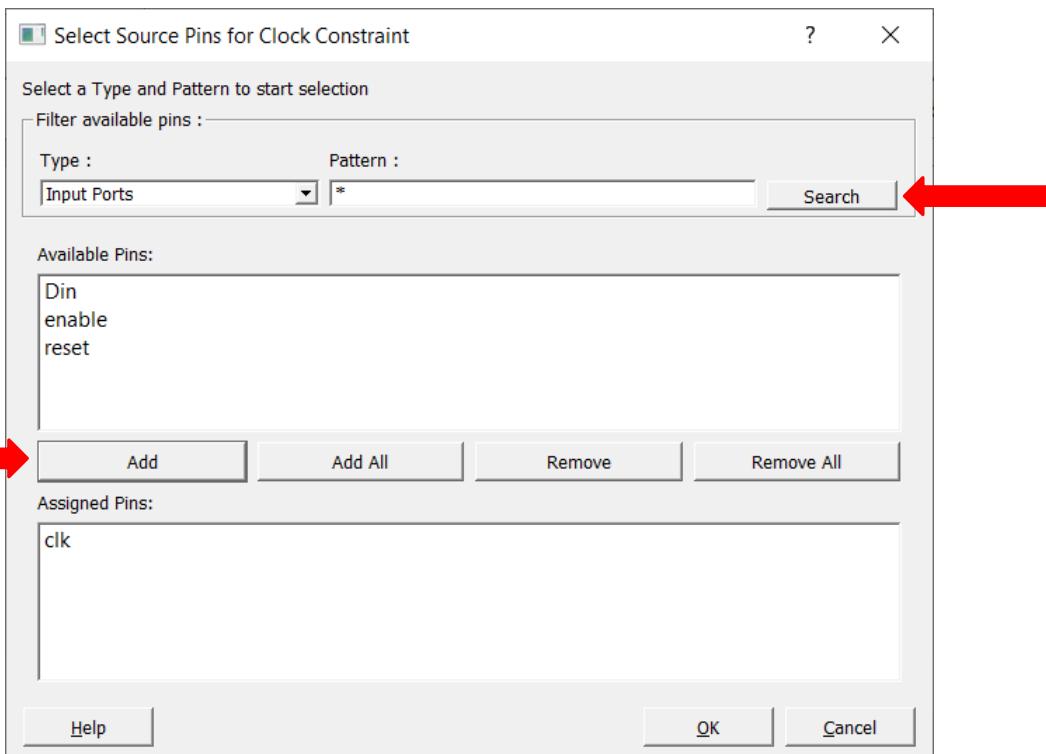




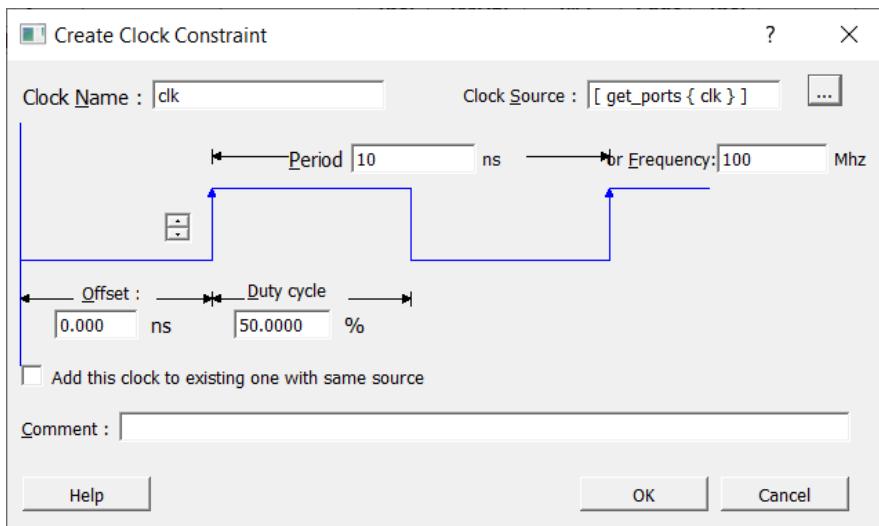
2. Double click in the first row of the Constraint Editor Spreadsheet. You could also do this by using the top menu, choose **Constraints > Clock** to open the Create Clock Constraint Editor.



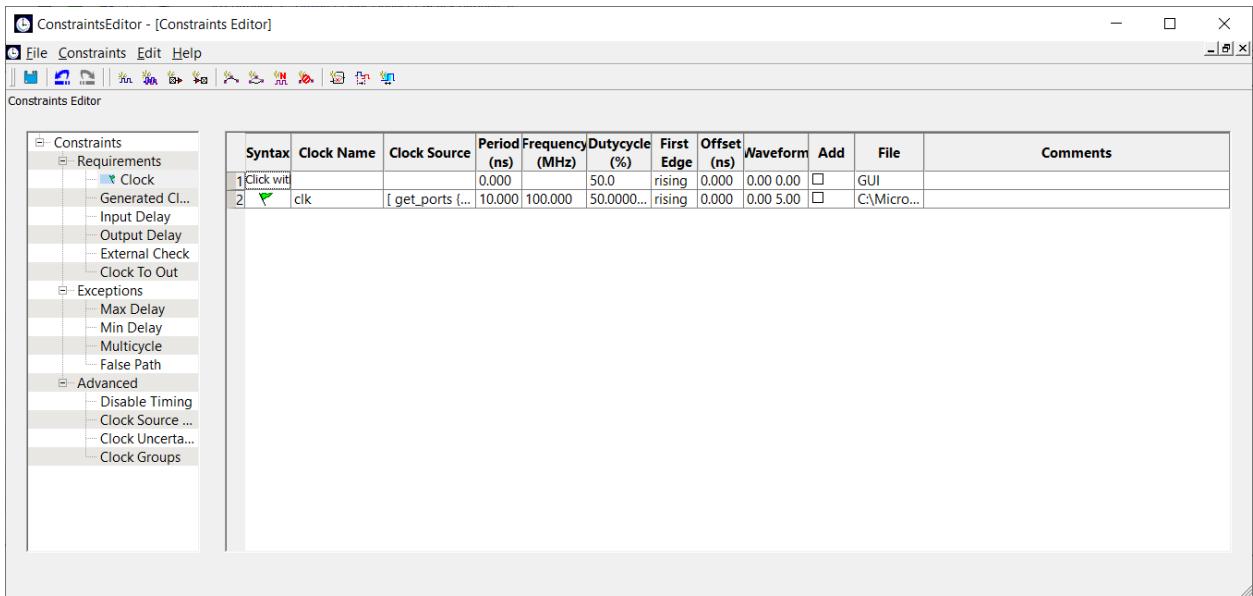
3. Set the **Clock Name** to **clk** and the **Frequency** to **100 MHz** (as shown in the figure below) and leave all other values at the default setting. Click the browse button to the right of the Clock Source box to add the clock source. In the Select Source Pins for Clock Constraint dialog box, click on Search, and then select CLK. Click Add and then OK.



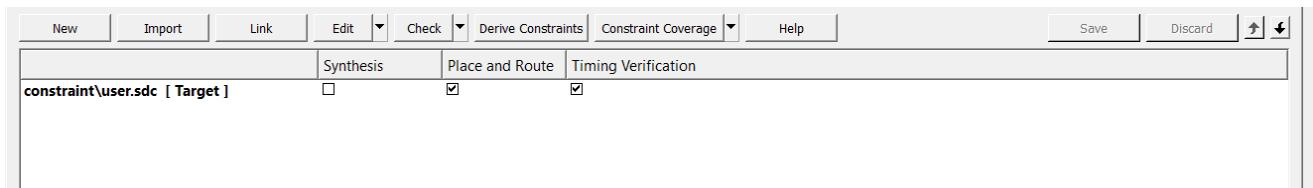
Click **OK** to continue.



4. The clock constraint appears in the SmartTime Constraints Editor (as shown in the figure below).



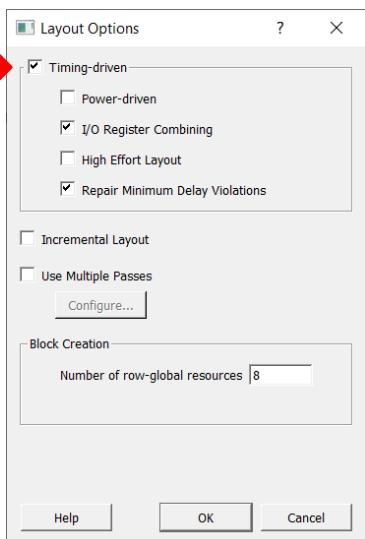
5. From the **File** menu, choose **Save** (was Commit) to save the constraints. Then Select File -> Exit.
6. Looking again at the Constraint Manager tab, make sure the Place and Route and Timing Verification boxes are checked:





## PERFORM TIMING-DRIVEN PLACE AND ROUTE

1. Right-click on **Place and Route** and select **Configure Options**. The Layout options dialog box should appear. Confirm that the Timing-Driven box is checked and click OK:



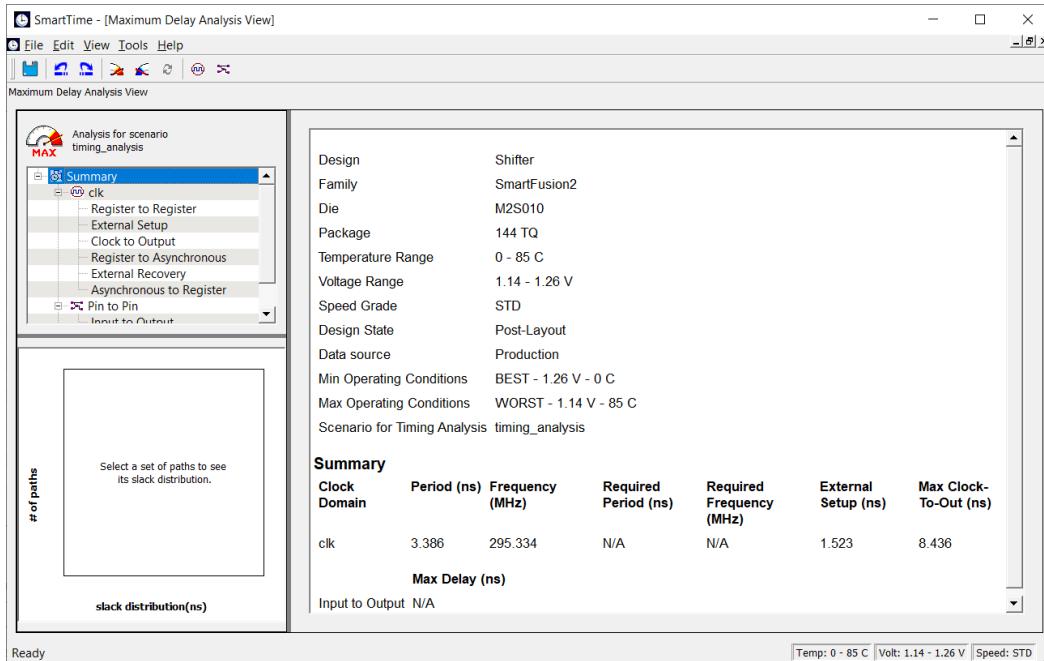
2. Run **Place and Route**.

## PERFORM MAXIMUM DELAY ANALYSIS

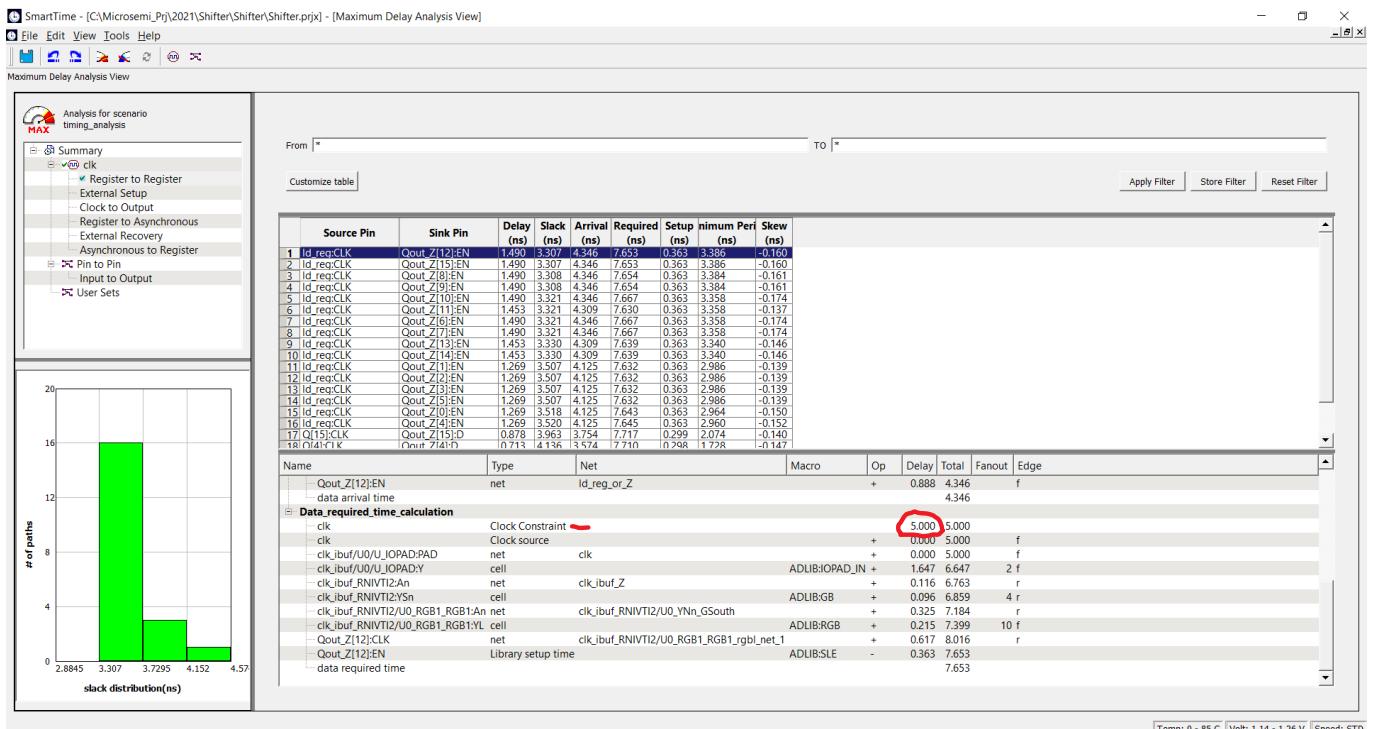
The SmartTime Maximum Delay Analysis window displays the design maximum operating frequency and lists any setup violations. **To perform Maximum Delay Analysis:**

1. Double-Click the **Open SmartTime** button below Place and Route in the Design Flow to open SmartTime. The Maximum Delay analysis window appears (as shown in the figure below). A green check next to the clock name indicates there are no timing violations for that clock domain. The Summary page displays a summary of the clock domain timing performance.





2. In this example, from the CLK summary you can see the maximum clock frequency for CLK is likely almost 300 MHz. The Register to Register summary shows the margin or slack for each path. If the values are all positive then there is no setup timing violations. Your result should look something like this, although it might not be exact.





3. Click to select row 1 and study the timing analysis (resize the Maximum Delay Analysis window as required). The path is from the control block (U1) to the output register (U2). Note that SmartTime uses 5 ns in the data required calculation (as shown in the figure below). This is because the source flip flop uses the rising edge of the clock and the destination flip-flop used the falling edge of the clock.

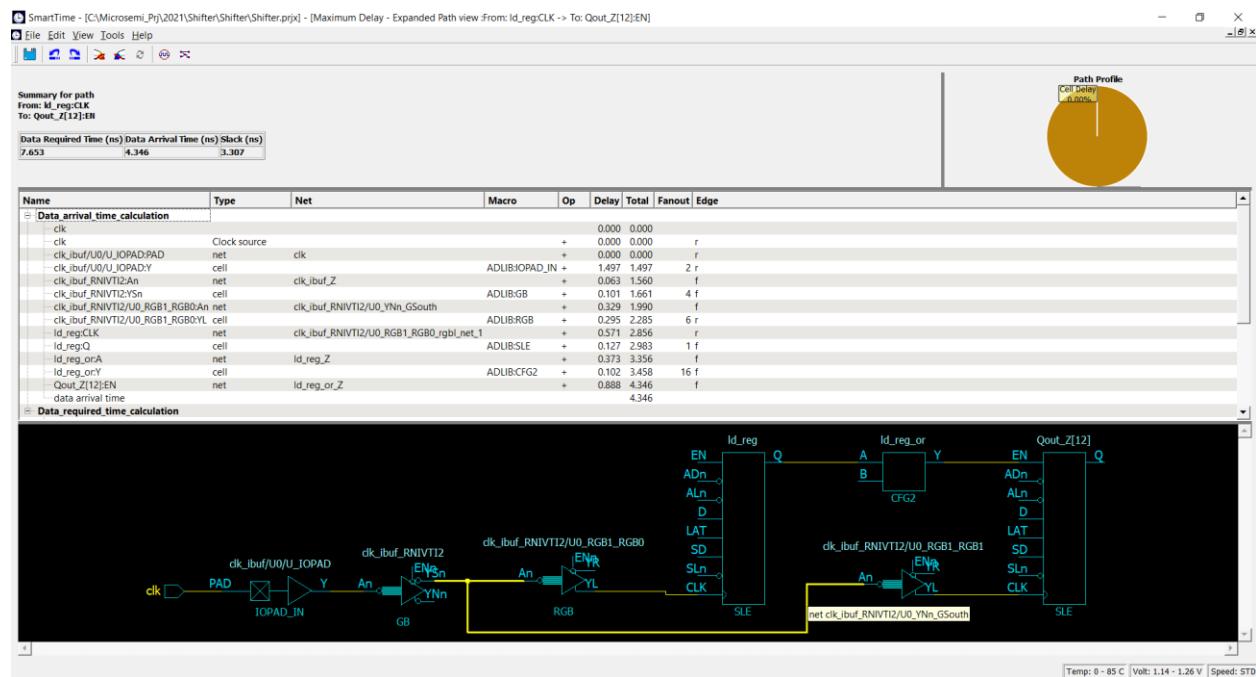
### CROSS PROBING WITH SMARTTIME - DESIGN USING BOTH CLOCK EDGES

You can use SmartTime to cross probe in Designer and analyze your design.

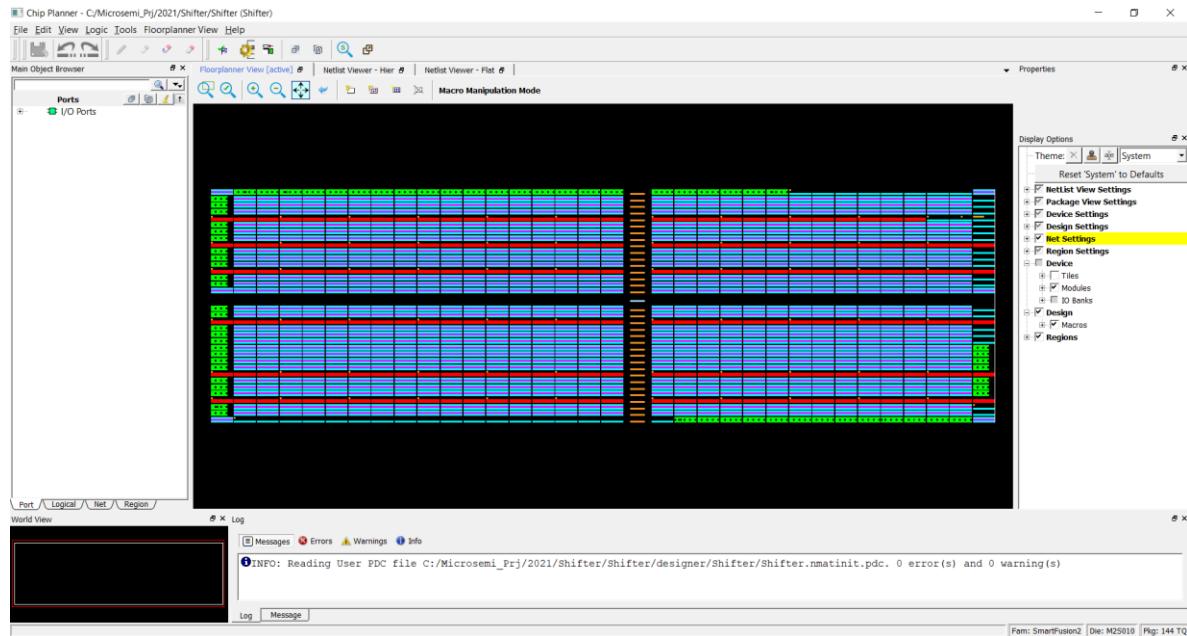
#### To cross probe with SmartTime:

1. Double-click the first row in the Maximum Delay Analysis view to open the **Expanded Path** window (as shown in the figure below). The window shows the required data and arrival time calculation and a schematic of the path.

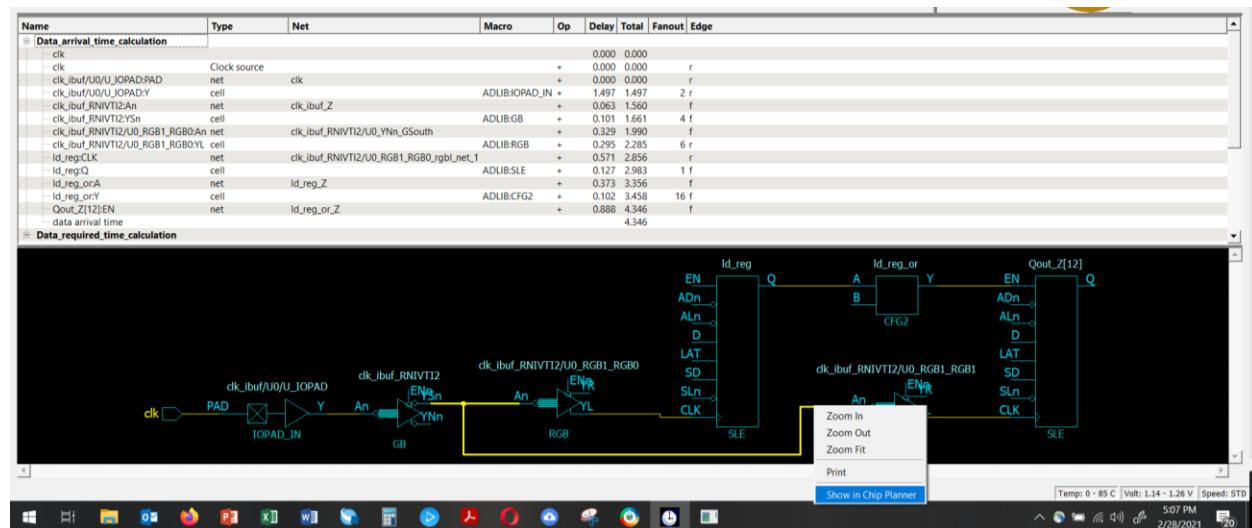
Click and drag in the schematic to view the selected area.



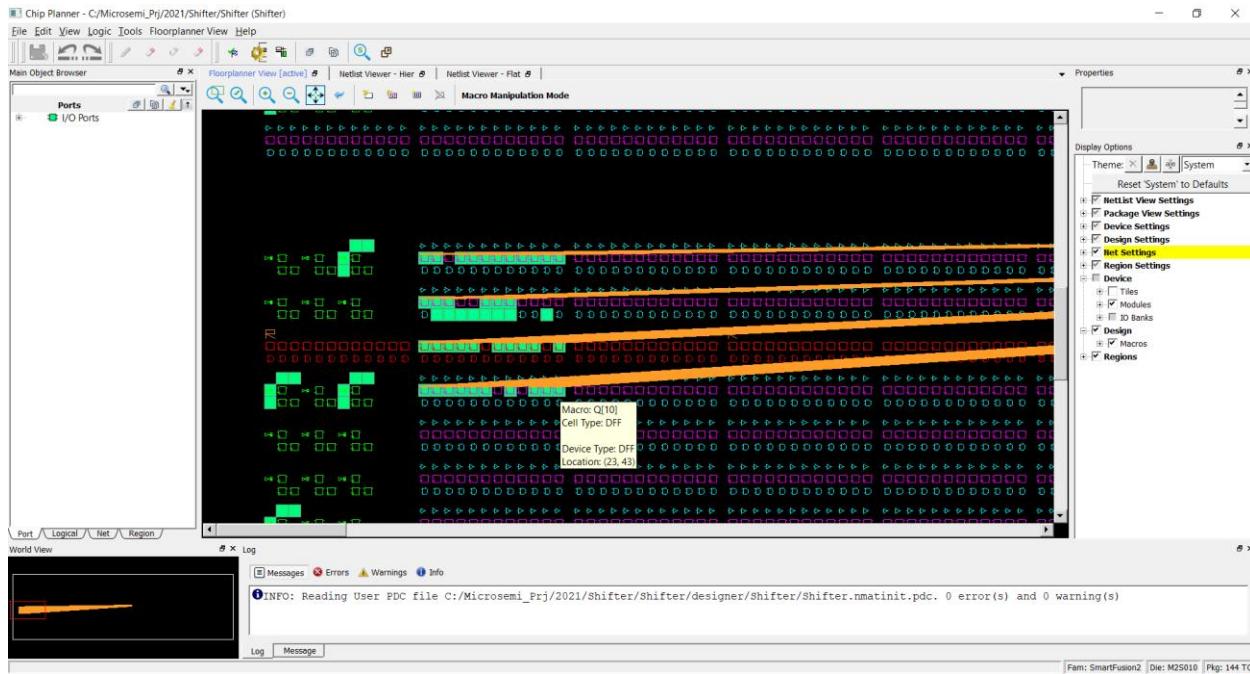
2. In Libero, return to the Constraints Window, and click on the **ChipPlanner tab** to open the tool.



3. In the SmartTime Expanded Path window select an object (such as a net), right-click it and choose **Cross-probe path**, as shown in the figure below.



View **ChipPlanner** and notice that the path you selected in SmartTime is highlighted in ChipPlanner, as shown in the figure below. See the ChipPlanner online help for more information on using the tool.



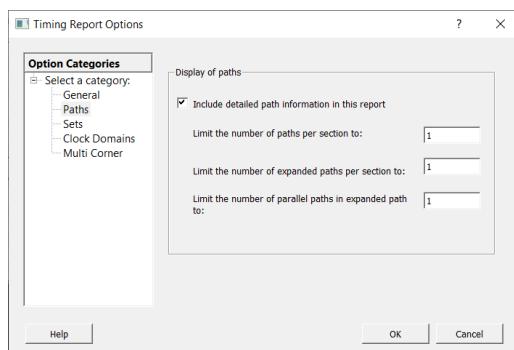
## GENERATE A TIMING REPORT - DESIGN USES BOTH CLOCK EDGES

Timing reports can be generated from SmartTime. Timing reports enable you to quickly determine if there are any timing problems. The timing report lists the following information:

- Design information including device, speed grade and operating conditions.
- Design performance summary (maximum frequency, external setup and hold, minimum and maximum clock-to-out)
- Clock domain details.
- Inter clock domain details.
- Pin to pin timing

The timing report can be printed and saved. **To generate a Timing Report:**

1. In SmartTime from the **Tools** menu, choose **Reports > Timing** to open the Timing Report Options Dialog box, as shown in the figure below.





2. Click the **Paths** category. Limit the number of reported paths to **1**, and click **OK**. The timing report opens in a new window, as shown in the figure below.

```
Timer Report
File Actions Help
Timing Report Max Delay Analysis
SmartTime Version v12.6
Microsemi Corporation - Microsemi Libero Software Release v12.6 (Version 12.900.20.24)
Date: Sun Feb 28 17:20:30 2021

Design: Shifter
Family: SmartFusion2
Die: M2S010
Package: 144 TQ
Temperature Range: 0 ~ 85 C
Voltage Range: 1.14 ~ 1.26 V
Speed Grade: STD
Design State: Post-Layout
Data source: PnD
Min Operating Conditions: BEST - 1.26 V - 0 C
Max Operating Conditions: WORST - 1.14 V - 85 C
Scenario for Timing Analysis: timing_analysis

-----
SUMMARY
Clock Domain: clk
Period (ns): 3.386
Frequency (MHz): 295.334
Required Period (ns): 10.000
Required Frequency (MHz): 100.000
External Setup (ns): 1.523
Max Clock-To-Out (ns): 8.436
Input to Output
Max Delay (ns): N/A
END SUMMARY
-----
Clock Domain clk
SET Register to Register
Path 1
From: ld_reg:CLK
To: Qout_Z[12]:EN
Delay (ns): 1.490
Slack (ns): 3.307
```

The timing report contains the following sections:

- Header
- Summary
- Clock domain details for CLK and expanded path information
- External setup information
- Clock to output delay information

3. Save the timing report as shifter\_timing.rpt and close the report window.

4. Close the timing report, Chip Planner, and SmartTime. Save the Project and close Libero.

If you did the standard installation, in order to get the simulation to work you need to change the path to the SmartFusion2 libraries to

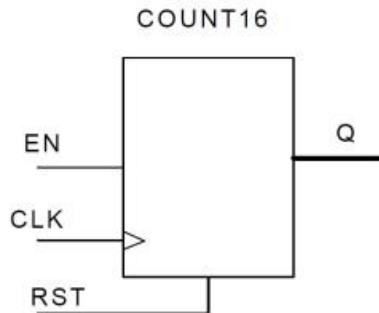
C:/Microsemi/Libero\_SoC\_v12.6/Designer/lib/modelsimpro/precompiled/vlog/smartfusion2

Do this from the Libero top menu in Project->ProjectSettings->Simulation libraries-> SmartFusion2



### III. 16-BIT BINARY COUNTER EXAMPLE

This example describes how to enter a clock constraint, input delay and output delay constraints for the 16-bit counter pictured in the figure below. You will import an SDC file with a clock constraint of 200 MHz and add input delay constraints of 8 ns and an output delay constraint of 5 ns using SmartTime. After routing the design you will analyze the timing and set multi-cycle path constraints to determine the maximum operating frequency.



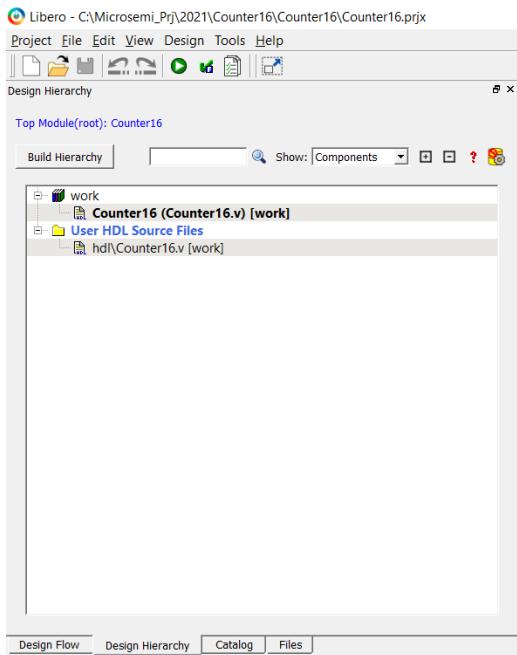
#### SET UP YOUR EXAMPLE DESIGN PROJECT

1. Invoke Libero SoC. From the **Project** menu, choose **New Project**.
2. Enter Shifter for your new project name and browse to a folder for your project location. Enter the following values for the project settings:

- Language: Verilog
- Family: SmartFusion2
- Package: 144 TQFP
- Speed: STD
- Die: M2S010
- Temperature Range: COM
- I/O: LVCMOS 2.5v
- PLL Supply Voltage: 2.5
- VDD supply ramp time: 100 ms.
- Design Templates: None
- HDL Source File: Import Counter16.v from the file provided

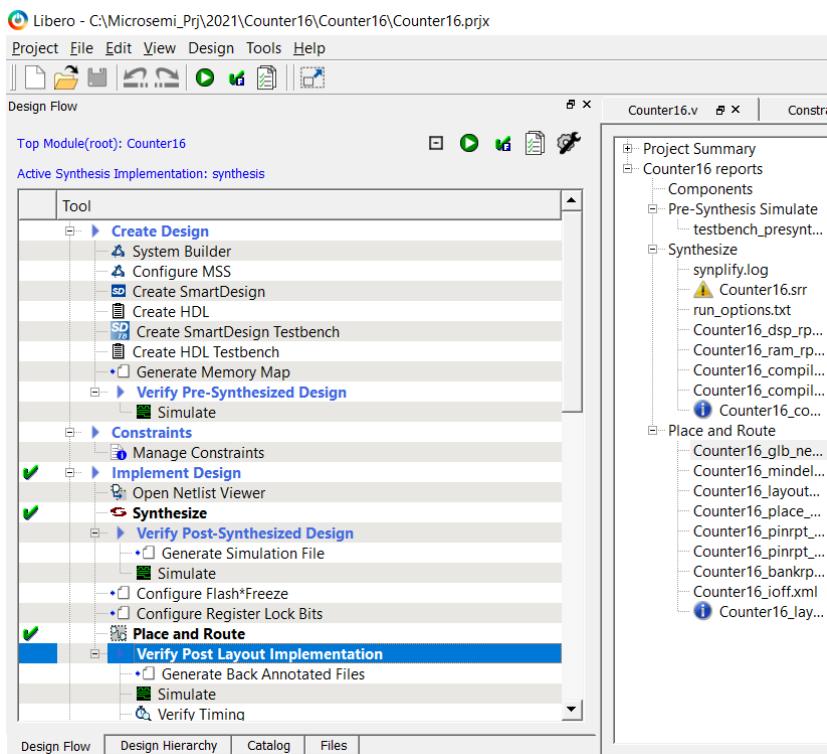
Confirm that the Counter16 design appears in the Design Hierarchy window





You may have to click on the “Build Hierarchy” button, and then right click on the Counter16 file to set it as root. Save the Project.

3. In the Design Flow window, double-click **Synthesize** to run Synplify Pro with default settings. A green check marks appears next to Synthesize when Synthesis is successful (as shown in the figure below).
4. Double-click **Place and Route** in the Design Flow window to run Compile with default settings. A green check mark appears next to Place and Route when it completes successfully (as shown below).





## CREATE A PIN ASSIGNMENT

1. In the **Design Flow window** double-click **Manage Constraints** and then select the first tab, **I/O Attributes** tab followed by Edit-> Edit with I/O Advisor to open the I/O Advisor
2. Click File-> Save and File -> Exit.
3. Verify the I/O Pin assignments. In the Constraints Manager, again select I/O Attributes and Edit with I/O Editor. The ports should be assigned pin numbers similar to those shown below:

Main Object Browser      Port View [active]      Pin View      Package View      Floorplanner View      Netlist Viewer - Hier      Netlist Viewer - Flat

Port Name	Direction	I/O Standard	Pin Number	Locked	Macro Cell	Rank Name	I/O state in FlashFreeze mode	Resistor Pull	I/O available
1 clk	INPUT	LVCMS25	20	<input type="checkbox"/>	INBUF	Bank7	TRISTATE	None	
2 en	INPUT	LVCMS25	144	<input type="checkbox"/>	INBUF	Bank0	TRISTATE	None	
3 Q	OUTPUT	LVCMS25		<input type="checkbox"/>	OUTBUF		TRISTATE	None	
4 Q[0]	OUTPUT	LVCMS25	24	<input type="checkbox"/>	OUTBUF	Bank6	TRISTATE	None	
5 Q[1]	OUTPUT	LVCMS25	30	<input type="checkbox"/>	OUTBUF	Bank6	TRISTATE	None	
6 Q[2]	OUTPUT	LVCMS25	14	<input type="checkbox"/>	OUTBUF	Bank7	TRISTATE	None	
7 Q[3]	OUTPUT	LVCMS25	21	<input type="checkbox"/>	OUTBUF	Bank7	TRISTATE	None	
8 Q[4]	OUTPUT	LVCMS25	27	<input type="checkbox"/>	OUTBUF	Bank6	TRISTATE	None	
9 Q[5]	OUTPUT	LVCMS25	29	<input type="checkbox"/>	OUTBUF	Bank6	TRISTATE	None	
10 Q[6]	OUTPUT	LVCMS25	36	<input type="checkbox"/>	OUTBUF	Bank6	TRISTATE	None	
11 Q[7]	OUTPUT	LVCMS25	10	<input type="checkbox"/>	OUTBUF	Bank7	TRISTATE	None	
12 Q[8]	OUTPUT	LVCMS25	13	<input type="checkbox"/>	OUTBUF	Bank7	TRISTATE	None	
13 Q[9]	OUTPUT	LVCMS25	7	<input type="checkbox"/>	OUTBUF	Bank7	TRISTATE	None	
14 Q[10]	OUTPUT	LVCMS25	23	<input type="checkbox"/>	OUTBUF	Bank6	TRISTATE	None	
15 Q[11]	OUTPUT	LVCMS25	22	<input type="checkbox"/>	OUTBUF	Bank7	TRISTATE	None	
16 Q[12]	OUTPUT	LVCMS25	28	<input type="checkbox"/>	OUTBUF	Bank6	TRISTATE	None	
17 Q[13]	OUTPUT	LVCMS25	16	<input type="checkbox"/>	OUTBUF	Bank7	TRISTATE	None	
18 Q[14]	OUTPUT	LVCMS25	32	<input type="checkbox"/>	OUTBUF	Bank6	TRISTATE	None	
19 Q[15]	OUTPUT	LVCMS25	19	<input type="checkbox"/>	OUTBUF	Bank7	TRISTATE	None	
20 rst	INPUT	LVCMS25	142	<input type="checkbox"/>	INBUF	Bank0	TRISTATE	None	

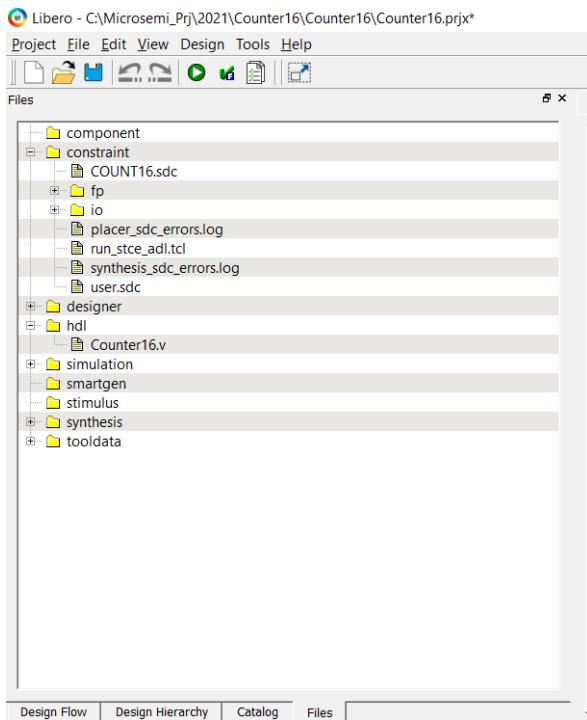
## IMPORT A TIMING CONSTRAINT FILE

The SDC file contains a Timing Constraint of 5.714 ns for the CLK of the COUNT16 design.

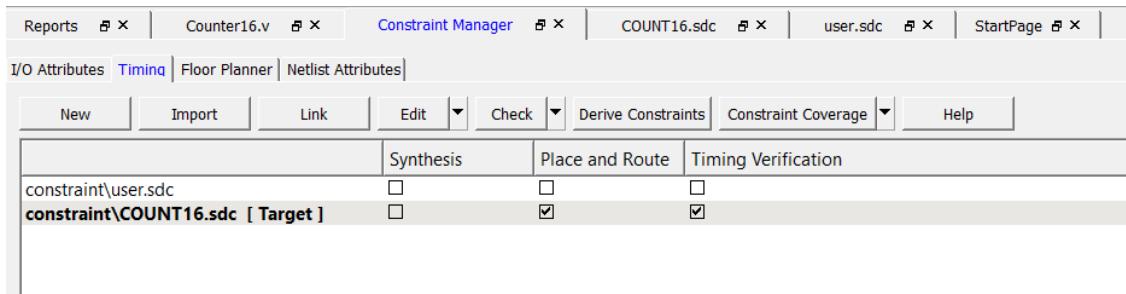
### To import the Timing Constraint:

1. From the **File** menu, choose **Import > Timing Constraint (SDC) Files**.
2. Navigate to the folder that contains the file COUNT16.sdc. Click to select it and click Open.
3. A pop-up dialog may appear to ask if you want to organize the constraint files for your current root (COUNT16). Click **Yes** to continue.
4. In the Libero SoC Files window, check that the COUNT16.sdc file appears in the constraint directory and that COUNT16.v appears in the synthesis directory, as shown in the figure below.





5. In the Design Flow window, run Place and Route after verifying the Timing constraints are similar to this:



You may have to right-click on the sdc file to set it as the Target constraint.

**Make a note of the Fmax.**

6. In the Constraint Editor, click the **Timing Tab** and choose **Edit Place and Route Constraints**. The SmartTime Constraints Editor opens.

7. Expand **Requirements** and click **Clock**. Notice the CLK Constraint of 5.714 ns period.

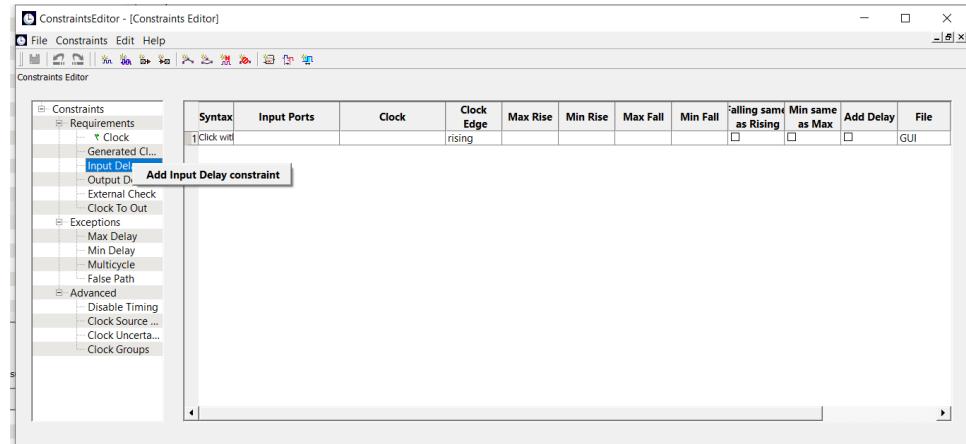
### ADD AN INPUT DELAY CONSTRAINT

Input Delay is part of the path delay budgeting. It makes allowances for delays external to the FPGA so that the external setup requirements to the FPGA can be met. If external setup requirements are not met, the design may not work on the board.

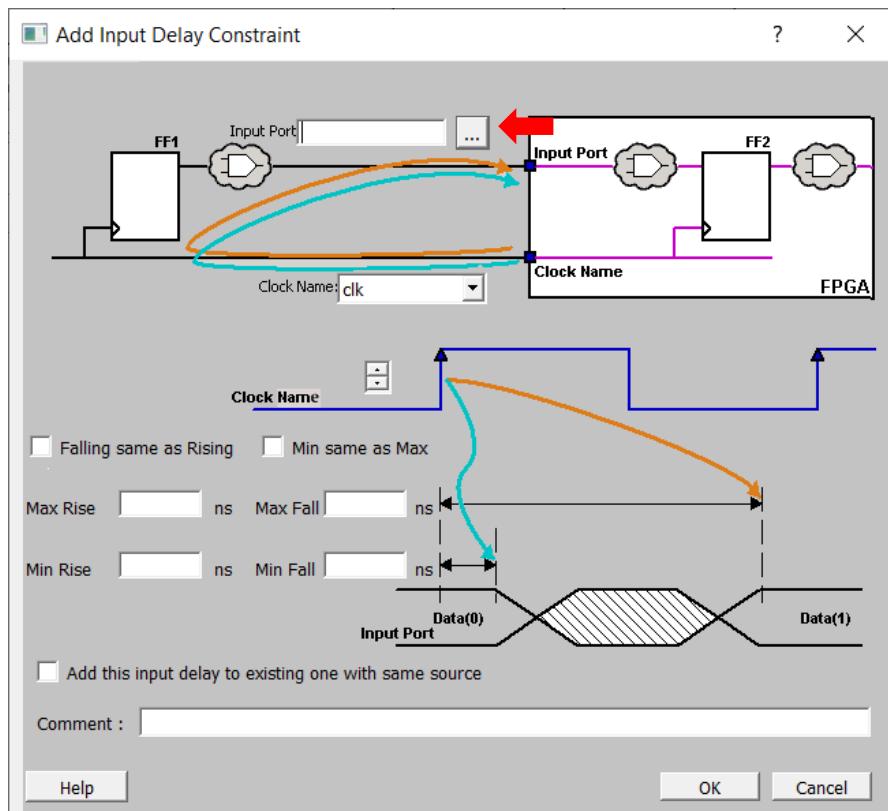
**To add an input delay constraint for the EN and RST ports:**



1. From the **Constraints Editor Requirements**, right-click on Input Delay and then choose **Constraint > Input Delay**.

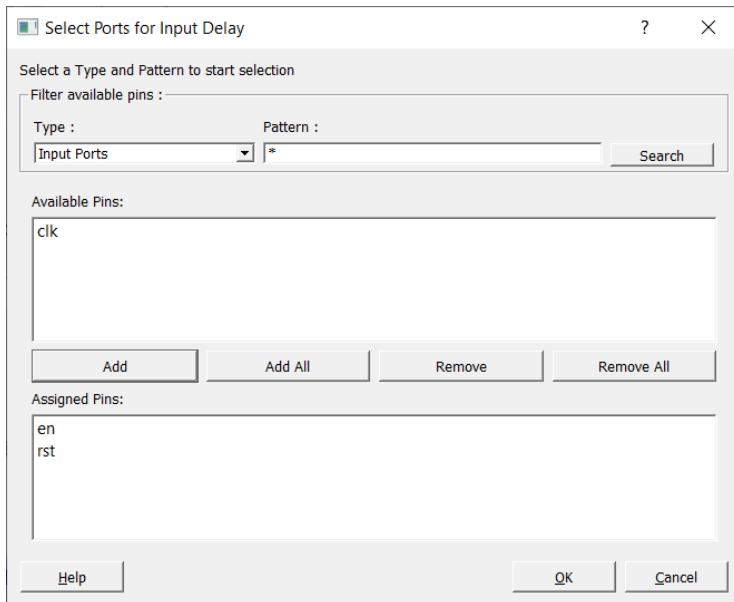


The Set Input Delay Constraint dialog box opens, as shown in the figure below.



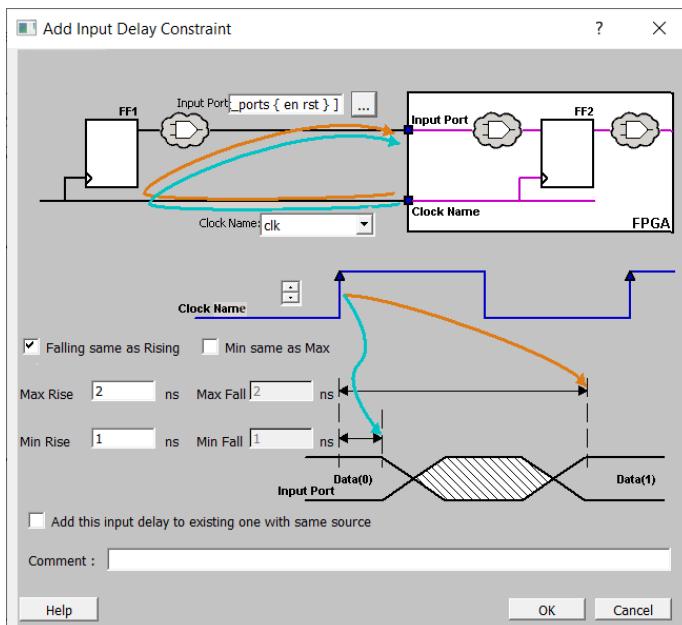
3. Select the Input port for the input delay constraint. Click the **Browse** button to open the Select Ports for Input Delay dialog box.

4. Click on Search. Select the ports **EN** and **RST** and click **Add** to move the pins to Assigned Pins list (as shown in the figure below). Click **OK** to continue.



5. Enter the following values in the **Set Input Delay Constraint** dialog box (as shown in the figure below):

- **Clock Port:** Select clk from the drop down menu.
- **Falling the same as Rising:** check
- **Max Rise:** 2 ns
- **Min Rise:** 1 ns





6. Click **OK** to continue.

Your new Input Delay constraints are visible in the SmartTime Constraints Editor, as shown in the figure below.

The screenshot shows the SmartTime Constraints Editor window. The left sidebar has a tree view under 'Constraints Requirements' with nodes like Clock, Generated Cl..., Input Delay, Output Delay, External Check, Clock To Out, Exceptions, Max Delay, Min Delay, Multicycle, False Path, Advanced, Disable Timing, Clock Source ..., Clock Uncerta..., and Clock Groups. The 'Input Ports' tab is selected in the main area, showing a table:

Syntax	Input Ports	Clock	Clock Edge	Max Rise	Min Rise	Max Fall	Min Fall	Falling same as Rising	Min same as Max	Add Delay	File
1 Click with [get_ports { en_rst }] clk			rising					<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	GUI
2	[get_ports { en_rst }] clk		rising	2.000	1.000	2.000	1.000	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	C:\Micro...

The status bar at the bottom shows the file path: C:\Microsemi\_Prj\2021\Counter16\Counter16\constraint\COUNT16.sdc.

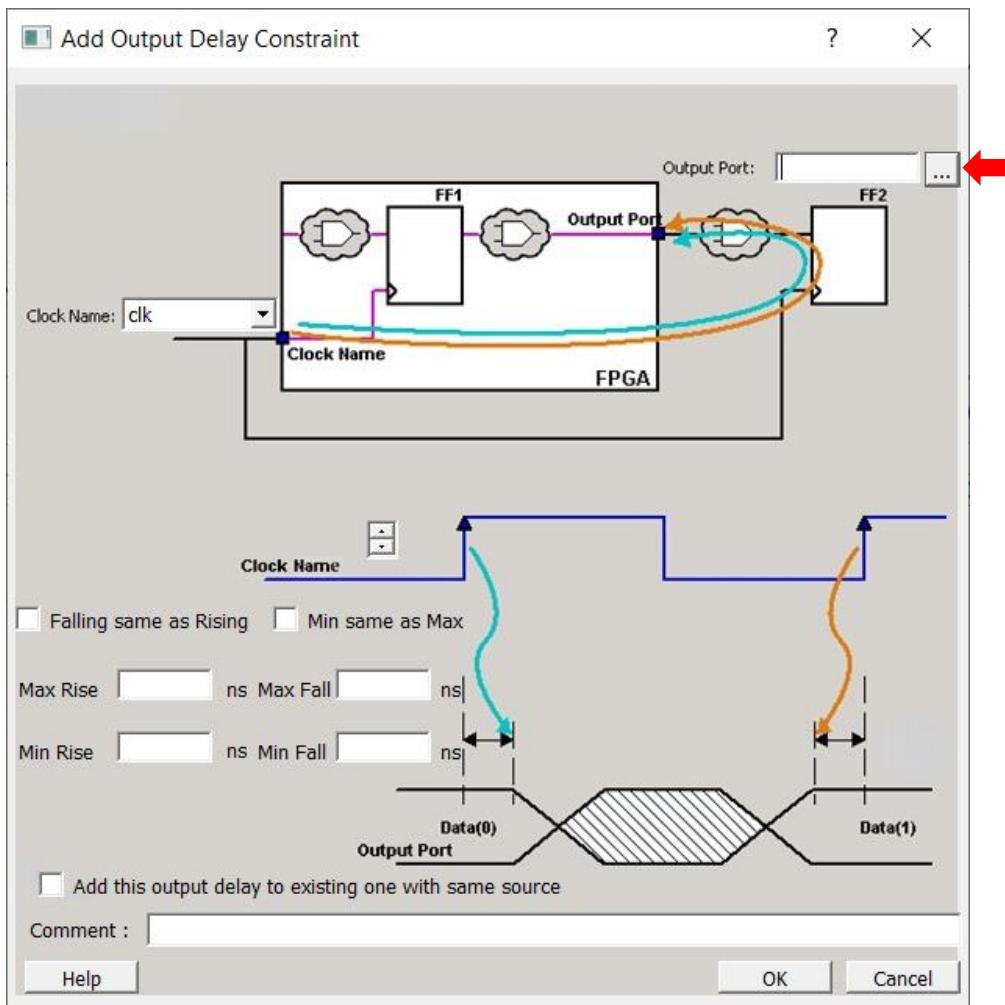
### ADD AN OUTPUT DELAY CONSTRAINT

Output Delay is part of the path delay budgeting. It makes allowances for delays external to the FPGA for the output ports of the design. If external output delay requirements are not met, the design may not work on the board. **To add an output delay constraint:**

- From the **Constraints Editor Requirements**, right-click on Output Delay and then choose **Constraint > Output Delay**.

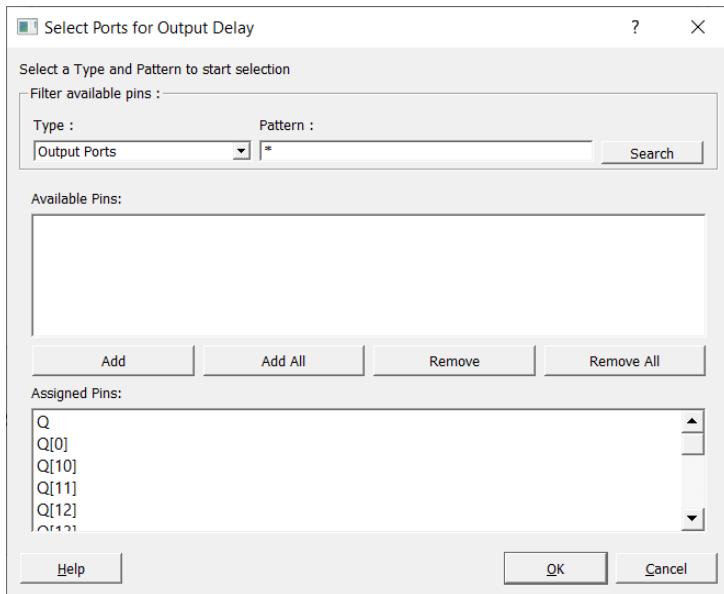
The screenshot shows the SmartTime Constraints Editor window. The left sidebar has a tree view under 'Constraints Requirements' with nodes like Clock, Generated Cl..., Input Delay, Output Delay, External, Clock To Out, Exceptions, Max Delay, Min Delay, Multicycle, False Path, Advanced, Disable Timing, Clock Source ..., Clock Uncerta..., and Clock Groups. The 'Output Delay' node is selected. A context menu is open over it, with the option 'Add Output Delay constraint' highlighted in blue. The 'Input Ports' tab is selected in the main area, showing the same table as the previous screenshot.

The Set output Delay Constraint dialog box opens, as shown in the figure below.



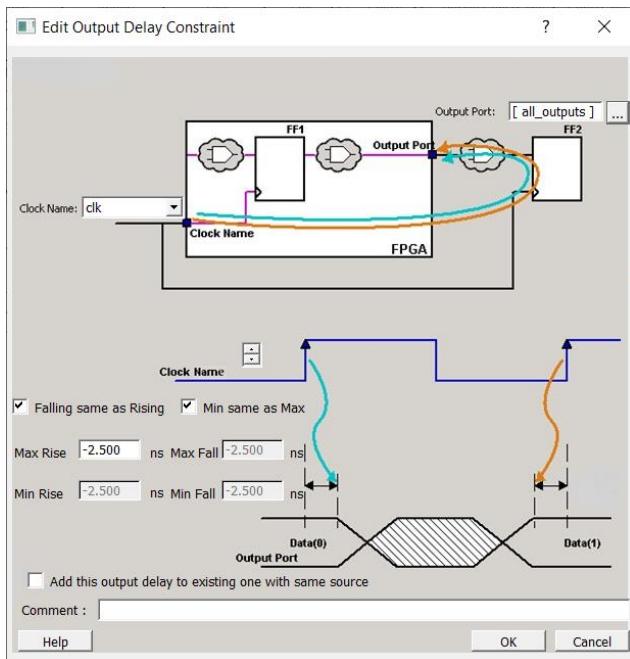
3. Select the Output port for the input delay constraint. Click the **Browse** button to open the Select Ports for Output Delay dialog box.
4. Click on Search. Click **Add All** to add all ports to the Assigned Pins list. Click **OK** to continue.





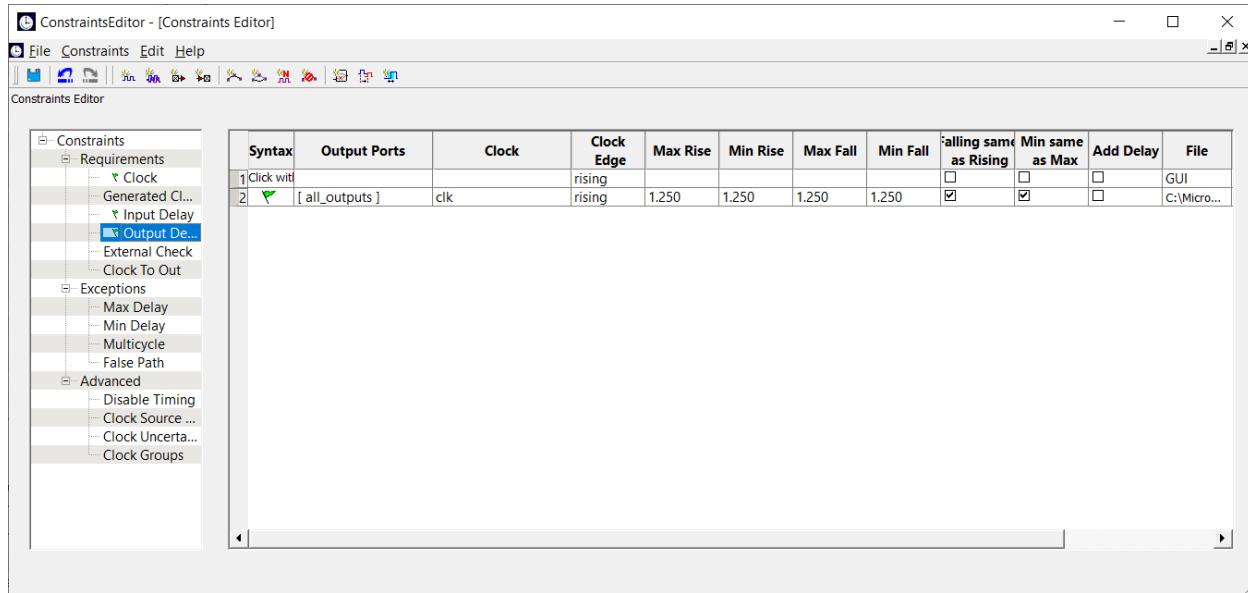
5. Enter the following values in the Set Output Delay Constraint dialog box (as shown in the figure above):

- **Clock Port:** Select **CLK** from the drop down menu
- Enable **Use same value for min and max, and Falling same as Rising**
- **Maximum Delay Rise:** -2.5 ns





6. Click **OK** to continue. The Output Delay constraint appears in the SmartTime Constraints Editor, as shown in the figure below.



7. From the **File** menu, choose **Save** to save your changes.

8. From **File** menu, choose **Exit** to close the Constraints Editor.

## PLACE AND ROUTE THE 16-BIT BINARY COUNTER DESIGN

**To run Layout on the design 'Counter16':**

1. In the Libero Design Flow, right-click **Place and Route**.
2. Choose Configure Options and click the checkbox to enable **Timing-Driven** layout in Layout Options and leave the other values at the default settings. Click **OK** to continue. Double click on Place and Route to complete the design.
3. Open SmartTime. **Write down the new Fmax** listed in the clk Summary.

