

Parity Generators and Parity Checkers

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Parity Generator and Parity Check

- Majority of modern communication is Digital in nature i.e., it is a combination of 1's and 0's.
- The digital data is transmitted either through wires (in case of wired communication) or wireless.
- Even in an advanced mode of communication, there will be errors while transmitting data (due to noise).
- The simplest of errors is corruption of a bit i.e., a 1 may be transmitted as a 0 or vice-versa.
- To confirm whether the received data is the intended data or not, we should be able to detect errors at the receiver.
- we will learn about Parity Bit, Even Parity, Odd Parity, Parity Generator and Parity Checker with a practical example and practical circuit.

What is Parity Bit?

- The parity generating technique is one of the most widely used error detection techniques for the data transmission.
- In digital systems, when binary data is transmitted and processed, data may be subjected to noise so that such noise can alter 0s (of data bits) to 1s and 1s to 0s.
- Hence, a Parity Bit is added to the word containing data in order to make number of 1s either even or odd.
- The message containing the data bits along with parity bit is transmitted from transmitter to the receiver.
- At the receiving end, the number of 1s in the message is counted and if it doesn't match with the transmitted one, it means there is an error in the data. Thus, the Parity Bit is used to detect errors, during the transmission of binary data.

Parity Generator and Checker

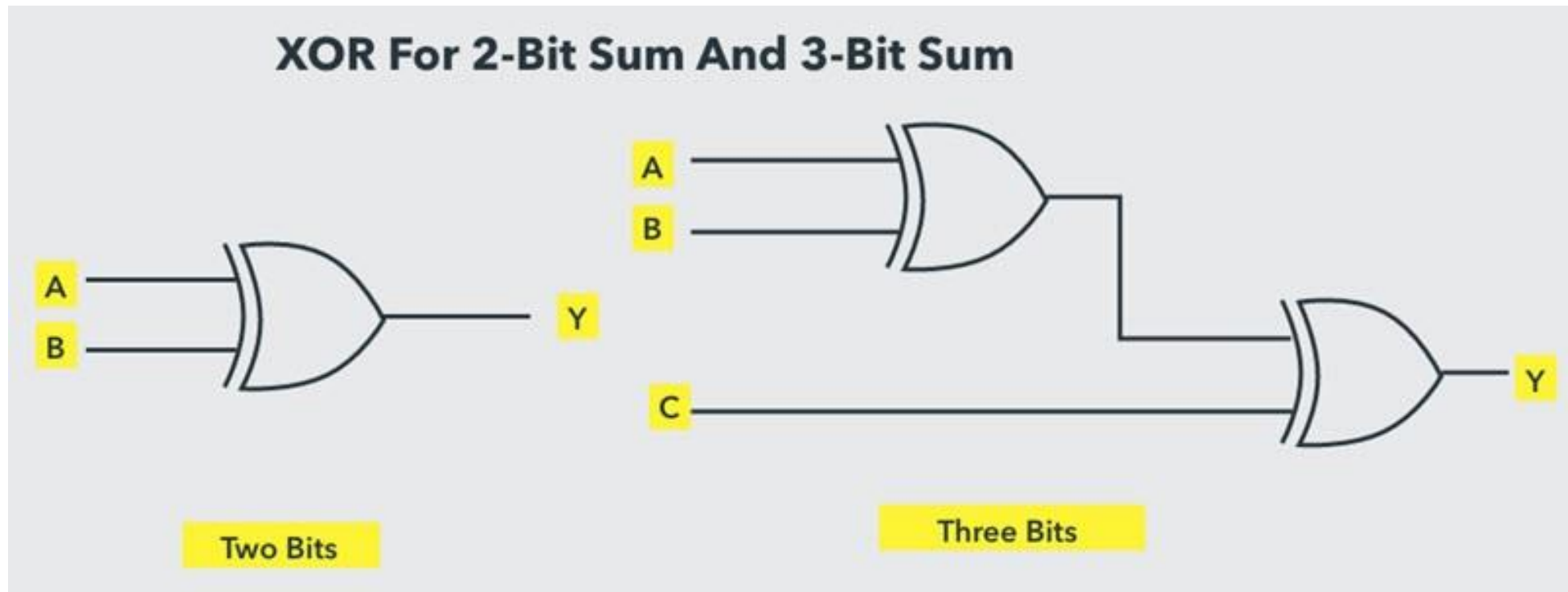
- A Parity Generator is a combinational logic circuit that generates the parity bit in the transmitter.
- A circuit that checks the parity in the receiver is called Parity Checker.
- A combined circuit or device of parity generators and parity checkers are commonly used in digital systems to detect the single bit errors in the transmitted data.

Even Parity and Odd Parity

- The sum of the data bits and parity bits can be even or odd. In even parity, the added parity bit will make the total number of 1s an even number, whereas in odd parity, the added parity bit will make the total number of 1s an odd number.
- The basic principle involved in the implementation of parity circuits is that sum of odd number of 1s is always 1 and sum of even number of 1s is always 0.
- Such error detecting and correction can be implemented by using Ex-OR gates (since Ex-OR gate produce zero output when there are even number of inputs).

Even Parity and Odd Parity

- To produce two bits sum, one Ex-OR gate is sufficient whereas for adding three bits, two Ex-OR gates are required as shown in below figure.



Parity Generator

- It is combinational circuit that accepts an $n-1$ bit data and generates the additional bit that is to be transmitted with the bit stream. This additional or extra bit is called as a Parity Bit.
- In even parity bit scheme, the parity bit is '0' if there are even number of 1s in the data stream and the parity bit is '1' if there are odd number of 1s in the data stream.
- In odd parity bit scheme, the parity bit is '1' if there are even number of 1s in the data stream and the parity bit is '0' if there are odd number of 1s in the data stream. Let us discuss both even and odd parity generators.

Even Parity Generator

- Let us assume that a 3-bit message is to be transmitted with an even parity bit. Let the three inputs A, B and C are applied to the circuit and output bit is the parity bit P. The total number of 1s must be even, to generate the even parity bit P.
- The figure shows the truth table of even parity generator in which 1 is placed as parity bit in order to make all 1s as even when the number of 1s in the truth table is odd.

3-bit message			Even parity bit generator (P)
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Even Parity Generator

- The K-map simplification for 3-bit message even parity generator is

K-Map For 3-Bit Even Parity Generator

A \ BC	00	01	11	10
0	0	1	0	1
1	1	0	1	0

The K-map is a 2x4 grid. The columns are labeled 00, 01, 11, and 10. The rows are labeled 0 and 1. The values in the cells are: (0,00)=0, (0,01)=1, (0,11)=0, (0,10)=1; (1,00)=1, (1,01)=0, (1,11)=1, (1,10)=0. There are four groups of 1s circled: (0,01), (0,10), (1,00), and (1,11). These groups represent the simplified Boolean expression for the even parity generator: $P = B \oplus C \oplus A$.

Even Parity Generator

- From the above truth table, the simplified expression of the parity bit can be written as

$$P = \bar{A} \bar{B} C + \bar{A} B \bar{C} + A \bar{B} \bar{C} + A B C$$

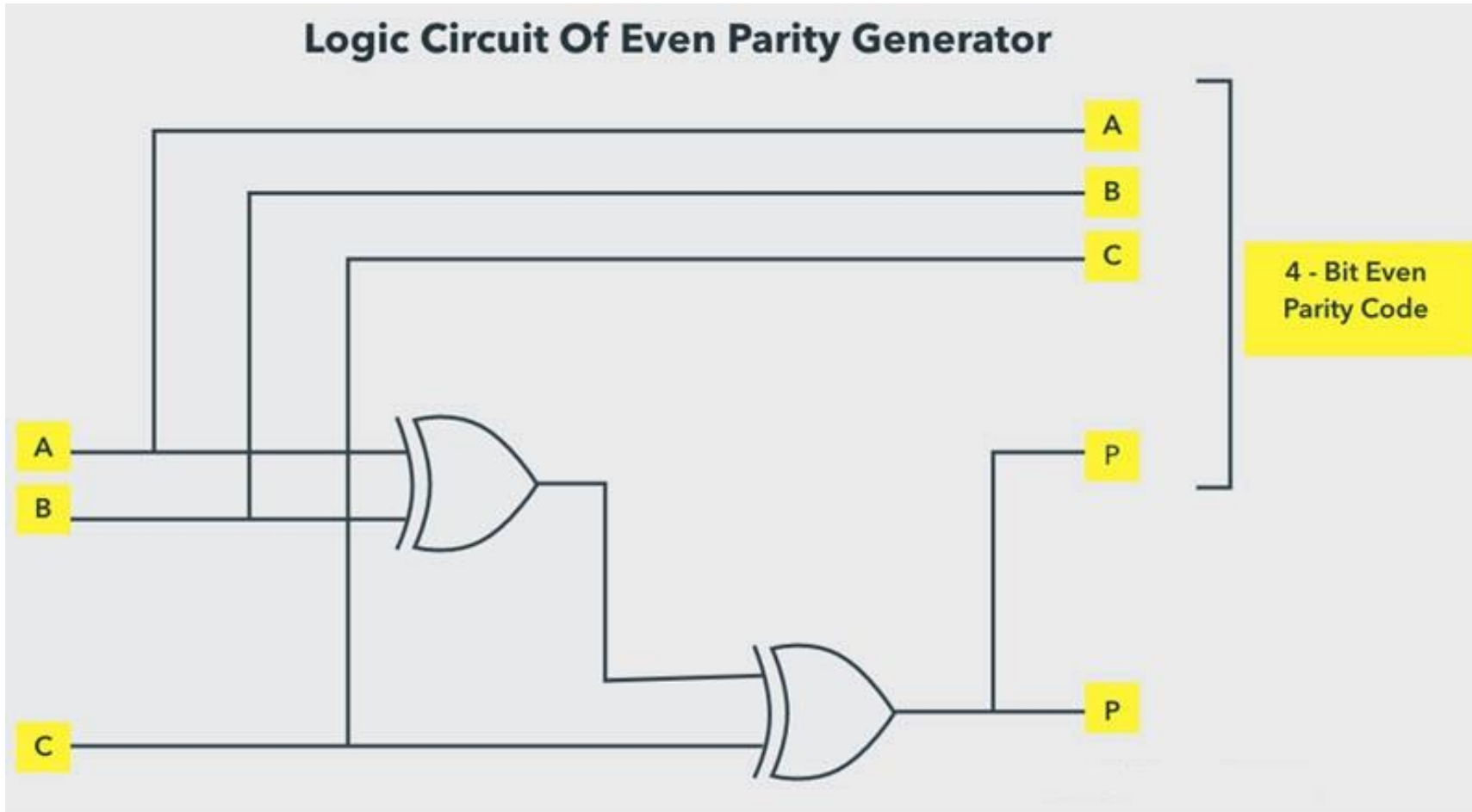
$$= \bar{A} (\bar{B} C + \underline{B} \bar{C}) + A (\bar{B} \bar{C} + B C)$$

$$= \bar{A} (B \oplus C) + A (\overline{B \oplus C})$$

$$P = A \oplus B \oplus C$$

Even Parity Generator

- The above expression can be implemented by using two Ex-OR gates. The logic diagram of even parity generator with two Ex – OR gates is shown below.



Odd Parity Generator

- Let us consider that the 3-bit data is to be transmitted with an odd parity bit. The three inputs are A, B and C and P is the output parity bit. The total number of bits must be odd in order to generate the odd parity bit.
- In the given truth table below, 1 is placed in the parity bit in order to make the total number of bits odd when the total number of 1s in the truth table is even.

3-bit message			Odd parity bit generator (P)
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Odd Parity Generator

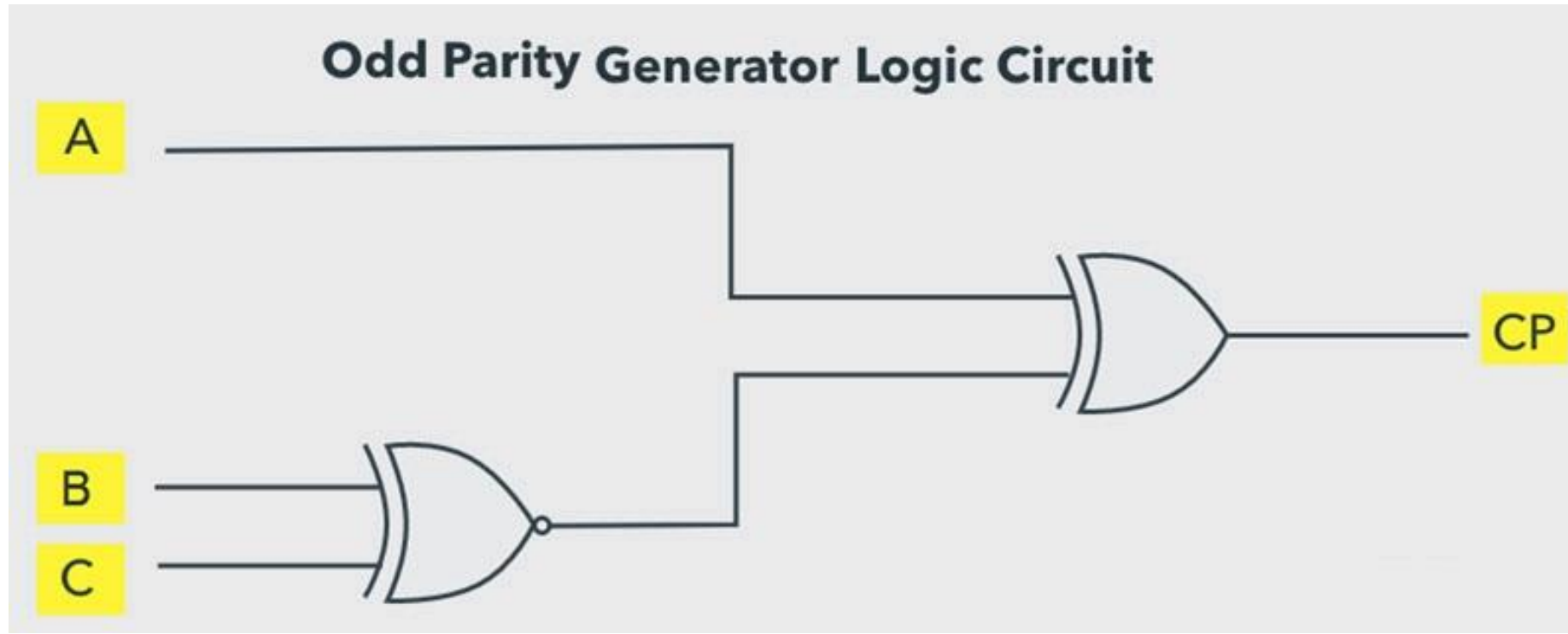
- The truth table of the odd parity generator can be simplified by using K-map as

K-Map For 3-Bit Odd Parity Generator

	BC			
	00	01	11	10
A = 0	1	0	1	0
A = 1	0	1	0	1

Odd Parity Generator

- The output parity bit expression for this generator circuit is obtained as
- $P = A \oplus (B \oplus C)'$



Parity Check

- It is a logic circuit that checks for possible errors in the transmission. This circuit can be an even parity checker or odd parity checker depending on the type of parity generated at the transmission end. When this circuit is used as even parity checker, the number of input bits must always be even.

Even Parity Checker

- Consider that three input message along with even parity bit is generated at the transmitting end. These 4 bits are applied as input to the parity checker circuit, which checks the possibility of error on the data. Since the data is transmitted with even parity, four bits received at circuit must have an even number of 1s.
- If any error occurs, the received message consists of odd number of 1s. The output of the parity checker is denoted by PEC (Parity Error Check).
- The below table shows the truth table for the Even Parity Checker in which $PEC = 1$ if the error occurs, i.e., the four bits received have odd number of 1s and $PEC = 0$ if no error occurs, i.e., if the 4-bit message has even number of 1s.

4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Even Parity Checker

- The above truth table can be simplified using K-map as shown below.

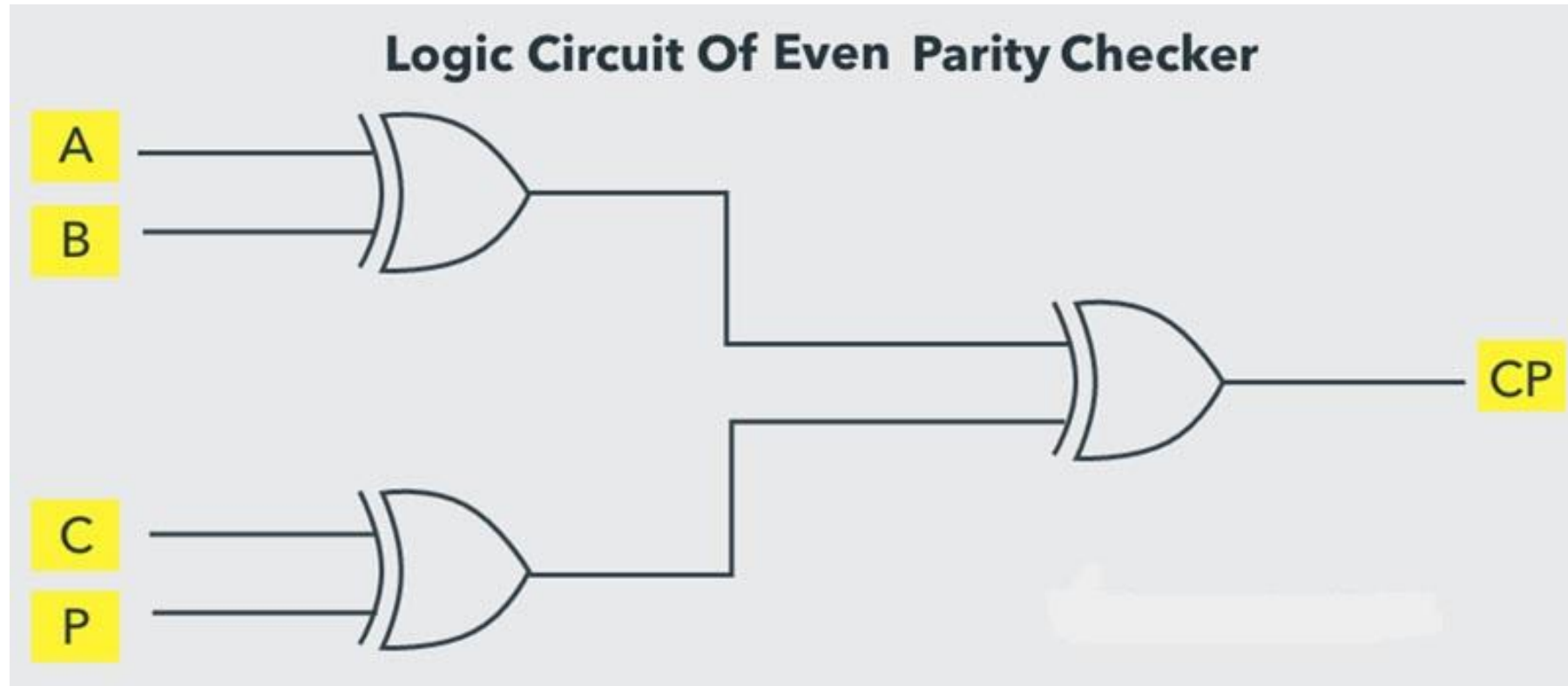
K-Map For Even Parity Checker

		cp			
AB		00	01	11	10
00	0	0	1	0	1
01	4	1	0	1	0
11	12	0	1	0	1
10	8	1	0	1	0

$$\begin{aligned}
 \text{PEC} &= \overline{A} \overline{B} (\overline{C} P + C \overline{P}) + \overline{A} B (\overline{C} \overline{P} + C P) + A B (\overline{C} P + C \overline{P}) + A \overline{B} (\overline{C} \overline{P} + C P) \\
 &= \overline{A} \overline{B} (C \oplus P) + \overline{A} B (\overline{C \oplus P}) + A B (C \oplus P) + A \overline{B} (\overline{C \oplus P}) \\
 &= (\overline{A} \overline{B} + A B) (C \oplus P) + (\overline{A} B + A \overline{B}) (\overline{C \oplus P}) \\
 &= (A \oplus B) \oplus (C \oplus P)
 \end{aligned}$$

Even Parity Checker

- The above logic expression for the even parity checker can be implemented by using three Ex-OR gates as shown in figure. If the received message consists of five bits, then one more Ex-OR gate is required for the even parity checking.



Odd Parity Checker

- Consider that a three bit message along with odd parity bit is transmitted at the transmitting end. Odd parity checker circuit receives these 4 bits and checks whether any error are present in the data.
- If the total number of 1s in the data is odd, then it indicates no error, whereas if the total number of 1s is even then it indicates the error since the data is transmitted with odd parity at transmitting end.
- The below figure shows the truth table for odd parity generator where $PEC = 1$ if the 4-bit message received consists of even number of 1s (hence the error occurred) and $PEC = 0$ if the message contains odd number of 1s (that means no error).

4-bit received message				Parity error check C_p
A	B	C	P	
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Odd Parity Checker

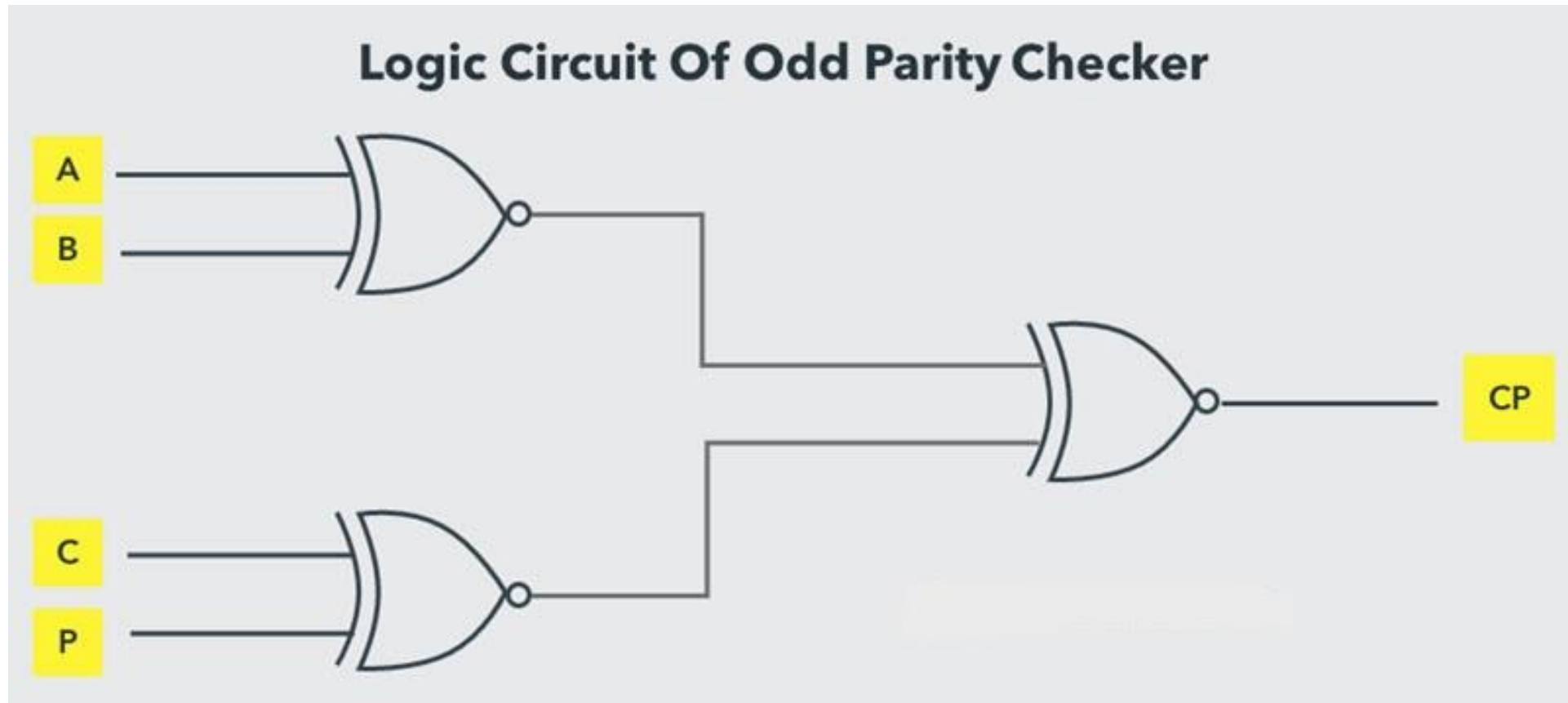
- The expression for the PEC in the above truth table can be simplified by K-map as shown below.

K-Map for 3-bit Odd Parity Checker

		CP			
		00	01	11	10
AB	00	0 1	1 0	3 1	2 0
	01	4 0	5 1	7 0	6 1
	11	12 1	13 0	15 1	14 0
	10	8 0	9 1	11 0	10 1

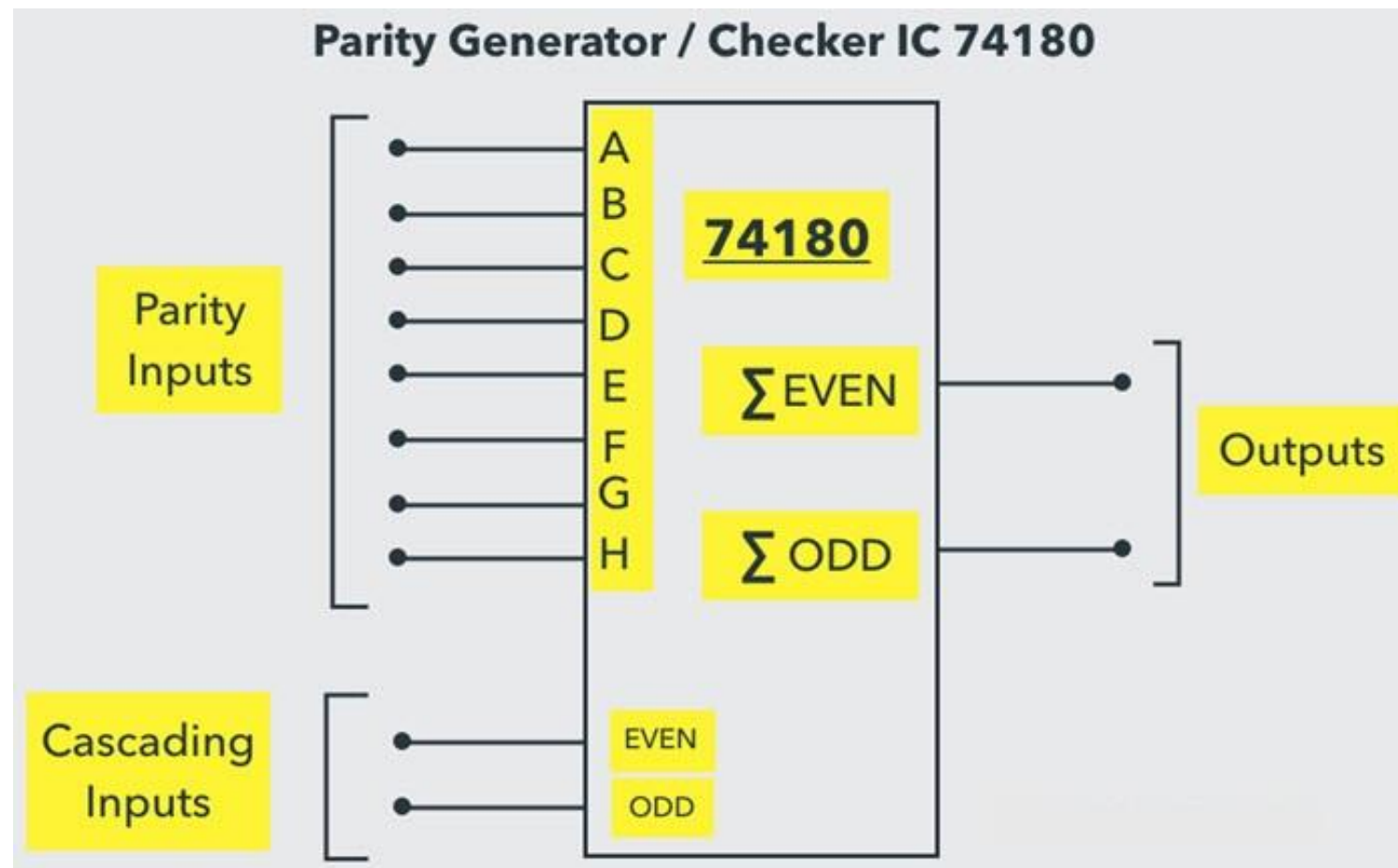
Odd Parity Checker

- After simplification, the final expression for the PEC is obtained as
$$PEC = (A \text{ Ex-NOR } B) \text{ Ex-NOR } (C \text{ Ex-NOR } P)$$



Parity Generator/Checker ICs

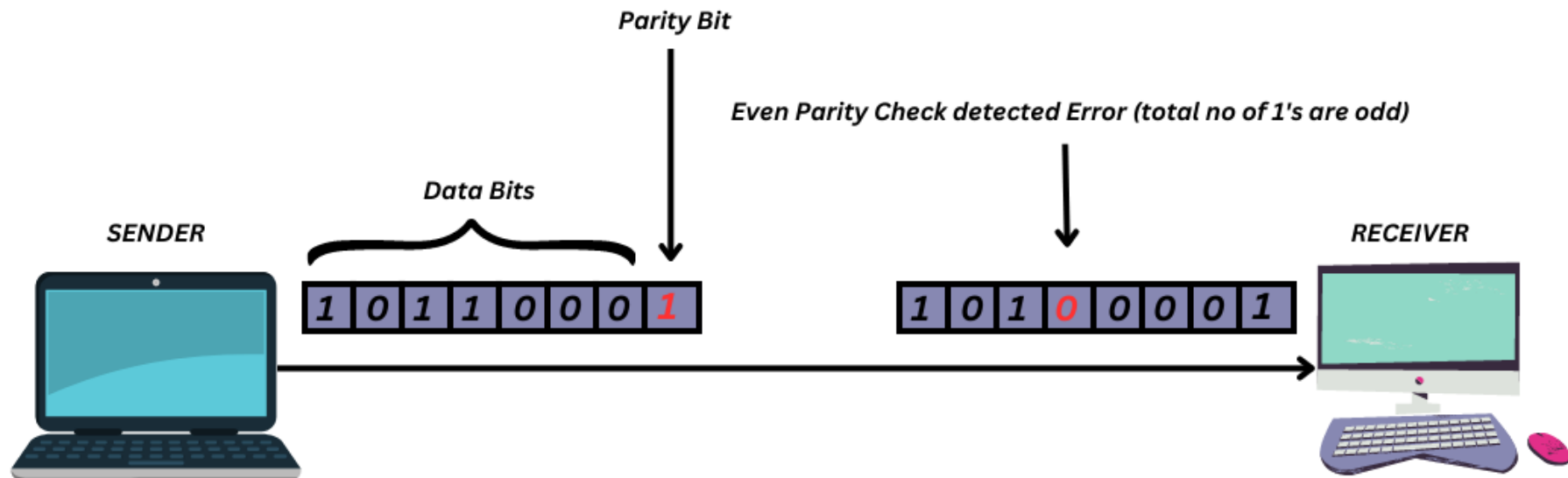
- There are different types of parity generator /checker ICs are available with different input configurations such as 5-bit, 4-bit, 9-bit, 12-bit, etc. One of the most commonly used and standard type of parity generator/checker IC is 74180.



Errors and Error Detection

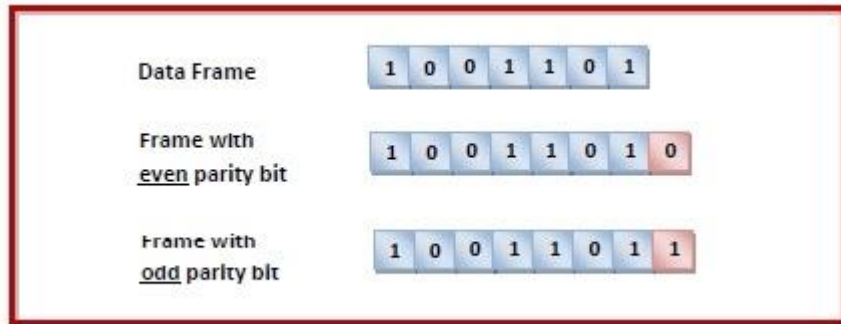
Without addition of redundant bits, it is not possible to detect errors in the received message. There are 3 ways in which we can detect errors in the received message :

1. Parity Bit
2. CheckSum
3. Cyclic Redundancy Check (CRC)

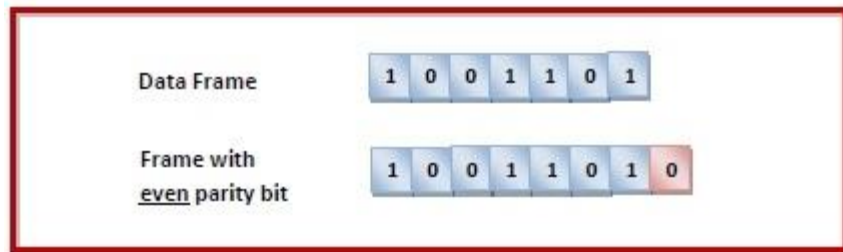


Errors and Error Detection

Error Detection by Parity Check



Sender's End



Receiver's End

