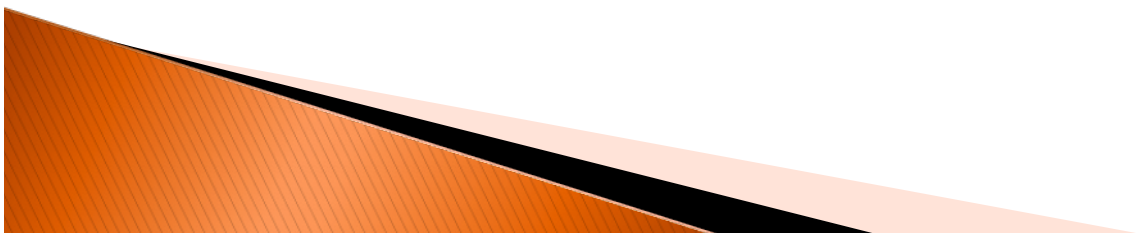
Programmable Interrupt Controller

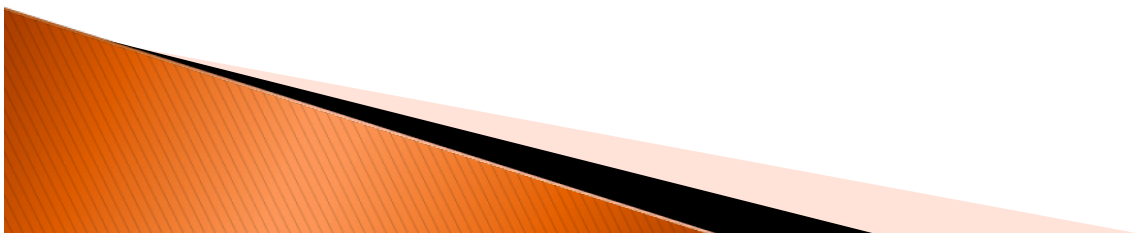
(8259A)

8259

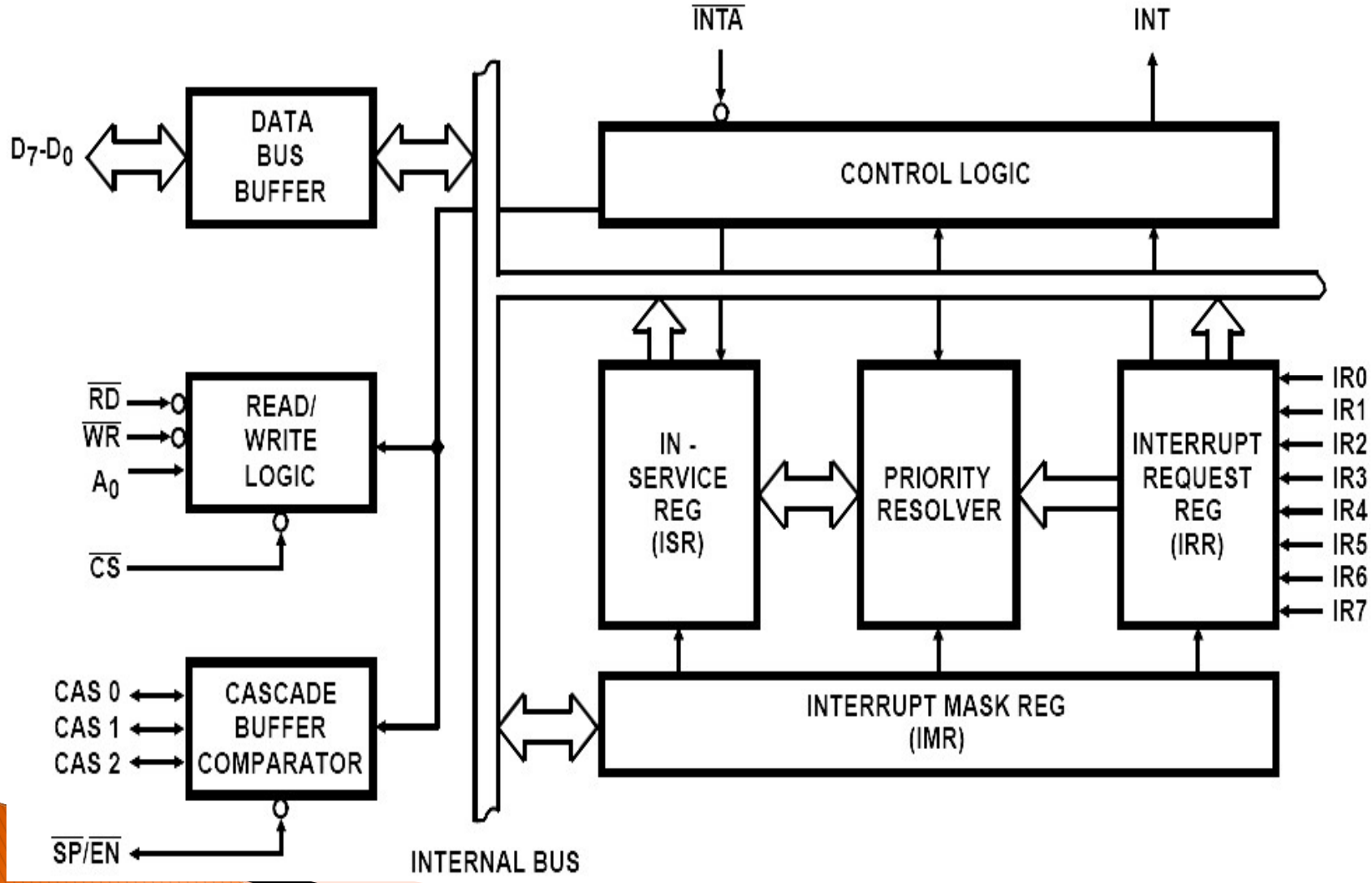
- Programmable Interrupt Controller designed to work with Intel microprocessors 8085, 8086 and 8088.
- 8259 – works with 8 bit processors
- 8259A – works with 8 bit and 16 –bit processors



- Manage 8 interrupts according to the instructions written into its control registers. [Expandable upto 64 in the cascaded mode]
- Prioritize these inputs
- Resolve 8 levels of interrupt priorities in a variety of modes, such as fully nested mode, automatic rotation mode, and specific rotation mode.



Block Diagram of the 8259A

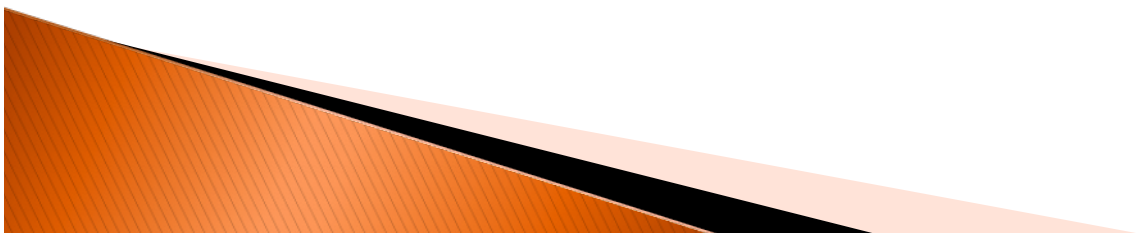


Pin description

PIN	DESCRIPTION
D7 - D0	Data Bus (Bidirectional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A0	Command Select Address
$\overline{CS}$	Chip Select
CAS 2 - CAS 0	Cascade Lines
$\overline{SP}/\overline{EN}$	Slave Program Input Enable
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0 - IR7	Interrupt Request Inputs

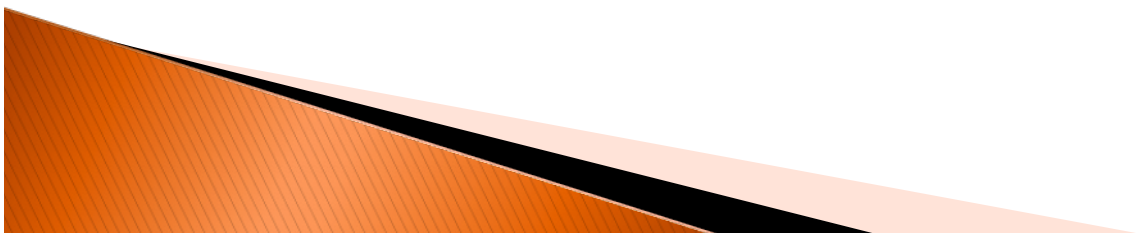
Interrupt Request Register (IRR) and In-Service Register(ISR)

- The IRR is used to indicate all the interrupt levels which are requesting service
- ISR is used to store all the interrupt levels which are currently being serviced.



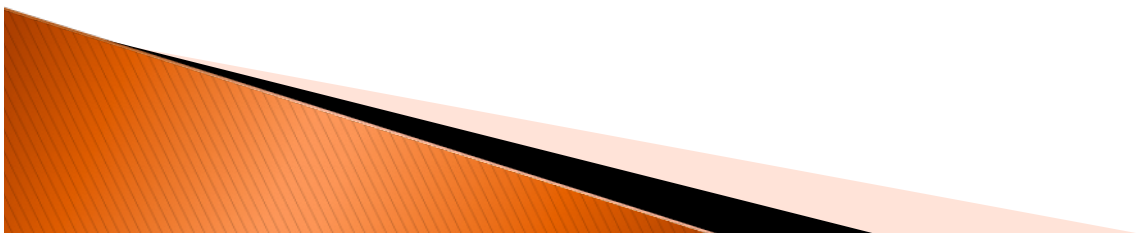
Priority Resolver

- This logic block determines the priorities of the bits set in the IRR.
- The highest priority is selected and strobed into the corresponding bit of the ISR during the INTA sequence.



Interrupt Mask Register (IMR)

- The IMR stores the bits which disable the interrupt lines to be masked.
- Masking of a higher priority input will not affect the interrupt request lines of lower priority.



Sequence of events

1. The IRR stores the requests.
2. The priority resolver checks three registers: the IRR , IMR, and ISR for the interrupt request being served. It resolves the priority and sets the INT high when appropriate.
3. The MPU acknowledges the interrupt by sending INTA.

4. After the INTA is received, the highest priority ISR bit is set and the corresponding IRR bit is reset.

5. The 8086 will initiate a second INTA pulse. During this period 8259A releases an 8 bit pointer (Type number) on to data bus from where it is read by CPU.

- 6. this completes the interrupt cycle. The ISR bit is reset at the end of the second INTA pulse if automatic end of interrupt (AEOI) mode is programmed. other wise ISR bit remains set until an appropriate EOI command is issued at the end of interrupt subroutine.

More than one 8259

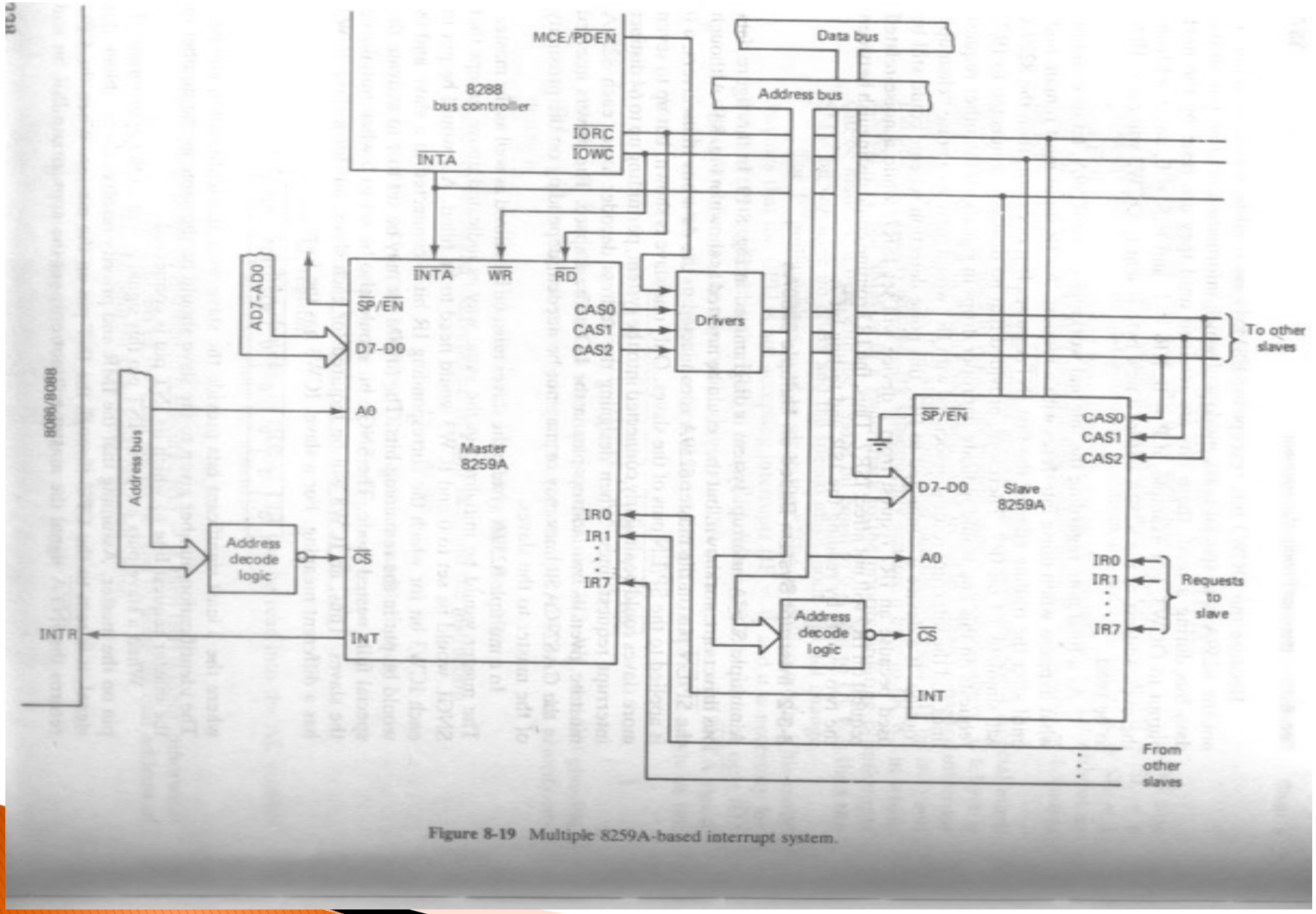
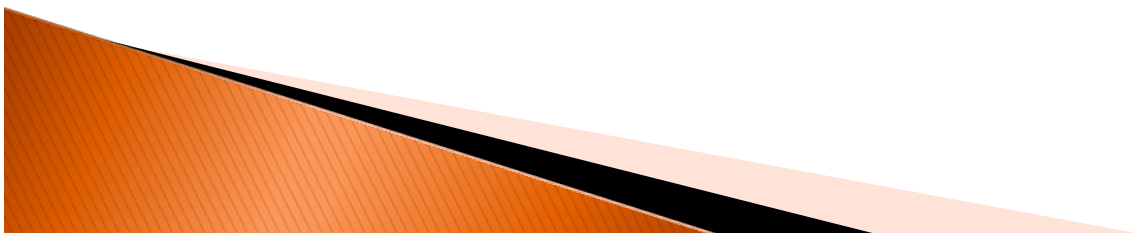


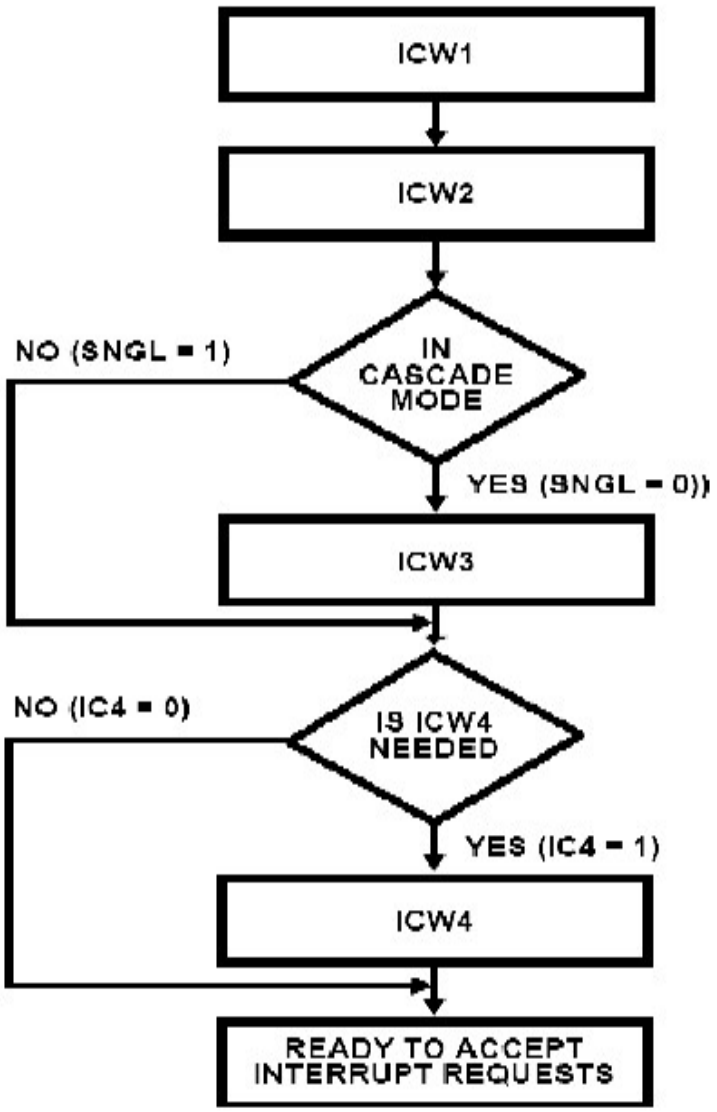
Figure 8-19 Multiple 8259A-based interrupt system.

Interrupt Operation

- The 8259A requires two types of control words:
  - Initialization Command Words (ICWs)
  - Operational Command Words(OCWs).

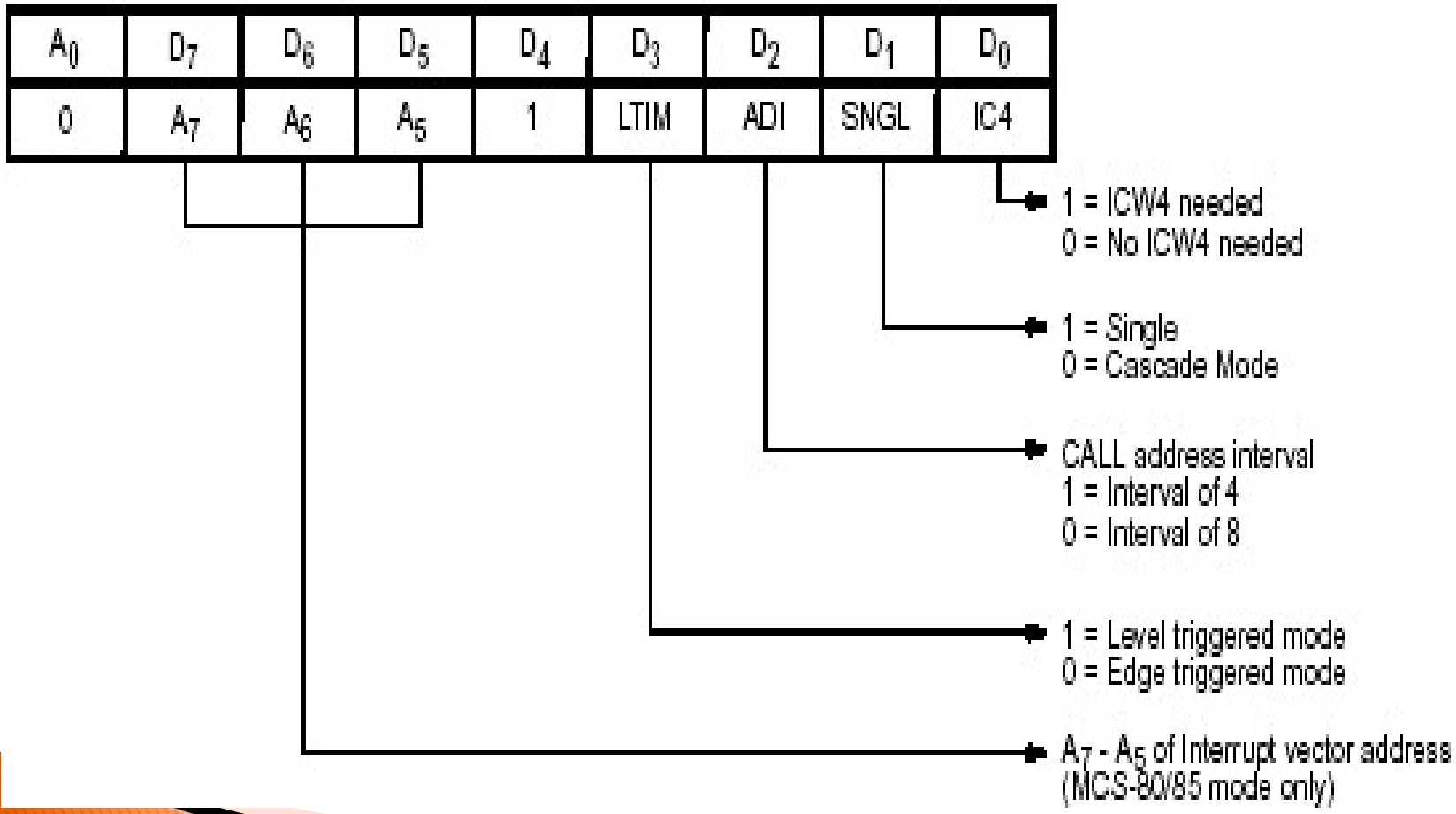


PROGRAMMING THE 8259A



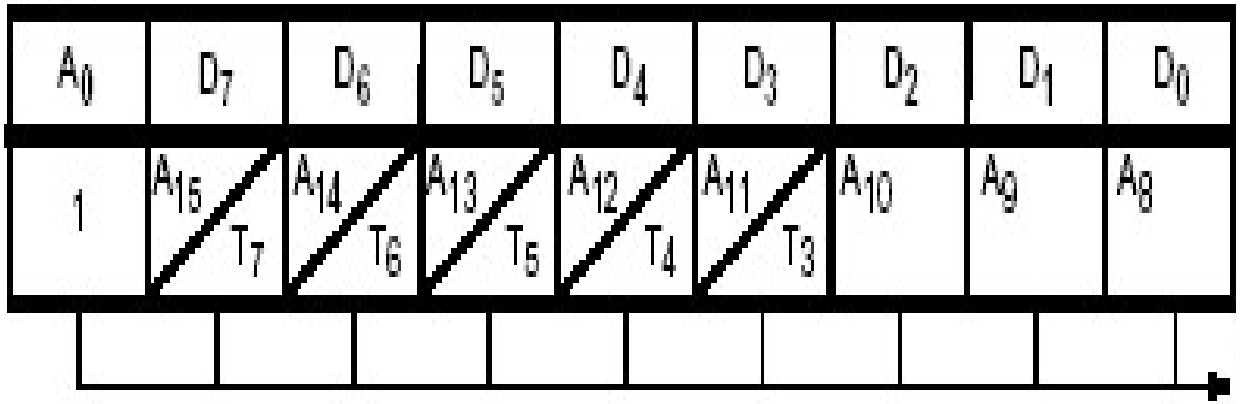
INTIALIZITATION COMMAND WORDS

ICW1



INTIALIZITATION COMMAND WORDS

ICW2



A_{15} - A_8 of interrupt vector address (MCS80/85 mode)

T_7 - T_3 of interrupt vector address (8086/8088 mode)

INTIALIZITATION COMMAND WORDS

ICW3 (MASTER DEVICE)

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0

1 = IR input has a slave
0 = IR input does not have a slave

ICW3 (SLAVE DEVICE)

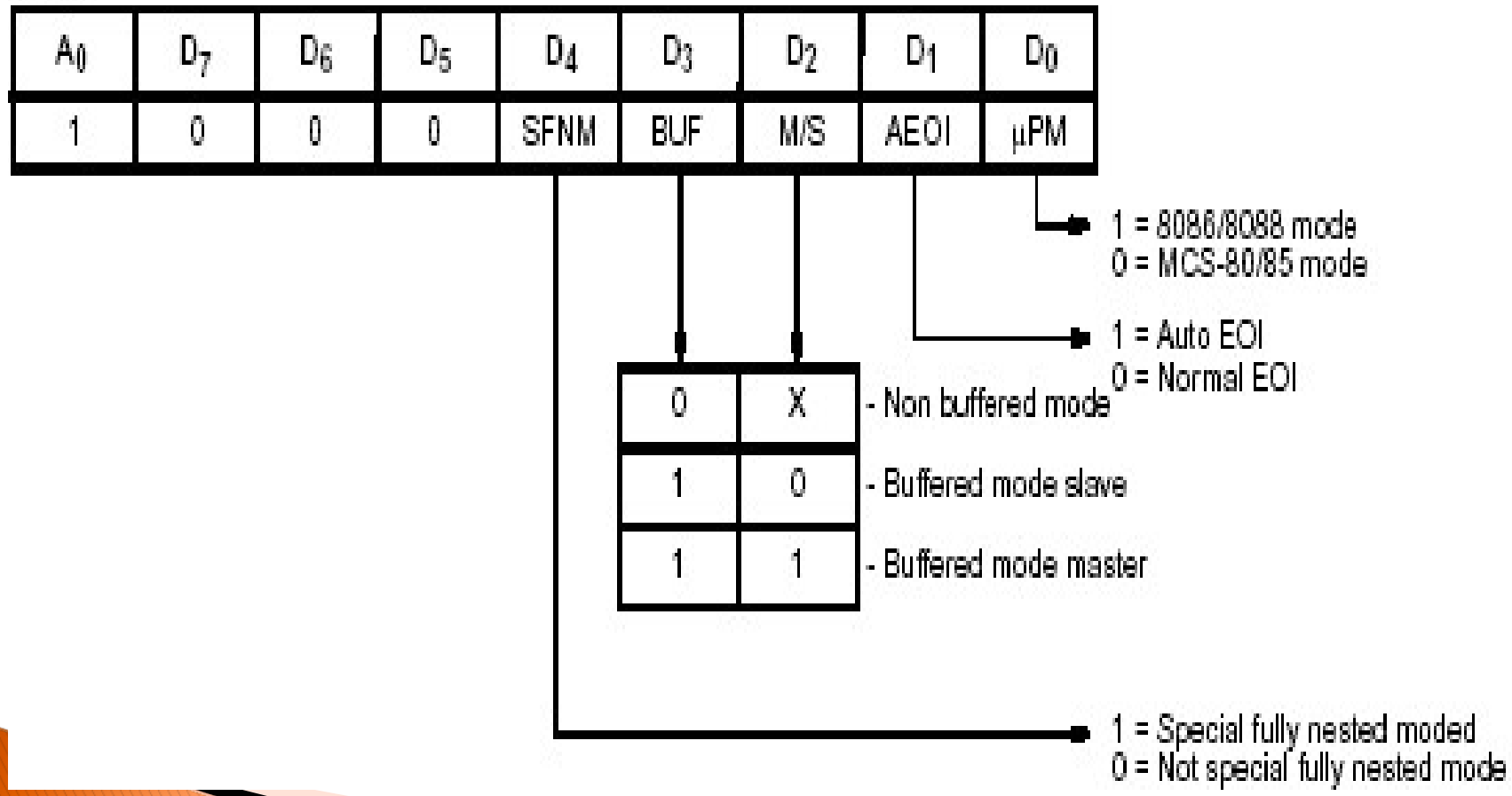
A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	0	0	0	ID_2	ID_1	ID_0

SLAVE ID (NOTE)

0	1	2	3	4	5	6	7
0	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

INTIALIZITATION COMMAND WORDS

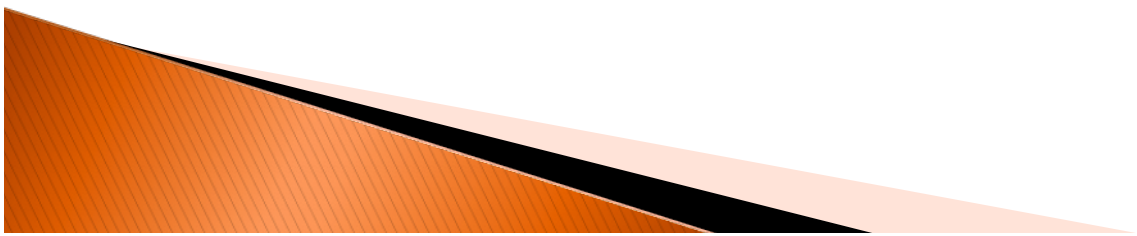
ICW4



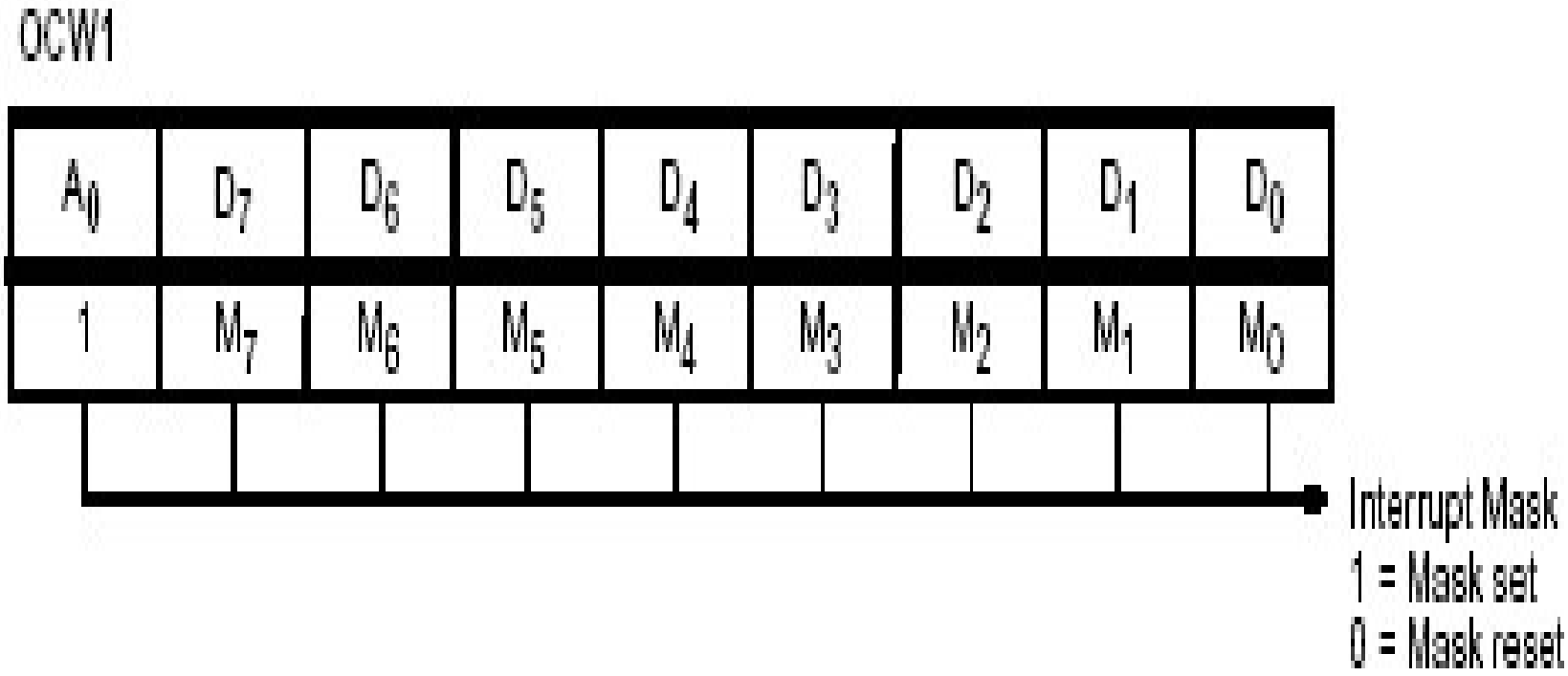
Operating modes of 8259

- **Fully nested mode**
  - Default mode, IR0 having highest priority
- **Special fully nested mode**
  - Used in cascading
- **End of Interrupt (EOI)**
  - Resets ISR bit on command
  - Specific, non specific (reset high priority interrupt bit)
- **Automatic EOI**
- **Automatic rotation**
  - IR level receives lowest priority after serving it.
- **Edge and Level Triggered mode**
- **Reading register mode**

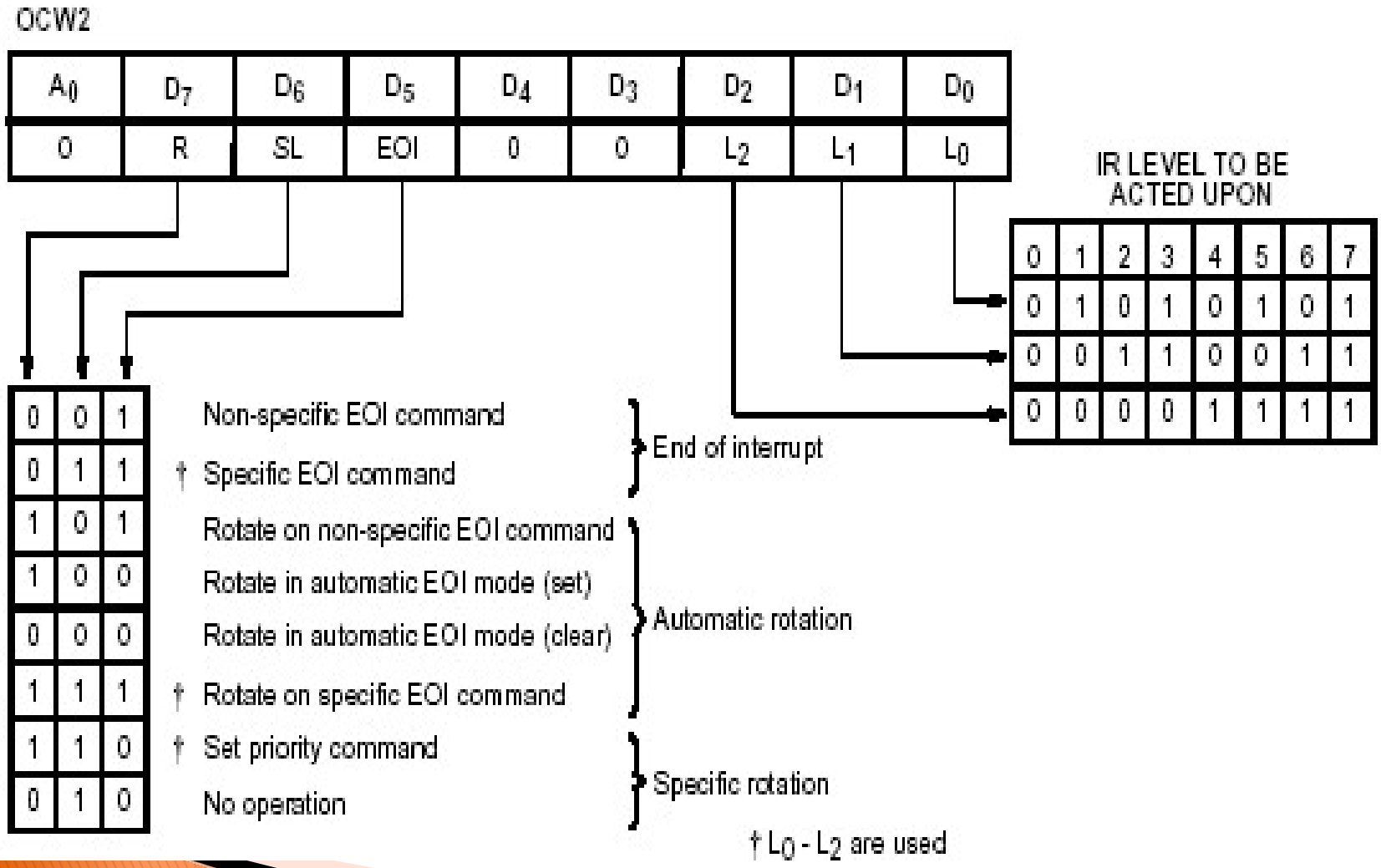
- **Specific rotation**
  - Bottom priority level can be selected (can tell which should have low priority)
- **Special mask mode**
  - Masking enabled
- **Poll command**
  - INT output neglected, 8259 polled by software in CPU
- **Buffered mode**
  - Sp/en enables buffer otherwise it enables master/slave
- **Cascade Mode**



OPERATIONAL COMMAND WORDS.



OPERATIONAL COMMAND WORDS.



OPERATIONAL COMMAND WORDS

OCW3

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	ESMM	SMM	0	1	P	RR	RIS

READ REGISTER COMMAND

0	1	0	1
0	0	1	1
No Action	Read IR reg on next $\overline{RD}$ pulse	Read IS reg on next $\overline{RD}$ pulse	

1 = Poll command
0 = No poll command

SPECIAL MASK MODE

0	1	0	1
0	0	1	1
No Action	Reset special mask	Set special mask	