Decoder and Encoder

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Decoders

- Digital information represented in some binary form must be converted into some alternate binary form.
- n to 2^n-line decoder.
- Only one of the 2^n output lines responds, with a logic-1, to a given input combination of values on its n-input lines.

Decoders

- **Definition**:

  A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines.

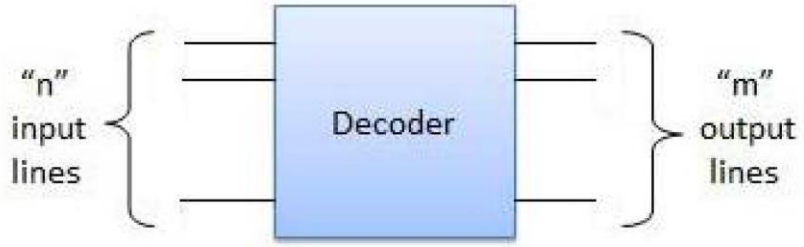
- If n-bit decoded information has unused or don't-care combinations, the decoder output will have less than 2^n outputs.

- The decoders presented here are called n-to-m line decoders where $m \leq 2^n$. Their purpose is to generate the 2^n (or less) minterms of n input variables.

Decoders

Application:

- Decoders are greatly used in applications where the particular output or group of outputs to be activated only on the occurrence of a specific combination of input levels. Some important application of decoder circuit is given below.
- **Address Decoders**: Amongst its many uses, a decoder is widely used to decode the particular memory location in the computer memory system. Decoders accept the address code generated by the CPU which is a combination of address bits for a specific location in the memory.



Decoders

- **Instruction Decoder**: Another application of the decoder can be found in the control unit of the central processing unit. This decoder is used to decode the program instructions in order to activate the specific control lines such that different operations in the ALU of the CPU are carried out.

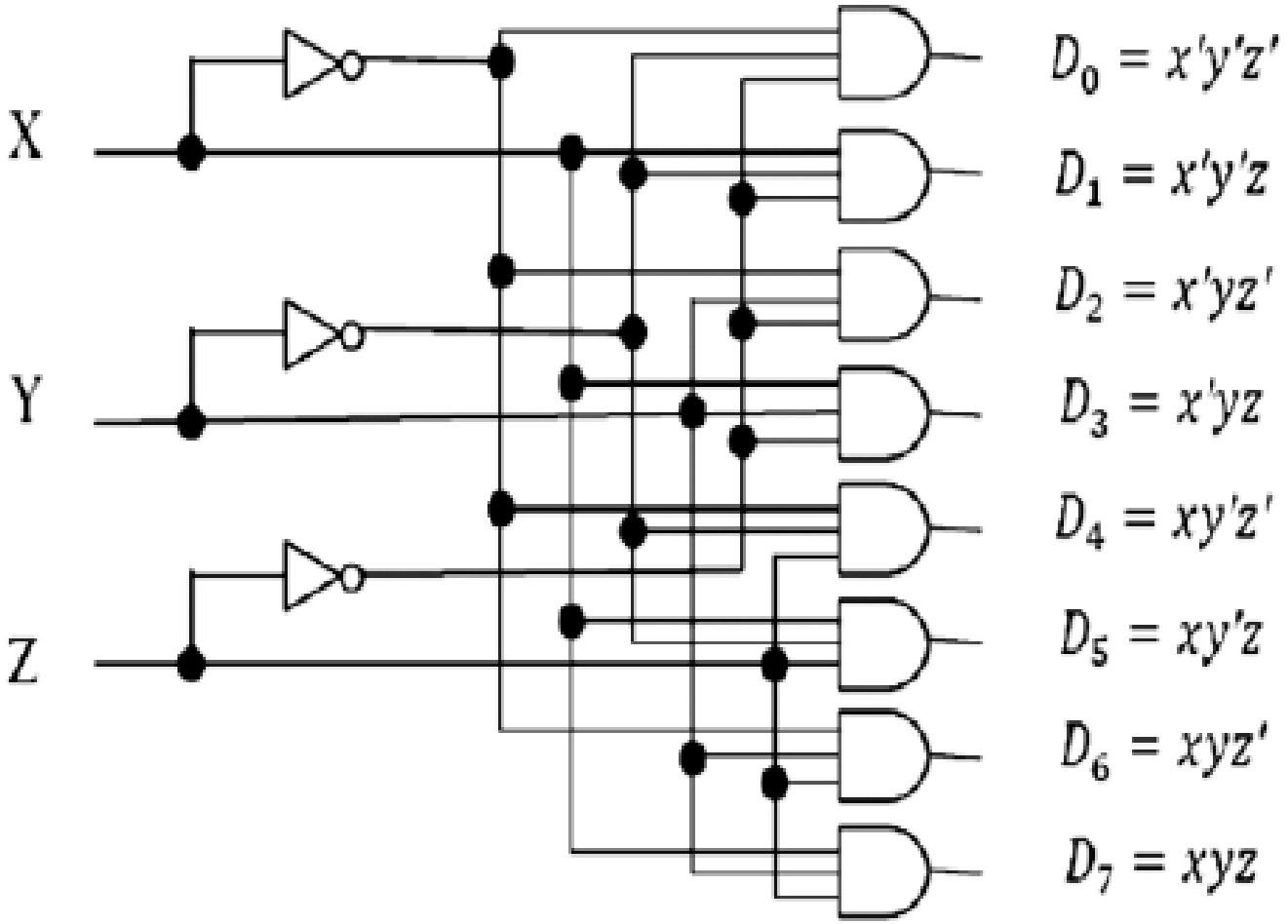
Decoders

3 X 8 Decoder:

- The three inputs are decoded into eight outputs, each output representing one of the minterms of the 3-input variables.

- A particular application of this decoder would be a binary-to-octal conversion. The input variable may represent a binary number and the outputs will then represent the eight digits in the octal number system

Decoders



3 to 8 LINE DECODER

Decoders

Truth Table of 3 X 8 line decoder:

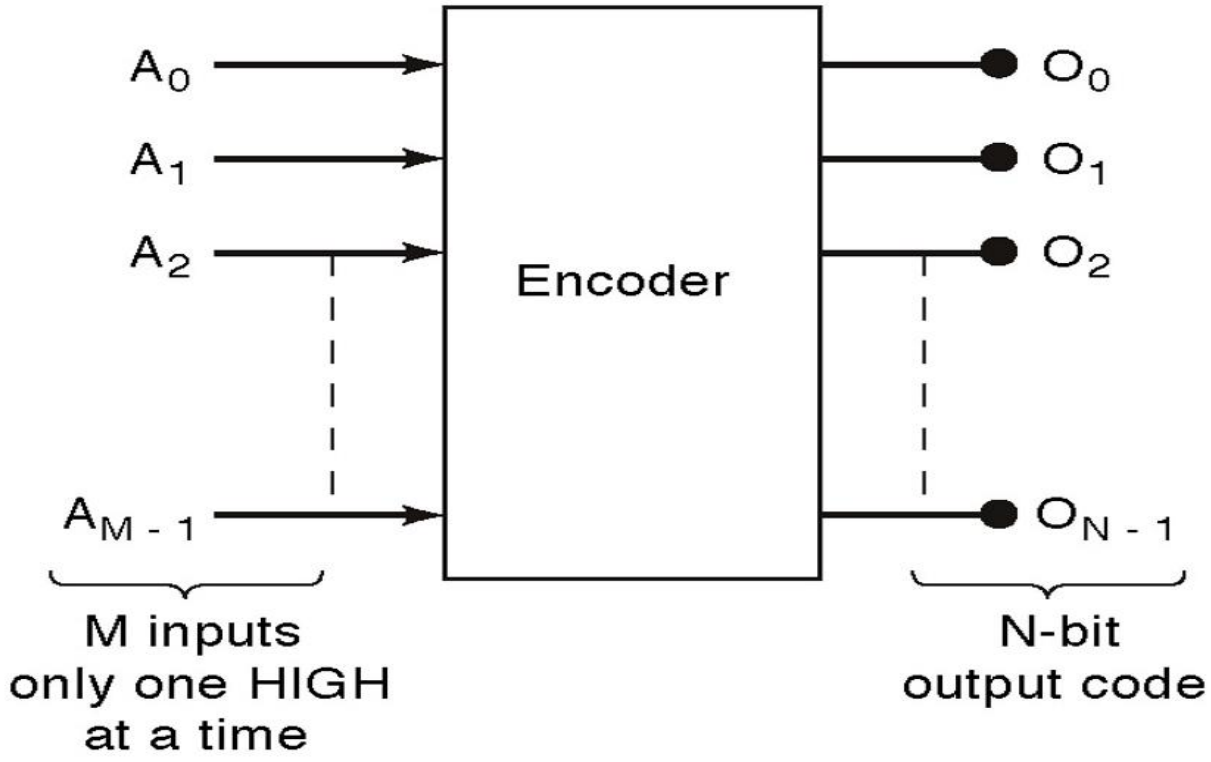
- From the truth table it is observed that the output variables are mutually exclusive because only one output can be equal to 1 at any one time. The output line whose value is equal to 1 represents the minterm equivalent of the binary number presently available in the input lines.

3 to 8 Line Decoder

Inputs			Outputs							
x	y	z	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Encoders

- An encoder has a number of input lines, only one of which input is activated at a given time and produces an N-bit output code, depending on which input is activated.

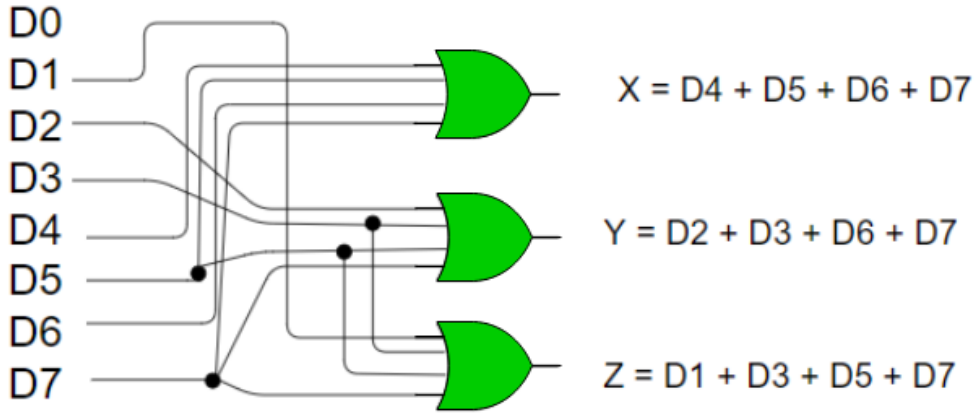


Encoders

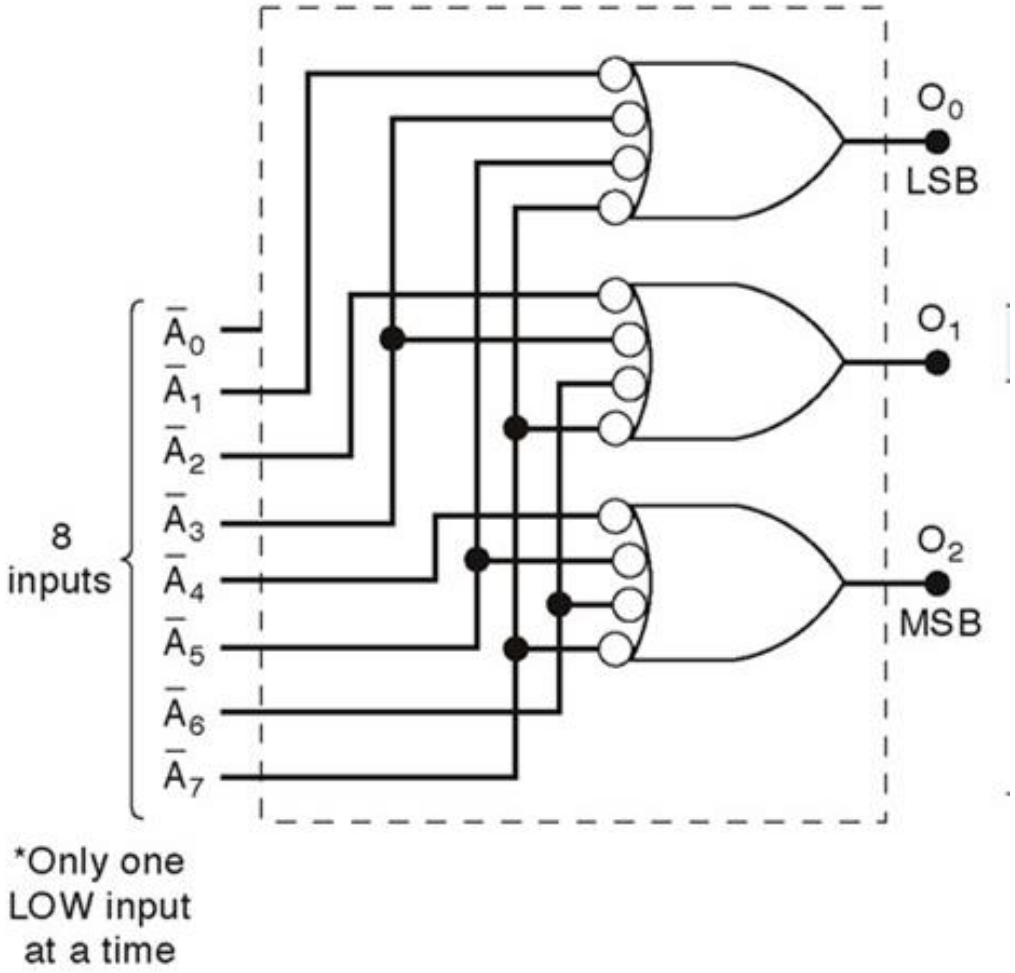
Encoder 8 x 3

D7	D6	D5	D4	D3	D2	D1	D0	X	Y	Z
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

$$X = D4 + D5 + D6 + D7$$
$$Y = D2 + D3 + D6 + D7$$
$$Z = D1 + D3 + D5 + D7$$



Encoders

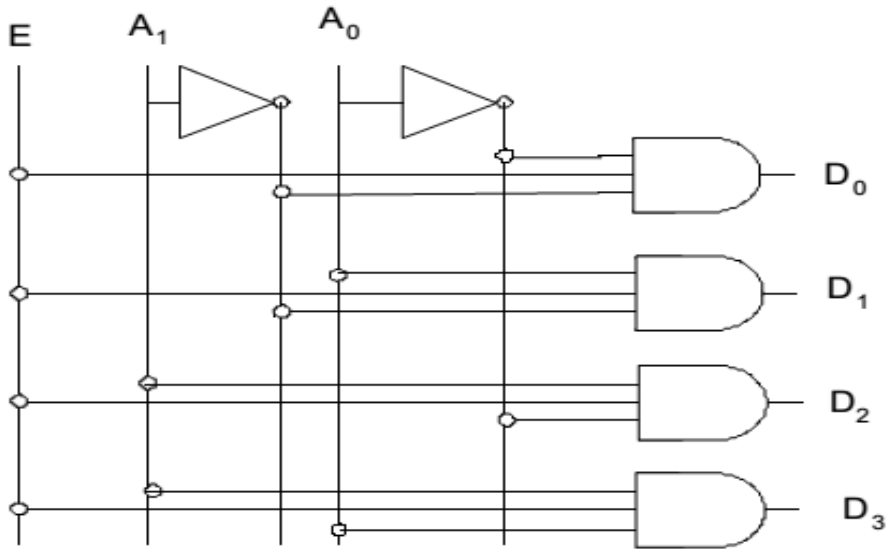


General diagram of encoder

Encoders

- A priority encoder is an encoder that includes the priority function
- If two or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

2-4 decoder with enable

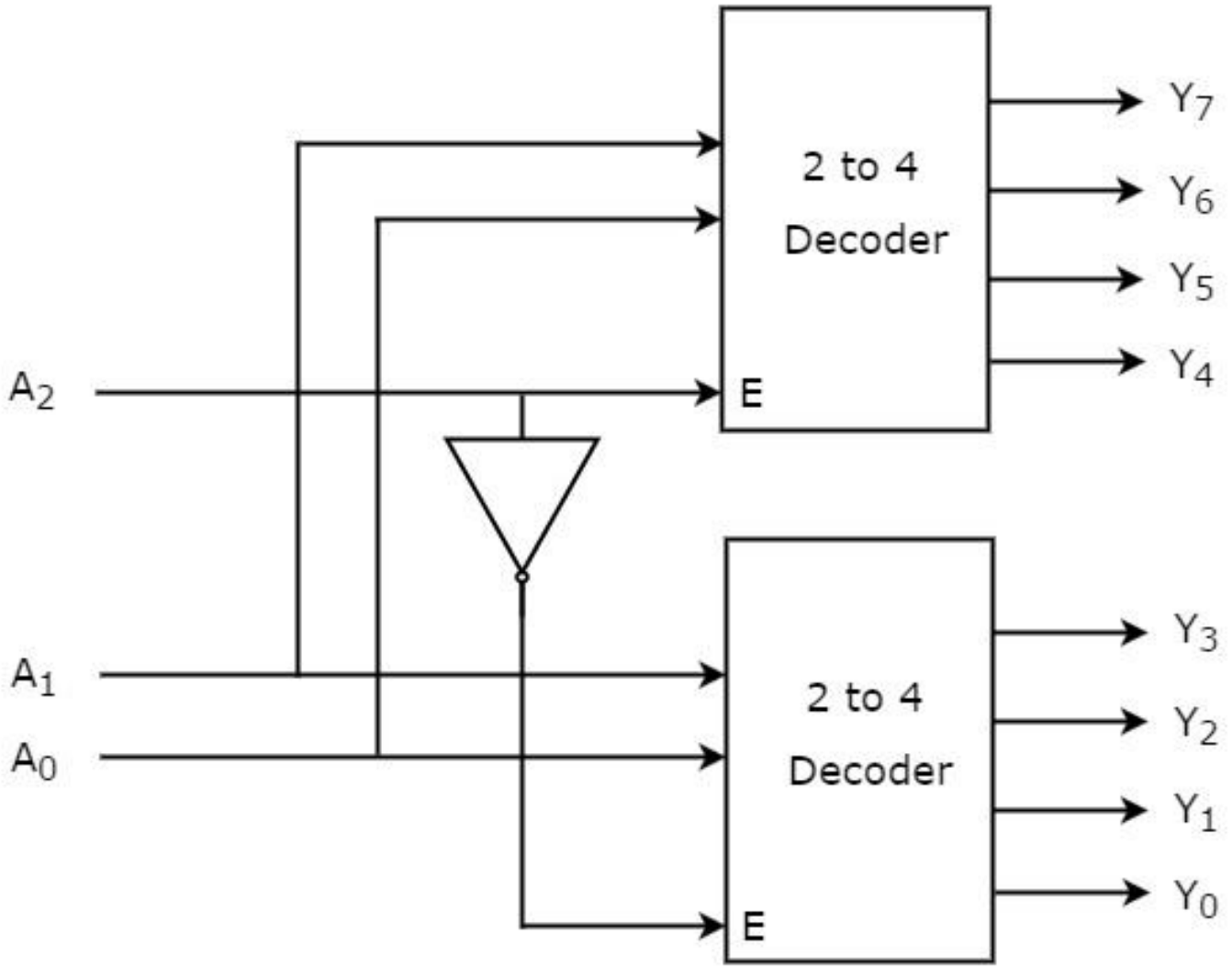


Implementation 2-to-4 decoder with enable

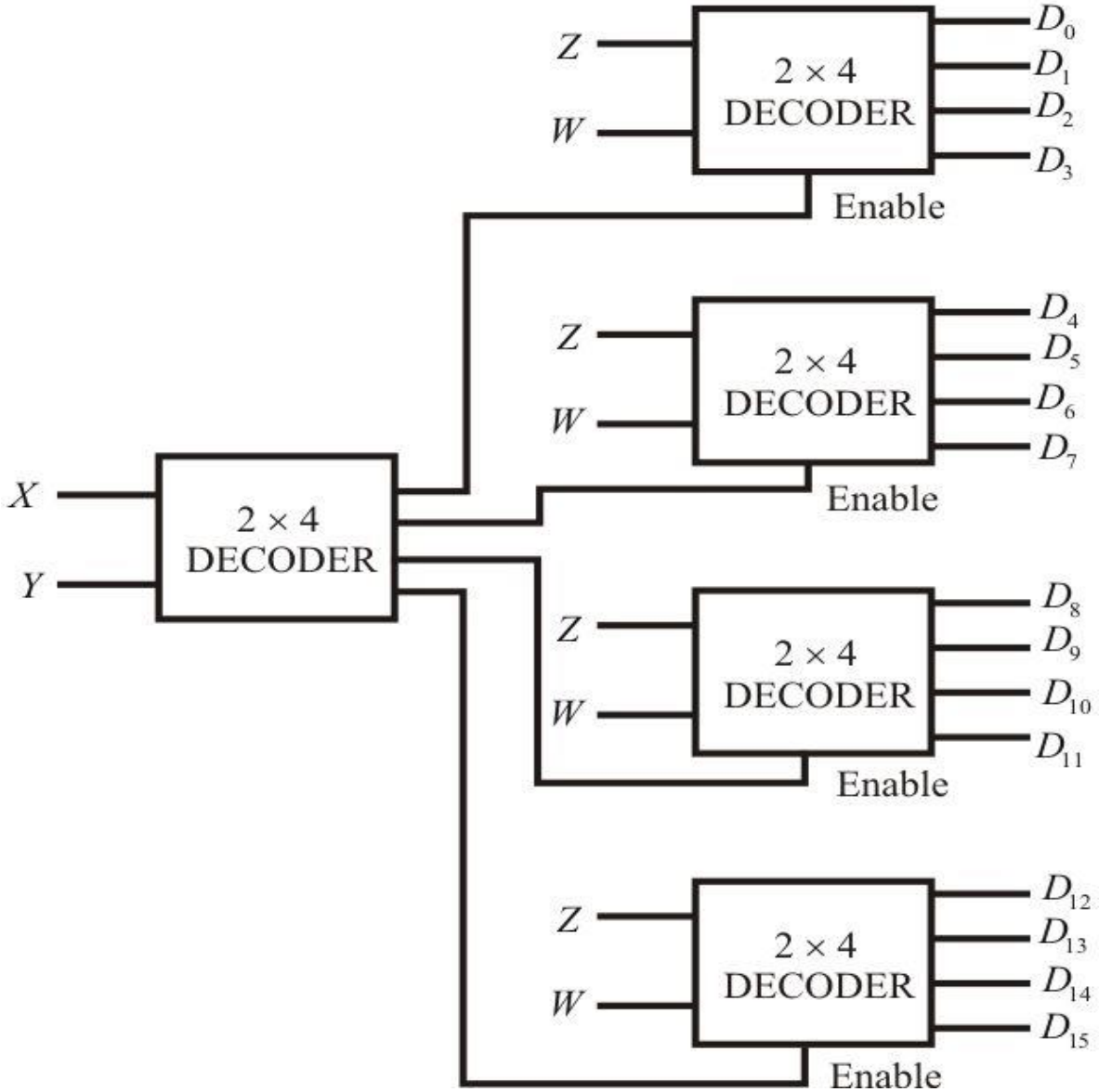
Decimal value	Enable	Inputs		Outputs			
	E	A_1	A_0	D_0	D_1	D_2	D_3
	0	X	X	0	0	0	0
0	1	0	0	1	0	0	0
1	1	0	1	0	1	0	0
2	1	1	0	0	0	1	0
3	1	1	1	0	0	0	1

Truth table of 2-to-4 decoder with enable

3 to 8 decoder using 2 to 4 decoder



4 to 16 decoder using 2 to 4 decoder



Decoders

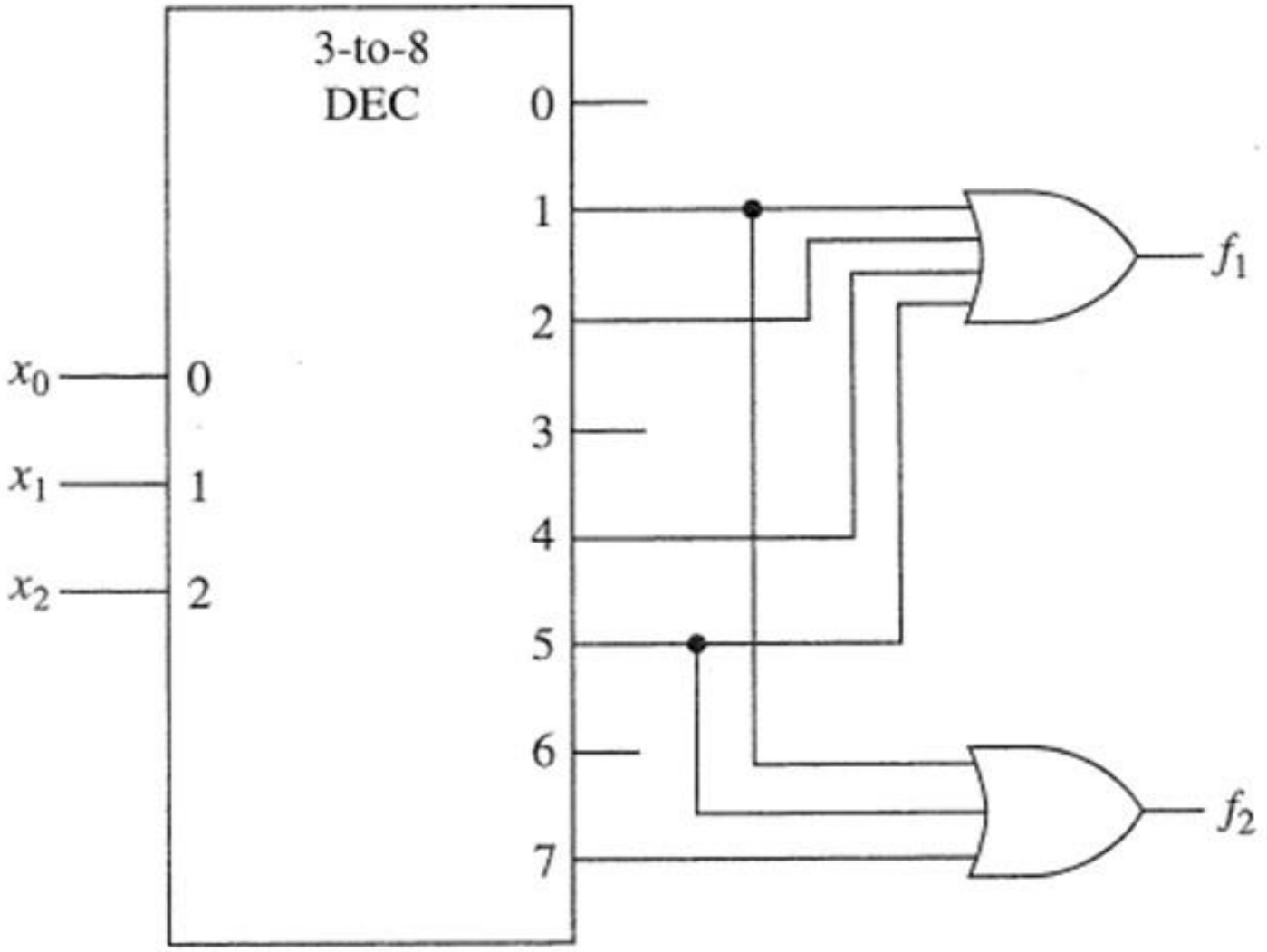
- **Combinational Logic Implementation**
  - Decoder provides 2^n minterms of n input variables.
  - Since any Boolean function can be expressed in sum of minterms canonical form, one can use a decoder to generate the minterms and an external OR gate to form the sum.

Decoders

- Example: Minterms using OR Gates

  f1(x, y, z) = ∑ (1, 2, 4, 5)

  f2(x, y, z) = ∑ (1,5,7)

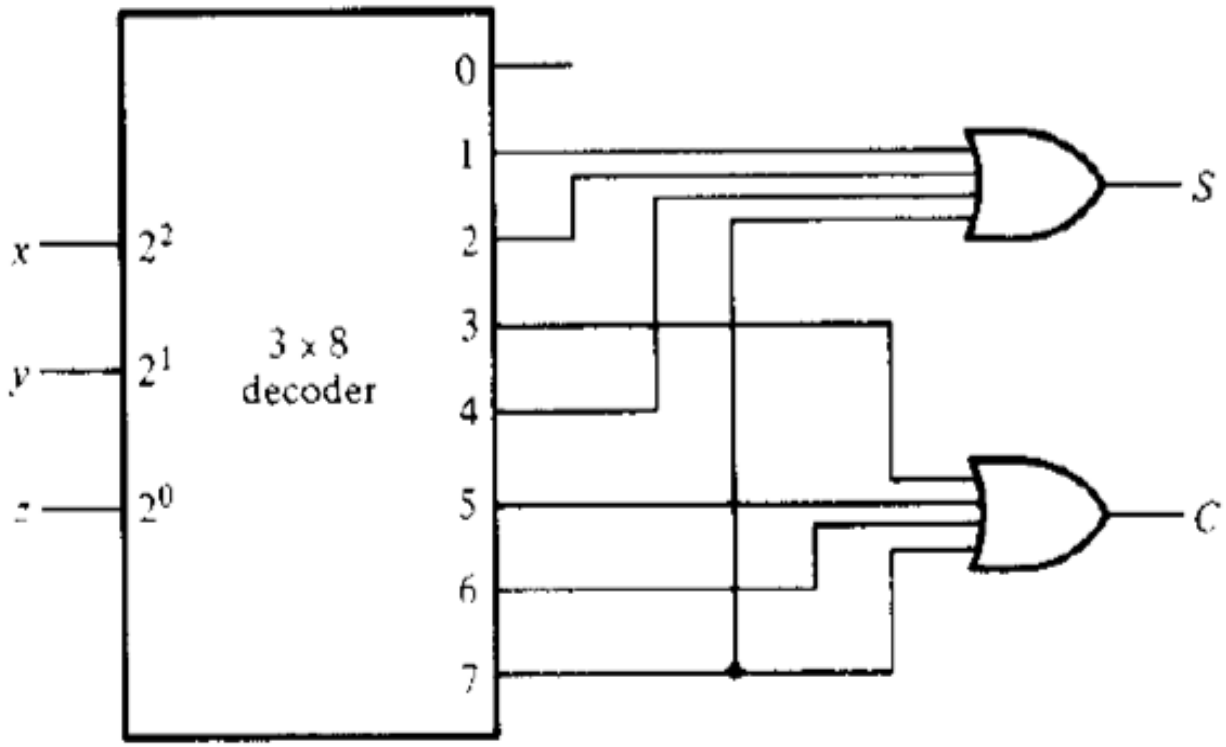


Decoders

- Example: Implement a full adder circuit with a decoder and two OR gates.

$S(x, y, z) = \sum (1, 2, 4, 7)$

$C(x, y, z) = \sum (3, 5, 6, 7)$



Full adder with decoder