School of Technology, Pandit Deendayal Energy University, Gandhinagar

Course File (A to Z Essentials)

Name of the Course:	Digital Electronics & Computer Organization
Course Code:	20CP203T
Program:	B.Tech.
Department	Computer Science Engineering
Semester:	III
Academic Year:	2023-2024
Name of Course Coordinator:	Dr. Samir Patel
Names of the Other Faculty Members:	Dr. Vipul Mishra, Mr. Himanshu Gajera, Ms. Krishna Brahmbhatt, Ms. Rashmi Bhattad

A.	Course Syllabus, Prerequisites for the Course, Teaching Scheme, List of Books and Reference Books, etc.
B.	Lesson Plan (Hour-to-Hour Plan)
C.	Academic Calendar, Course Timetable, Faculty Timetable
D.	Course Outcomes (COs)
E.	Mapping of Course Outcomes with Programme Outcomes (POs)
F.	Evaluation Scheme and Rubrics
G.	Class Notes, Handouts, Course Material, etc.
H.	Course Presentations (PPTs) – If Applicable
I.	Tutorials, Assignments, Case Studies, Quiz, etc.
J.	Course-related ICT: Web links, Software, E-books, Relevant NPTEL and MOOC, Video Lectures, Blogs, Virtual labs, Animation, Simulation, etc.
K.	Laboratory Manuals – If Applicable
L.	List of International / National Journals related to the Course – If Applicable
M.	List of well-known Conferences related to the Course – If Applicable
N.	List of Classic Journal Papers / Articles / Review Papers related to the Course – If Applicable
O.	List of Renowned Industries / Organizations / working in the Course related areas
P.	List of Renowned Scientists / Academicians working in the Course related areas
Q.	Copies of the Mid and End Semester Examination Question Papers and Sample Answer Sheets
R.	Attendance Record
S.	Records of the Continuous Assessment (Assignment, Quiz, Laboratory Work, etc.)
T.	Details of Remedial Classes (with evidences)
U.	Details of Expert Lectures / Industrial Visits/Events (Only related to the Course)
V.	List of Slow and Advanced Learners, activity planned and executed
W.	Direct Assessment (Result of mid, end and internal assessment components)
X.	Indirect Assessment (Exit Survey/Post Test)
Y.	Final Attainment of COs and POs and Interpretation
Z.	Actions to be taken if COs and POs are not achieved

Date:

Signature of Subject Teachers **Signature of Department Coordinator (IQAC)** **Signature of Head of the Department**

A- Course Syllabus, Prerequisites for the Course, Teaching Scheme, List of Books and

Pandit Deendayal Energy University School of Technology

20CP203T					Digital Electronics and Computer Organization					
Teaching Scheme					Examination Scheme					
L	T	P	C	Hrs/Week	Theory			Practical		Total Marks
					CE	MS	ES	LW	LE/Viva	
3	0	0	3	3	25	25	50	-	-	100

Reference Books, etc.

COURSE OBJECTIVES

- To introduce the basics involved in data representation and digital logic circuits used in the computer system including logic elements, and their use in combinational and sequential logic circuit design.
- To understand the architecture of processing, memory and I/O organization in a computer system.
- To understand the state transition diagrams to prepare circuits.

UNIT 1 NUMBER SYSTEMS **10 Hrs.**

Introduction to Number Systems, Conversion from one to another, 1's and 2's Complements, Introduction to Boolean Algebra: Addition and Multiplication in Boolean algebra: Binary Logic Functions, Logical Gates and Truth Tables; DEMORGAN's Theorem, Combinational Logic: Forms; Sum of Products Form, Product of Sum Form, K – Map: Plotting a Boolean expression and Logic expression simplification with grouping cells, Quine McClusky Method

UNIT 2: COMBINATIONAL AND SEQUENTIAL CIRCUITS **12 Hrs.**

Analysis and Design of Combinational Logic: Introduction: Binary adders; Half adder, Full adder: Binary Subtractor; Half subtractor, Full subtractor, Decoders; Encoders; Multiplexers, Demultiplexers: Parity Generators and Parity Checkers; Parity, Detecting an Error.

Latches: The S-R Latch (NOR, NAND); Gated Latches; Gated S-R Latches, Gated D-Latch or D-flip-flop: Edge triggered Flip-Flops; Edge triggered S-R Flip-Flop (S-R FF), Edge triggered D-Flip-Flop (D-FF), Edge triggered J-K Flip-Flop (J-K FF), Master-Slave J-K Flip Flop

UNIT 3: CENTRAL PROCESSING UNIT (CPU) **9 Hrs.**

General register organization, the operation of memory stack, variety of addressing modes, instruction format. RISC architecture and CISC architecture. Examples of processors and instruction execution employing RISC and CISC architecture, Introduction to control unit (Hardwired, Microprogrammed).

UNIT 4: INPUT-OUTPUT ORGANIZATION **8 Hrs.**

Computer communication with input and output devices. I/O interface units are presented to show the way that the processor interacts with external peripherals. Memory Organization - The concept of memory hierarchy: cache memory, main memory, auxiliary memory. Virtual memory, Memory Management: physical address and logical address mapping

Max. 39 Hrs

COURSE OUTCOME

CO1: Describe basic gate operations and laws of Boolean algebra.
CO2: Explain basic structure of digital computer, stored program concept and different arithmetic and control unit operations.
CO3: Understand basic structure of different combinational circuits- multiplexer, decoder, encoder.
CO4: Analyze various digital electronic circuits.
CO5: Identify the basic aspects of instruction execution, and examine the sub-operations of computer arithmetic.
CO6: Categorize the organization of memory, and I/O modules.

TEXT/REFERENCE BOOKS

1. V. Rajaraman, T. Radhakrishnan, "Digital Logic and Computer Organization", Prentice Hall India Learning Private Limited; 1 edition (2006)
2. Nikrouz Faroughi, "Digital Logic Design and Computer Organization: With Computer Architecture for Security", 2015 McGraw-Hill Education
3. Yale N. Patt, Sanjay J. Patel, "Introduction to Computing Systems" McGraw Hill
4. C.Hamacher, Z.Vranesic and S.Zaky, Computer Organization, 5th Ed., McGraw-Hill, 2002

END SEMESTER EXAMINATION QUESTION PAPER PATTERN

Max. Marks: 100 **Exam Duration: 3 Hrs**

Part A: 10 Questions of 2 marks each-No choice 20 Marks
Part B: 2 Questions from each unit with internal choice, each carrying 20 marks 80 Marks

B. Lesson Plan (Hour-to-Hour Plan)

Lecture No.	Topic to be covered	Teaching Aid to be used	Remarks (Text book/Unit No etc.)
1	Introduction to Number Systems, Conversion from one to another	BW + PPT	Unit 1
2	1's and 2's Complements	BW + PPT	Unit 1
3	Introduction to Boolean Algebra	BW + PPT	Unit 1
4	Addition and Multiplication in Boolean algebra	BW + PPT	Unit 1
5	Logical Gates and Truth Tables	BW + PPT	Unit 1
6	Binary Logic Functions	BW + PPT	Unit 1
7	DEMORGAN's Theorem, Combinational Logic	BW + PPT	Unit 1
8	Forms; Sum of Products Form, Product of Sum Form	BW + PPT	Unit 1
9	K – Map: Plotting a Boolean expression and Logic expression simplification with grouping cells	BW + PPT	Unit 1
10	Quine McClusky Method	BW + PPT	Unit 1
11	Analysis and Design of Combinational Logic circuit	BW + PPT	Unit 2
12	Binary adders; Half adder	BW + PPT	Unit 2
13	Full adder	BW + PPT	Unit 2
14	Binary Subtractor; Half subtractor, Full subtractor	BW + PPT	Unit 2
15	Decoders; Encoders	BW + PPT	Unit 2
16	Multiplexers, Demultiplexers	BW + PPT	Unit 2
17	Parity Generators and Parity Checkers; Detecting an Error.	BW + PPT	Unit 2
18	Latches: The S-R Latch (NOR, NAND)	BW + PPT	Unit 2
19	Gated Latches; Gated S-R Latches, Gated D-Latch or D-flip-flop	BW + PPT	Unit 2
20	Edge triggered Flip-Flops; Edge triggered S-R Flip-Flop (S-R FF)	BW + PPT	Unit 2
21	Edge triggered D-Flip-Flop (D-FF), Edge triggered J-K Flip-Flop (J-K FF)	BW + PPT	Unit 2
22	Master-Slave J-K Flip Flop	BW + PPT	Unit 2
23	General register organization	BW + PPT	Unit 3
24	The operation of memory stack	BW + PPT	Unit 3
25	Variety of addressing modes	BW + PPT	Unit 3
26	Instruction format	BW + PPT	Unit 3
27	RISC architecture and CISC architecture	BW + PPT	Unit 3
28	Examples of processors	BW + PPT	Unit 3
29	instruction execution employing RISC and CISC architecture	BW + PPT	Unit 3
30	Introduction to control unit (Hardwired control)	BW + PPT	Unit 3
31	Introduction to control unit (Microprogrammed control)	BW + PPT	Unit 3
32	Computer communication with input and output devices	BW + PPT	Unit 4

33	I/O interface units are presented to show the way that the processor interacts with external peripherals	BW + PPT	Unit 4
34	Memory Organization	BW + PPT	Unit 4
35	The concept of memory hierarchy	BW + PPT	Unit 4
36	Cache memory	BW + PPT	Unit 4
37	Main memory, Auxiliary memory	BW + PPT	Unit 4
38	Virtual memory	BW + PPT	Unit 4
39	Memory Management: physical address and logical address mapping	BW + PPT	Unit 4

Legends: BW (Board Work), PPT (Power Point Presentation)

C-

C.1 Academic Calendar

PANDIT DEENDAYAL ENERGY UNIVERSITY
Academic Calendar: 2023-24

Particulars	Date
Odd Semester: UG Sem.1/3/5/7 & PG Sem. 1/3 (FoET) & UG Sem. 1/3/5/7 & PG Sem 1/3 (FoLS)	
Semester Registration & Commencement of classes-FoET & FoLS- 1st Sem	17th July (Mon) 2023
Semester Registration, Department Orientation & Commencement of classes for 3/5/7 Sem – FoET & FoLS	24th Jul (Mon). 2023
Evaluation of Rural Internship/CSSI & Evaluation of Industry Orientation, & Evaluation of Industrial Internship	7th (Mon)-11th (Fri)Aug. 2023
Independence Day Celebration	15th Aug. (Thes) 2023
Attendance Review-1 (After 4 week)	17th (Thur)-18th (Fri) Aug. 2023
Internal Assesment-1 (Quiz, Test, Assignment etc.)** Student mentoring week – 1	21st (Mon)-25th (Fri)Aug. 2023
Mid Semester Examination / Project Phase 1 Review	11th Sept. (Mon) 2023 Onwards
Attendance Review-2 (After 8 week)	14th (Thur)-15th (Fri)Sept 2023
Parent Teacher Meeting (Saturday)	23rd Sept.(Sat) 2023
Last date of showing evaluated answer books of Mid Semester Examination	27th Sept. (Wed) 2023
Declaration of Mid Semester Exam Result	6th Oct. (Fri) 2023
360 Degree Feedback from Students by School Admin	9th (Mon)-13th (Fri)Oct. 2023
Attendance Review-3 (After 12 week)	12th (Thur)-13th (Fri)Oct 2023
Rangtaal – Navratri Celebration	13th Oct.(Fri) 2023
Internal Assesment-2 (Quiz, Test, Assignment etc)** Student mentoring week – 2	25th (Wed)-31st (Tues)Oct. 2023
Tesseract – The Science & Technical Fest	03(Fri)-04(Sat)-05(Sun) Nov. 2023
Declaration of Detention list of students (during 13th Week)	By 20th Oct (Fri) 2023
Diwali Vacation	13th (Mon)-17th (Fri) Nov. 2023
Classes End	21st (Tues) Nov. 2023
Practical Examinations, submission of Term Work and Seminars	22nd Nov.(Wed) 2023 Onwards
Dissertation presentation for UG and PG for FOLS	22nd Nov.(Wed) 2023 onwards
End Semester Examinations - FoET& FoLS	28th Nov.(Tues) 2023 Onwards
Last date of Submission of Marks of End sem. Exam	15th Dec. (Fri) 2023
Rural Internship for FoLS students	During Dec 2023
Project Phase I Exam for PG program of FoET & Progress Review for Ph. D.	18th (Mon)-22nd (Fri)Dec. 2023
Winter Break	26th (Tues)-29th (Fri)Dec. 2023
Alumni Day	29th Dec (Fri) 2023
Even Semester: UG Sem. 2/4/6/8 & PG Sem. 2/4 (FoET) & UG Sem.2/4/6/8 & PG Sem. 2/4 (FoLS)	
Next semester registration	27th (Wed)-30th (Sat) Dec. 2023
Start of Next Semester	1st Jan. (Mon) 2024

C.2 Faculty Timetable

Samir Patel
Computer Science &Engineering

Autumn Semester 2023 w.e.f : 24th July 2023

Day	08:00-09:00	09:00-10:00	10:00-11:00	11:00-12:00	12:00-13:00	13:00-14:00	14:00-15:00	15:00-16:00	16:00-17:00	17:00-18:00	18:00-19:00
Monday				G1 (20DS516T) F-103, MDS(1) - P			G3G4 (20CP203T) F-402, CP(3) - L		G1 (20DS516T) F-401, MDS(1) - L		
Tuesday											
Wednesday		G3G4 (20CP203T) F-402, CP(3) - L		G1G2 (20CP203T) F-503, CP(3) - L			G1 (20DS516T) F-401, MDS(1) - L	G3G4 (20CP203T) F-402, CP(3) - L	G1G2 (20CP203T) F-503, CP(3) - L		
Thursday											
Friday		G1 (20CP203P) F-104, CP(3) - P		G1G2 (20CP203T) F-503, CP(3) - L				G1 (20DS516T) F-401, MDS(1) - L			

Location Abbr.	Location Name
F-103	F, HPC LAB
F-104	F, Data Analytics Lab
F-401	F, Lecture Hall
F-402	F, Lecture Hall
F-503	F, Lecture Hall

Subject Abbr.	Subject Name
20CP203P	Digital Electronics &Computer Organization Lab
20CP203T	Digital Electronics &Computer Organization
20DS516T	Big Data Analytics Lab
20DS516T	Big Data Analytics

D- Course Outcomes (COs)

Course Outcomes (CO's): On completion of the course, students will be able to

CO1. **Understand** the basic gate operations and laws of Boolean algebra, basic aspects of instruction execution, and examine the sub-operations of computer arithmetic.

CO2. **Explain** the basic structure of digital computer, stored program concept and different arithmetic and control unit operations

CO3. **Apply** different combinational circuits- multiplexer, decoder, encoder etc. and Perform different operations with sequential circuits

CO4. **Analyzed** the organization of memory, the basics of I/O modules.

CO5. **Determine** the logic components necessary to design an electronic circuit.
Create or design of digital electronic circuits

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	-	1	2	-	3	1	1	-	-	1	1	3	-	-
2	1	1	-	2	-	3	1	1	-	-	1	1	2	-	-
3	2	1	1	-	-	3	1	1	-	-	1	1	2	-	-
4	2	3	3	1	-	2	1	1	-	-	2	1	2	-	-
5	1	2	3	2	-	2	1	1	-	-	1	1	2	-	-
6	1	2	3	1	-	2	1	1	-	-	2	1	2	-	-
	1.6	1.5	1.8	1.3	-	2.5	1	1	-	-	1.3	1	2.1	-	-

Program Articulation Matrix

PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PS01	PSO2	PSO3
3	3	2	1	1	2	1	1	2	2	2	3	3	3	3

Correlation levels 1, 2 or 3 as defined below:

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High)

F- Evaluation Scheme and Rubrics

Course code: 20CP203T **Course name:** Digital Electronics & Computer Organization

Course Outcomes (CO's): On completion of the course, students will be able to

CO6. Understand the basic gate operations and laws of Boolean algebra, basic aspects of instruction execution, and examine the sub-operations of computer arithmetic.
CO7. Explain the basic structure of digital computer, stored program concept and different arithmetic and control unit operations
CO8. Apply different combinational circuits- multiplexer, decoder, encoder etc. and Perform different operations with sequential circuits
CO9. Analyzed the organization of memory, the basics of I/O modules.
CO10. Determine the logic components necessary to design an electronic circuit.
CO11. Create or design of digital electronic circuits

Co Assessment Tools (Direct Assessment):
Various assessment tools used to evaluate CO's (Rubrics) and the frequency with which the assessment processes are carried out are listed below.

Assessment Method	Assessment Tool	Description	Marks	Mapping with CO	Contribution to CO's
Direct (Continuous Evaluation)	Internal Assessment -1	Quiz / MCQ Problem Solving / Design Problem / Case Study	25	CO1, CO2, CO3	It fractionally contributes to 25% weightage of Direct Assessment to CO attainment.
	Internal Assessment -2	Quiz / MCQ Problem Solving / Design Problem / Case Study		CO4, CO5, CO6	
Direct	Mid-Sem Examination	Problem Solving/ Descriptive Answering	25	CO1, CO2, CO3, CO4, CO5, CO6	It contributes to 25% weightage of Direct Assessment to CO attainment.
Direct	End-Sem Examination	Problem Solving/ Descriptive Answering	50	CO1, CO2, CO3, CO4, CO5, CO6	It contributes to 50% weightage of Direct Assessment to CO attainment.

G- **Class Notes, Handouts, Course Material, etc**.

In separate folder will be merge at the end of the course

H- Course Presentations (PPTs)
In separate folder will be merge at the end of the course

I- Tutorials, Assignments, Case Studies, Quiz, etc
In separate folder will be merge at the end of the course

J- **Course-related ICT: Web links, Software, E-books, Relevant NPTEL and MOOC, Video** Lectures, Blogs, Virtual labs, Animation, Simulation, etc.
Swayam MOOC- https://onlinecourses.nptel.ac.in/noc21_ee39/preview
https://onlinecourses.swayam2.ac.in/cec21_cs16/preview
EDA Play Ground- https://edaplayground.com/
Video Lecture- https://youtube.com/playlist?list=PLme7l5iEFnEWKFfwh6acaIVhKI1aBP9TJ

K- Laboratory Manuals – Not Applicable

L- List of International / National Journals related to the Course

IEEE Transactions on Very Large Scale Integration (VLSI) Systems
Nature Electronics
Nature Nanotechnology

M- List of well-known Conferences related to the Course

Design Automation Conference
International Conference on Computer-Aided Design
Asia and South Pacific Design Automation Conference
Design Automation and Test in Europe

N- List of Classic Journal Papers / Articles / Review Papers related to the Course

1. Logic Synthesis For VLSI Design By Richard L Rudell 1989
2. Cortadella, Jordi, et al. "RTL synthesis: From logic synthesis to automatic pipelining." Proceedings of the IEEE 103.11 (2015): 2061-2075.
3. Scarabottolo, I., Ansaloni, G., Constantinides, G. A., Pozzi, L., & Reda, S. (2020). Approximate logic synthesis: A survey. Proceedings of the IEEE, 108(12), 2195-2213.

O- List of Renowned Industries / Organizations / working in the Course related areas
Intel, AMD, Xilinx, Cadence, Mentor Graphics

P- List of Renowned Scientists / Academicians working in the Course related areas
Krishnendu Chakrabarty, Jingsheng Jason Cong, Wan-Ping Lee, Sharad Malik, Anand Raghunathan, Nikil Dutt

Q- Copies of the Mid and End Semester Examination Question Papers and Sample Answer Sheets

R- Attendance Record

Available at TCSIon

S- Records of the Continuous Assessment (Assignment, Quiz, Laboratory Work, etc.)

T- Details of Remedial Classes (with evidences)

U- Details of Expert Lectures / Industrial Visits/Events

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