CPRE 488 Spring 2024: Embedded Systems Design
HW 1: Pulse Position Modulation

Jonathan Hess
GitHub Page

Task 1: Relearning VHDL

1. Read Sections 7-7.1 of the Free Range VHDL book[1].
   (a) Describe an unclear aspect and post a question on the "In-Class Discussion" topic on Blackboard. If everything was clear, describe Listing 7.1 line-by-line.
   (b) In Section 7.4, complete exercises 1 and 2.

Task 2: Pulse Position Modulation

1. Compare PWM and PPM.
2. Draw a 6-channel PPM frame with a 20ms period, specified in milliseconds and clock cycles.
3. Design a Mealy-type state machine for capturing PPM frames (bubble diagram).
4. Design a Mealy-type state machine for generating PPM frames (bubble diagram).

Task 3: HW/SW Interface Table

Read through the entire MP-1 document and provide a table with columns for:

- Register Name
- Relative Register Offset
- Short Register Description

Task 4: High-level Architecture

Draw the high-level architecture of the MP-1 PPM interfacing system illustrating the location and interconnection of primary components.

[1] http://class.ece.iastate.edu/cpre488/resources/free_range_vhdl.pdf