RISC-V Processor

Milestone 02: Single Cycle Implementation

Computer Architecture

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- **Project Description**

The completed second milestone of this project marks a significant advancement in our endeavor to implement a RISC-V processor. At this stage, we have successfully crafted a robust Verilog description that supports the full range of RV32I instructions as specified in the RISC-V architecture. Additionally, we have developed a suite of basic test cases to validate the functionality and correctness of our implementation. This milestone represents a crucial step forward in realizing our project's objectives, laying a solid foundation for the subsequent stages of pipelined architecture design, comprehensive testing, and the incorporation of optional bonus features. With the successful completion of milestone two, we are well-positioned to advance further towards our ultimate goal of achieving a fully functional and optimized RISC-V processor implementation on FPGA hardware.

- **Supported Instructions**

Developed and Tested Instructions:

R-Type: ADD, SUB, SLL, SLT, SLTU, XOR, SRL, SRA, OR, AND

I-Type: LW, ADDI, SLTI, SLTIU, XORI, ORI, SLLI, SRLI, SRAI

U-Type: LUI, AUIPC

J-Type: JAL

B-Type: BEQ

S-Type: SW

Developed But yet to Be Tested:

B-Type: BNE, BLT, BGE, BLTU, BGEU

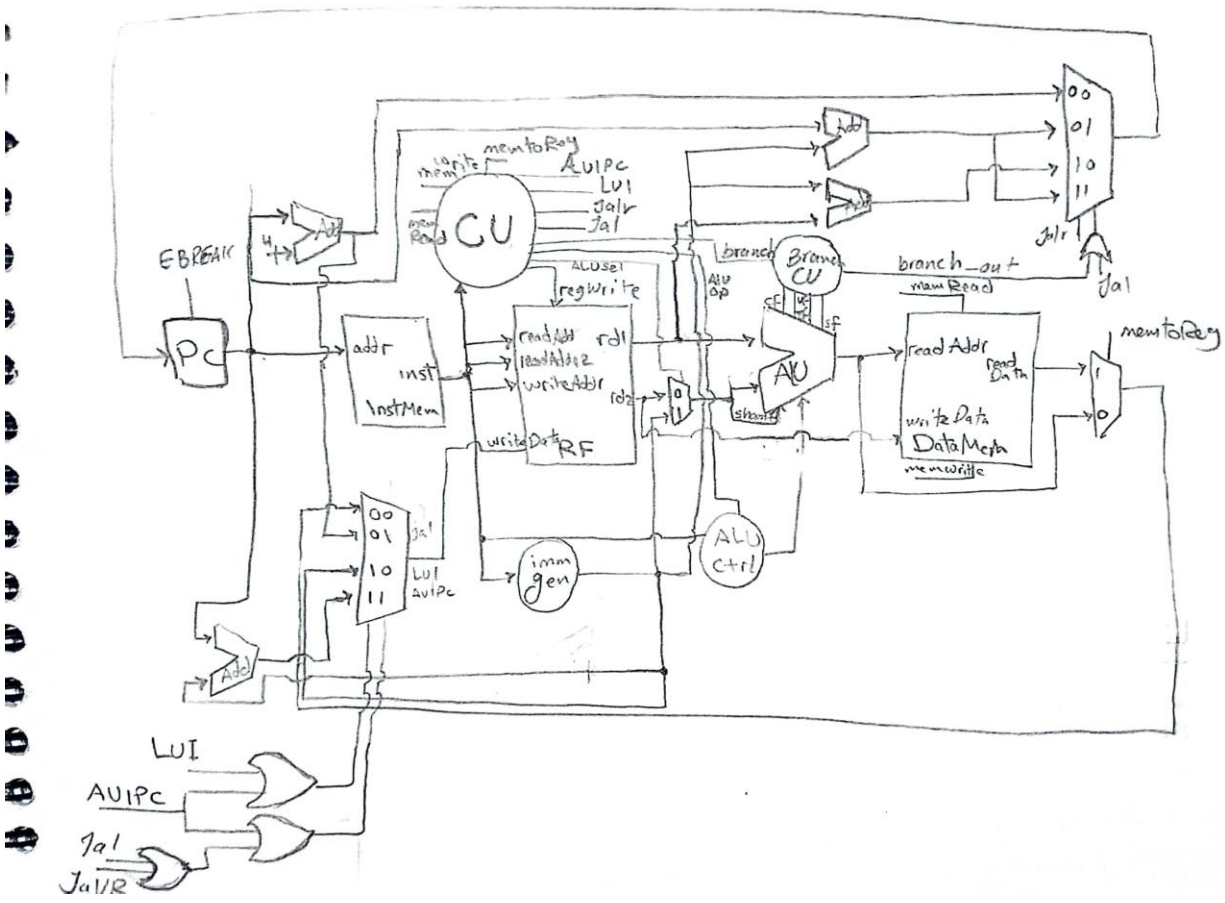
Yet to Be Developed:

I-Type: LB, LH, LBU,LHU

S-Type: SB, SH

ECALL, EBREAK

- **Implemented Datapath**



- **Simulations**