American International University- Bangladesh (AIUB)
Faculty of Engineering (EEE)

Course Name:	Digital Logic Circuits	**Course Code:**	EEE 3101
Semester:	Fall 24-25	**Section:**	S
Faculty:	Md. Shahariar Parvez	**Term:**	Final
Marks:	20	**Assignment Name:**	OBE Assignment
Student Name:	Chinmoy Guha	**Student ID:**	22-48056-2
Submission Date:	28.01.2025	**Department:**	CSE

COs/ CLOs Number	COs/CLOs Statements	K	P	A	Assessed Program Outcome Indicator	BNQF Indicator	Teaching-Learning Strategy
CO2	**Develop** a system in context of Digital logic circuits with 555 timer and transistors for **conflicting requirements** of complex engineering problem.	**3**	**P1,P2, P6**	**-**	**P.a.3.C3**	**FS.1**	**OBE Assignment** (Final Term)

Instructions Related to Use Variables:
Note that this problem uses the variables a, b, c, d, e, f, g and h, which are the digits of your student ID (ab-cdefg-h).
Any value in student ID comes '0' will be replaced by '(a+b+h)'

a	b	-	c	d	e	f	g	-	h
2	2	-	4	8	0	5	6	-	2

Marking Rubrics (to be filled by Faculty):

Complex Problem	Task	Assessment Criteria	Evaluation Criteria				Marks
P1, P2, P6	**I.**	Outline the necessary steps of block diagram	**Excellent (2.5)**	**Good (2-1.5)**	**Average (1-.5)**	**Poor (0)**	
			All the steps have been identified and in the correct sequences	Not All the steps have been identified and in the correct sequences	Few steps have been identified and in the correct sequences	All the steps have been found in wrong sequences	
		Design counter with necessary diagram	**Excellent (2.5)**	**Good (2-1.5)**	**Average (1-.5)**	**Poor (0)**	
			All the designs were accurate and working	Not All the designs were accurate and working	Few designs were accurate and working	All the design were wrong and not working	
	II.	Design of timer circuits 1 & 2	**Excellent (7)**	**Good (6-5)**	**Average (4-2)**	**Poor (1-0)**	
			Timer circuit design is correct and comply with the problem	Timer circuit is correct but not comply with the problem	Timer circuit is incorrect and does not comply with the problem	Timer circuit is wrong and not comply with the problem	
		Limitations of the developed system	**Excellent (3)**	**Good (2.5-2)**	**Average (1.5-1)**	**Poor (0)**	
			Provides limitations and analyzes the performance	Provides limitation only	Provides improper limitation and performance analyze	Provides no limitation and gives no performance analysis	
	III.	CMOS logic design	**Excellent (5-4)**	**Good (3-2)**	**Average (1.5-1)**	**Poor (0)**	
			The CMOS logic design is fully correct.	The CMOS logic design is mostly correct, with minor errors.	The CMOS logic design has significant errors, with multiple incorrect or missing segments.	The CMOS logic design is not attempted.	

Marks Obtained:

Digital Parking Control System:

The problem is to monitor available spaces in a (**a+g+h**)-space parking garage and provide an indication of a "FULL" by illuminating a display sign in seven seven-segment display along with driving a "Gate control" motor. From the Figure below, two sensors from the entrance and exit will be connected to the counter circuit to count. (i.e. the clock is synchronized with the sensors) and it will be placed into the register according to the binary bit value. Now, Keypad is used to provide your maximum available space, when the spaces are all filled up and the count is full then the display in seven segment display will show the "Full" Indication until the space is empty, and at the same time, the entrance gate control will turn on the "Gate Control" motor.

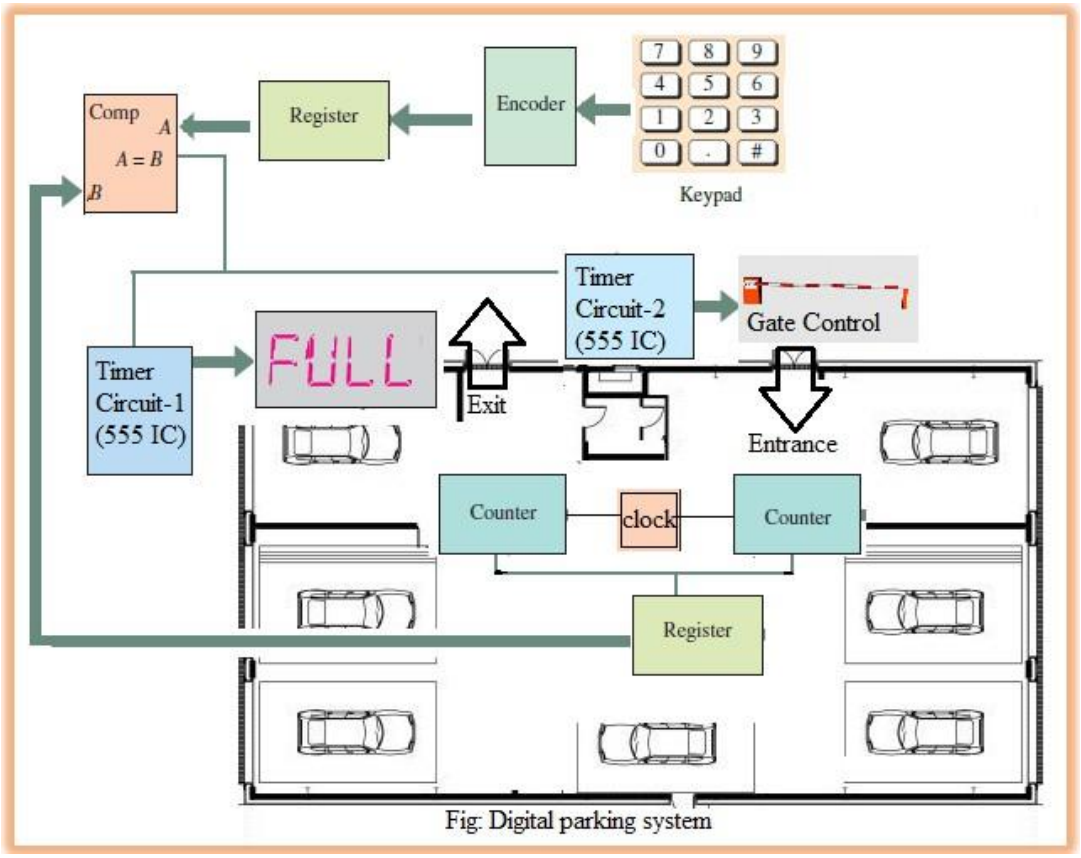


Fig: Digital parking system

Your task is to:

i. Outline the essential steps in the correct sequence to develop a block diagram for designing an automated parking control system. This system should include an actuated gate mechanism, a "FULL" indication using a seven-segment display, and a counter circuit. In addition, Design the counter circuit which is capable of simultaneous UP/DOWN counting. Include additional sequential and combinational logic components, if required, to ensure smooth control and operation, providing appropriate reasoning for selecting these components.

ii. Design the timer circuit 1 and the timer circuit 2 with a suitable frequency based on your requirement, in which the capacitor value will be C = (c*g+20) µF. Identify the limitations of the designed system and analyze the impact of increasing the number of parking spaces on its performance.

iii. Design the functions of your seven-segment display using CMOS technology to represent one of the letters in the word "FULL".

Name: Chinmoy Guha
ID: 22-48056-2
ab-cdefg-h

(i) Steps to develop a block diagram:

1) Provide a numeric keypad for the user to input the maximum number of parking spaces.
   - For Example -> '10' for a parking lot with 10 spaces

2) Use an Encoder to convert the input from the keypad into binary value:
   - For Example -> '10' becomes '1010'

3) Use a Register as a data storage (PIPO) to store the current value from the encoder and feed it to the comparator. This is register A.

4) Place two IR sensors at the entrance and exit to detect incoming and outgoing cars. The sensor generates a pulse which acts as clock signals for counter.

5) Use a bidirectional Counter (UP/DOWN) to keep track of when the parking spaces fill up.
   - When a car enters -> the sensor generates a clock pulse that increments the counter
   - When a car exits -> the sensor generates a clock pulse that decrements the counter.

6) Use another register to store the current count from the counter. This is register B.

7) Use 4bit comparator to take input from register A and register B. This will compare the current count from register B with maximum capacity from register A.

8) The output from the comparator is fed into two 555 IC Timers, 1 and 2. Timer Circuit 1 connects to a seven-segment display and Timer Circuit 2 connects to a gate control mechanism.

9) Drive the seven-segment display using a BCD to seven-segment decoder. When the comparator outputs full, it displays the word 'FULL' on the display.

10) The Timer circuit 2 manages the time delay between gate opening and gate closing. A motor is used for the gate control that is activated to rotate to open the gate. When the comparator outputs 'FULL', the entrance gate is disabled by stopping this motor.

* UP / Down Counter Circuit:

The parking capacity = 10 (at 8th) = (2+6+2) = 10
→ 10 in binary is 1010 → This requires 4 bits.
∴ we need a 4-bit UP/down counter.

UP	$Q_3 Q_2 Q_1 Q_0$	Down
↓	0 0 0 0	
↓	0 0 0 1	
↓	0 0 1 0	
↓	0 0 1 1	
↓	0 1 0 0	
↓	0 1 0 1	
↓	0 1 1 0	
↓	0 1 1 1	
↓	1 0 0 0	
↓	1 0 0 1	
↓	1 0 1 0	
↓	1 0 1 1	
↓	1 1 0 0	
↓	1 1 0 1	
↓	1 1 1 0	
↓	1 1 1 1	

$J_0 = K_0 = 1$

$J_1 = K_1 = (Q_0 \cdot UP) + (\overline{Q_0} \cdot \overline{Down})$

$J_2 = K_2 = (Q_1 Q_0 UP) + (\overline{Q_1}\,\overline{Q_0}\,\overline{Down})$

$J_3 = K_3 = (Q_2 Q_1 Q_0 UP) + (\overline{Q_2}\,\overline{Q_1}\,\overline{Q_0}\,\overline{Down})$

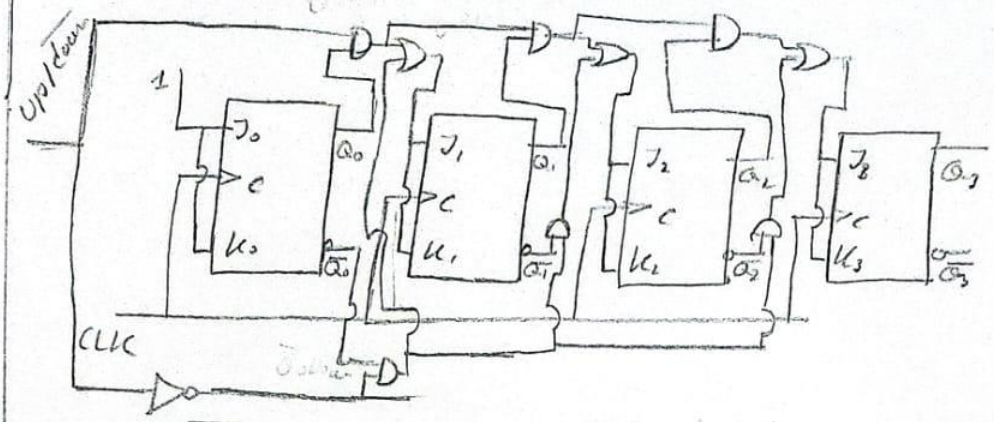


Fig. The UP/Down Counter

(ii) $C = (c * g + 20) = (4 * 6 + 20) = 44\mu F$

Timer Circuit 1 : (Astable)

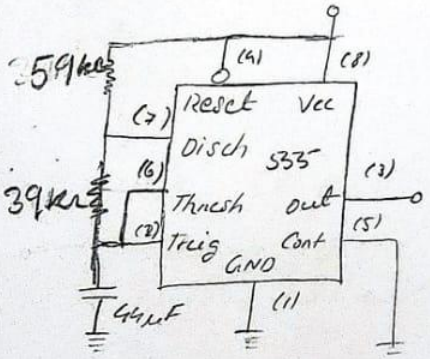
Lets assume $T_H = 3s$, $T_L = 1.2s$. $\therefore T = 3 + 1.2 = 4.2s$

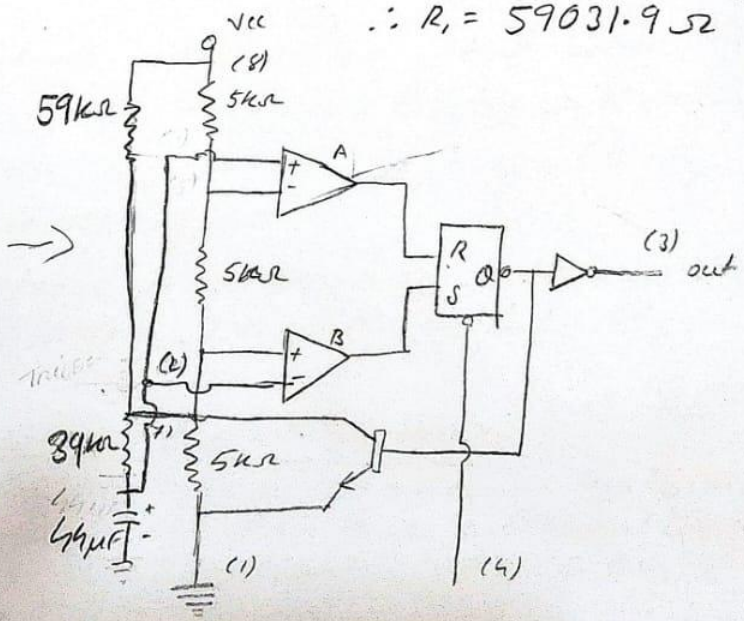
$\therefore F = \frac{1}{T} = \frac{1}{4.2} = 0.238\,Hz$

$T_L = 0.693\,C\,R_2 \Rightarrow R_2 = \frac{1.2}{0.693 \times 44 \times 10^{-6}} = 39354.6\,\Omega$

$T_H = 0.693\,(R_1 + R_2)C \Rightarrow R_1 + R_2 = \frac{3}{0.693 \times 44 \times 10^{-6}} = 98386.5\,\Omega$

$\therefore R_1 = 59031.9\,\Omega$





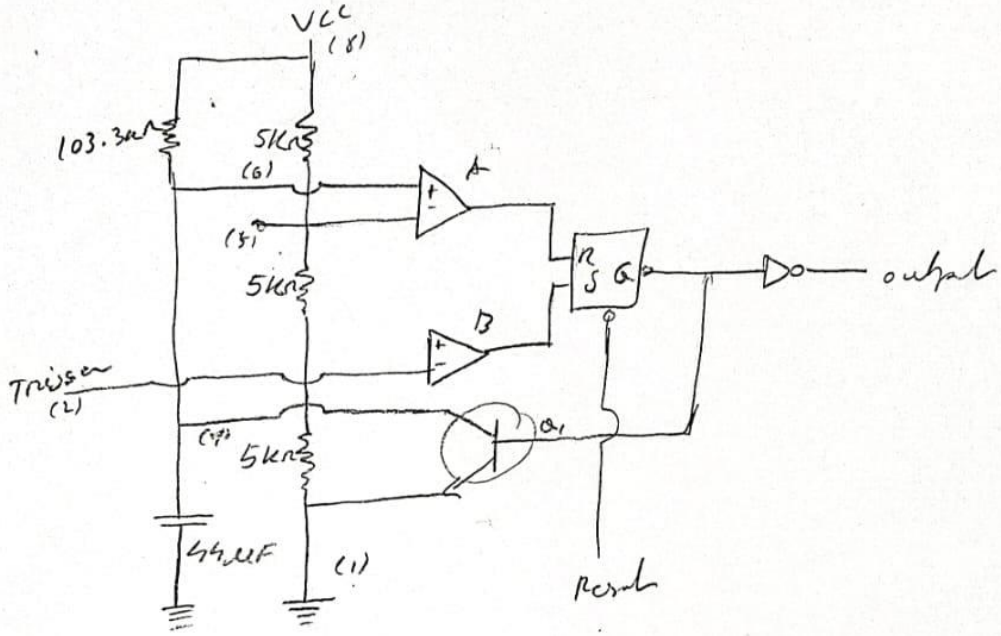
Timer Circuit 2: (Monostable)

If we take $T_W = 5s$, $C = 44\mu F$

$T_W = 1.1RC$

$R = \frac{5}{1.1 \times 44 \times 10^{-6}} = 103305.78$

$= 103\ k\Omega$



Limitations:

- One of the limitations in this system is that when the parking space is full, the 7-segment display will show an F but when a car leaves, the display still may show Full even if there is space.
- Moreover if the entrance or exit sensor misdetects an object which is not a car, it may incorrectly update the counter.

Impact of increasing number of parking spaces:

Since we are using a 4bit counter it can count upto 16 spaces, but if it increase more than that, we would need a greater counter like (8bit) counter. A BCD based seven segment display only supports 0-9 so for higher counts a multiplexed display or LCD would be needed.

With more cars the entry/exit frequency will increase so Timer 2 may need more adjustment for a faster operation. The overall design will get bigger and may decrease efficiency.

(iii) A seven-segment display consists of seven LEDs labeled a, b, c, d, e, f, g.

To display 'F' the following segments should be

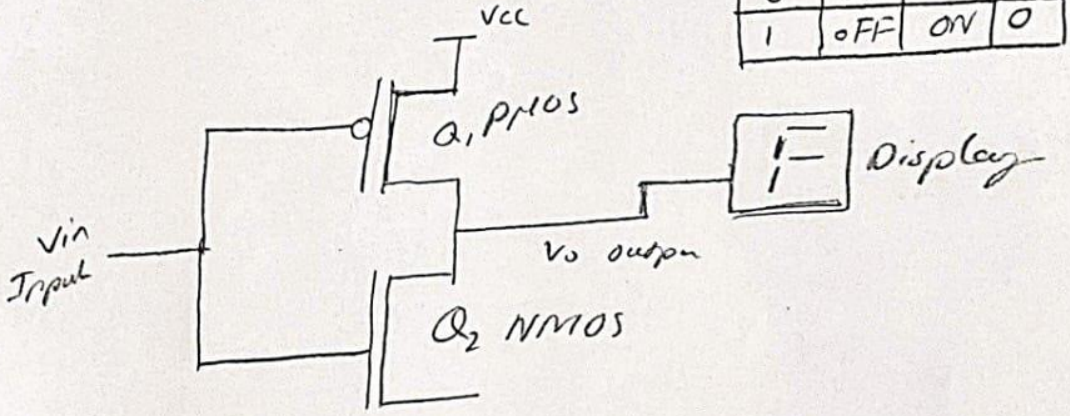
ON: a, e, f, g

OFF: b, c, d.

a	b	c	d	e	f	g
1	0	0	0	1	1	1

Vin	Q_1	Q_2	V_o
0	ON	OFF	1
1	OFF	ON	0

Using CMOS →



Vin