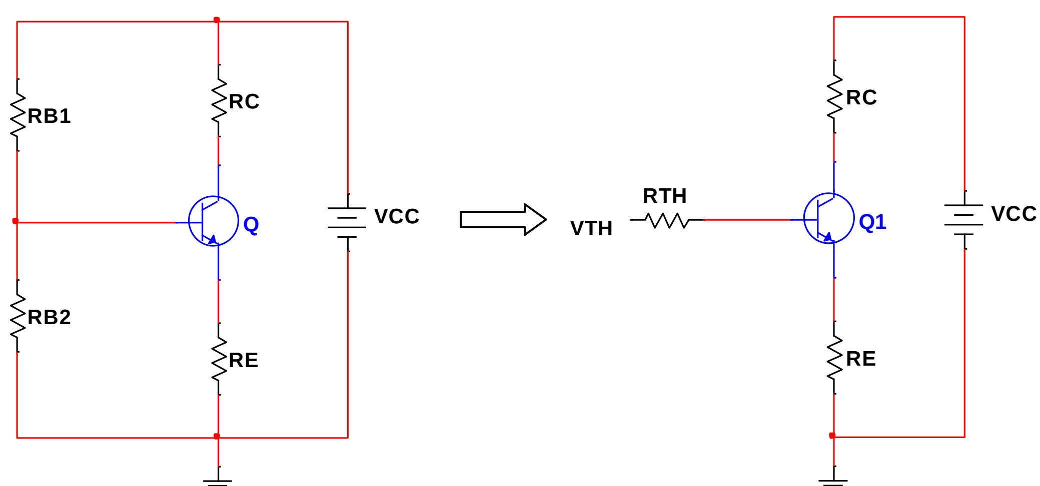
American International University- Bangladesh
Faculty of Engineering (FE)
Department of Electrical and Electronic Engineering (EEE)
EEE 2104: Electronic Devices Lab

Title of the Experiment: Study of BJT Biasing Circuit – Fixed Bias and Self-Bias Circuits.

Objectives:
The objectives of this experiment are to
1. Establish the proper DC operating point of a bipolar transistor.
2. Study the stability of the operating point with respect to changing β in different biasing circuits.

Theory:
The operating point (Q) of a BJT is very important for amplifiers since a wrong 'Q' point selection increases amplifier distortion. It is imperative to have a stable 'Q' point, meaning that the operating point should not be sensitive to variation in temperature or gain of BJT (β), which can vary widely. In this experiment, four different circuits will be analyzed for two different β to check the stability of biasing points.
The analysis of the BJT circuits is a systematic process. Initially, the operating point of a transistor circuit is determined then the small signal BJT model parameters are calculated. Finally, the DC sources are eliminated, the BJT is replaced with an equivalent circuit model, and the resulting circuit is analyzed to determine the voltage amplification (A_V), current amplification (A_I), Input impedance (Z_i), Output Impedance (Z_o), and the phase relation (θ) between the input voltage (V_i) and the output voltage (V_o).
The experiment is a very good practical realization of the Bipolar Junction Transistor (BJT) biasing circuit. A BJT biasing circuit will be designed and simulated to find a DC operating point using a circuit simulation tool. Then a fixed-biasing and a self-biasing BJT circuits will be implemented on the trainer board to find a DC operating point for two different β of the transistor.
The DC analysis is done to determine the mode of operation of the BJT and to determine the voltages at all nodes and currents in all branches. The operating point of a transistor circuit can be determined by mathematical or graphical (using transistor characteristic curves) means. Here, we will describe only the mathematical solution.



(a) Original circuit (b) Thevenin equivalent circuit

Figure 1: Circuit diagram for biasing of an npn transistors.

We will use the most applied biasing circuit to operate the BJT as an amplifier. A single power supply is used and the voltage divider network consisting of two resistors at the base, R_{B1} and R_{B2} is used to adjust the base voltage. Using the Thevenin theorem, the voltage divider network may be modeled by a Thevenin equivalent circuit and is replaced by Thevenin equivalent voltage, V_{TH} and Thevenin equivalent resistance, R_{TH} where,

$V_{TH} = \frac{R_{B2}}{R_{B1}+R_{B2}} V_{CC}$, applying the VDR across two-resistor network.
$R_{TH} = \frac{R_{B1}R_{B2}}{R_{B1}+R_{B2}}$, shorting the voltage source, V_{CC} at the base terminal.

The DC analysis of the circuit is simple by applying KVL at the input and the output loops of Fig. 1 (b). Applying KVL in the input loop of Fig. 1 (b).

$$V_{TH} = I_B R_{TH} + V_{BE} + I_E R_E = I_B R_{TH} + V_{BE} + (I_B + I_C) R_E$$
$$\Rightarrow V_{TH} = I_B R_{TH} + V_{BE} + (I_B + \beta I_B) R_E = I_B \{R_{TH} + (1+\beta) R_E\} + V_{BE}$$
$$\Rightarrow I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (1+\beta) R_E}$$

Applying KVL in the output loop of Fig. 1 (b).

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E = I_C R_C + V_{CE} + (I_B + I_C) R_E$$
$$\Rightarrow V_{CC} = I_C R_C + V_{CE} + I_C R_E;\ \ I_C \gg I_B$$
$$\Rightarrow I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}$$

So, the quiescent point collector and emitter currents as well as collector-to-emitter voltage can be written as-

$$I_{CQ} = \beta I_B$$
$$I_{EQ} = (1+\beta) I_B$$
$$V_{CEQ} = V_{CC} - I_{CQ} R_C - I_{EQ} R_E$$

If the BJT is in the active mode, the following typical values can be observed-

$$V_{BE} = 0.7 \text{ V and } I_C = \beta I_B$$

The collector resistance, R_C is used to adjust the collector voltage, V_C. Finally, the emitter resistance, R_E is used to stabilize the DC biasing point (operating point or quiescent point or Q-point). Using the above equations, the stability of biasing points for different transistors of β can be calculated.

Note: It is a good idea to set the bias for a single stage amplifier to half the supply voltage, as this allows maximum output voltage swing in both directions of an output waveform. For maximum symmetrical swing, it is clear from the figure that the collector-to-emitter voltage, V_{CE} should be equal to the half of the collector supply voltage, V_{CC} that is, $V_{CE} = V_{CC}/2$.

Circuit Configuration:

Figure 2 shows the symbol for the npn transistor and pnp transistor. The emitter of the BJT is always marked by an arrow, which indicates whether the transistor is an npn or a pnp transistor

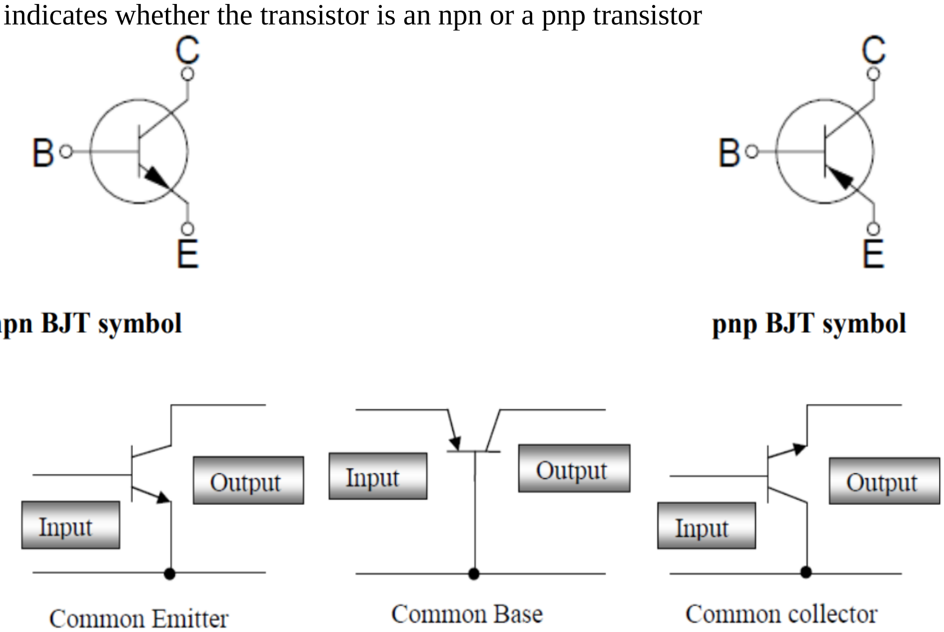


Figure 2: Emitter, collector, and base of transistors and the connection modes.

There are three basic ways in which a BJT can be configured as shown in Fig. 2. In each case, one terminal is common to both the input and output circuits shown in the figure above.

1. The common emitter configuration is used for voltage and current amplification and is the most common configuration for transistor amplifiers.
2. The common collector configuration is often called an emitter follower since its output is taken from the emitter resistor. It is useful as an impedance-matching device since its input impedance is much higher than its output impedance.
3. The common base configuration is used for high-frequency applications because the base separates the input and output, minimizing oscillations at high frequencies. It has a high voltage gain, relatively low input impedance, and high output impedance compared to the common collector.

Biasing of Bipolar Junction Transistors:
In most cases, the BJT is used as an amplifier or switch. To perform these functions, the transistor must be correctly biased. Depending on the bias condition (forward or reverse) of each of the BJT junctions, different modes of operation of the BJT are obtained.
The three modes are defined as follows:

1. **Active Mode:** The emitter junction is forward-biased, and the collector junction is reverse-biased. If the BJT is operated in active mode, then the BJT can be used as an amplifier.
2. **Saturation Mode:** Both the emitter and collector junctions are forward-biased. If the BJT is used as a switch, the saturation mode corresponds to the on-state of the BJT.
3. **Cut-off Mode:** Both the emitter and collector junction are reverse-biased. If the BJT is used as a switch, the cut-off mode corresponds to the off state of the BJT.

In this experiment, we will learn how to set the transistor in the **active mode**, that is the operating point should be set in the active region of operation (blue shaded portion) in the output characteristics of the transistor as shown in Fig. 3. To do this, we need to set a constant base current by adjusting the base bias resistor values.

Output Characteristics:
The output characteristics curves for a common emitter configured BJT are plotted between the collector current, I_C, and the collector-to-emitter voltage drop by keeping the base current, I_B constant as shown in Fig. 3. These curves are almost horizontal. The output dynamic resistance again can be calculated from the ratio of the small change of emitter-to-collector voltage drop to the small change of the collector current.

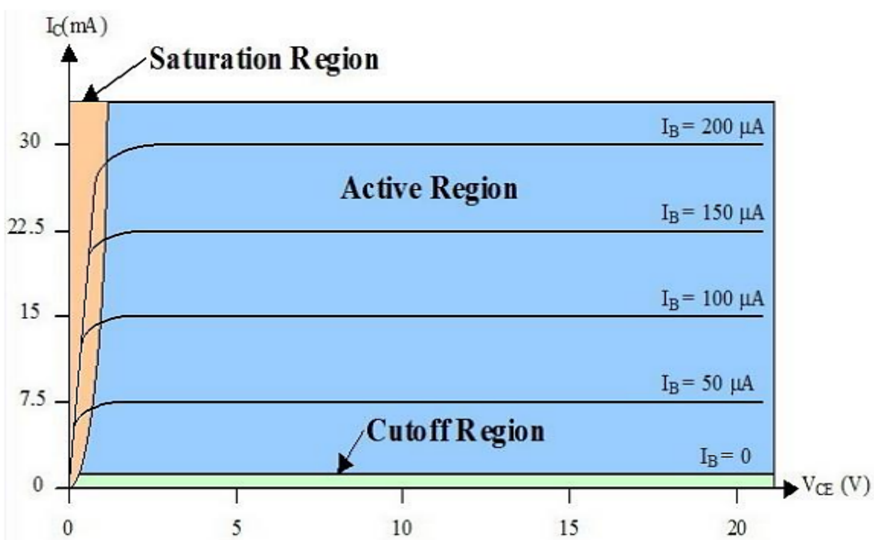


Figure 3: BJT Common Emitter Output Characteristics.

Pre-Lab Homework:
Students will be provided with the upcoming lab manuals, and they will be asked to prepare the theoretical (operations/working principle) information on the topic from the textbook.

Besides, they must implement the circuit (as given in Figure 4) using a MultiSIM simulator. Observe the base and collector currents as well as collector to emitter voltage through simulations (I_B, I_C, and V_{CE}) and take snapshots using the snipping tool. Measure the values of different key parameters and fill up the table (Table 1) based on the simulation results. For simulation, use a 2N2222, or a C828, or BD135 transistor.

Apparatus:

SL#	Apparatus	Quantity
1	BJT (2N2222, C828, BD135)	1 each
2	Resistance ($R_{B,POT}$ = 0-500 kΩ, R_C = 470 Ω, R_E = 560 Ω, R = 22 kΩ)	1 each
4	Project Board	1
7	DC milliammeter (0-50 mA)	1
8	DC microammeter (0-500 μA)	1
9	Multimeter	1
10	Connecting Leads	10

Precaution!

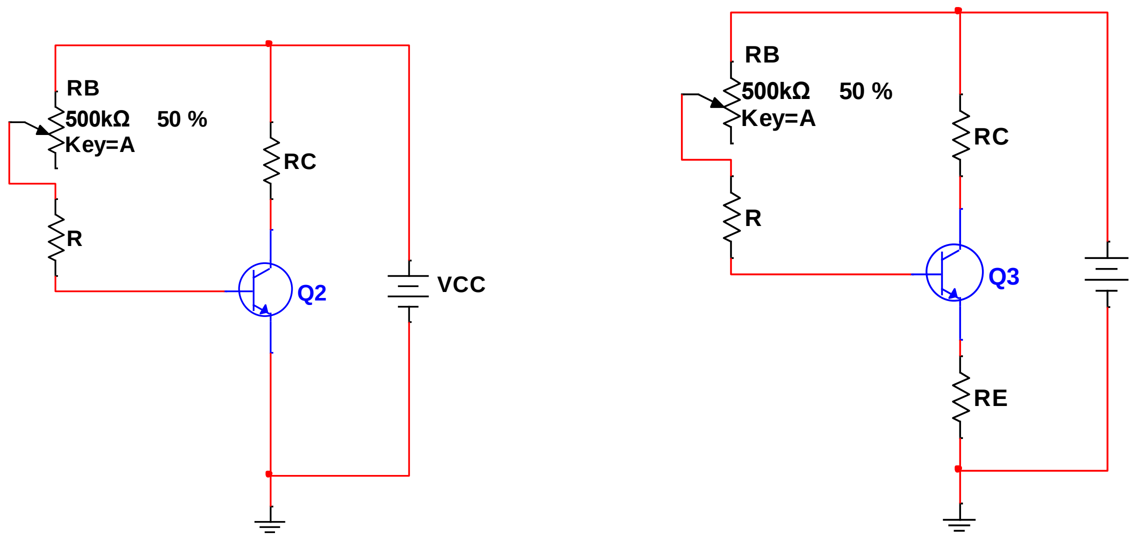
The following is a list of some of the special safety precautions that should be taken into consideration when working with transistors:

1. **Never remove or insert a transistor into a circuit with voltage applied.**
2. **Ensure a replacement transistor into a circuit is in the correct direction.**
3. **Transistors are sensitive to being damaged by electrical overloads, heat, humidity, and radiation. Damage of this nature often occurs by applying the incorrect polarity voltage to the collector circuit or excessive voltage to the input circuit.**
4. **One of the most frequent causes of damage to a transistor is the electrostatic discharge from the human body when the device is handled.**
5. **The applied voltage and current should not exceed the maximum rating of the given transistor.**
6. **Change the components or any of their properties by turning off the power/stopping the simulation.**

Experimental Procedures:

(A) Study of BJT Fixed-Bias and Self-Bias Circuits:

1. Measure the actual values of the base and collector resistors.
2. Identify the terminals of the transistor and record the value of Beta (β).
3. Connect the circuit and connect the microammeter and milliammeter as shown in Fig. 4 (a).
4. Connect the multimeter (voltmeter mode) to measure the base resistance voltage (V_B) and input voltage (V_{BE}).
5. Turn on both the DC power supply with the voltage control nob at 0 V and then set the collector supply voltage, V_{CC} to 15 V.
6. Now, adjust the 500 kΩ potentiometer until the collector-to-emitter voltage, V_{CE} is approximately equal to the half of the collector supply voltage, V_{CC} that is, $V_{CE} = V_{CC}/2$.
7. Measure collector-to-emitter voltage, V_{CE}, base-to-emitter voltage, V_{BE}, base current, I_B, and collector current, I_C. Calculate the based current, I_B from the collector current, I_C. Record them in Table 1.
8. Now replace the first transistor by the second one (having a different value of β) and repeat the steps 6-7.
9. Construct the self-bias circuit shown in Fig. 4 (b).
10. Measure the actual values of the base, emitter, and collector resistors, and repeat steps 2-8. In step 7, you need to measure emitter current, I_E.
11. Record the images of the hardware circuit diagrams.
12. Turn off the DC power supply.



(a) Fixed-Bias Circuit; (b) Self-Bias Circuit

Figure 4: Circuit diagram for the study of CE transistor bias circuits

Table 1 Data for the measurement of various bias circuit and transistor parameters

	Transistor	**β**	V_{CE}	V_{BE}	I_B	I_C	I_E
Fig. 4 (a)							
% of Change							
Fig. 4 (b)							
% of Change							

Questions:

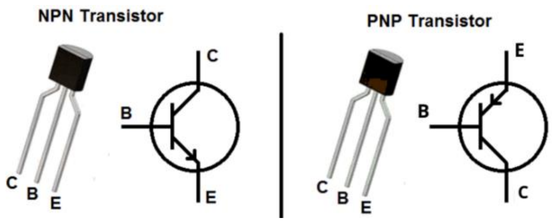
1. Show the difference between your simulated and measured values. Comment on the results and interpret the experimental and simulation data.
1. From the obtained data draw the output characteristic curves for a BJT and point out the Q point. Explain the behavior of the circuit in this region of operation.
2. Determine the BJT parameters from the data sheet.
3. Why biasing is necessary for BJT?
4. What is the Q-point? What do you mean by stability? Discuss the significance of Q point in relation to stability of the transistor circuit.
5. Compare the circuits of Figs. 4 (a) and 4 (b) with respect to stability against variation in β. Compare the stability of fixed bias circuits to that of self-bias circuits.
6. Give your suggestions regarding this experiment.
7. Discuss the overall aspects of the experiment. Did your results match the expected ones? If not, explain.

References:

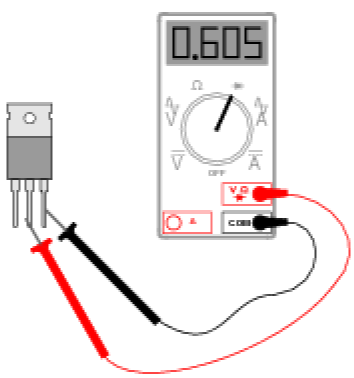
[1] Robert L. Boylestad, Louis Nashelsky, Electronic Devices and Circuit Theory, 9th Edition, 2007-2008
[2] Adel S. Sedra, Kenneth C. Smith, Microelectronic Circuits, Saunders College Publishing, 3rd ed., ISBN: 0-03-051648-X, 1991.
[3] American International University–Bangladesh (AIUB) Electronic Devices Lab Manual.
[4] David J. Comer, Donald T. Comer, Fundamentals of Electronic Circuit Design, John Wiley & Sons Canada, Ltd., ISBN: 0471410160, 2002.
[5] J. Keown, ORCAD PSpice and Circuit Analysis, Prentice Hall Press (2001)
[6] Resistor values: *https://www.eleccircuit.com/how-to-basic-use-resistor/*, accessed on 20 September 2023.

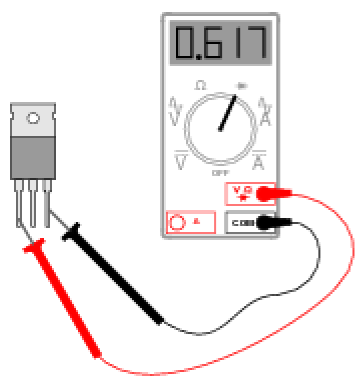
List the references that you have used to answer the "Discussion" section.

Appendix A: Identifying the terminals of an npn or a pnp transistor:



Following are the steps to identify npn and pnp transistors:
Step 1: Take the transistor you want to identify.
Step 2: Turn on a digital multimeter and set it to the DC voltage/resistance measurement mode.
Step 3: Make sure that you have connected the probes in their correct respective multimeter sockets, i.e., the black probe to the COM port and the red probe to the V/Ω/ port.
Step 4: Randomly start connecting the multimeter probes to the terminal of an unknown type of transistor and watch readings on the screen.
Step 5: Now, some random connections will give you a voltage/resistance reading on the multimeter screen.
Step 6: Once you get results i.e., any values (must be less than 1 for voltage reading) on the screen, start from the right side with the transistor's flat side upward direction, and write or mark the probes attached to the terminals of the transistor.
Step 7: If it is a black probe first and a red probe second then transfer the black probe to the third terminal (left-most terminal). If you get a similar result on the screen then write n, p, and n, that is the transistor is of npn type.
Step 8: If it is a red probe first and then a black probe second then transfer the red probe to the third terminal (left-most terminal). If you get a similar result on the screen then write p, n, and p, that is the transistor is of pnp type.
Step 9: The values you get on the multimeter screen after and before transferring the probe from the right-most side to the left-most side will differ slightly, the higher value-giving terminal is called the emitter and the lower value-giving terminal is called the collector, and the common terminal in the middle is called the base.

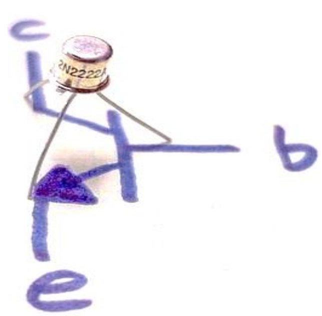




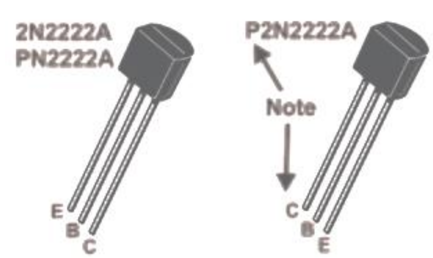
Based on the above procedural steps using a multimeter in diode mode, the left terminal of this transistor is a p-type emitter (producing larger value), the middle one is a p-type collector (less value), and the right one is called a base (common black terminal, so n-type). As such, this is a pnp-type transistor.

Appendix B: The 2N2222 Data Sheet

The 2N2222 is a common NPN bipolar junction transistor (BJT) used for general-purpose low-power amplifying or switching applications. It is designed for low to medium current, low power, medium voltage, and can operate at moderately high speeds. It was originally made in the TO-18 metal can as shown in the picture.



2N2222A in metal TO-18 package with the emitter, base and collector identified as E, B, and C respectively.



Pinout of 2N2222 variants in plastic TO-92 package.

2N2222A in metal TO-18 package with the emitter, base and collector identified as E, B, and C respectively.

Philips Semiconductors **Product specification**

NPN switching transistors 2N2222; 2N2222A

FEATURES

- High current (max. 800 mA)
- Low voltage (max. 40 V).

APPLICATIONS

- Linear amplification and switching.

DESCRIPTION

NPN switching transistor in a TO-18 metal package.
PNP complement: 2N2907A.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector, connected to case

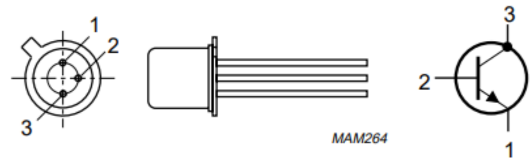


Fig.1 Simplified outline (TO-18) and symbol.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	2N2222		–	60	V
	2N2222A		–	75	V
V_{CEO}	collector-emitter voltage	open base			
	2N2222		–	30	V
	2N2222A		–	40	V
I_C	collector current (DC)		–	800	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	500	mW
h_{FE}	DC current gain	I_C = 10 mA; V_{CE} = 10 V	75	–	
f_T	transition frequency	I_C = 20 mA; V_{CE} = 20 V; f = 100 MHz			
	2N2222		250	–	MHz
	2N2222A		300	–	MHz
t_{off}	turn-off time	I_{Con} = 150 mA; I_{Bon} = 15 mA; I_{Boff} = –15 mA	–	250	ns

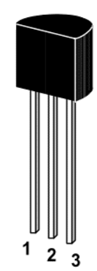
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter			
	2N2222		–	60	V
	2N2222A		–	75	V
V_{CEO}	collector-emitter voltage	open base			
	2N2222		–	30	V
	2N2222A		–	40	V
V_{EBO}	emitter-base voltage	open collector			
	2N2222		–	5	V
	2N2222A		–	6	V
I_C	collector current (DC)		–	800	mA
I_{CM}	peak collector current		–	800	mA
I_{BM}	peak base current		–	200	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	–	500	mW
		$T_{case} \leq 25$ °C	–	1.2	W
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature		–	200	°C
T_{amb}	operating ambient temperature		–65	+150	°C

Appendix C: The C828 Data Sheet

ST 2SC828 / 828A is an NPN Silicon Epitaxial Planar Transistor for switching and AF amplifier applications. These transistors are subdivided into three groups Q, R and S according to their DC current gain. On special request, these transistors can be manufactured in different pin configurations. TO-92 Plastic Package Weight approx. 0.19 gm.



1. Emitter 2. Collector 3. Base

Pin configuration of TO-92 Plastic Package.

Absolute Maximum Ratings (T_a = 25°C)

	Symbol	Value		Unit
		ST 2SC828	ST 2SC828A	
Collector Base Voltage	V_{CBO}	30	45	V
Collector Emitter Voltage	V_{CEO}	25	45	V
Emitter Base Voltage	V_{EBO}	7		V
Peak Collector Current	I_{CM}	100		mA
Collector Current	I_C	50		mA
Power Dissipation	P_{tot}	400		mW
Junction Temperature	T_j	150		°C
Storage Temperature Range	T_S	-55 to +150		°C

Characteristics at T_{amb}=25 ^{O}C

	Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at I_C=2mA, V_{CE}=5V Current Gain Group Q	h_{FE}	130	-	280	-
R	h_{FE}	180	-	360	-
S	h_{FE}	260	-	520	-
Collector Base Breakdown Voltage at I_C=10μA ST 2SC828	$V_{(BR)CBO}$	30	-	-	V
ST 2SC828A	$V_{(BR)CBO}$	45	-	-	V
Collector Emitter Breakdown Voltage at I_C=2mA ST 2SC828	$V_{(BR)CEO}$	25	-	-	V
ST 2SC828A	$V_{(BR)CEO}$	45	-	-	V
Emitter Base Breakdown Voltage at I_E=10μA	$V_{(BR)EBO}$	7	-	-	V
Collector Saturation Voltage at I_C=50mA, I_B=5mA	$V_{CE(sat)}$	-	0.14	-	V
Base Emitter Voltage at I_C=10mA, V_{CE}=5V	V_{BE}	-	-	0.8	V
Gain Bandwidth Product at I_C=-2mA, V_{CE}=10V	f_T	-	220	-	MHz
Noise Figure at V_{CE}=5V,I_E=0.2mA, R_G=2kΩ,f=1kHz	NF	-	6	-	dB