American International University- Bangladesh
Faculty of Engineering (FE)
Department of Electrical and Electronic Engineering (EEE)
EEE 2104: Electronic Devices Lab

Title of the Experiment: Study of Inverter Circuits using MOSFET and BJT.

Objectives:
The objectives of this experiment are to
1. Design and implement RTL BJT inverter, RTL NMOS inverter, and CMOS inverter circuits.
2. Understand the basic operation of inverter circuits.
3. Measure the input and output voltage to obtain the transfer characteristics of inverter circuits.
4. Verify the truth tables of inverter circuits.

Theory:
This experiment gives an excellent practical realization of the RTL BJT inverter, RTL NMOS inverter, and CMOS inverter. At first, a CMOS inverter will be designed, simulated, and understood. Then all kinds of inverter circuits mentioned above will be designed on the project board in the laboratory and the theoretical concepts will be developed and the practical results will be analyzed. The circuit symbol of an inverter circuit is given in Fig. 1, and the truth table of the same is given in Table 1.

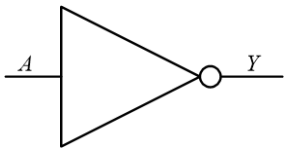

Figure 1: Circuit symbol of an inverter circuit.

Table 1 Truth Table of an Inverter Circuit.

A	***Y***
0	1
1	0

RTL Inverter:

Resistor-Transistor Logic (RTL) is a large step beyond Diode Logic (DL). Basically, RTL replaces the diode switch with a transistor switch. If a +5V signal (logic 1) is applied to the base of the transistor (through an appropriate resistor to limit base-emitter forward voltage and current), the transistor turns fully on and grounds the output signal. If the input is grounded (logic 0), the transistor turns off and the output signal rises to +5 volts. In this way, the transistor inverts the logic sense of the signal, but it also ensures that the output voltage will always be a valid logic level under all circumstances. RTL circuits can be cascaded indefinitely, whereas DL circuits cannot be cascaded reliably at all.

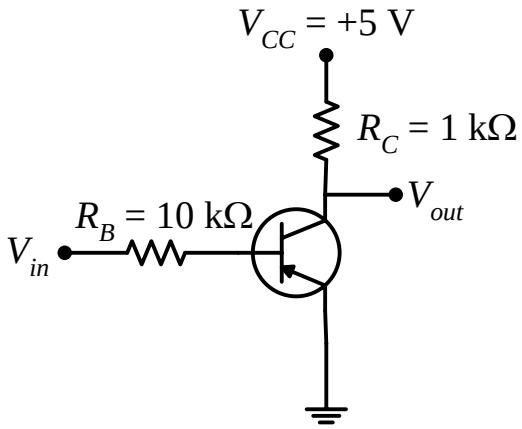

Figure 2: BJT-based RTL inverter circuit.

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NMOS Inverter:

An inverter can be designed with a single NMOS and a resistor. In the case of an NMOS inverter, two NMOS are used where one is used as a load and another one is used for inverting the input. The load transistor must have a high and the switching transistor must have low resistance.

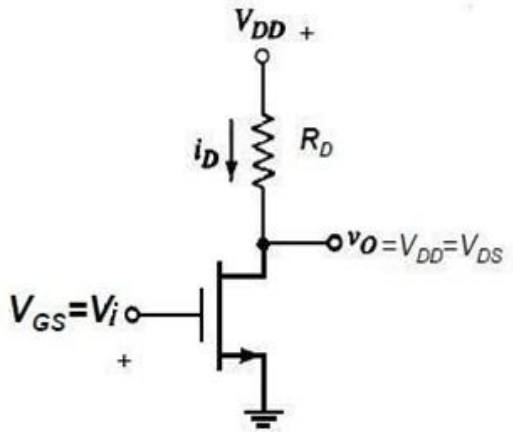

Figure 3: NMOS-based RTL inverter circuit

CMOS Inverter:

The two MOSFETs are designed to have matching characteristics. Thus, they are complementary to each other. When off, their resistance is effectively infinite; when on, their channel resistance is about 200 Ω. Since the gate is essentially an open circuit it draws no current, and the output voltage will be equal to either ground or to the power supply voltage, depending on which transistor is conducting.

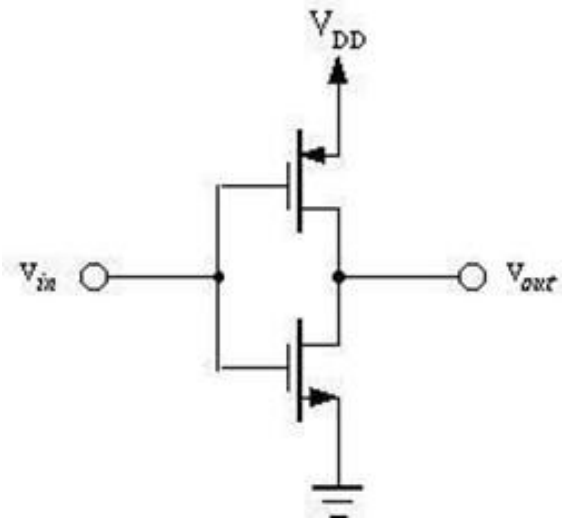

Figure 4: CMOS-based inverter circuit.

When input A is grounded (logic 0), the N-channel MOSFET is unbiased and therefore has no channel enhanced within itself. It is an open circuit and therefore leaves the output line disconnected from the ground. At the same time, the P-channel MOSFET is forward-biased, so it has a channel enhanced within itself. This channel has a resistance of about 200 Ω, connecting the output line to the +V supply. This pulls the output up to +V (logic 1). When input A is at +V (logic 1), the P-channel MOSFET is off and the N-channel MOSFET is on, thus pulling the output down to ground (logic 0). Thus, this circuit correctly performs logic inversion, and at the same time provides active pull-up and pull-down, according to the output state.

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Pre-Lab Homework:

Students will be provided with the upcoming lab manuals, and they will be asked to prepare the theoretical (operations/working principle) information on the topic from the textbook.

Besides, they must implement the circuit (as given in Figures 9-10) using a **MultiSIM simulator**. Observe the gate and drain voltages and currents through simulations (I_D, I_G, V_{DS}, V_{GS}) and take snapshots using the snipping tool. Measure the values of different key parameters and fill up the tables (Tables 1-4) based on the simulation results. For simulation, use a J176 as the p-channel JFET, a 2N7000/IRF540N/BUK444/IRF740/IRF840 as the n-channel MOS transistor, and 9540 as the p-channel MOS transistor. Perform the following tasks as well:

1. Draw and explain the operation of the inverter circuits using truth tables.
2. Draw and explain the transfer characteristics of inverter circuits.

Apparatus:

SL#	Apparatus	Quantity
1	**C828/2N4124** (npn BJT); 2N7000/**IRF540N** (n-channel enhancement type MOSFET); **9540** (p-channel enhancement type MOSFET).	1 each
2	Resistance (R = 1 kΩ , 10 kΩ, 100 kΩ)	1 each
3	Project Board	1
4	Function Generator + DC Power Supply	1 each
5	DC milliammeter (0-50 mA)	1
6	Oscilloscope	1
7	Multimeter	1
8	Connecting Leads	10

Precaution!

The following is a list of some of the special safety precautions that should be taken into consideration when working with transistors:

1. **Never remove or insert a transistor into a circuit with voltage applied.**
2. **Ensure a replacement transistor into a circuit is in the correct direction.**
3. **Transistors are sensitive to being damaged by electrical overloads, heat, humidity, and radiation. Damage of this nature often occurs by applying the incorrect polarity voltage to the collector circuit or excessive voltage to the input circuit.**
4. **One of the most frequent causes of damage to a transistor is the electrostatic discharge from the human body when the device is handled.**
5. **The applied voltage and current should not exceed the maximum rating of the given transistor.**
6. **Change the components or any of their properties by turning off the power/stopping the simulation.**
7. **Have your instructor check all your connections after you are done setting up the circuit and make sure that you apply only enough voltage (within V_{DD}) to turn on the transistors and/or chip, otherwise, it may get damaged.**
8. **MOSFET transistors are very susceptible to breakdown due to electrostatic discharge. It is recommended that you always ground yourself before picking up the MOSFET chip. Do not touch any of the pins of the chip.**

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Experimental Procedures:

A. Study of Basic Operation of Inverter Circuits

1. Measure the actual value of the base/collector/drain resistors (Figs. 5-7).
2. Identify the terminals of the transistor.
3. Connect the circuit as shown in Figs. 5-7.
4. Connect the multimeter (voltmeter mode) to measure the input (V_{in}) and output voltages (V_o).
5. Turn on the DC power supply (V_{CC}/V_{DD}) with the voltage control nob at 0 V and then set the collector/drain supply voltage, V_{CC}/V_{DD} to 5 V.
6. Turn on the DC power supply (V_{in}) with the voltage control nob at 0 V and then set the base/gate supply voltage, V_{BB}/V_{GG} to 5 V.
7. Measure the input (V_{in}) and output voltages (V_o) using a multimeter for two different base/gate supply voltages of 0 V and 5 V. Use the SPDT (Single Pole Double Throw) switch to change the voltage levels.
8. Record the measured values in Tables 2-4.
9. Record the images of the hardware and simulation circuit diagrams as well as various wave shapes.
10. Turn off the DC power supply.

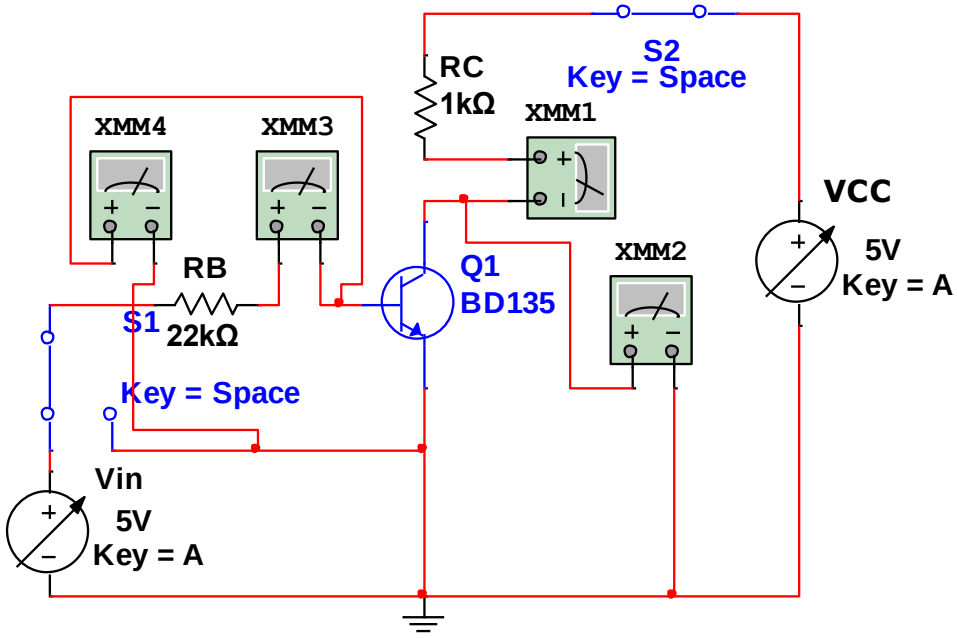

Figure 5: BJT-based RTL inverter circuit

Table 2 Measured Data of the BJT-Based RTL Inverter Circuit.

RTL BJT Inverter	V_{in}	V_{CE}	V_{BE}	I_B	I_C
$A = 0$					
$A = 1$					

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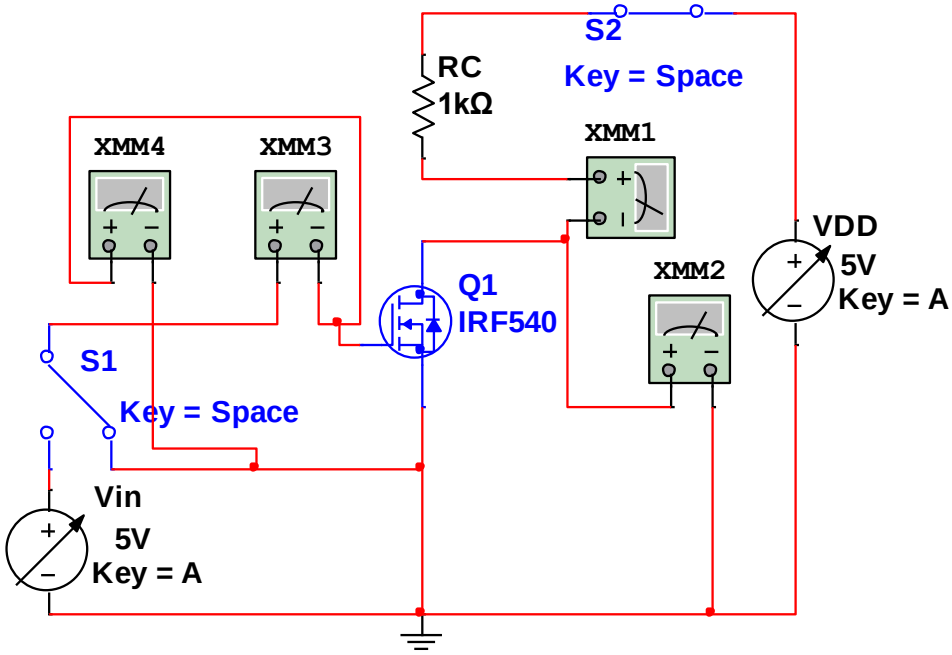

Figure 6: NMOS-based RTL inverter circuit

Table 3 Measured Data of the NMOS-based RTL Inverter Circuit.

RTL NMOS Inverter	V_{in}	V_{GS}	V_{DS}	I_D	I_G
$A = 0$					
$A = 1$					

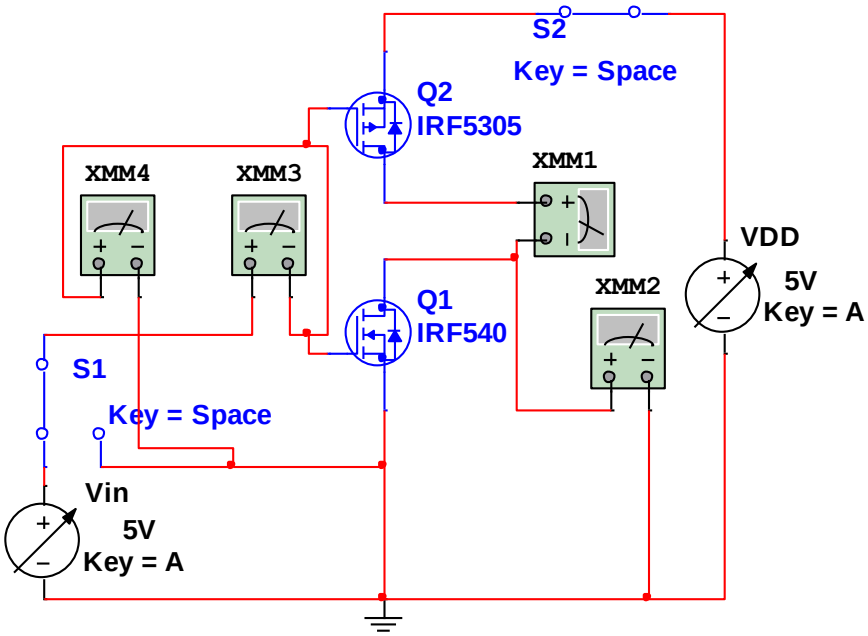

Figure 7: CMOS-based inverter circuit

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Table 4 Measured Data of the CMOS-based Inverter Circuit.

CMOS Inverter	MOSFET Type	V_{in}	V_{GS}	V_{DS}	I_D	I_G
$A = 0$	PMOS					
	NMOS					
$A = 1$	PMOS					
	NMOS					

B. Transfer Characteristics of Inverter Circuit

1. Connect the circuit as shown in Figs. 4-6.
2. Connect the multimeter (voltmeter mode) to measure the input (V_{in}) and output voltages (V_o).
3. Turn on the DC power supply (V_{CC}/V_{DD}) with the voltage control nob at 0 V and then set the collector/drain supply voltage, V_{CC}/V_{DD} to 5 V.
4. Turn on the DC power supply (V_{in}) with the voltage control nob at 0 V and then set the base/gate supply voltage, V_{BB}/V_{GG} to 0 V.
5. Vary the input voltage (V_{in}) from 0 V to 5 V in steps of 0.5 V. Measure the input (V_{in}) and output voltages (V_o) using a multimeter.
6. Record the measured values in Table 5 (use the same table format three times for three inverters).
7. Record the images of the hardware and simulation circuit diagrams as well as various wave shapes.
8. Turn off the DC power supply.

Table 5 Measured Data of the Transfer Characteristics of the Inverter Circuit.

V_{in} (V)	V_{out} (V) (CMOS)	V_{out} (V) (NMOS)	V_{out} (V) (BJT)
0			
0.5			
1			
1.5			
2			
2.5			
3			
3.5			
4			
4.5			
5			

Questions:

1. Show the difference between your simulated and measured values. Comment on the results and interpret the experimental and simulation data.
2. From the obtained data, draw the transfer characteristic curve of all inverter circuits in one figure.

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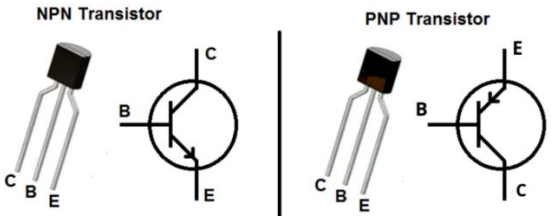
3. Explain the behavior of the inverter circuits in the different input combinations.
4. Compare the inverter circuits and discuss the advantages or disadvantages of one over the other.
5. Design an inverter circuit using diode logic.
6. Give your suggestions regarding this experiment.
7. Discuss the overall aspects of the experiment. Did your results match the expected ones? If not, explain.

References:

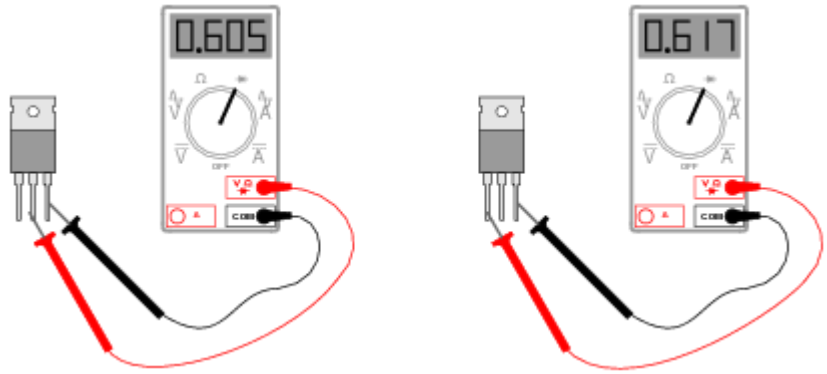
[1] Robert L. Boylestad, Louis Nashelsky, Electronic Devices and Circuit Theory, 9th Edition, 2007-2008
[2] Adel S. Sedra, Kenneth C. Smith, Microelectronic Circuits, Saunders College Publishing, 3rd ed., ISBN: 0-03-051648-X, 1991.
[3] American International University–Bangladesh (AIUB) Electronic Devices Lab Manual.
[4] David J. Comer, Donald T. Comer, Fundamentals of Electronic Circuit Design, John Wiley & Sons Canada, Ltd., ISBN: 0471410160, 2002.
[5] J. Keown, ORCAD PSpice and Circuit Analysis, Prentice Hall Press (2001)
[6] Resistor values: *https://www.eleccircuit.com/how-to-basic-use-resistor/*, accessed on 20 September 2023.

List the references that you have used to answer the "Discussion" section.

Appendix A: Identifying the terminals of an npn or a pnp transistor:



Following are the steps to identify npn and pnp transistors:
Step 1: Take the transistor you want to identify.
Step 2: Turn on a digital multimeter and set it to the DC voltage/resistance measurement mode.
Step 3: Make sure that you have connected the probes in their correct respective multimeter sockets, i.e., the black probe to the COM port and the red probe to the V/Ω/ port.
Step 4: Randomly start connecting the multimeter probes to the terminal of an unknown type of transistor and watch readings on the screen.
Step 5: Now, some random connections will give you a voltage/resistance reading on the multimeter screen.
Step 6: Once you get results i.e., any values (must be less than 1 for voltage reading) on the screen, start from the right side with the transistor's flat side upward direction, and write or mark the probes attached to the terminals of the transistor.
Step 7: If it is a black probe first and a red probe second then transfer the black probe to the third terminal (left-most terminal). If you get a similar result on the screen then write n, p, and n, that is the transistor is of npn type.
Step 8: If it is a red probe first and then a black probe second then transfer the red probe to the third terminal (left-most terminal). If you get a similar result on the screen then write p, n, and p, that is the transistor is of pnp type.
Step 9: The values you get on the multimeter screen after and before transferring the probe from the right-most side to the left-most side will differ slightly, the higher value-giving terminal is called the emitter and the lower value-giving terminal is called the collector, and the common terminal in the middle is called the base.



Based on the above procedural steps using a multimeter in diode mode, the left terminal of this transistor is a p-type emitter (producing larger value), the middle one is a p-type collector (less value), and the right one is called a base (common black terminal, so n-type). As such, this is a pnp-type transistor.

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Appendix B: The BD135 Data Sheet

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Order this document
by BD135/D

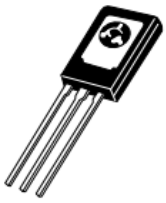
Plastic Medium Power Silicon NPN Transistor

BD135
BD137
BD139

. . . designed for use as audio amplifiers and drivers utilizing complementary or quasi complementary circuits.

- DC Current Gain — h_{FE} = 40 (Min) @ I_C = 0.15 Adc
- BD 135, 137, 139 are complementary with BD 136, 138, 140

1.5 AMPERE
POWER TRANSISTORS
NPN SILICON
45, 60, 80 VOLTS
10 WATTS



CASE 77–08
TO–225AA TYPE

MAXIMUM RATINGS

Rating	Symbol	Type	Value	Unit
Collector–Emitter Voltage	V_{CEO}	BD 135 BD 137 BD 139	45 60 80	Vdc
Collector–Base Voltage	V_{CBO}	BD 135 BD 137 BD 139	45 60 100	Vdc
Emitter–Base Voltage	V_{EBO}		5	Vdc
Collector Current	I_C		1.5	Adc
Base Current	I_B		0.5	Adc
Total Device Dissipation @ T_A = 25°C Derate above 25°C	P_D		1.25 10	Watts mW/°C
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D		12.5 100	Watt mW/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}		–55 to +150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	θ_{JC}	10	°C/W
Thermal Resistance, Junction to Ambient	θ_{JA}	100	°C/W

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BD135 BD137 BD139

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Type	Min	Max	Unit
Collector–Emitter Sustaining Voltage* (I_C = 0.03 Adc, I_B = 0)	BV_{CEO}*	BD 135 BD 137 BD 139	45 60 80	— — —	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0) (V_{CB} = 30 Vdc, I_E = 0, T_C = 125°C)	I_{CBO}		— —	0.1 10	µAdc
Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)	I_{EBO}		—	10	µAdc
DC Current Gain (I_C = 0.005 A, V_{CE} = 2 V) (I_C = 0.15 A, V_{CE} = 2 V) (I_C = 0.5 A V_{CE} = 2 V)	h_{FE}*		25 40 25	— 250 —	—
Collector–Emitter Saturation Voltage* (I_C = 0.5 Adc, I_B = 0.05 Adc)	$V_{CE(sat)}$*		—	0.5	Vdc
Base–Emitter On Voltage* (I_C = 0.5 Adc, V_{CE} = 2.0 Vdc)	$V_{BE(on)}$*		—	1	Vdc

* Pulse Test: Pulse Width ≦ 300 µs, Duty Cycle ≦ 2.0%.

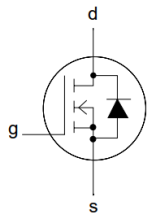
Appendix C: The IRF540 Data Sheet

N-channel TrenchMOS™ transistor — IRF540, IRF540S

FEATURES

- **'Trench'** technology
- Low on-state resistance
- Fast switching
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 100 V

I_D = 23 A

$R_{DS(ON)} \leq 77\ m\Omega$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope using '**trench**' technology.

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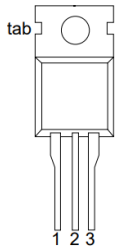
Applications:-
- d.c. to d.c. converters
- switched mode power supplies
- T.V. and computer monitor power supplies

The IRF540 is supplied in the SOT78 (TO220AB) conventional leaded package.
The IRF540S is supplied in the SOT404 (D^2PAK) surface mounting package.

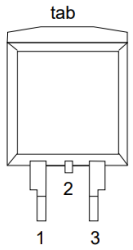
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404 (D^2PAK)



LIMITING VALUES

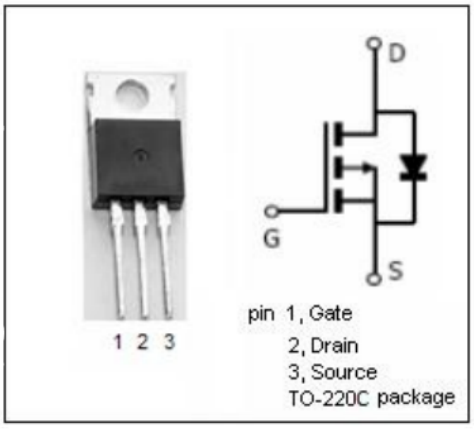
Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 ˚C to 175˚C	-	100	V
V_{DGR}	Drain-gate voltage	T_j = 25 ˚C to 175˚C; R_{GS} = 20 kΩ	-	100	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Continuous drain current	T_{mb} = 25 ˚C; V_{GS} = 10 V	-	23	A
		T_{mb} = 100 ˚C; V_{GS} = 10 V	-	16	A
I_{DM}	Pulsed drain current	T_{mb} = 25 ˚C	-	92	A
P_D	Total power dissipation	T_{mb} = 25 ˚C	-	100	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	˚C

Appendix D: The IRF5305 Data Sheet

isc P-Channel MOSFET Transistor — IRF5305,IIRF5305

- **FEATURES**
- Static drain-source on-resistance:
  $R_{DS(on)} \leqslant 0.06\Omega$
- Enhancement mode:
- 100% avalanche tested
- Minimum Lot-to-Lot variations for robust device performance and reliable operation



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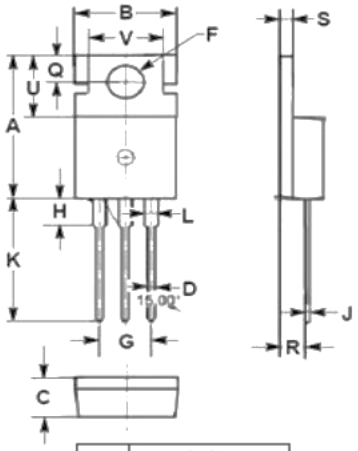
• **ABSOLUTE MAXIMUM RATINGS(T_a=25℃)**

SYMBOL	PARAMETER	VALUE	UNIT
V_{DSS}	Drain-Source Voltage	-55	V
V_{GS}	Gate-Source Voltage	±20	V
I_D	Drain Current-Continuous	-31	A
I_{DM}	Drain Current-Single Pulsed	-110	A
P_D	Total Dissipation @T_C=25℃	110	W
T_j	Max. Operating Junction Temperature	175	℃
T_{stg}	Storage Temperature	-55~175	℃

• **THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	MAX	UNIT
Rth(j-c)	Channel-to-case thermal resistance	1.4	℃/W
Rth(j-a)	Channel-to-ambient thermal resistance	62	℃/W



DIM	mm MIN	MAX
A	15.50	15.90
B	9.90	10.20
C	4.20	4.50
D	0.70	0.90
F	3.40	3.70
G	4.98	5.18
H	2.68	2.90
J	0.44	0.60
K	13.00	13.40
L	1.10	1.45
Q	2.70	2.90
R	2.30	2.70
S	1.29	1.35
U	6.45	6.65
V	8.66	8.86

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