American International University- Bangladesh
Faculty of Engineering (FE)
Department of Electrical and Electronic Engineering (EEE)
EEE 2104: Electronic Devices Lab

Title of the Experiment: Study of JFET and MOSFET Characterization.

Objectives:
The objectives of this experiment are to
1. Understand the basic operation of JFETs and MOSFETs and determine the threshold voltages.
2. Measure the current and voltage to obtain the *I-V* characteristics.
3. Find the different operating regions for both JFETs and MOSFETs.

Theory:
The most common transistor types are the Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and the Bipolar Junction Transistors (BJT). BJT-based circuits dominated the electronics market in the 1960s and 1970s. Nowadays, most electronic circuits, particularly integrated circuits (ICs), are made of MOSFETs. The BJT-based circuits are mainly used for specific applications like analog circuits (e.g., amplifiers), high-speed circuits, or power electronics.
There are two main differences between BJTs and FETs. The first is that FETs are voltage-controlled devices while BJTs are current-controlled devices. The second difference is that the input impedance of the FETs is very high while that of BJT is relatively low. As for the FET transistors, there are two main types: the Junction Field Effect Transistor (JFET) and the Metal Oxide Semiconductor Field Effect Transistor (MOSFET). The power dissipation of a JFET is high in comparison to MOSFETs. Therefore, JFETs are less important if it comes to the realization of ICs, where transistors are densely packed. The power dissipation of a JFET-based circuit would be very high. The MOSFET became the most popular field effect device in the 1980s.
The combination of n-type and p-type MOSFETs allows for the realization of the Complementary Metal Oxide Semiconductor (CMOS) devices. CMOS-based technology is the most important technology in the electronics industry nowadays. All microprocessors and memory products are based on CMOS technology. The very low power dissipation of CMOS circuits allows for the integration of millions of transistors in a single chip.

JFET Structure and Operation
A transistor is a kind of current-controlled device, and its generating current includes electron flow and hole flow. The transistor is therefore referred to as a bipolar junction transistor.
FET is a unipolar device, in which the current of n-channel FET is formed by electron flow and the current of p-channel is formed by hole flow. FET is a kind of voltage-controlled device. FET can also perform the functions that general transistors (BJT) do, with the only exception that the bias conditions and characteristics are different. Their applications shall thus be chosen in accordance with related advantages and drawbacks.
The characteristics of FET are listed as follows:
1. FET has a very high input impedance, typically around 100 MΩ.
2. When FET is used as a switch, there is no offset voltage.
3. FET is relatively independent of radiation, whereas BJT is very sensitive to radiation (β varies).
4. The intrinsic noise of FET is lower than that of BJT, which makes FET suitable for the input stage of low-level amplifiers.
5. During operation the thermal stability of FET is higher than that of BJT.

However, FET also has some drawbacks when compared with BJT, its gain and bandwidth product is smaller, and it is easier to be damaged by static electricity.
The internal structure of a JFET is shown in Fig. 1. The n-channel JFET is formed by diffusing one pair of p-type regions into a slab of n-type material as shown in Fig. 1 (a). On the contrary, the p-channel JFET is formed by diffusing one pair of n-type regions into a slab of p-type material as shown in Fig. 1 (b). The p-channel JFET is constructed in the same manner as the n-channel device of but with a reversal of the p- and n-type materials.

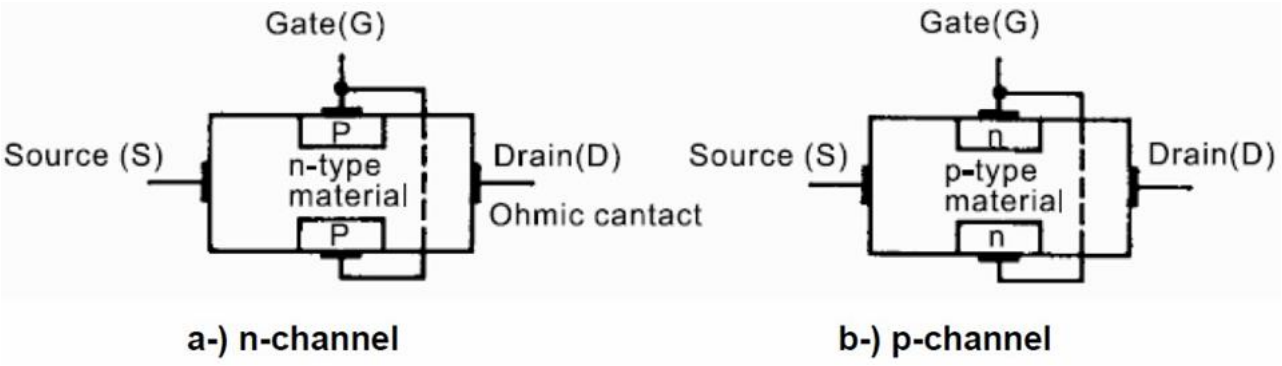


Figure 1: Internal structure of n-channel and p-channel JFETs.

Since the p-channel and n-channel JFETs are constructed by reversing the p- and n-type materials their current directions are also reversed due to reversal of the actual polarities for the voltages V_{GS} and V_{DS}. For the p-channel device, the channel will be constricted by increasing positive voltages from gate to source, and the drain-to-source voltage V_{DS} will result in a negative on the characteristics curve shown in Fig. 3. The curve shows a drain saturation current (I_{DSS}) of 6 mA and a pinch-off voltage (V_P) of +6 V.

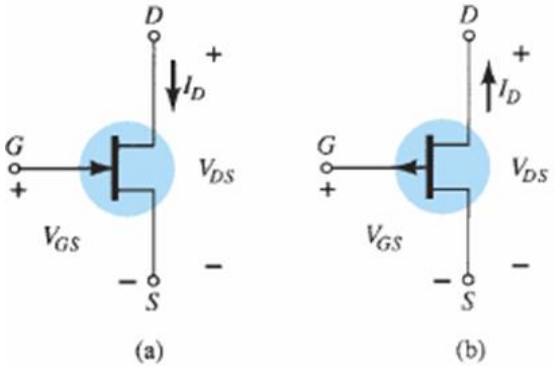


Figure 2: JFET symbols: (a) n-channel (b) p-channel

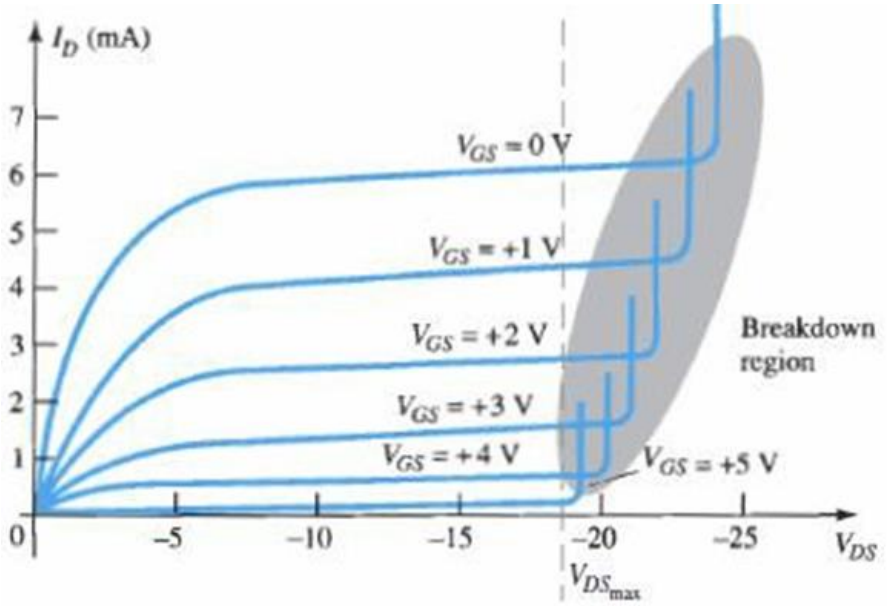


Figure 3: p-channel JFET drain-source characteristics with I_{DSS} = 6 mA and V_P = +6 V.

Figure 4 shows the transfer characteristics of a JFET. The curve shows a drain saturation current (I_{DSS}) of 4 mA and a pinch-off voltage (V_P) of +3 V.

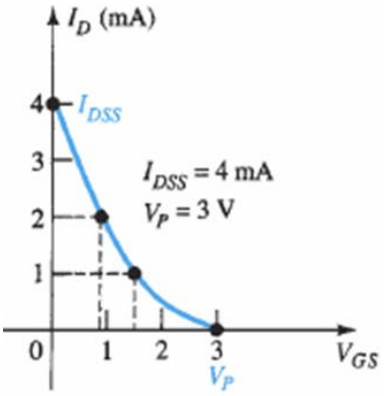


Figure 4: Transfer characteristics of p-channel JFET with I_{DSS} = 4 mA and V_P = +3 V.

MOSFET Structure and Operation

The MOSFETs are the most widely used FETs. Strictly speaking, MOSFET devices belong to the group of Insulated Gate Field Effect Transistors (IGFETs). As the name implies, the gate is insulated from the channel by an insulator. In most cases, the insulator is formed by a silicon dioxide (SiO_2) layer, which leads to the term MOSFET. MOSET, like all other IGFETs, has three terminals, which are called Gate (G), Source (S), and Drain (D). In certain cases, the transistors have a fourth terminal, which is called the bulk or body terminal (B). In PMOS, the body terminal is held at the most positive voltage terminal in the circuit, and in NMOS, it is held at the most negative voltage terminal in the circuit.

There are four types of MOSFETs, such as enhancement mode n-type MOSFET, enhancement mode p-type MOSFET, depletion mode n-type MOSFET, and depletion mode p-type MOSFET. The type depends on whether the channel between the drain and source is an induced channel or is a physically implanted one and whether the current flowing in the channel is an electron current or a hole current. If the channel between the drain and the source is an induced channel, the transistor is called an enhancement-type transistor. If the channel between the drain and source is physically implanted, then the transistor is called a depletion-type transistor. If the current flowing in the channel is an electron current, the transistor is called an n-type MOSFET or NMOS transistor. If the current flow is a hole current, then the transistor is called a p-type MOSFET or PMOS transistor. Throughout this laboratory manual, we will concentrate on analyzing the enhancement-type MOSFET. The cross-section of an enhancement NMOS transistor is shown in Fig. 5.

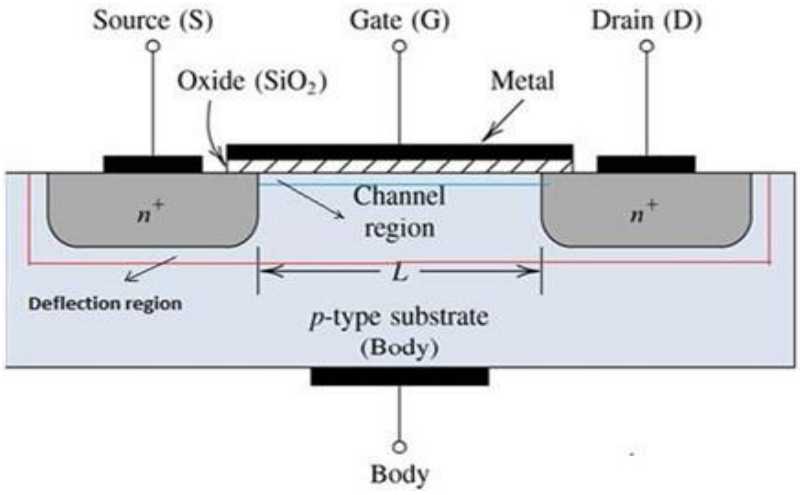


Figure 5: Schematic cross-section of an enhancement-type NMOS transistor.

If we put the drain and source on ground potential and apply a positive voltage to the gate, the free holes (positive charges) are repelled from the region of the substrate under the gate (channel region) due to the positive voltage applied to the gate. The holes are pushed away downwards into the substrate leaving behind a depletion region.

At the same time, the positive gate voltage attracts electrons into the channel region. When the concentration of electrons near the surface of the substrate under the gate is equal to or greater than the concentration of holes, an n-channel is created, connecting the source and the drain regions. This is called enhancement and inversion mode as it enhances the channel by inverting its type at the surface of the device. The induced n-region thus forms the channel for current flow from drain to source. The channel is only a few nanometers wide. Nevertheless, the entire current transport occurs in this thin channel between the drain and the source. Now, if a voltage is applied between the drain and source electrodes, an electron current can flow through the induced channel. Increasing the voltage applied to the gate above a certain threshold voltage enhances the channel.

In the case of an enhancement-type NMOS transistor, the threshold voltage is positive, whereas an enhancement-type PMOS transistor has a negative threshold voltage. So, for the current to flow from drain to source, the condition that should be satisfied is $V_{GS} > V_{th}$, where V_{GS} is the gate-to-source voltage and V_{th} is the threshold voltage defined as the minimum voltage required to form a channel between the drain and source regions at the surface of the device so that carriers can flow through the channel. By changing the applied gate-to-source voltage, we can modulate the conductance of the channel.

Depletion-type MOSFETs use a different approach. The channel is already conductive for a gate-to-source voltage of 0 V. Such kind of MOS transistors are realized by the physical implantation of an n-type region between the drain and the source.

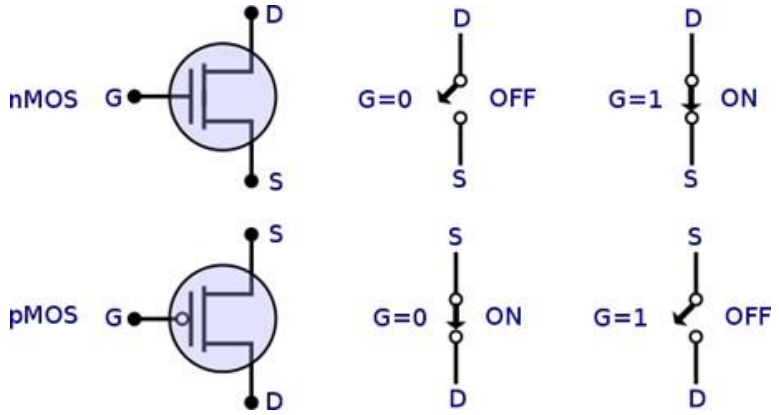


Figure 6: Symbols for enhancement-type NMOS and PMOS transistors.

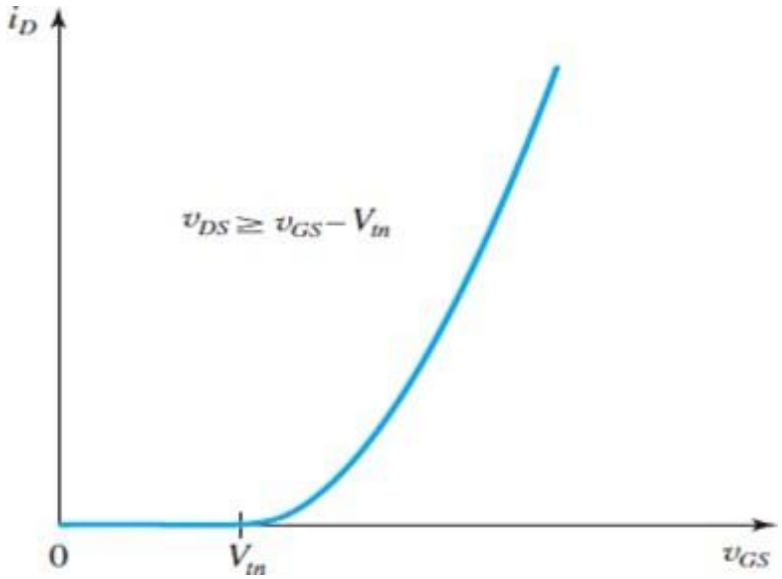


Figure 7: Drain current, I_D vs. gate-to-source voltage, V_{GS} graph of an enhancement type NMOS transistor for a drain-to-source voltage above the gate overdrive voltage ($V_{GS} - V_{th}$) showing threshold voltage V_{tn}.

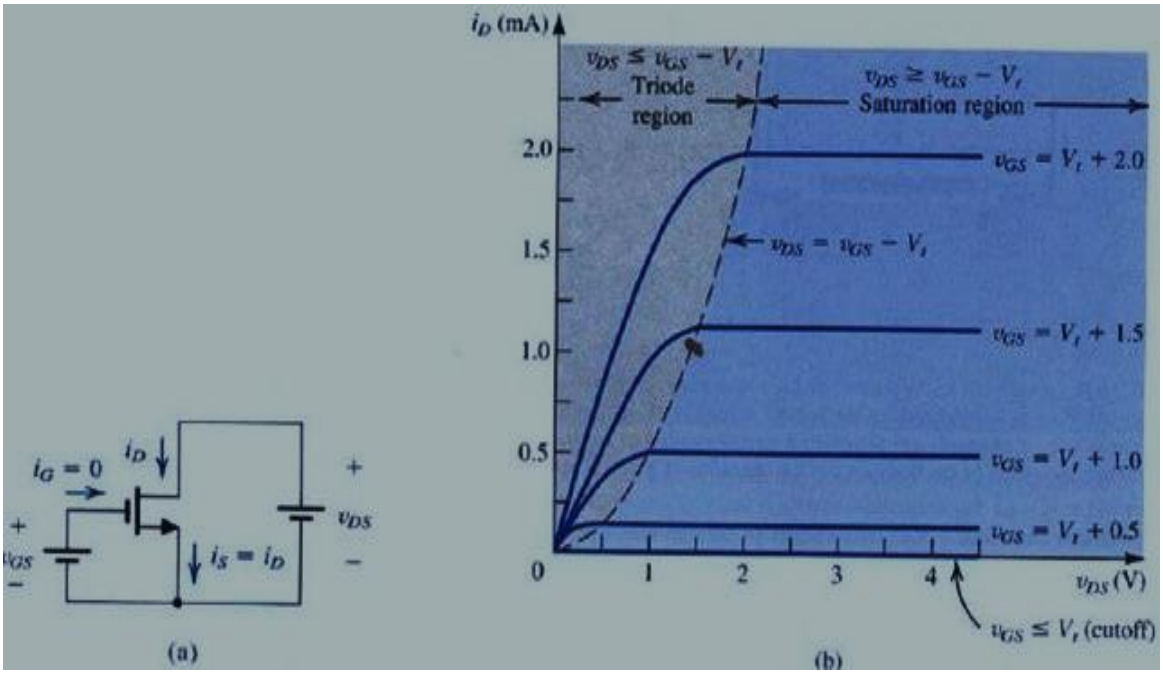


Figure 8: (a) an n-channel enhancement type MOSFET with V_{GS} and V_{DS} applied (b) the $I_{DS} - V_{DS}$ characteristics curve of a device with $k_n'(W/L) = 1$ mA/V^2 showing the three operating regions.

Pre-Lab Homework:

Students will be provided with the upcoming lab manuals, and they will be asked to prepare the theoretical (operations/working principle) information on the topic from the textbook.

Besides, they must implement the circuit (as given in Figures 9-10) using a **MultiSIM simulator**. Observe the gate and drain voltages and currents through simulations (I_D, I_G, V_{DS}, V_{GS}) and take snapshots using the snipping tool. Measure the values of different key parameters and fill up the tables (Tables 1-4) based on the simulation results. For simulation, use a J176 as the p-channel JFET, a 2N7000/IRF540N/BUK444/IRF740/IRF840 as the n-channel MOS transistor, and 9540 as the p-channel MOS transistor. Perform the following tasks as well:

1. Draw and explain the transfer characteristics and output characteristics of an n-channel and a p-channel JFET using the simulation data of Tables 1-4. Define the term pinch-off voltage.
2. Explain the differences between an enhancement and depletion type MOSFET.
3. Explain the differences between an NMOS and a PMOS transistor.
4. Draw and explain the transfer characteristics and output characteristics of an n-channel and a p-channel enhancement type MOSFETs. Define the term threshold voltage.

Apparatus:

SL#	Apparatus	Quantity
1	**J176** (p-channel JFET); 2N7000/**IRF540N** (n-channel enhancement type MOSFET); **9540** (p-channel enhancement type MOSFET).	1 each
2	Resistance (R = 1 kΩ)	1
3	Project Board	1
4	DC Power Supply	1
5	DC milliammeter (0-50 mA)	1
6	DC microammeter (0-500 μA)	1
7	Multimeter	1
8	Connecting Leads	10

Precaution!

The following is a list of some of the special safety precautions that should be taken into consideration when working with transistors:

1. **Never remove or insert a transistor into a circuit with voltage applied.**
2. **Ensure a replacement transistor into a circuit is in the correct direction.**
3. **Transistors are sensitive to being damaged by electrical overloads, heat, humidity, and radiation. Damage of this nature often occurs by applying the incorrect polarity voltage to the collector circuit or excessive voltage to the input circuit.**
4. **One of the most frequent causes of damage to a transistor is the electrostatic discharge from the human body when the device is handled.**
5. **The applied voltage and current should not exceed the maximum rating of the given transistor.**
6. **Change the components or any of their properties by turning off the power/stopping the simulation.**
7. **Have your instructor check all your connections after you are done setting up the circuit and make sure that you apply only enough voltage (within V_{DD}) to turn on the transistors and/or chip, otherwise, it may get damaged.**
8. **MOSFET transistors are very susceptible to breakdown due to electrostatic discharge. It is recommended that you always ground yourself before picking up the MOSFET chip. Do not touch any of the pins of the chip.**

Experimental Procedures:

A. Transfer Characteristics of p-channel JFET (J176)

1. Measure the actual value of the drain resistor (as the load of Fig. 9).
2. Identify the terminals of the transistor.
3. Connect the circuit and connect the milliammeter as shown in Fig. 9.
4. Connect the multimeter (voltmeter mode) to measure the drain current (I_{DS}) and gate voltage (V_{GS}).
5. Turn on both the DC power supply with the voltage control nob at 0 V and then set the gate supply voltage, V_{GS} to 0 V.
6. Measure the gate-to-source voltage, $V_{GS,}$ and drain-to-source current, I_{DS} for a fixed drain-to-source voltage (V_{DS} = 1 V) by varying the gate-to-source voltage, V_{GS} from 0 V to 12 V in the step of 1 V.
7. Plot the I_{DS} vs V_{GS} curve using the data of Table 1 and measure the pinch-off voltage, V_P.
8. Record the measured values in Table 1.
9. Record the images of the hardware and simulation circuit diagrams as well as various wave shapes.
10. Turn off the DC power supply.

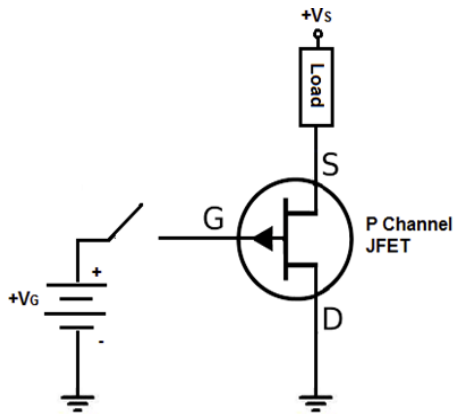


Figure 9: Circuit for plotting the I_{DS} vs V_{GS} that is, transfer characteristics of p-channel JFET (J176)

Table 1 Measured data of the voltage and current for the transfer characteristic curve of a JFET. Dain-to-Source voltage, V_{DS} = 1 V.

Gate Voltage, V_{GS} (V)	Drain Current, I_{DS} (mA)

B. Output Characteristics of p-channel JFET (J176)

1. Measure the actual value of the drain resistor (as the load of Fig. 9).
2. Identify the terminals of the transistor.
3. Connect the circuit and connect the milliammeter as shown in Fig. 9.
4. Connect the multimeter (voltmeter mode) to measure the drain current (I_{DS}) and drain voltage (V_{GS}).
5. Turn on both the DC power supply with the voltage control nob at 0 V and then set the gate supply voltage, V_{GS} to 5 V.
6. Measure the drain-to-source voltage, $V_{DS,}$ and drain-to-source current, I_{DS} for a fixed gate-to-source voltage (V_{GS} = 5 V) by varying the drain-to-source voltage, V_{DS} from 0 V to 15 V in the step of 1 V.
7. Plot the I_{DS} vs V_{DS} curve using the data of Table 2 and indicate different operating regions.
8. Record the measured values in Table 2.
9. Record the images of the hardware and simulation circuit diagrams as well as various wave shapes.
10. Turn off the DC power supply.

Table 2 Measured data of the voltage and current for the transfer characteristic curve of a JFET. Gate-to-Source voltage, V_{GS} = 5 V.

Drain Voltage, V_{DS} (V)	Drain Current, I_{DS} (mA)

Drain Voltage, V_{DS} (V)	Drain Current, I_{DS} (mA)

C. Transfer Characteristics of n-channel MOSFET (IRF540)

1. Measure the actual value of the drain resistor (as the load of Fig. 10).
2. Identify the terminals of the MOS transistor.
3. Connect the circuit and connect the milliammeter as shown in Fig. 10.
4. Connect the multimeter (voltmeter mode) to measure the drain current (I_{DS}) and gate voltage (V_{GS}).
5. Turn on both the DC power supply with the voltage control nob at 0 V and then set the gate supply voltage, V_{GS} to 0 V.
6. Measure the gate-to-source voltage, $V_{GS,}$ and drain-to-source current, I_{DS} for a fixed drain-to-source voltage (V_{DS} = 1 V) by varying the gate-to-source voltage, V_{GS} from 0 V to 10 V in the step of 1 V.
7. Plot the I_{DS} vs V_{GS} curve using the data of Table 3 and measure the pinch-off voltage, V_P.
8. Record the measured values in Table 3.
9. Record the images of the hardware and simulation circuit diagrams as well as various wave shapes.
10. Turn off the DC power supply.

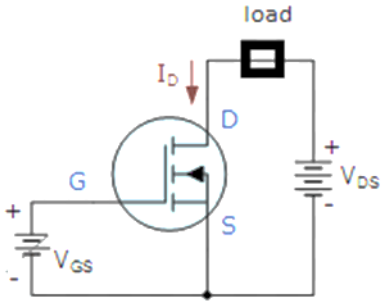


Figure 10: Circuit for plotting the I_{DS} vs V_{GS} that is, transfer characteristics of n-channel MOSFET (IRF540)

Table 3 Measured data of the voltage and current for the transfer characteristic curve of a MOSFET. Dain-to-Source voltage, V_{DS} = 1 V.

Gate Voltage, V_{GS} (V)	Drain Current, I_{DS} (mA)

Gate Voltage, V_{GS} (V)	Drain Current, I_{DS} (mA)

D. Output Characteristics of n-channel MOSFET (IRF540)

1. Measure the actual value of the drain resistor (as the load of Fig. 10).
2. Identify the terminals of the MOS transistor.
3. Connect the circuit and connect the milliammeter as shown in Fig. 10.
4. Connect the multimeter (voltmeter mode) to measure the drain current (I_{DS}) and drain voltage (V_{GS}).
5. Turn on both the DC power supply with the voltage control nob at 0 V and then set the gate supply voltage, V_{GS} to 5 V.
6. Measure the drain-to-source voltage, $V_{DS,}$ and drain-to-source current, I_{DS} for a fixed gate-to-source voltage (V_{GS} = 5 V) by varying the drain-to-source voltage, V_{DS} from 0 V to 15 V in the step of 1 V.
7. Plot the I_{DS} vs V_{DS} curve using the data of Table 4 and indicate different operating regions.
8. Record the measured values in Table 4.
9. Record the images of the hardware and simulation circuit diagrams as well as various wave shapes.
10. Turn off the DC power supply.

Table 4 Measured data of the voltage and current for the transfer characteristic curve of a JFET. Gate-to-Source voltage, V_{GS} = 5 V.

Drain Voltage, V_{DS} (V)	Drain Current, I_{DS} (mA)

Drain Voltage, V_{DS} (V)	Drain Current, I_{DS} (mA)

Questions:

1. Show the difference between your simulated and measured values. Comment on the results and interpret the experimental and simulation data.
2. From the obtained data, draw the transfer and output characteristic curves of JFET and MOSFET.
3. Explain the behavior of the JFET and MOSFET circuits in the different regions of operation.
4. Determine the JFET and MOSFET parameters from the data sheet. Compare it with the measured data.
5. Compare JFET and MOSFET.
6. Give your suggestions regarding this experiment.
7. Discuss the overall aspects of the experiment. Did your results match the expected ones? If not, explain.

References:

[1] Robert L. Boylestad, Louis Nashelsky, Electronic Devices and Circuit Theory, 9th Edition, 2007-2008
[2] Adel S. Sedra, Kenneth C. Smith, Microelectronic Circuits, Saunders College Publishing, 3rd ed., ISBN: 0-03-051648-X, 1991.
[3] American International University–Bangladesh (AIUB) Electronic Devices Lab Manual.
[4] David J. Comer, Donald T. Comer, Fundamentals of Electronic Circuit Design, John Wiley & Sons Canada, Ltd., ISBN: 0471410160, 2002.
[5] J. Keown, ORCAD PSpice and Circuit Analysis, Prentice Hall Press (2001)
[6] Resistor values: *https://www.eleccircuit.com/how-to-basic-use-resistor/*, accessed on 20 September 2023.

List the references that you have used to answer the "Discussion" section.

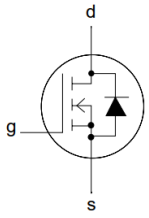
Appendix A: The IRF540 Data Sheet

N-channel TrenchMOS™ transistor — IRF540, IRF540S

FEATURES

- **'Trench'** technology
- Low on-state resistance
- Fast switching
- Low thermal resistance

SYMBOL



QUICK REFERENCE DATA

V_{DSS} = 100 V

I_D = 23 A

$R_{DS(ON)} \leq 77\ m\Omega$

GENERAL DESCRIPTION

N-channel enhancement mode field-effect power transistor in a plastic envelope using '**trench**' technology.

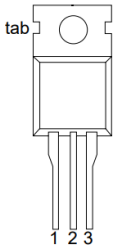
Applications:-
- d.c. to d.c. converters
- switched mode power supplies
- T.V. and computer monitor power supplies

The IRF540 is supplied in the SOT78 (TO220AB) conventional leaded package.
The IRF540S is supplied in the SOT404 (D^2PAK) surface mounting package.

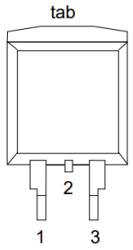
PINNING

PIN	DESCRIPTION
1	gate
2	drain[1]
3	source
tab	drain

SOT78 (TO220AB)



SOT404 (D^2PAK)

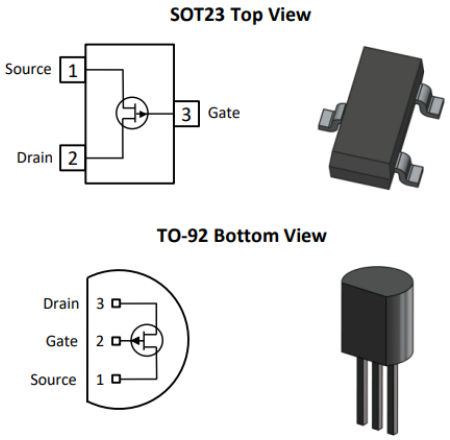


LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DSS}	Drain-source voltage	T_j = 25 ˚C to 175˚C	-	100	V
V_{DGR}	Drain-gate voltage	T_j = 25 ˚C to 175˚C; R_{GS} = 20 kΩ	-	100	V
V_{GS}	Gate-source voltage		-	± 20	V
I_D	Continuous drain current	T_{mb} = 25 ˚C; V_{GS} = 10 V	-	23	A
		T_{mb} = 100 ˚C; V_{GS} = 10 V	-	16	A
I_{DM}	Pulsed drain current	T_{mb} = 25 ˚C	-	92	A
P_D	Total power dissipation	T_{mb} = 25 ˚C	-	100	W
T_j, T_{stg}	Operating junction and storage temperature		- 55	175	˚C

Appendix B: The J176 Data Sheet



P-channel silicon field-effect transistors

J174; J175; J176; J177

DESCRIPTION

Silicon symmetrical p-channel junction FETs in a plastic TO-92 envelope and intended for application with analog switches, choppers, commutators etc.

A special feature is the interchangeability of the drain and source connections.

PINNING

1 = source
2 = gate
3 = drain

Note: Drain and source are interchangeable.

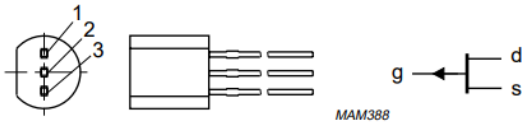


Fig.1 Simplified outline and symbol, TO-92.

QUICK REFERENCE DATA

Drain-source voltage	$\pm V_{DS}$	max.		30			V
Gate-source voltage	V_{GSO}	max.		30			V
Gate current	$-I_G$	max.		50			mA
Total power dissipation up to T_{amb} = 50 °C	P_{tot}	max.		400			mW
			J174	**J175**	**J176**	**J177**	
Drain current $-V_{DS}$ = 15 V; V_{GS} = 0	$-I_{DSS}$	min.	20	7	2	1.5	mA
		max.	135	70	35	20	mA
Drain-source ON-resistance $-V_{DS}$ = 0.1 V; V_{GS} = 0	$R_{DS\,on}$	max.	85	125	250	300	Ω

