for (i=0; i<N; i++){
    c[i]=a[i]*b[i];
    ...;
}

HLL program

op   op
op   op
op op op

IR(DFG/CFG)

| A-core | C-core | C-core | C-core: control core |

Interconnection

| Mem | Mem | Mem |

A-core: arithmetic core

MARC

| PE | PE | PE | PE | PE: processing element
| PE | PE | PE | PE |
| PE | PE | PE | PE |

SCGRA

always@(*) begin
    c=a*b;
    ...
end

RTL description

| IF | C | IF | C | IF | C: connection box
| C | C | C | C |
| IF | C | IF | C | IF |

IF: Intermediate fabric

VFPGA

LUT   DSP
    PLL
Ram block   IP

FPGA

High   Medium   Low

Abstraction level

fast   medium   slow

Processing speed

① RTL design flow ② Conventional HLS ③ Virtual FPGA(VFPGA) based HLS

④ SCGRA based HLS ⑤ Many-core approach to reconfigurable computing(MARC)