Alpha Data ADM-PCIE-7v3 Memory Bandwidth Test

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1 Memory Bandwidth Test Report

In order to get an overview of the memory bandwidth of the ADM-PCIE-7v3 board, we have both sequential and random memory access bandwidth tested. Half of the memory access is read and the other half is write. Also note that there are two different pieces of memory on the system. The host DDR memory and the FPGA DDR memory. Here we just tested the bandwidth of the FPGA DDR memory bandwidth accessed from FPGA. As it is the probably the bottleneck for memory intensive applications running on FPGA.

Figure Figure 1 and Figure Figure 1 show the measured memory bandwidth with sequential memory access and random access respectively. Basically, it can be found that sequential memory access bandwidth drops dramatically when the data size gets smaller while the random memory access is relatively less senseitive to the data size. Meanwhile, the sequential memory access is a dozens of times more efficient than the random memory access.

Another thing is that the Alpha-Data ADM-PCIE-7v3 board has two SODIMM DDR. Each of them can goes up to 1333MT/s i.e. 10.6GB/s according to the spec [1]. However, we can only utilize one SODIMM on the FPGA due to the DSA provided in SDAccel and the best bandwidth that we can achieve in sequential access manner is around 8.6GB/s.

References

[1] Alpha-Data. ADM-PCIE-7v3. `http://www.alpha-data.com/dcp/products.php?product=adm-pcie-7v3`, 2017. [Online; accessed 17-July-2017].

Figure 1: Memory Bandwidth with Sequential Memory Access

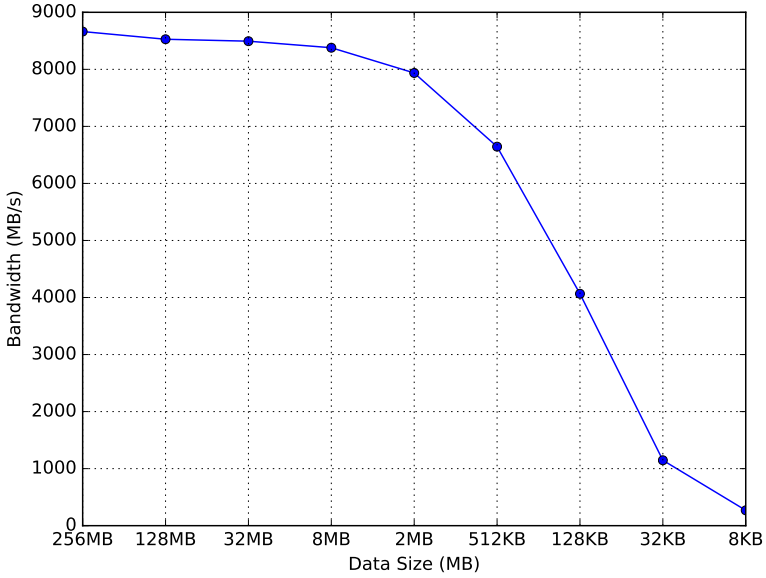

Figure 2: Memory Bandwidth with Random Memory Access