FPGA Accelerator

CPU

Main Memory

System Interconnection

AddrOBuf
AddrIBuf
AccCtrl
OBuf
IBuf

Low Freq

PE PE ••• PE
PE PE ••• PE
PE PE ••• PE
PE PE ••• PE

SCGRA

High Freq

Start → AddrCtrl → Instruction Mem
Store

Load
N-In
E-In
S-In
W-In

Data Mem

ALU

Bypass

N-Out
E-Out
S-Out
W-Out

Write Port0
Write Port1

Primitive BRAM

Read Port0
Read Port1

Primitive BRAM

Read Port2
Read Port3

Primitive BRAM

Read Port4
Read Port5

Dina
Wea
Clka

Dinb
Web
Clkb

Primitive BRAM

Doa
Addra

Dob
Addrb

Src0
Src1
Src2

OP0
OP1
OP2

OPN

Sel

Dst

Highly pipelined, good scalability, simple and easy to extend