CHENG LIU

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School of Computing, National University of Singapore, Singapore

EDUCATION

The University of Hong Kong	*Sep 2011 - Apr 2016*
Ph.D in Computer Engineering	
Harbin Institute of Technology	*Sep 2007 - Jul 2009*
M.E. in Electronic Engineering	
Harbin Institute of Technology	*Sep 2003 - Jul 2007*
B.E. in Electronic Engineering	

RESEARCH INTEREST

FPGA Acceleration, FPGA Overlay, Hardware/Software Co-design, Network-on-Chip

EXPERIENCE

School of Computing, National University of Singapore   Dec 2016 - present
Project: Graph acceleration on heterogeneous CPU-FPGAs

· In this project, we aim to develop a software programmable high-performance graph accelerator library targeting large scale-free graph processing on both loosely coupled and closely coupled CPU-FPGA computing system. Currently, we have implemented an FPGA resource aware BFS accelerator on Alpha-Data FPGA acceleration cards. And we are also exploring the general pipelined co-design accelerator framework for graph processing on Intel Harp System (Xeon-FPGA).

SenseTime Group Limited   Apr 2016 - Oct. 2016
Project: Convolutional neural network (CNN) acceleration on Zynq

· A highly flexible hardware accelerator for general convolution layer of CNN was developed. It allows arbitrary tiling for various CNN configurations such as kernel size and stride size so that it can be rapidly configured for different application scenarios. The design was implemented on Xilinx ZC706 SoC and used for face recognition demo.

The University of Hong Kong   Sep 2011 - Dec 2015
Research Project: Promoting FPGA design productivity using soft CGRA overlay

· In this project, a rapid FPGA loop accelerator design framework was developed. By using a regular soft coarse-grained reconfigurable array (SCGRA) overlay as an intermediate layer, it is able to compile a high-level (C/C++) nested loop to an FPGA loop accelerator bitstream in seconds with pre-built empty SCGRA bitstream. In addition, the overlay allows intensive customization specifically to an application or a domain of applications for the sake of performance with a few manual optimization routines. To facilitate applying this framework on a CPU-FPGA system, we also provide a template for generating the communication interface between the CPU and the resulting FPGA accelerator. The framework is demonstrated on Zedboard. The resulting accelerators exhibit significant performance speedup on regular compute inetensive applications over the software counterparts on the ARM processor.

· We also ported the SCGRA accelerator to a simple RISCV processor and analyzed the potential benefits of adding configurable accelerator to the general processor.

Institute of Computing Technology, Chinese Academy of Sciences   Sep 2009 - Mar 2011
Research Project: Highly reliable network-on-chip design

· In this project, we aimed to enhance NoC reliability by innovating on NoC micro-architecture. With the observation that Vertical Through Silicon Vias (TSV) in a classical 3D NoC is under-utilized, a TSV sharing method was developed for homogeneous 3D NoC with negligible 2D area overhead. This can either be used to improve the reliability of 3D NoC or shrink the TSV consumption. For regular 2D NoC, a flexible data path salvaging scheme was proposed to build highly reliable NoC.

Harbin Institute of Technology   Oct 2006 - Jul 2009
Research Project: High performance network-on-chip design

· In this project, we aimed to improve NoC performance as well as power efficiency. A number of design optimization methods including specific virtual channel allocation, dynamic buffer regulator and adaptive power gating were proposed and implemented for this purpose.

PUBLICATIONS

Book Chapter

· Hayden Kwok-Hay So and **Cheng Liu**, "FPGA overlays", in press FPGAs for Software Engineers, Dirk Koch, Frank Hannig and Daniel Ziener, Ed., 2016.

Journal

· Ying Wang, Yinhe Han, Lei Zhang, Binzhang Fu, **Cheng Liu**, Huawei Li, and Xiaowei Li. "Economizing TSV Resources in 3-D Network-on-Chip Design." Very Large Scale Integration (VLSI) Systems, IEEE Transactions on 23, no. 3 (2015): 493-506. (cited 12)
· Yinhe Han, **Cheng Liu**, Hang Lu, Wenbo Li, Lei Zhang, and Xiaowei Li. "RevivePath: Resilient network-on-chip design through data path salvaging of router." Journal of Computer Science and Technology 28, no. 6 (2013): 1045-1053. (cited 3)
· Qingli Zhang, **Cheng Liu**, Liyi Xiao, Fangfa Fu. Low Latency Router Design Supporting both Deterministic Routing and Adaptive Routing. Journal of Computer-Aided Design & Computer Graphics, 21(12), 2009 (in Chinese)

Conference & Workshop

· Ho-Cheung Ng, **Cheng Liu** and Hayden Kwok-Hay So. "A Soft Processor Overlay with Tightly-coupled FPGA Accelerator," Overlay Architectures for FPGAs (OLAF), Second International Workshop on, pp. 1-6, Feb, 2016.
· **Cheng Liu**, Ho-Cheung Ng, and Hayden Kwok-Hay So. "Automatic Nested Loop Acceleration on FPGAs Using Soft CGRA Overlay", FPGAs for Software Programmers (FSP), 2nd International Workshop on, Sep. 2015. (cited 12)
· **Cheng Liu**, Ho-Cheung Ng, and Hayden Kwok-Hay So. "QuickDough: A Rapid FPGA Loop Accelerator Design Framework Using Soft CGRA Overlay", Field Programmable Technology, International Conference on (FPT), Dec. 2015 (cited 11)
· **Cheng Liu**, Lei Zhang, Yinhe Han, and Xiaowei Li. "Vertical interconnects squeezing in symmetric 3D mesh Network-on-Chip." In Proceedings of the 16th Asia and South Pacific Design Automation Conference, pp. 357-362. IEEE Press, 2011. (Cited 55)
· **Cheng Liu**, Lei Zhang, Yinhe Han, and Xiaowei Li. "A resilient on-chip router design through data path salvaging." In Proceedings of the 16th Asia and South Pacific Design Automation Conference, pp. 437-442. IEEE Press, 2011. (Cited 23)

Poster

- **Cheng Liu**, and Hayden Kwok-Hay So. "Automatic Soft CGRA Overlay Customization for High-Productivity Nested Loop Acceleration on FPGAs." In Field-Programmable Custom Computing Machines (FCCM), 2015 IEEE 23rd Annual International Symposium on, pp. 101-101. IEEE, 2015.
- **Cheng Liu**, Colin Lin Yu, and Hayden Kwok-Hay So. "A soft coarse-grained reconfigurable array based high-level synthesis methodology: Promoting design productivity and exploring extreme FPGA frequency." In Field-Programmable Custom Computing Machines (FCCM), 2013 IEEE 21st Annual International Symposium on, pp. 228-228. IEEE, 2013.

TEACHING EXPERIENCE

Teaching Assistant to Dr. V. Tam
In ELEC1503, Object Oriented Programming and Data Structures, 2012
Performed the lab demonstrations and Q&A upon request

Teaching Assistant to Dr. Hayden So
In ELEC3441 Computer Architecture, 2014-2015
Developed part of the homework, prepared the lab environment, Q&A upon request

Teaching Assistant to Dr. Hayden So, Dr. Edmund Lam, and Dr. Kenneth K. Y. Wong
In ENGG1203, Introduction to Electrical and Electronic Engineering, 2013-2014
Performed the lab demonstrations and Q&A upon request

Teaching Assistant - to Dr. Bingsheng He
Gave lecture "System Optimizations and Performance Tuning for New Generation FPGAs"
in NUS Winter School Course "Big Data Systems on Future Hardware", 2018

AWARDS

Postgraduate Studentship, The University of Hong Kong, Sep 2011 - Aug 2015

First Class Scholarship, Harbin Institute of Technology, Sep 2007- Jul 2009

Outstanding Postgraduate Student, Key Lab of Computing System and Architecture, ICT Dec 2010

Second Award of National Postgraduate Mathematical Modeling Contest, May 2008

Second Award of Electronic Design Contest, Heilongjiang Province, Mar 2007

SKILLS

Programming Languages
- Proficient: SystemC, C/C++, Matlab, Verilog, VHDL, HLS, OpenCL for FPGA
- Competent: JAVA, Python

REFERENCE

Dr. Bingsheng He (hebs@comp.nus.edu.sg)

Dr. Hayden Kwok-Hay So (hso@eee.hku.hk)

Dr. Jinxiang Wang (jxwang@hit.edu.cn)

Dr. Liyi Xiao (xiaoly@hit.edu.cn)

Dr. Ying Wang (wangying2009@ict.ac.cn)

Dr. Fangfa Fu (fff1984292@hit.edu.cn)

Dr. Lei Zhang (zlei@ict.ac.cn)

Dr. Xiaowei Li (lxw@ict.ac.cn)

Dr. Yinhe Han (yinhes@ict.ac.cn)