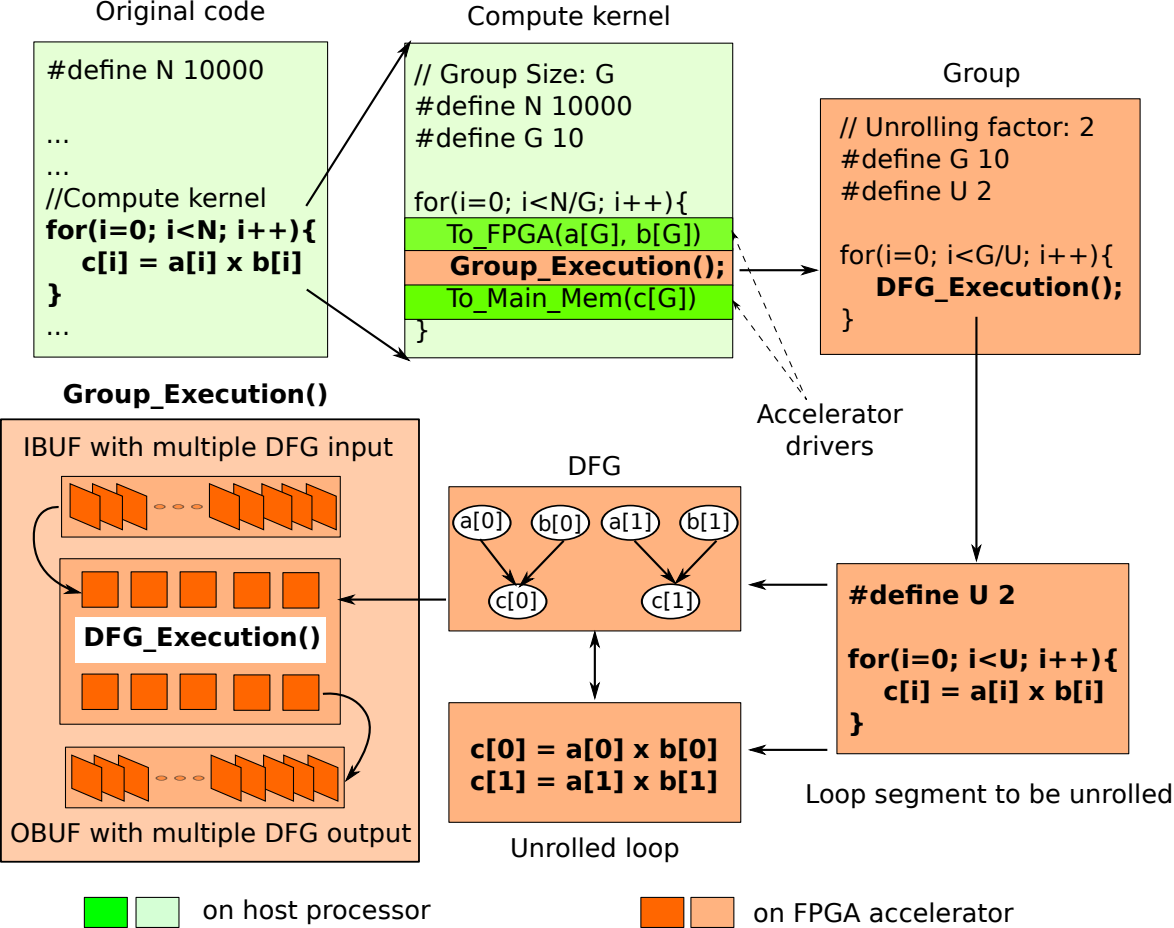
Original code
#define N 10000
...
...
//Compute kernel
for(i=0; i<N; i++){
c[i] = a[i] x b[i]
}
...
Compute kernel
// Group Size: G
#define N 10000
#define G 10
for(i=0; i<N/G; i++){
To_FPGA(a[G], b[G])
Group_Execution();
To_Main_Mem(c[G])
}
Group
// Unrolling factor: 2
#define G 10
#define U 2
for(i=0; i<G/U; i++){
DFG_Execution();
}
Accelerator drivers
Group_Execution()
IBUF with multiple DFG input
DFG_Execution()
OBUF with multiple DFG output
DFG
a[0]
b[0]
a[1]
b[1]
c[0]
c[1]
#define U 2
for(i=0; i<U; i++){
c[i] = a[i] x b[i]
}
Loop segment to be unrolled
c[0] = a[0] x b[0]
c[1] = a[1] x b[1]
Unrolled loop
on host processor
on FPGA accelerator