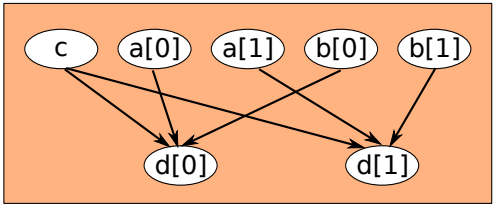
Text DFG

```
//dst op src0, src1, src2
d[0] MULADD a[0] a[1] c
d[1] MULADD a[1] b[1] c
```

DFG




DFG_Execution

```
// Unrolling factor: U
// input: a[U], b[U], c
// output: d[U]

for(i=0; i<U; i++){
    d[i] = a[i] x b[i] + c
}
```

Original Compute Kernel

```
#define N 10000

// input: a[N], b[N], c
// output: d[N]
for(i=0; i<N; i++){
    d[i] = a[i] x b[i] + c
}
```

Accelerated Compute Kernel

```
// Block Size: B
#define N 10000
#define B 10

// input: a[N], b[N], c
// output: d[N]
for(i=0; i<N/B; i++){
    Move input of the block to FPGA
    Block_Execution();
    Move FPGA result back
}
```

Block_Execution

```
// Block Size: B
// Unrolling Factor: U
#define B 10
#define U 2

// input: a[B], b[B], c
// output: d[B]
for(i=0; i<B/U; i++){
    DFG_Execution();
}
```

Block IO Mapping

| DFG-ID | it=0 | it=1 | ... |
|---|---|---|---|
| c | 0(c) | 0(c) | ... |
| a[0] | 1(a[0]) | 3(a[2]) | ... |
| a[1] | 2(a[1]) | 4(a[3]) | ... |
| b[0] | 11(b[0]) | 13(b[2]) | ... |
| b[1] | 12(b[1]) | 14(b[3]) | ... |
| d[0] | 0(d[0]) | 2(d[2]) | ... |
| d[1] | 1(d[1]) | 3(d[3]) | ... |

Assumed Data Layout in IO Buffer

```
c, a[0], a[1], a[2], ..., a[9],
b[0], b[1], b[2], ..., b[9],
```

```
d[0], d[1], ..., d[9]
```