

Automatic Nested Loop Acceleration On A Highly Predictable Soft Coarse-Grained Reconfigurable Array Overlay

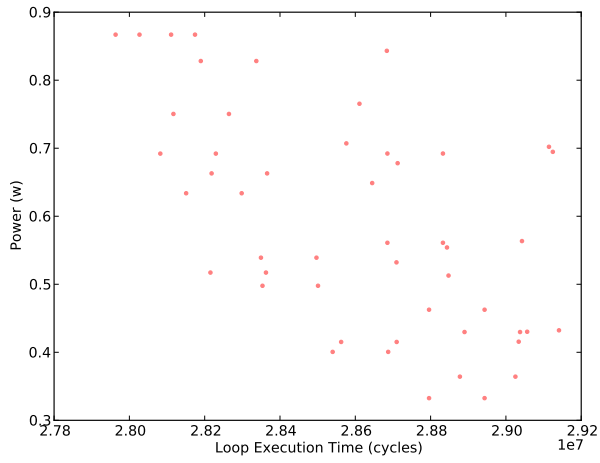
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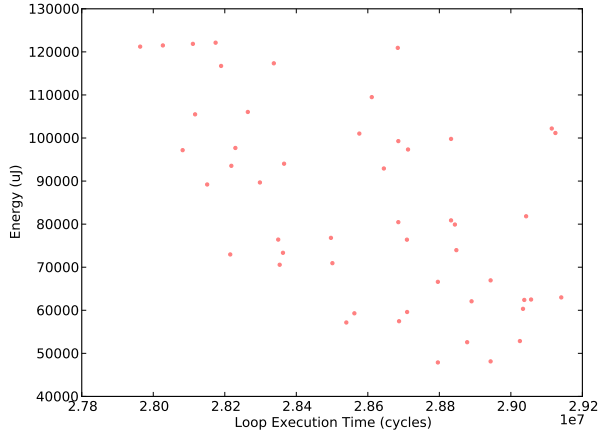
ABSTRACT

We present an automatic hardware/software co-design framework for accelerating a nested loop on a hybrid CPU+FPGA system. It partially unrolls the inner loop, maps the unrolled part to a soft coarse-grained reconfigurable array (SCGRA) overlay based FPGA accelerator built on top of the off-the-shelf FPGAs and generates corresponding drivers to utilize the FPGA accelerator to complete the whole loop. It will delicately leverage the communication cost and computation benefits on FPGA and the users can acquire an optimal co-design by simply providing the high-level user constraints such as energy and hardware resource budgets instead of manually improving the hardware and software design repeatedly. In addition, as the SCGRA based FPGA accelerator has highly predictable hardware overhead, power consumption and performance, the design space exploration (DSE) becomes fast and easy to converge. According to the experiments, it takes 5 minutes to 30 minutes to complete the DSE for each application of the benchmark.

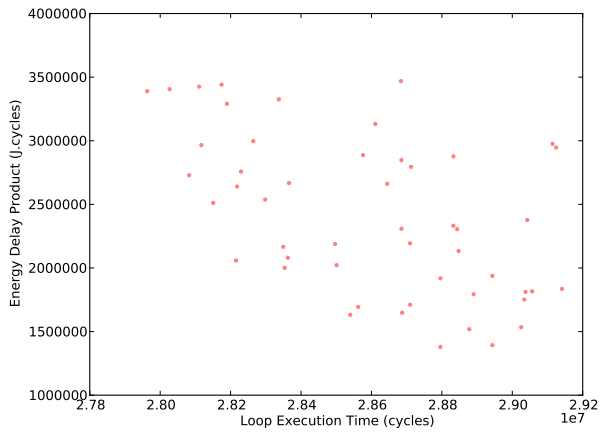
1. INTRODUCTION
2. RELATED WORK
3. SCGRA OVERLAY BASED FPGA ACCELERATOR DESIGN
4. REVENUE AWARE DESIGN SPACE EXPLORATION
5. EXPERIMENTS
6. FUTURE WORK AND LIMITATION
7. CONCLUSION
8. REFERENCES



(a) ExeTime-Power Distribution

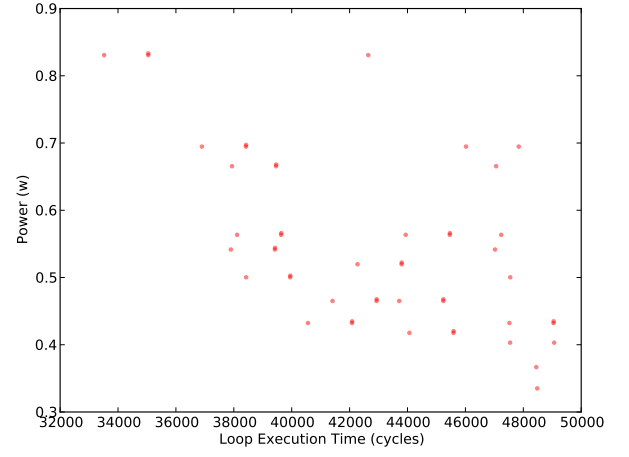


(b) ExeTime-Energy Distribution

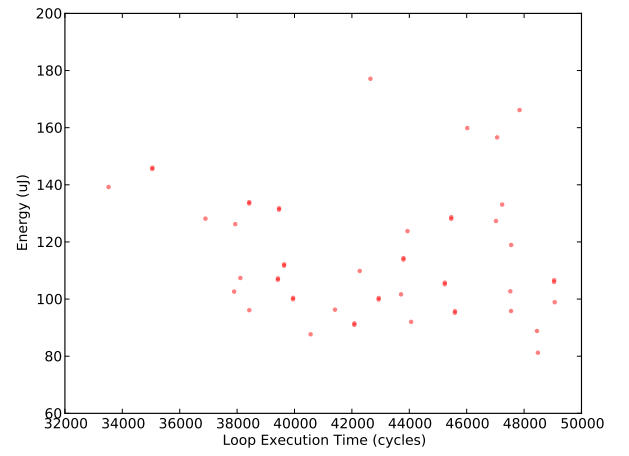


(c) ExeTime-EDP Distribution

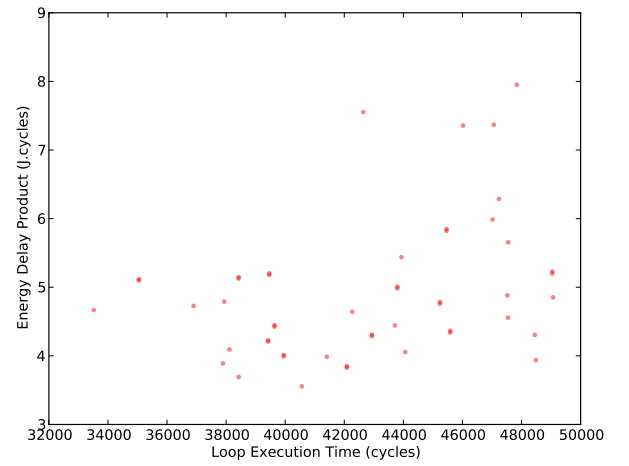
Figure 1: Design Space of Matrix Multiplication, Matrix Size is 128x128



(a) ExeTime-Power Distribution

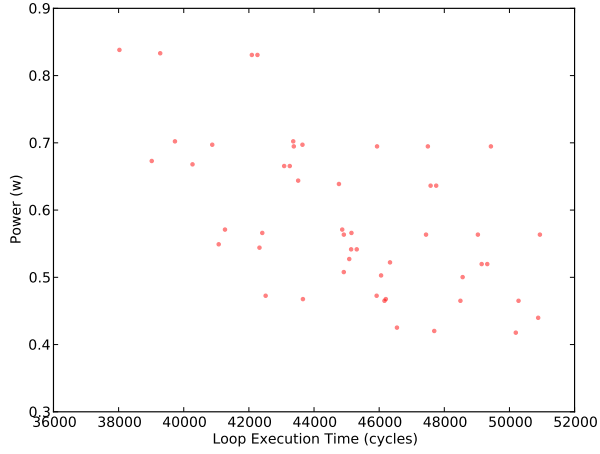


(b) ExeTime-Energy Distribution

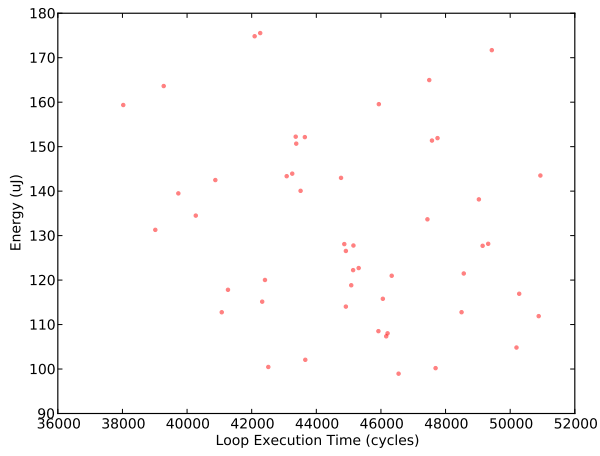


(c) ExeTime-EDP Distribution

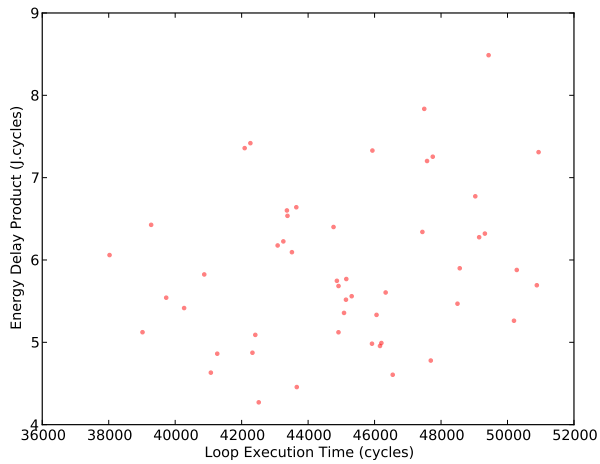
Figure 2: Design Space of Fir, Input signal length is 1024 and coefficient length is 64



(a) ExeTime-Power Distribution

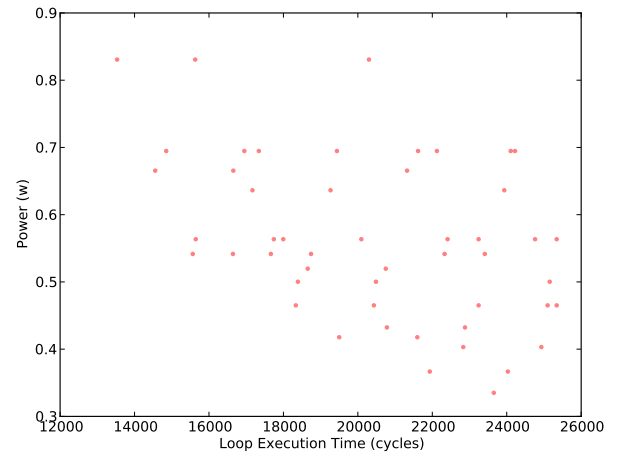


(b) ExeTime-Energy Distribution

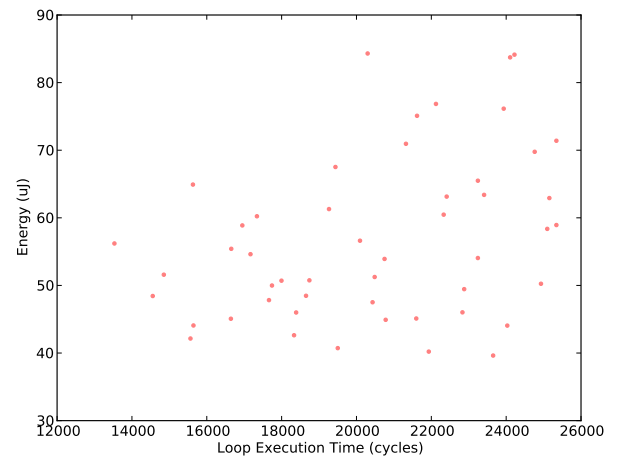


(c) ExeTime-EDP Distribution

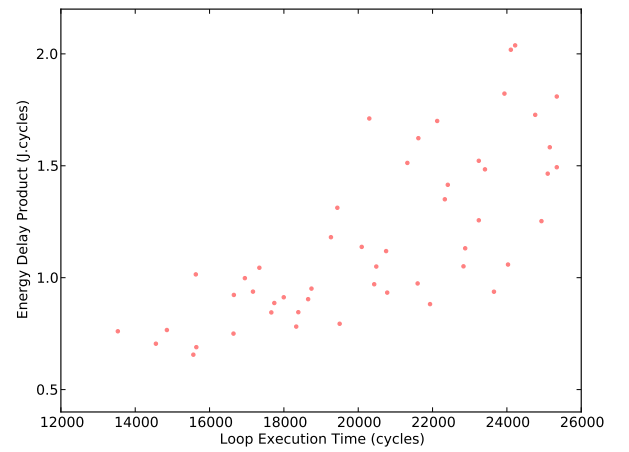
Figure 3: Design Space of Kmean, Number of Nodes is 1024, Numer of centroids is 4, Node dimension is 2



(a) ExeTime-Power Distribution



(b) ExeTime-Energy Distribution



(c) ExeTime-EDP Distribution

Figure 4: Design Space of Sobel Edge Detector, Figure size is 128x8