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个人简介

中科院计算技术研究所，副研究员, 主要研究方向为领域专用芯片设计、容错芯片设计以及新型 EDA 技术，主持来自中科院先导、科技部、军工、基金委以及航天科技等多个领域专用芯片与系统的研究项目，将专用芯片应用于星载智能计算、舰载大数据处理、端侧智能计算等多个关键场景。发表集成电路设计相关的学术论文 60 余篇（CCF 推荐 A 类 21 篇, IEEE/ACM 汇刊 22 篇），出版英文专著 1 部，其中通信/一作论文 30 余篇，获得国际最佳论文奖 2 次。获得中科院科技成果转化特等奖 1 次，指导学生在 CVPR 低功耗计算机视觉挑战赛、DAC 系统设计竞赛、ICCAD 的 EDA 竞赛等国际竞赛中多次获得冠亚军。担任 FCCM、FPT、ICLR、NIPS、ICML 等国际学术会议的程序委员，TCAD、TVLSI、TC 等多个集成电路领域期刊的审稿人。

教育与工作经历

中科院计算所 *2018-06 - 至今*

计算机体系结构国家重点实验室/处理器芯片全国重点实验室，副研究员

新加坡国立大学 *2016-12 - 2018-06*

计算机学院，博后

香港大学 *2011-09 - 2016-11*

计算机工程专业，电机与电子工程系

哈尔滨工业大学 *2007-09 - 2009-07*

微电子学与固体电子学专业，航天学院

哈尔滨工业大学 *2003-09 - 2007-07*

电子信息科学与技术专业，航天学院

科研项目

跨层芯片设计与优化软硬件平台课题 *2024 - 2028*

中科院先导 B 计划，主持

面向遥感图像识别的智能计算系统可靠性评测 *2024 - 2024*

航天科技集团，主持

AI 辅助的领域专用芯片设计自动化方法研究 *2023 - 2024*

处理器芯片重点实验室培育项目，主持

基于智能计算存储器的大数据处理系统设计 *2023 - 2024*

1XX 创新项目，主持

领域专用芯片跨层参数优化方法 *2023 - 2025*

国家重点研发计划子课题，主持

面向 COTS 器件的深度学习容错工具链设计 *2023 - 2023*

航天科技集团，主持

弹性深度学习处理器芯片设计 *2022 - 2025*
自然科学基金面上项目，主持
基于 FPGA 的高能效图计算加速器定制设计 *2020 - 2022*
自然科学基金青年项目，主持
深度学习处理器设计自动化加固设计方法 *2021 - 2022*
计算机体系结构重点实验室培育项目，主持
物端智能无人机系统设计 *2019 - 2020*
1XX 项目子课题，参与
开源物端智能处理器 *2020 - 2021*
中科院先导 C 课题，参与
基于智能网卡与智能存储设备的流式计算系统研究 *2020 - 2021*
华为，参与

论文

书籍

- Xiaowei Li, Guihai Yan, **Cheng Liu**, Built-in Fault-tolerant Computing Paradigm for Resilient Large-Scale Chip Design, Springer Nature, 2023
- Xuntao Cheng, **Cheng Liu**, Bingsheng He, "Emerging Hardware Technologies", In Book Encyclopedia of Big Data Technologies, pp.1-5, Jan 2018
- Hayden Kwok-Hay So and **Cheng Liu**, "FPGA overlays", in press FPGAs for Software Engineers, Dirk Koch, Frank Hannig and Daniel Ziener, Ed., 2016.

期刊

- 1 Haitong Huang, Cheng Liu(通信作者), Xinghua Xue, Bo Liu, Huawei Li, Xiaowei Li, MRFI: An Open Source Multi-Resolution Fault Injection Framework for Neural Network Processing, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2024.
- 2 Mingkai Chen, Cheng Liu(通信作者), Shengwen Liang, Lei He, Ying Wang, Lei Zhang, Huawei Li, Xiaowei Li, An Energy-Efficient In-Memory Accelerator for Graph Construction and Updating, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2024.
- 3 Xinmiao Zhang, Cheng Liu(通信作者), Jiacheng Ni, Yuanqing Cheng*, Lei Zhang, Huawei Li, Xiaowei Li, PDG: A Prefetcher for Dynamic Graph Updating, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023.
- 4 Xinghua Xue, Cheng Liu(通信作者), Ying Wang, Bing Yang, Tao Luo, Lei Zhang, Huawei Li, Xiaowei Li, Soft Error Reliability Analysis of Vision Transformers, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2023.
- 5 Xinghua Xue, Cheng Liu(通信作者), Bo Liu, Haitong Huang, Ying Wang, Tao Luo, Lei Zhang, Huawei Li, Xiaowei Li, "Exploring Winograd Convolution for Cost-effective Neural Network Fault Tolerance", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2023.
- 6 Cheng Chu, Cheng Liu(通信作者), Dawen Xu, Ying Wang, Tao Luo, Huawei Li, Xiaowei Li, "Accelerating Deformable Convolution Networks with Dynamic and Irregular Memory Accesses", ACM Transactions on Design Automation of Electronic Systems (TODAES), 2023.

· 7 Haitong Huang, Xinghua Xue, Cheng Liu(通信作者), Ying Wang, Tao Luo, Long Cheng, Huawei Li, Xiaowei Li, "Statistical Modeling of Soft Error Influence on Neural Networks", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2023.

· 8 Cheng Liu, Cheng Chu, Dawen Xu, Ying Wang, Qianlong Wang, Huawei Li, Xiaowei Li, Kwang-Ting Cheng, "HyCA: A Hybrid Computing Architecture for Fault Tolerant Deep Learning", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2022

· 9 Dawen Xu, Zhuangyu Feng, Cheng Liu(通信作者), Li Li, Ying Wang, Huawei Li, Xiaowei Li, "Taming Process Variations in CNFET for Efficient Last Level Cache Design", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021.

· 10 Dawen Xu, Meng He, Cheng Liu(通信作者), Ying Wang, Long Cheng, Huawei Li, Xiaowei Li, Kwang-Ting Cheng, "R2F: A Remote Retraining Framework for AIoT Processors with Computing Errors", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021.

· 11 Dawen Xu, Ziyang Zhu, Cheng Liu(通信作者), Ying Wang, Shuang Zhao, Lei Zhang, Huaguo Liang, Huawei Li, Kwang-Ting Cheng, "Reliability Evaluation and Analysis of FPGA-based Neural Network Acceleration System", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 2021

· 12 Dawen Xu(共同一作), Cheng Liu(共同一作), Ying Wang, Kaijie Tu, Bingsheng He, and Lei Zhang. "Accelerating Generative Neural Networks on Unmodified Deep Learning Processors-A Software Approach." IEEE Transactions on Computers (2020).

会议

· 1 Erjing Luo(共同一作), Haitong Huang(共同一作), Cheng Liu(通信作者), Guoyu Li, Bing Yang, Ying Wang, Huawei Li, Xiaowei Li, "DeepBurning-MixQ: An Open Source Mixed-Precision Neural Network Accelerator Design Framework for FPGAs", ICCAD, 2023.

· 2 Cheng Liu, Zhen Gao, Siting Liu, Xuefei Ning, Huawei Li, and Xiaowei Li, "Fault-Tolerant Deep Learning: A Hierarchical Perspective", in The 40th IEEE VLSI Test Symposium (VTS), 2022.

· 3 Xinghua Xue, Haitong Huang, Cheng Liu(通信作者), Tao Luo, Lei Zhang, Ying Wang, "Winograd Convolution: A Perspective from Fault Tolerance", In proceedings of ACM/IEEE Design Automation Conference (DAC), 2022.

· 4 Cangyuan Li, Ying Wang(通信作者), Cheng Liu(通信作者), Shengwen Liang, Huawei Li, Xiaowei Li, "GLIST: Towards In-Storage Graph Learning", USENIX Annual Technical Conference(ATC), 2021.

· 5 Lei He(共同一作), Cheng Liu(共同一作), Ying Wang, Shengwen Liang, Huawei Li, and Xiaowei Li, "GCiM: A Near-Data Processing Accelerator for Graph Construction",In proceedings of ACM/IEEE Design Automation Conference (DAC), 2021.

· 6 Yuquan He, Ying Wang(通信作者), Cheng Liu(通信作者), and Lei Zhang, "PicoVO: A Lightweight RGB-D Visual Odometry Targeting Resource-Constrained IoT Devices", In The 2021 IEEE International Conference on Robotics and Automation (ICRA), 2021.

· 7 Dawen Xu, Cheng Chu, Cheng Liu(通信作者), Qianlong Wang, Ying Wang, Lei Zhang, Huaguo Liang and Kwang-Ting Tim Cheng, A Hybrid Computing Architecture for Fault-tolerant Deep Learning Accelerators, The 38th IEEE International Conference on Computer Design(ICCD), October, 2020.

· 8 Shengwen Liang(共同一作), Cheng Liu(共同一作), Ying Wang, Huawei Li, Xiaowei Li, DeepBurning-GL: an Automated Framework for Generating Graph Neural Network Accelerators, IEEE/ACM International Conference on Computer-Aided Design (ICCAD), November, 2020

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· 10 Dawen Xu, Cheng Chu, Cheng Liu(通信作者), Ying Wang, Xianzhong Zhou, Lei Zhang, Huawei Li, Huaguo Liang, Multi-task Scheduling for PIM-based Heterogeneous Computing System, In IEEE Great Lakes Symposium on VLSI (GLVLSI), 2020.

· 11 Dawen Xu, Xinke Chu, Cheng Liu(通信作者), Ying Wang, Huawei Li, Lei Zhang, CNT-Cache: an Energy-Efficient Carbon Nanotube Cache with Adaptive Encoding , IEEE/ACM Proceedings of Design, Automation and Test in Europe conference (DATE), 2020

· 12 Cheng Liu, Xinyu Chen, Bingsheng He, Ying Wang, Xiaofei Liao, Lei Zhang, OBFS: OpenCL Based BFS Optimization on Software Programmable FPGAs, In 2019 International Conference on Field Programmable Technology (FPT), Dec 11-13, 2019

· 13 Dawen Xu, Kouzi Xing, Cheng Liu(通信作者), Ying Wang, Yulin Dai, Long Cheng, Huawei Li, Lei Zhang, Resilient Neural Network Training for Accelerators with Computing Errors, The 30th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), July 15-17, 2019

· 14 Kouzi Xing, Dawen Xu, Cheng Liu(通信作者), Ying Wang, Huawei Li and Xiaowei Li, Squeezing the Last MHz for CNN Acceleration on FPGAs , The 3rd International Test Conference in Asia (ITC-Asia), 2019

· 15 Cheng Liu, Ho-Cheung Ng, and Hayden Kwok-Hay So. QuickDough: a rapid FPGA loop accelerator design framework using soft CGRA overlay . In International Conference on Field Programmable Technology (FPT), pp. 56-63. IEEE, 2015.

· 16 Cheng Liu, Ho-Cheung Ng, Hayden Kwok-Hay So, Automatic nested loop acceleration on fpgas using soft CGRA overlay, The Second International workshop of FPGAs for Software Programmers (FSP), 2015

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· 18 Cheng Liu, Colin Lin Yu, and Hayden Kwok-Hay So. A soft coarse-grained reconfigurable array based high-level synthesis methodology: Promoting design productivity and exploring extreme FPGA frequency. In 2013 IEEE 21st Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), pp. 228-228. IEEE, 2013 (poster)

· 19 Cheng Liu, Hayden Kwok-Hay So, QuickDough: A Rapid FPGA Accelerator Generation Framework using Soft Coarse-Grained Reconfigurable Array Overla,y The 1st International Workshop on Overlay Architectures for FPGAs (OLAF), 2013.

· 20 Cheng Liu, Lei Zhang, Yinhe Han, and Xiaowei Li. Vertical interconnects squeezing in symmetric 3D mesh network-on-chip. In Proceedings of the 16th Asia and South Pacific Design Automation Conference (ASP-DAC), pp. 357-362. IEEE Press, 2011.

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