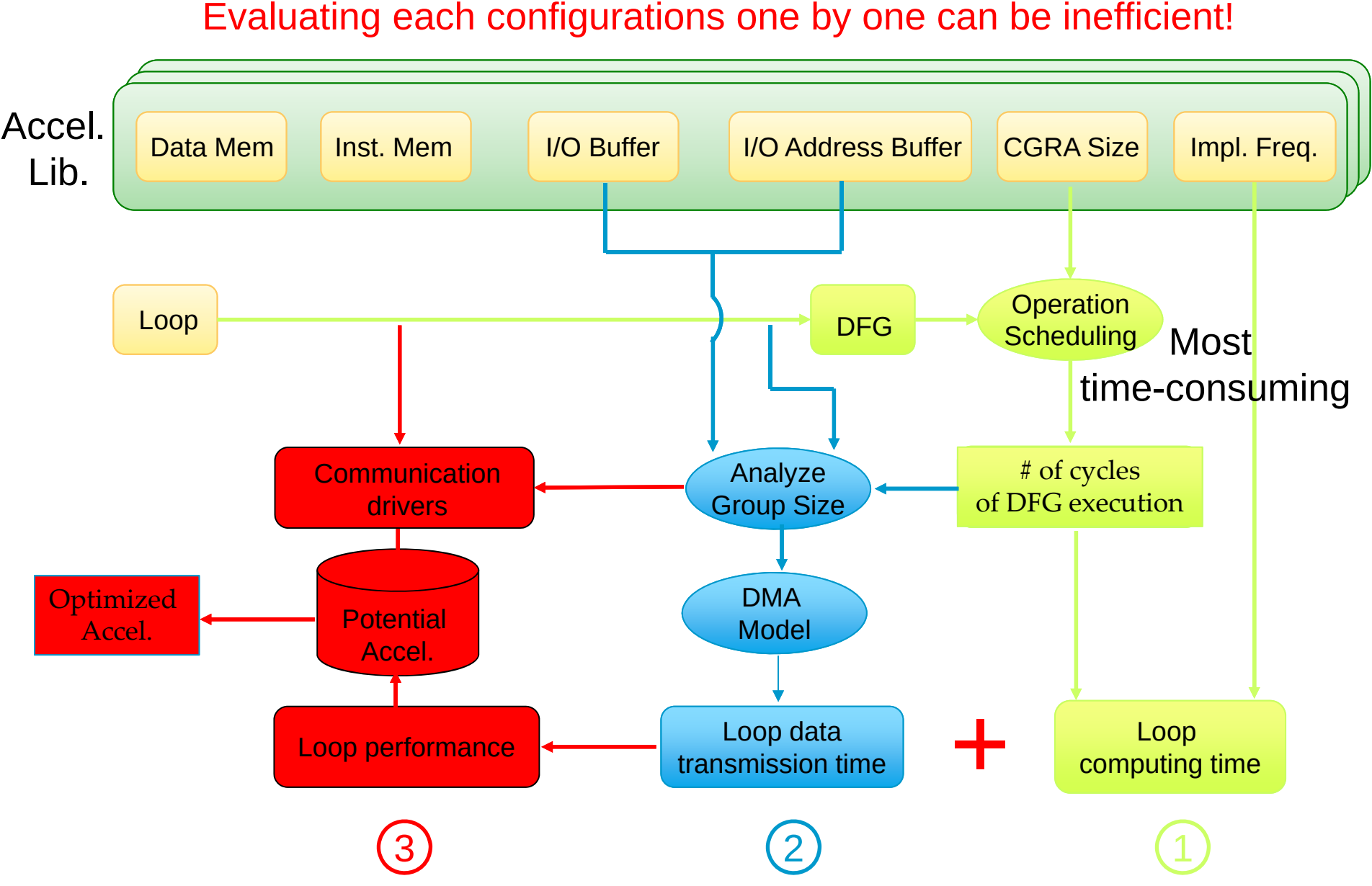
Evaluating each configurations one by one can be inefficient!
Accel. Lib.
Data Mem
Inst. Mem
I/O Buffer
I/O Address Buffer
CGRA Size
Impl. Freq.
Loop
DFG
Operation Scheduling
Most time-consuming
Communication drivers
Analyze Group Size
# of cycles of DFG execution
Optimized Accel.
Potential Accel.
DMA Model
Loop performance
Loop data transmission time
+
Loop computing time
3
2
1