Abstraction level

High / Medium / Low

Processing speed: fast / medium / slow

```
for (i=0; i<N; i++){
    c[i]=a[i]*b[i];
    ...;
}
```
HLL program

op — op — op — op / op — op — op
IR(DFG/CFG)

A-core | C-core | C-core   C-core: control core
Interconnection
Mem | Mem | Mem   A-core: arithmetic core
MARC

PE | PE | PE | PE   PE: processing element
PE | PE | PE | PE
PE | PE | PE | PE
SCGRA

```
always@(*) begin
    c=a*b;
    ...
end
```
RTL design

IF | C | IF | C | IF   C: connection box
C | C | C | C
IF | C | IF | C | IF   IF: Inter mediate fabric
VFPGA

LUT   DSP
clock
Ram block   IP
FPGA

① RTL design flow ② Conventional HLS ③ Virtual FPGA(VFPGA) based HLS

④ SCGRA based HLS ⑤ Many-core approach to reconfigurable computing(MARC)