Lab Report: Digital Filters

Team Members:

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Introduction:

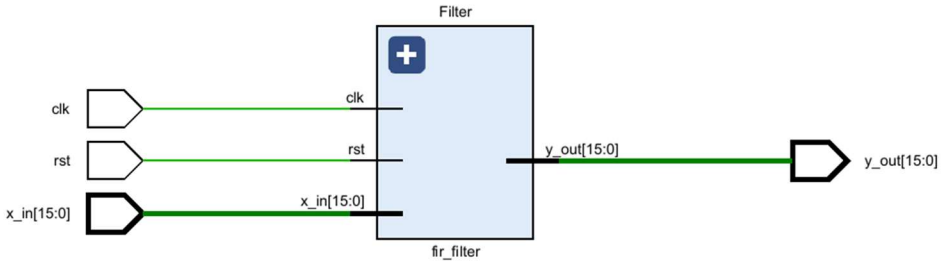
In this project, we focus on the design and implementation of a digital averaging filter for noise cancellation using VHDL (VHSIC Hardware Description Language). The objective is to develop a filter that can effectively attenuate noise from a noisy signal while preserving the desired signal components. The filter operates by averaging multiple samples over time to suppress random variations and enhance the signal-to-noise ratio.

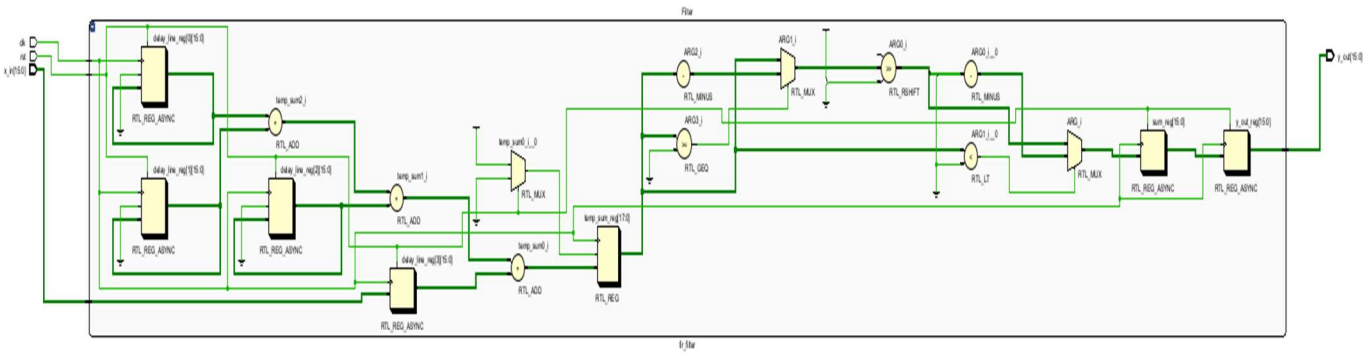
The digital averaging filter is a fundamental component of noise cancellation systems, finding applications in various domains such as audio processing, biomedical signal analysis, and communications. By leveraging digital filtering techniques, we aim to provide a robust and efficient solution for noise reduction in practical scenarios.

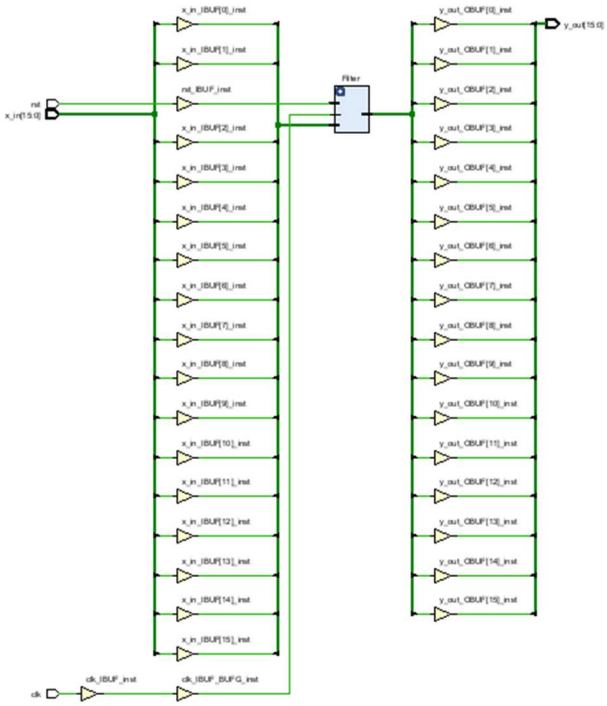
Through this project, we seek to gain insights into digital filter design, VHDL programming, and signal processing concepts. By designing and testing the digital averaging filter, we aim to understand its behavior, evaluate its performance, and explore potential optimizations for noise cancellation applications.

Hardware Architecture:

Block Diagram:







Description:

Our hardware architecture consists of a Finite Impulse Response (FIR) filter module. The FIR filter is designed to process incoming samples and produce an output that represents the average of the input samples over a specific window size.

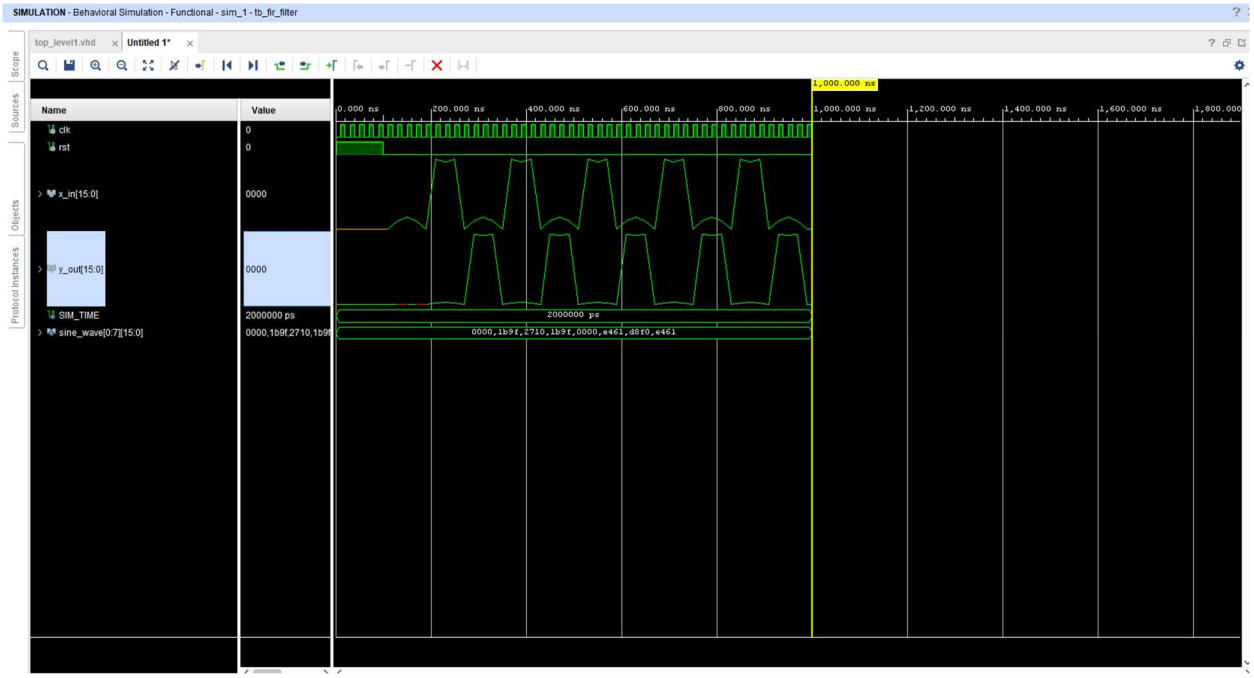
Behavior of Individual Components:

FIR Filter:

The FIR filter module consists of a shift register to store the incoming samples and an accumulator to compute the sum of the samples. The sum is then divided by the number of taps in the filter to obtain the average value.

Simulation Results:

Testbench Simulation:



Discussion of Results:

Performance Evaluation:

The performance of the digital averaging filter was evaluated based on its ability to suppress noise while preserving signal integrity. The filter demonstrated satisfactory noise cancellation capabilities, as evidenced by the simulation results.

Comparison with Expected Behavior:

The behavior of the filter closely matched our expectations based on the design specifications. The filter effectively attenuated noise components, leading to a cleaner output signal.

Work Distribution Among Members:

Team Member Contributions:

Zia:

Designed the FIR filter architecture.

Implemented the VHDL code for the FIR filter module.

Conducted simulations and analyzed the filter's performance.

Contributed to writing the lab report

Max:

Developed the top-level entity architecture.

Integrated the FIR filter module into the top-level design.

Designed and implemented the testbench for simulation.

Conducted additional simulations for validation.

Provided support in compiling project files and managing versions.

Code Screen Shot;

PROJECT MANAGER - project_1

Sources | Source File Properties

Project Summary | top_level1.vhd | fir_filter.vhd | tb_fir_filter.vhd

C:/Users/mzia1/OneDrive/Desktop/EECS 443 lab/Hosainzada_Djafarov_Final_Project/Final_project/project_1.srcs/sources_1/new/top_level1.vhd

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity top_level1 is
    port (
        clk   : in std_logic;
        rst   : in std_logic;
        x_in  : in signed(15 downto 0);
        y_out : out signed(15 downto 0)
    );
end entity;

architecture Structural of top_level1 is
    component fir_filter
        generic (N : integer);
        port (
            clk   : in std_logic;
            rst   : in std_logic;
            x_in  : in signed(15 downto 0);
            y_out : out signed(15 downto 0)
        );
    end component;
begin
    Filter: fir_filter
        generic map (N => 4)
        port map (
            clk   => clk,
            rst   => rst,
            x_in  => x_in,
            y_out => y_out
        );
end Structural;

```

PROJECT MANAGER - project_1

Sources | Source File Properties

Project Summary | top_level1.vhd | fir_filter.vhd | tb_fir_filter.vhd

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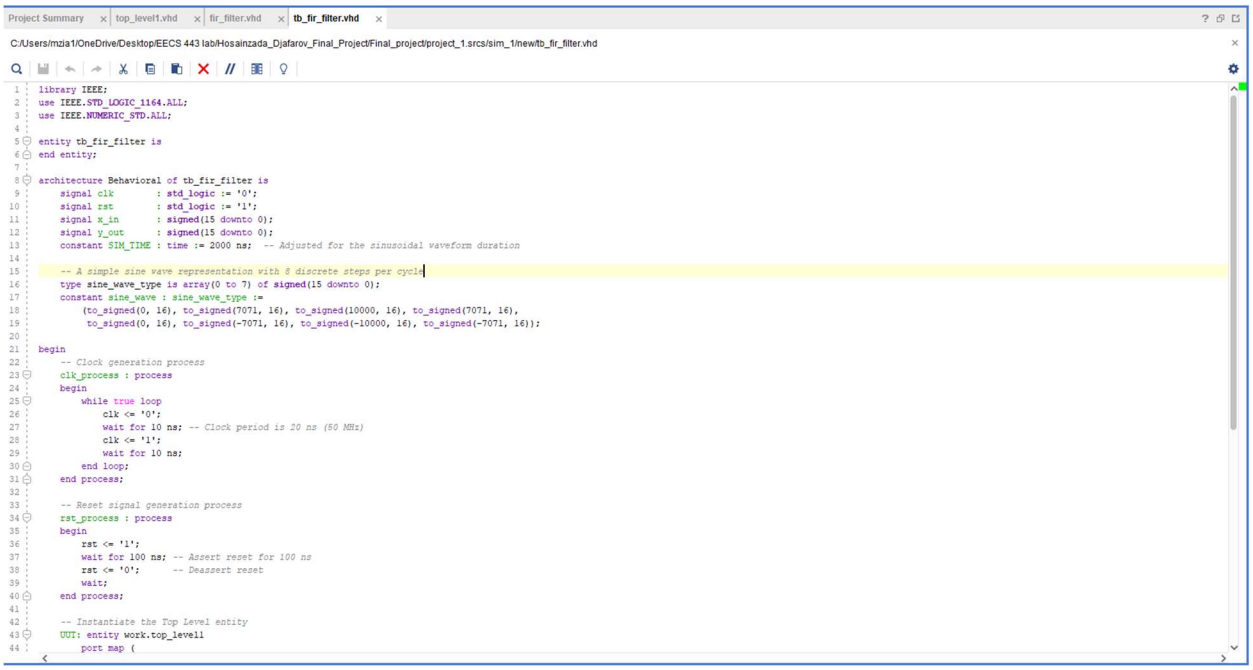
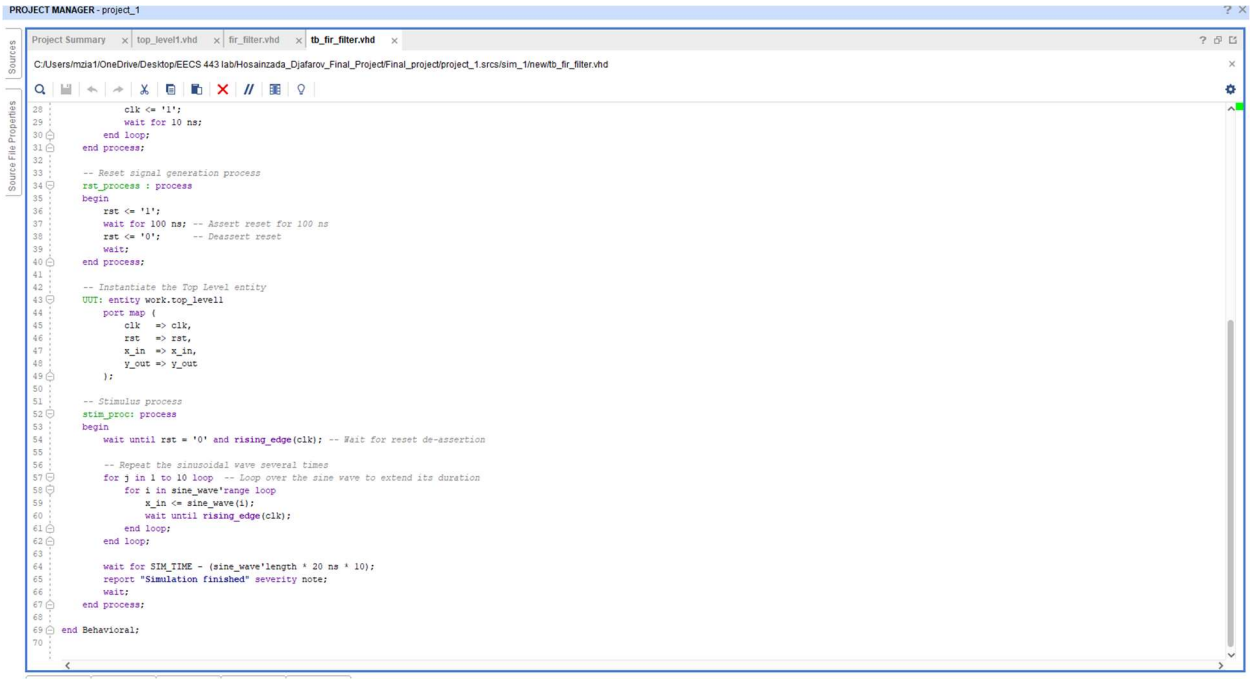
```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity fir_filter is
    generic (
        N : integer := 7  -- Changed number of taps to 7
    );
    port (
        clk   : in std_logic;
        rst   : in std_logic;
        x_in  : in signed(15 downto 0);
        y_out : out signed(15 downto 0)
    );
end entity;

architecture Behavioral of fir_filter is
    type shift_reg is array (N-1 downto 0) of signed(15 downto 0);
    signal delay_line : shift_reg := (others => (others => '0'));
    signal sum : signed(15 downto 0) := (others => '0');
    signal temp_sum : signed(17 downto 0); -- Ensure enough bits to prevent overflow
begin
    process(clk, rst)
        variable acc : signed(17 downto 0); -- Accumulation variable, expanded for summing up to N terms
    begin
        if rst = '1' then
            delay_line <= (others => (others => '0'));
            sum <= (others => '0');
            y_out <= (others => '0');
        elsif rising_edge(clk) then
            delay_line <= x_in & delay_line(N-2 downto 0); -- Shift the input into the delay line
            acc := (others => '0'); -- Reset the accumulator

            for i in 0 to N-1 loop -- Accumulate the delayed values
                acc := acc + resize(delay_line(i), acc'length);
            end loop;

            temp_sum <= acc; -- Store the accumulated value

            -- For N not a power of 2, replace shift right with division
            sum <= resize(temp_sum / to_signed(N, temp_sum'length), sum'length);

            y_out <= sum; -- Output the averaged sum
        end if;
```





Conclusion:

In this project, we designed and implemented a digital averaging filter for noise cancellation using VHDL. The filter, based on the Finite Impulse Response (FIR) technique, was successfully developed and tested using synthetic data. Through simulations, we evaluated the performance of the filter and assessed its effectiveness in attenuating noise while preserving signal integrity.

Our results demonstrate that the digital averaging filter effectively suppresses high-frequency noise components, leading to a smoother output signal. The filter's behavior closely aligns with our expectations, as outlined in the project specifications. By averaging multiple samples over time, the filter provides a reliable method for noise cancellation, enhancing the quality of the output signal.

Overall, this project highlights the importance and effectiveness of digital filtering techniques in mitigating noise in signal processing applications. The successful implementation of the digital averaging filter underscores the potential for VHDL-based designs in real-world noise reduction scenarios.

In conclusion, the digital averaging filter developed in this project represents a valuable contribution to noise cancellation techniques and lays the foundation for future research and development in this field.