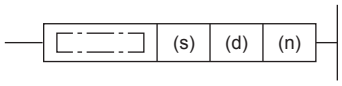
8.22 Check Code

Check code

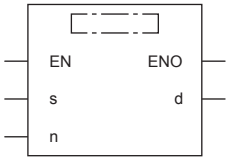
CCD(P)

FX5S FX5UJ FX5U FX5UC

These instructions calculate the horizontal parity value and sum check value in the error check methods used in communication. There is another check method, called CRC (cyclic redundancy check). For obtaining CRC value, use the CRC(P) instructions.

Ladder diagram	Structured text
	ENO:=CCD(EN,s,n,d); ENO:=CCDP(EN,s,n,d);

FBD/LD



Setting data

■Descriptions, ranges, and data types

Operand	Description	Range	Data type	Data type (label)
(s)	Head device number of applicable device	—	16-bit signed binary	ANY16
(d)	Head device number storing the calculated data	—	16-bit signed binary	ANY16_ARRAY (Number of elements: 2)
(n)	Number of data	1 to 32767	16-bit unsigned binary	ANY16_U
EN	Execution condition	—	Bit	BOOL
ENO	Execution result	—	Bit	BOOL

■Applicable devices

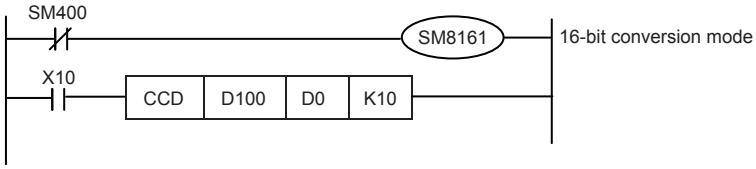
Operand	Bit	Word			Double word		Indirect specification	Constant			Others
	X, Y, M, L, SM, F, B, SB, S	T, ST, C, D, W, SD, SW, R	U□\G□	Z	LC	LZ		K, H	E	$	
(s)	○	○*1	○	—	—	—	○	—	—	—	—
(d)	○	○*1	○	—	—	—	○	—	—	—	—
(n)	○	○	○	○	—	—	○	○	—	—	—

*1 T, ST, and C cannot be used.

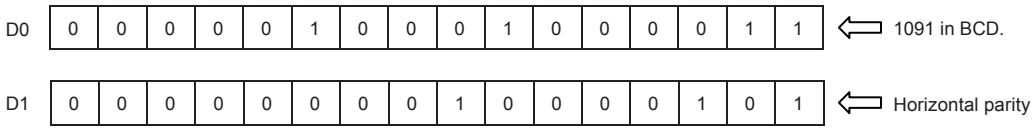
Processing details

- These instructions calculate the addition data and horizontal parity value of data stored in (s) to (s)+(n)-1. The addition data is stored to (d), and the horizontal parity value is stored to (d)+1. The 16-bit mode and 8-bit mode are available for these instructions. For the operation in each mode, refer to the proceeding pages.
  - 16-bit conversion mode (while SM8161 is OFF)

    With regard to (n) data points starting from (s), the addition data and horizontal parity data of high-order 8 bits and low-order 8 bits are stored to (d) and (d)+1 respectively.
    SM8161 is shared with the ASCI(P), HEXA(P), and CRC(P) instructions. SM8161 must always be off in the 16-bit mode.
    SM8161 is cleared when the CPU module mode is changed from RUN to STOP.
    In the following program, conversion is executed as follows:

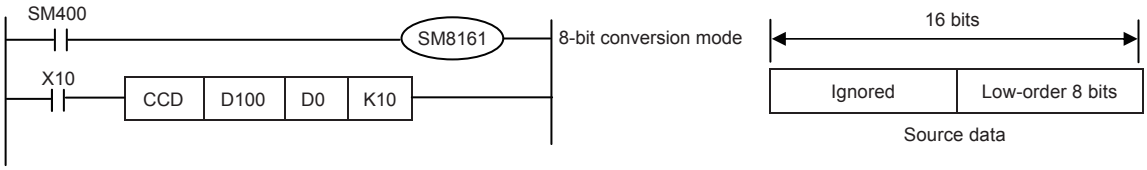


(s)	Example of data contents	
D100 lowest-order byte	K100 = 0 1 1 0 0 1 0 0	
D100 highest-order byte	K111 = 0 1 1 0 1 1 1 (1)	←
D101 lowest-order byte	K100 = 0 1 1 0 0 1 0 0	
D101 highest-order byte	K 98 = 0 1 1 0 0 0 1 0	
D102 lowest-order byte	K123 = 0 1 1 1 1 0 1 (1)	←
D102 highest-order byte	K 66 = 0 1 0 0 0 0 1 0	
D103 lowest-order byte	K100 = 0 1 1 0 0 1 0 0	
D103 highest-order byte	K 95 = 0 1 0 1 1 1 1 (1)	←
D104 lowest-order byte	K210 = 1 1 0 1 0 0 1 0	
D104 highest-order byte	K 88 = 0 1 0 1 1 0 0 0	
Total	K1091	
Horizontal parity	1 0 0 0 0 1 0 (1)	← When the number of "1" is odd, the horizontal parity is "1". When the number of "1" is even, the horizontal parity is "0".

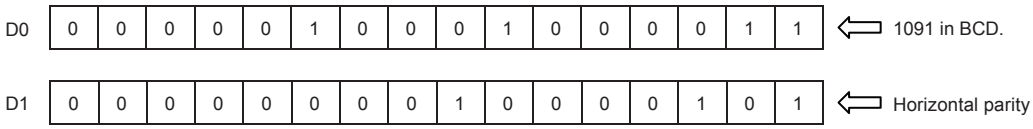


• 8-bit conversion mode (while SM8161 is ON)

With regard to (n) data points starting from (s), the addition data and horizontal parity data of only low-order 8 bits are stored to (d) and (d)+1 respectively.
SM8161 is shared with the ASCI(P), HEXA(P), and CRC(P) instructions. SM8161 must always be on in the 8-bit mode.
SM8161 is cleared when the CPU module mode is changed from RUN to STOP.
In the following program, conversion is executed as follows:



(s)	Example of data contents	
D100	K100 = 0 1 1 0 0 1 0 0	
D101	K111 = 0 1 1 0 1 1 1 (1)	←
D102	K100 = 0 1 1 0 0 1 0 0	
D103	K 98 = 0 1 1 0 0 0 1 0	
D104	K123 = 0 1 1 1 1 0 1 (1)	←
D105	K 66 = 0 1 0 0 0 0 1 0	
D106	K100 = 0 1 1 0 0 1 0 0	
D107	K 95 = 0 1 0 1 1 1 1 (1)	←
D108	K210 = 1 1 0 1 0 0 1 0	
D109	K 88 = 0 1 0 1 1 0 0 0	
Total	K1091	
Horizontal parity	1 0 0 0 0 1 0 (1)	← When the number of "1" is odd, the horizontal parity is "1". When the number of "1" is even, the horizontal parity is "0".



Operation error

Error code (SD0/SD8067)	Description
2820H	The device range specified by (s) or (d) exceeds the corresponding device range.
3405H	The value specified by (n) is outside the following range. 1 to 32767