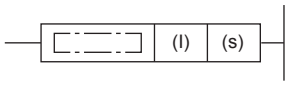
Disabling/enabling the specified interrupt pointer

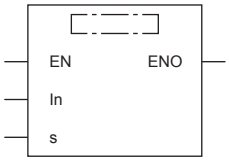
SIMASK

FX5S FX5UJ FX5U FX5UC

This instruction enables or disables the interrupt pointer number specified by (I) according to the value of (s).

Ladder diagram	Structured text
	ENO:=SIMASK(EN,In,s);

FBD/LD



Setting data

■Descriptions, ranges, and data types

Operand	Description	Range	Data type	Data type (label)
(I)*1	Interrupt pointer number for which interrupts are enabled or disabled	■FX5S CPU module I0 to I31 ■FX5UJ/FX5U/FX5UC CPU module I0 to I177	Device name	POINTER
(s)	Enabled or disabled state of the specified interrupt pointer number	0: Disabled 1: Enabled	16-bit signed binary	ANY16
EN	Execution condition	—	Bit	BOOL
ENO	Execution result	—	Bit	BOOL

*1 In the case of the ST language and the FBD/LD language, I displays as In.

■Applicable devices

Operand	Bit	Word			Double word		Indirect specification	Constant			Others
	X, Y, M, L, SM, F, B, SB, S	T, ST, C, D, W, SD, SW, R	U□\G□	Z	LC	LZ		K, H	E	$	
(I)	—	—	—	—	—	—	—	—	—	—	○
(s)	○	○	○	○	—	—	○	○	—	—	—

Processing details

- This instruction enables or disables the execution of the interrupt program with the interrupt pointer number specified by (I) according to the data specified by (s)
- When 1 is set in (s): The execution of the interrupt program is enabled.
- When 0 is set in (s): The execution of the interrupt program is disabled.
- When the power is turned on or the CPU module is reset, execution of the interrupt programs is enabled.

■FX5S CPU module
Interrupt program: I0 to I31
■FX5UJ/FX5U/FX5UC CPU module
Interrupt program: I0 to I177

• The execution-enabled/disabled states of interrupt pointers are stored in the IMASK instruction mask pattern.

■FX5S CPU module

IMASK instruction mask pattern: SD1400 to SD1401

■FX5UJ/FX5U/FX5UC CPU module

IMASK instruction mask pattern: SD1400 to SD1411

Operation error

Error code (SD0/SD8067)	Description
3405H	The interrupt pointer number specified by (I) exceeds the range of the interrupt pointer number (I0 to I177).
	The value in (s) is other than the interrupt disabled (0) or interrupt enabled (1).