1.4 Acceleration of Instruction Processing Time

High-speed instruction

In some instructions, when the device and label specified in each operand satisfy the specific condition, the instruction processing time is accelerated.
Such accelerated instructions are called high-speed instructions.

The instructions capable of accelerating and the conditions of acceleration

The table below shows the instructions capable of accelerating and the conditions of acceleration (conditions of non-acceleration).

Classification	Instruction symbol	Conditions of non-acceleration
Contact instruction	LD, LDI, AND, ANI, OR, ORI, LDP, LDF, ANDP, ANDF, ORP, ORF, LDPI, LDFI, ANDPI, ANDFI, ORPI, ORFI	• When indexing is executed • When link register (W) is specified, the number of points of file register (R) + the number of link register (W) > 32767 • When link special register (SW) is specified, the number of points of file register (R) + the number of points of link register (W) + the number of link special register (SW) > 32767 • When module access device (Un\Gn) is specified • When direct access input (DX) is specified • When direct access output (DY) is specified • In OUT, SET, RST instructions, annunciator (F) or step relay (S) is specified in the operand • In OUT T instruction, routine timer is specified in the operand • In OUT T, OUT ST, OUTH T, OUTH ST, OUTHS T, OUTHS ST, OUT C instructions, a data other than constant is specified in the second operand • In OUT T, OUT ST instructions, K0 is specified in the second operand • In RST instruction, a data other than the bit type is specified in the operand
Association instruction	ANB, ORB, MPS, MRD, MPP, INV, MEP, MEF	
Output instruction	OUT, OUT T, OUTH T, OUTHS T, OUT ST, OUTH ST, OUTHS ST, OUT C, SET, RST, ALT	
Shift instruction	SFR, SFL	
Comparison operation instruction	LD=, AND=, OR=, LD=_U, AND=_U, OR=_U, LD<>, AND<>, OR<>, LD<>_U, AND<>_U, OR<>_U, LD>, AND>, OR>, LD>_U, AND>_U, OR>_U, LD<=, AND<=, OR<=, LD<=_U, AND<=_U, OR<=_U, LD<, AND<, OR<, LD<_U, AND<_U, OR<_U, LD>=, AND>=, OR>=, LD>=_U, AND>=_U, OR>=_U, LDD=, ANDD=, ORD=, LDD=_U, ANDD=_U, ORD=_U, LDD<>, ANDD<>, ORD<>, LDD<>_U, ANDD<>_U, ORD<>_U, LDD>, ANDD>, ORD>, LDD>_U, ANDD>_U, ORD>_U, LDD<=, ANDD<=, ORD<=, LDD<=_U, ANDD<=_U, ORD<=_U, LDD<, ANDD<, ORD<, LDD<_U, ANDD<_U, ORD<_U, LDD>=, ANDD>=, ORD>=, LDD>=_U, ANDD>=_U, ORD>=_U	• When indexing is executed • When link register (W) is specified, the number of points of file register (R) + the number of link register (W) > 32767 • When link special register (SW) is specified, the number of points of file register (R) + the number of points of link register (W) + the number of link special register (SW) > 32767 • When module access device (Un\Gn) is specified • When the indirect specification is used • When specifying the nibble of a device, the number of digits is other than K4 or K8 • When specifying the nibble of a device, the head device number is other than a multiple of 8 (Example) K4M8: Acceleration available, K4M9: Acceleration not available • When specifying the nibble of a label[*1]

Classification	Instruction symbol	Conditions of non-acceleration
Arithmetic operation instruction	+ (2 operands), +_U (2 operands), + (3 operands), +_U (3 operands), - (2 operands), -_U (2 operands), - (3 operands), -_U (3 operands), D+ (2 operands), D+_U (2 operands), D+ (3 operands), D+_U (3 operands), D- (2 operands), D-_U (2 operands), D- (3 operands), D-_U (3 operands), *, *_U, INC, INC_U, DEC, DEC_U, DINC, DINC_U, DDEC, DDEC_U	• When indexing is executed • When link register (W) is specified, the number of points of file register (R) + the number of link register (W) > 32767 • When link special register (SW) is specified, the number of points of file register (R) + the number of points of link register (W) + the number of link special register (SW) > 32767 • When module access device (Un\Gn) is specified • When the indirect specification is used • When specifying the nibble of a device, the number of digits is other than K4 or K8 • When specifying the nibble of a device, the head device number is other than a multiple of 8 (Example) K4M8: Acceleration available, K4M9: Acceleration not available • When specifying the nibble of a label*1 • When specifying timer (T), retentive timer (ST), counter (C), long counter (LC), timer type label, retentive timer type label, counter type label, and long counter type label in the operand with the data type of word/double word
Logical operation instruction	WAND (2 operands), WAND (3 operands), DAND (2 operands), DAND (3 operands), WOR (2 operands), WOR (3 operands), DOR (2 operands), DOR (3 operands), WXOR (2 operands), WXOR (3 operands), DXOR (2 operands), DXOR (3 operands), WXNR (2 operands), WXNR (3 operands), DXNR (2 operands), DXNR (3 operands)	
Bit processing instruction	BSET, BRST, TEST, DTEST	
Data conversion instruction	INT2UINT, INT2UDINT, INT2DINT, UINT2INT, UINT2DINT, UINT2UDINT, DINT2INT, DINT2UINT, DINT2UDINT, UDINT2INT, UDINT2DINT, UDINT2UINT	
Real number instruction	INT2FLT, DINT2FLT, UINT2FLT, UDINT2FLT, EMOV, DEMOV	

*1 When specifying the nibble of a label, some instructions are accelerated depending on the assignment position of the label. However, because the assignment position of label cannot be checked and changed, check the actual operation.

Execution time of high-speed instruction

For execution time of high-speed instruction, refer to the following.

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