8.3 Program Execution Control Instruction
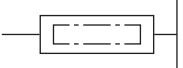
Disabling/enabling interrupt programs
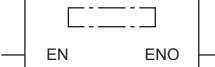
DI, EI

`FX5S` `FX5UJ` `FX5U` `FX5UC`

Interrupts are usually disabled in CPU module. These instructions enable interrupts in CPU module (EI instruction) or disable interrupts again (DI instruction).

- DI: Disables the execution of the interrupt program.
- EI: Releases the execution disabled state of interrupt programs.

| Ladder diagram	Structured text
──[:─:]──	ENO:=DI(EN); ENO:=EI(EN);

FBD/LD
[:─:] EN   ENO

Processing details
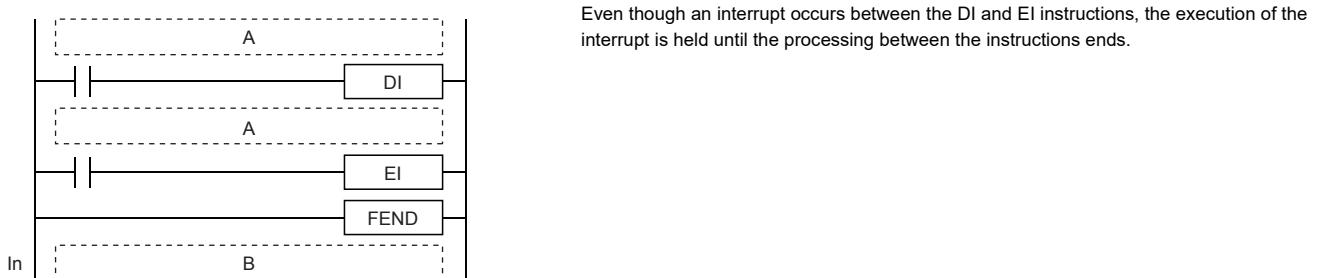
■DI

- This instruction disables the execution of the interrupt program until the EI instruction is executed, even if the interrupt cause occurs.
- When the power is turned on or the CPU module is reset, the state in which the DI instruction is executed is applied.
- For the operation of the DI instruction (DI instruction without an argument) when using the interrupt disable instruction with a specified priority or lower (DI instruction with an argument), refer to ☞Page 443 Disabling the interrupt program with specified priority or lower.
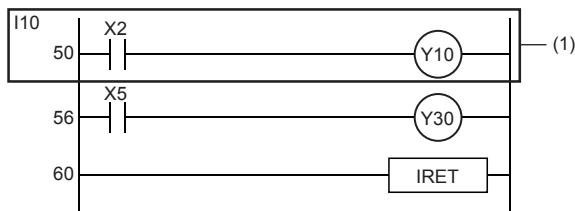
■EI

- This instruction releases the execution disabled state of interrupt programs when the DI instruction is executed, and enables the execution of the interrupt program with the interrupt pointer number enabled by the IMASK instruction.
- For the operation of the EI instruction when using the interrupt disable instruction with a specified priority or lower (DI instruction with an argument), refer to ☞Page 443 Disabling the interrupt program with specified priority or lower.

Even though an interrupt occurs between the DI and EI instructions, the execution of the interrupt is held until the processing between the instructions ends.

A: Sequence program
B: Interrupt Program

- An interrupt pointer occupies two steps. (In (1) below, I10 is the step 50, X2 is the step 52, and Y10 is the step 54.)

```
I10    X2
  50  ─┤├──────────────────────( Y10 )──── (1)
       X5
  56  ─┤├──────────────────────( Y30 )
  60  ──────────────────────────[ IRET ]
```

- If the master control contains the EI or DI instruction, such an instruction is executed regardless of the execution of the MC instruction.

Precautions

Interrupts (requests) that are generated after the DI instruction execution, are processed after the EI instruction is executed.

Operation error

Error code (SD0/SD8067)	Description
3362H	Nesting of the DI instruction exceeds 16 levels.