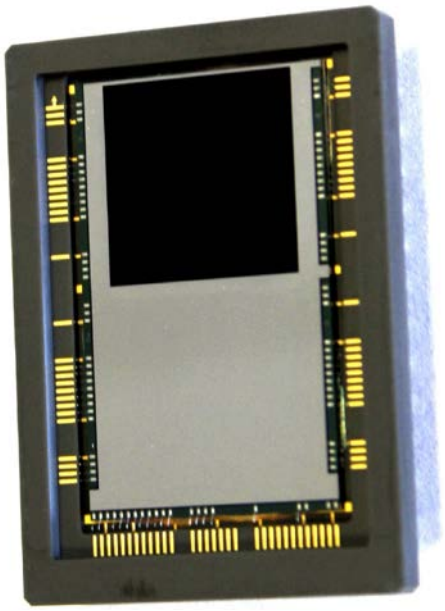
CCD201-20
Back-illuminated 2-Phase IMO Series Electron-multiplying CCD Sensor

FEATURES

- Nominally 1024 x 1024 pixels each 13 µm square
- Frame transfer operation
- Two-phase Inverted Mode Operation
- Multiplication gain
- Back-illuminated
- Low-noise output circuits



INTRODUCTION

The CCD201 is a 1024 x 1024 pixel frame-transfer sensor in the e2v L3Vision™ range of products. This device uses a novel output arrangement that is capable of operating at an equivalent output noise of less than one electron at pixel rates of over 15 MHz. This makes the sensor well suited for scientific imaging where the illumination is limited.

The sensor functions by converting photons to charge in the image area during the integration time, then transferring this charge as a frame through the image to the store section, and finally line-by-line transfer into the read-out register. Each line of charges is transferred through the read-out register and then through a second register in which multiplication gain occurs before conversion to a voltage by an output amplifier. Read-out is also possible without using the gain register.

The image and store sections utilise two-phase clocking to provide both fastest possible frame transfer and inverted-mode operation to minimise the dark current, which can be the dominant source of noise. The register is three-phase, and there are two extra phases for the gain register – RØDC and RØ2HV. Control of the gain is achieved by adjusting the high level of RØ2HV.

The sensor has two output amplifiers available; a large signal type (LS) for when multiplication gain is employed and a low noise, high responsivity type (HR) for normal CCD operation.

The basic device type is back-illuminated with a mid-band antireflection coating. Other coatings are available, please contact e2v for details.

GENERAL DATA

Format

Image area	13.3 x 13.3 mm
Active pixels	1024 (H) x 1024 (V) (usable)
Pixel size	13 x 13 µm
Storage area	13.3 x 13.3 mm
Number of output amplifiers	2
Fill factor	100%
Additional dark reference columns	16 +16
Additional over scan rows	6 + 2

Package (ceramic)

Package size	37.4 x 26.5 mm
Number of pins	36
Inter-pin spacing	2.54 mm

The pin 1 marker is shown in Fig. 15.

ORDERING INFORMATION

Part number CCD201-20-G-XYZ

Where G is the grade and XYZ is the build type.

e.g. XYZ = 122 for a basic type with the mid-band coating.

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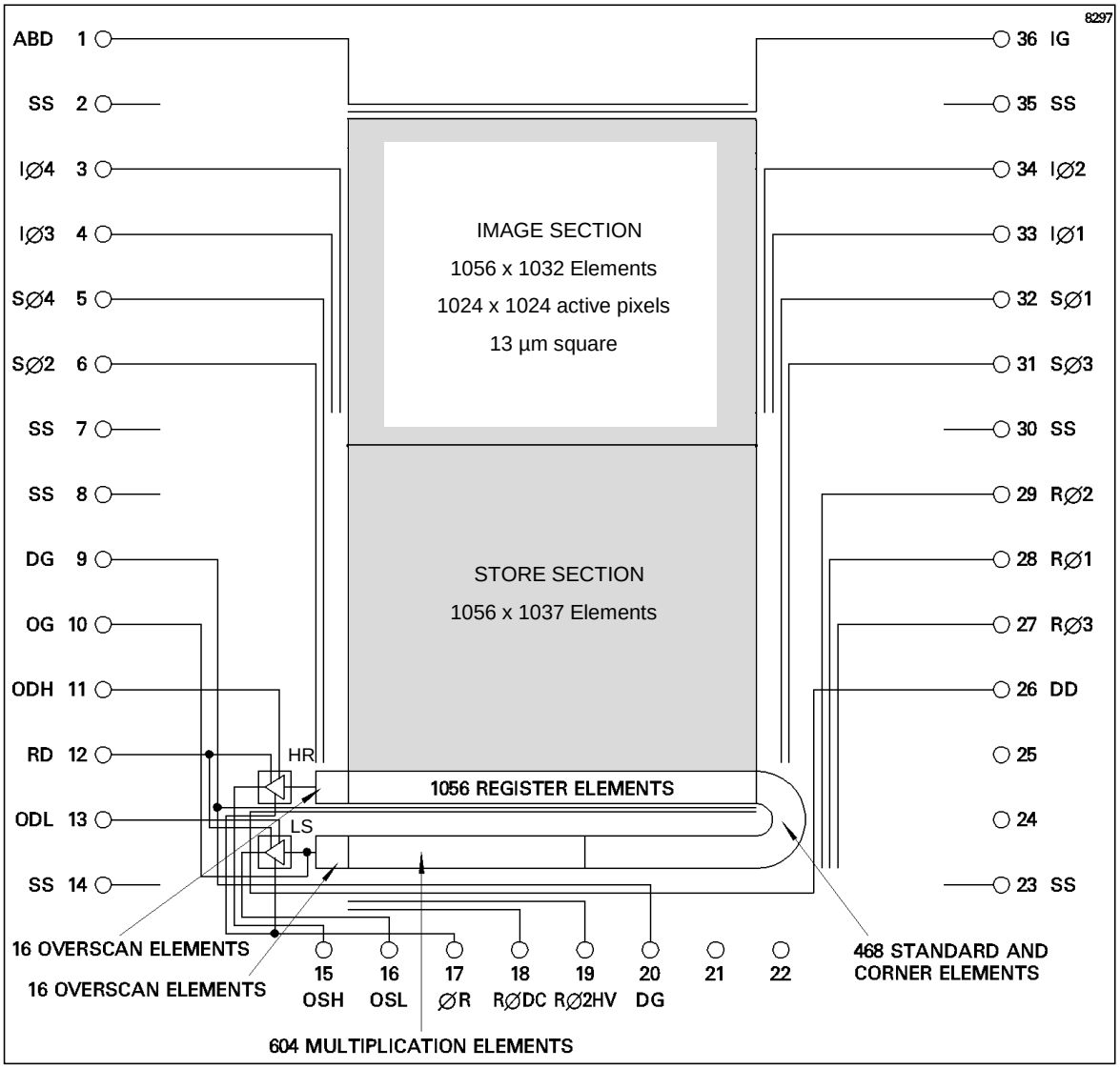
Template: DF764388A-5
CR 118818

Figure 1: SCHEMATIC CHIP DIAGRAM



The device comprises an image section with a total number of elements 1056(H) x 1032(V), each 13 µm square. Optical shielding is used to provide nominally 1024(H) x 1024(V) active pixels. There are nominally 16 shielded columns on either side of the image section, 6 shielded rows at the top and 2 shielded rows at the bottom. These may be used for overscan or dark reference purposes. Note, however, that the rows and colums immediately adjacent to the active image area may be only partially shielded, i.e. transition elements, and should not be used for reference purposes. The optically-shielded store section has a total of 1056(H) x 1037(V) elements.

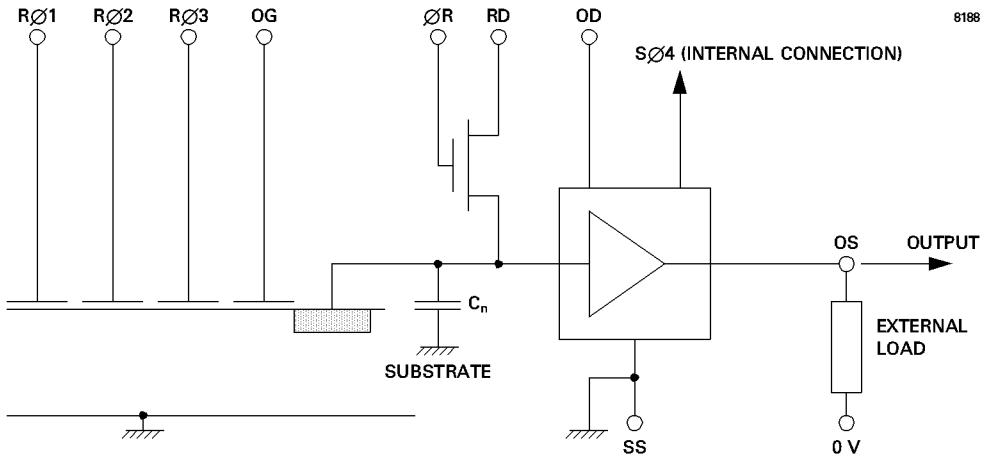
The electrodes of the image and store sections are configured for four-phase clocking, but adjacent phases need to be joined off chip to run in two phase operation.

Below the store section is a standard three-phase read-out register with 1056 elements. Charge signals can be transferred to the left for output via 16 additional overscan elements to a high-responsivity low-noise amplifier HR. Alternatively charges can be transferred to the right through 468 standard elements, 604 multiplication elements and 16 overscan elements to reach a large signal amplifier LS. The multiplication register requires two extra drive phases, RØDC and RØ2HV. With transfer either to the left or right, a total of 1072 clock cycles is required to read out a line, but with the signals going through the gain register being subject to a one line delay.

There is a dump drain DD below the 1056 register elements adjacent to the store section with the charge dumping operation controlled by the dump gate DG.

Details of the package are given later.

Figure 2: OUTPUT CIRCUIT SCHEMATIC (HR and LS Amplifiers)



The amplifiers have a DC restoration circuit that is internally activated whenever S∅4 is high.

Nominal design features are as follows.

Feature	HR	LS
Output	OSH (pin 15)	OSL (pin 16)
Responsivity µV/e-	5.3 µV/e^-	1.4 µV/e^-
External load	5 kΩ or 5 mA	3.3 kΩ or 7.5 mA
Output impedance	400 Ω	350 Ω
On-chip dissipation	30 mW	50 mW

ELECTRICAL INTERFACE CHARACTERISTICS

Electrode capacitances at mid-clock level					Series Resistance	
Connection	**To SS**	**Inter-Phase**	**Total**	**Units**		**Units**
IØ1 + IØ2	7.8	4.8	12.6	nF	8	Ω
IØ3 + IØ4	7.8	4.8	12.6	nF	8	Ω
SØ1 + SØ2	7.8	4.8	12.6	nF	8	Ω
SØ3 + SØ4	7.8	4.8	12.6	nF	8	Ω
RØ1	68	98	166	pF	6	Ω
RØ2	56	68	124	pF	6	Ω
RØ3	89	74	163	pF	6	Ω
RØ2HV	15	18	33	pF	8	Ω

TYPICAL PERFORMANCE SPECIFICATIONS

Except where otherwise specified, the following are measured for operation at a pixel rate of 15 MHz, with typical operating voltages. Parameters are given at 223 K unless specified otherwise. Where parameters are different in the normal and high gain mode, both are given.

PARAMETER	UNIT	MIN	TYPICAL	MAX
Output amplifier responsivity, HR amplifier (normal mode) (see note 1)	$\mu V/e^-$	-	5.3	-
Output amplifier responsivity, LS amplifier (normal mode) (see note 1)	$\mu V/e^-$	-	1.4	-
Multiplication register gain, LS amplifier (high gain mode) (see notes 2, 3 and 4)		1	-	1000
Peak signal - 2-phase IMO	e^-/pixel	65k	80k	-
Charge handling capacity of multiplication register (see notes 5 and 6)	e^-/pixel	-	730k	-
Charge handling capacity of HR amplifier (see note 6)	e^-	-	280k	-
Charge handling capacity of LS amplifier (see note 6)	e^-	-	1M	-
Read-out noise at 50 kHz with CDS, HR amplifier (normal mode) (see note 6)	e^- rms	-	3.1	-
Read-out noise at 1 MHz with CDS, HR amplifier (normal mode) (see note 6)	e^- rms	-	6.0	-
Amplifier reset noise (without CDS), HR amplifier (normal mode) (see note 6)	e^- rms	-	50	-
Read-out noise at 15 MHz with CDS, LS amplifier (normal mode) (see note 6)	e^- rms	-	43	-
Amplifier reset noise (without CDS), LS amplifier (normal mode) (see note 6)	e^- rms	-	100	1
Readout noise at 1 MHz (high gain mode) (see note 6)	e^- rms	-	<1	-
Maximum frequency (settling to 1%), HR amplifier (see notes 6 and 7)	MHz	-	-	3
Maximum frequency (settling to 5%), HR amplifier (see notes 6 and 7)	MHz	-	-	4.5
Maximum frequency (settling to 1%), LS amplifier (see notes 6 and 7)	MHz	-	-	13
Maximum frequency (settling to 5%), LS amplifier (see notes 6 and 7)	MHz	-	-	20
Maximum parallel transfer frequency (see notes 1 and 6)	MHz	-	0.9	-
Dark signal at 293 K (see notes 8 and 9)	e^-/pixel/s	-	260	530
Dark signal non-uniformity (DSNU) at 293 K (see notes 6 and 10)	e^-/pixel/s	-	90	-
Excess noise factor (see note 11)		-	$\sqrt{2}$	-

NOTES

1. Measured at a pixel rate of 1 MHz.
2. The typical variation of gain with R∅2HV is shown in Fig. 3.
3. The variation of gain with R∅2HV at different temperatures is shown in Fig. 3.
4. Some increase of R∅2HV may be required throughout life to maintain gain performance. Adjustment of R∅2HV should be limited to the maximum specified under Operating Conditions.
5. When multiplication gain is used and clock timings optimised, a linear response of output signal with input signal of better than 3% is achieved for output signals up to 400 ke^- typically.
6. These values are inferred by design and not measured.
7. The quoted maximum frequencies assume a 20 pF load and that correlated double sampling is being implemented.
8. The quoted dark signal has the usual temperature dependence for inverted mode operation. For operation at high frame rates with short integration times, there will also be a component generated during read-out through the register. Operating at a temperature of 293 K and 10 Hz frame rate, the read-out component contributes 5.8 e^-/pixel/frame typically, at a gain of 1000 and referenced to the image area, and has a temperature dependence consistent with non-inverted mode operation.

   There exists a further weakly temperature dependent component, the clock induced charge, which is independent of the integration time. The clock induced charge is dependent on the operating biases and timings employed and is typically 0.2 e^-/pixel/frame at T = –55 °C.

   For more information, refer to the technical note "Dark Signal and Clock-Induced Charge in L3Vision™ CCD Sensors".
9. For fringe suppression variants, the dark signal will be higher (typical 600, maximum 900).
10. DSNU is defined as the 1σ variation of the dark signal.
11. The excess noise factor is defined as the factor by which the multiplication process increases the shot noise on the image when multiplication gain is used.

Figure 3: TYPICAL VARIATION OF MULTIPLICATION GAIN WITH RØ2HV AT DIFFERENT TEMPERATURES

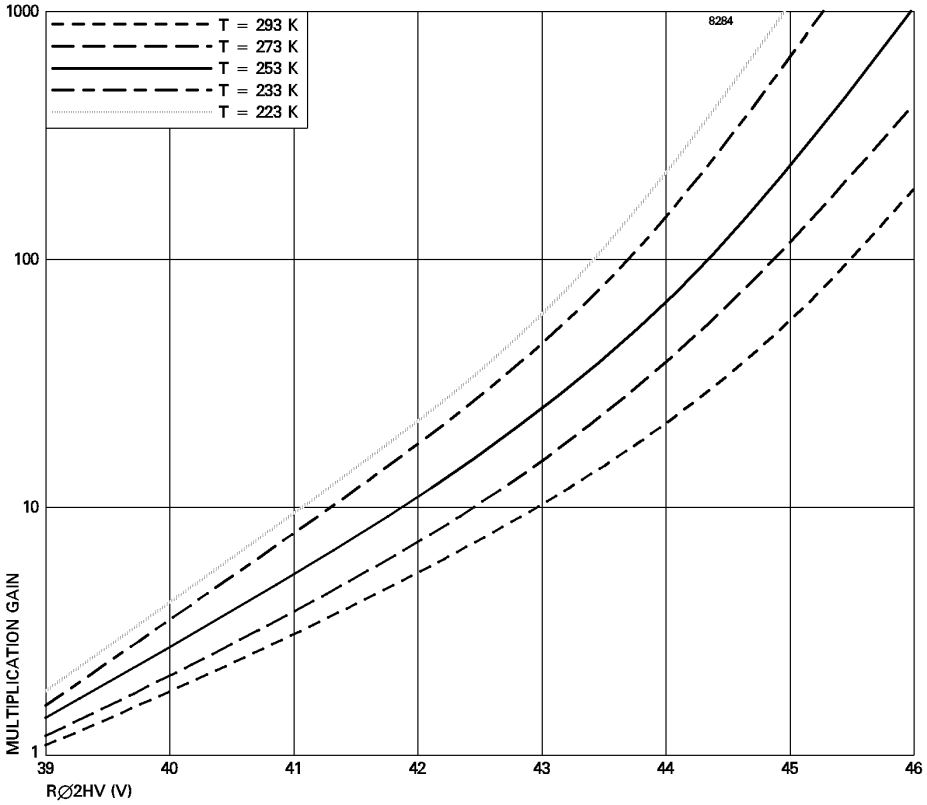


Figure 4: TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE

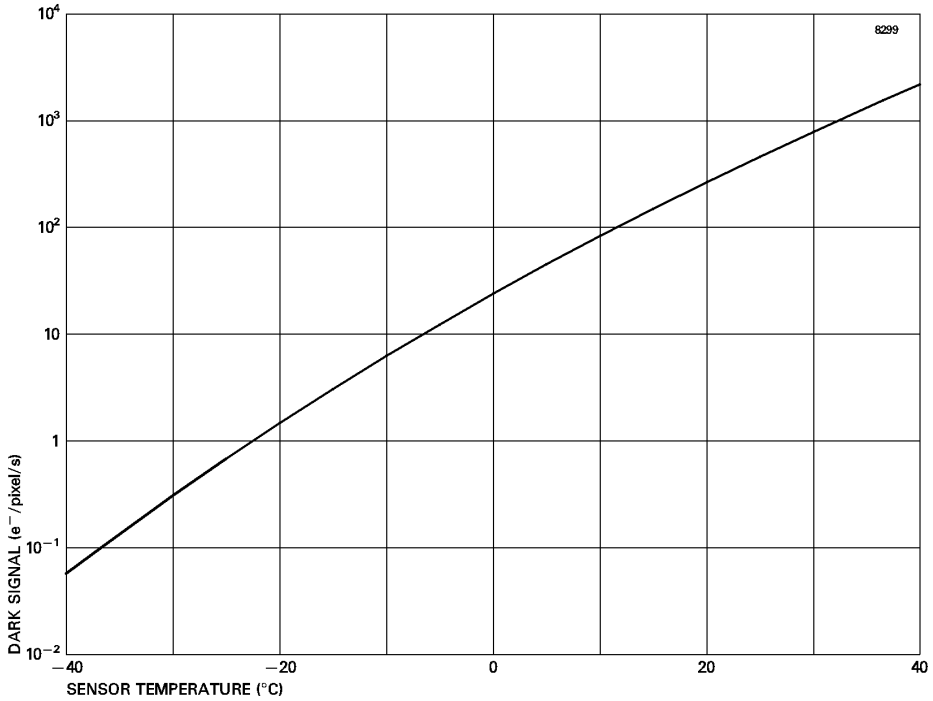
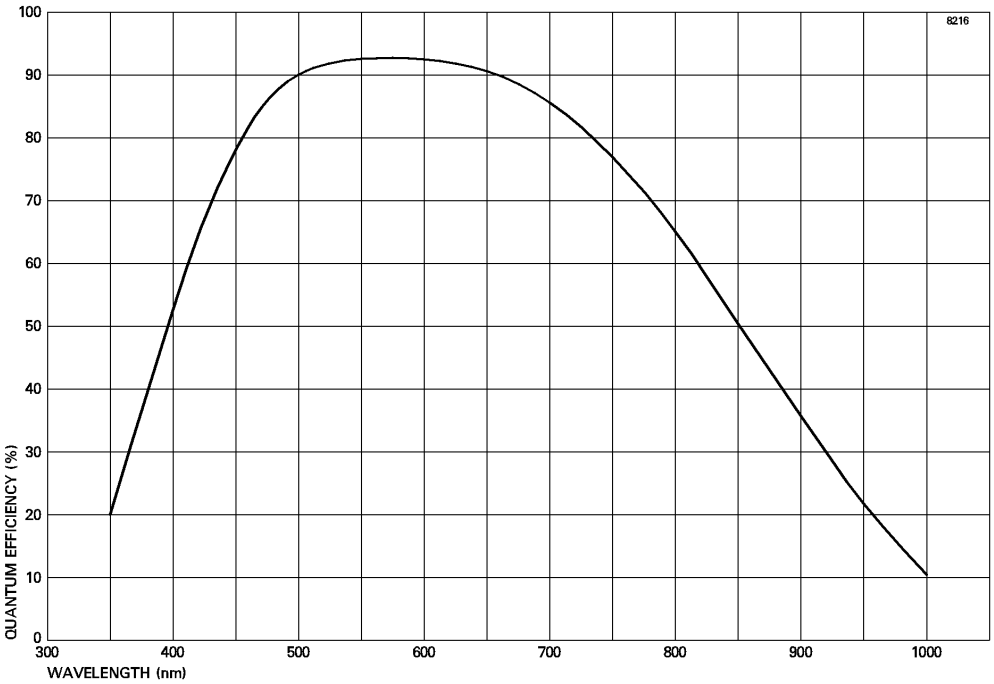


Figure 5: TYPICAL SPECTRAL RESPONSE (At –20 °C, no window, midband coating)



Devices can be supplied with an alternative anti-reflection coating that peaks at a different wavelength – details from e2v.

ESD HANDLING PROCEDURES

CCD sensors, in common with most high performance IC devices, are static sensitive. In certain cases a static electricity discharge may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench.
- Operator wearing a grounded wrist strap.
- All receiving socket pins to be positively grounded.
- Unattended CCDs should not be left out of their conducting foam or socket.

All devices are provided with internal protection circuits to most gate electrodes but not to the other pins.

Evidence of incorrect handling will terminate the warranty.

EXPOSURE TO RADIATION

Exposure to radiation may irreversibly damage the device and result in degradation of performance. Users wishing to operate the device in a radiation environment are advised to consult e2v technologies.

ABSOLUTE MAXIMUM RATINGS

Maximum ratings are with respect to SS.

PIN	CONNECTION	DESCRIPTION	MIN (V)	MAX (V)
1	ABD	Anti-Blooming Drain (see note 12)	–0.3	+25
2	SS	Substrate	0	
3	IØ4	Image Clock 4	–20	+20
4	IØ3	Image Clock 3	–20	+20
5	SØ4	Store Clock 4	–20	+20
6	SØ2	Store Clock 2	–20	+20
7	SS	Substrate	0	
8	SS	Substrate	0	
9	DG	Dump Gate	–20	+20
10	OG	Output Gate	–20	+20
11	ODH	Output Drain (HR Amplifier)	–0.3	+32
12	RD	Reset Drain	–0.3	+25
13	ODL	Output Drain (LS Amplifier)	–0.3	+32
14	SS	Substrate	0	
15	OSH	Output Source (HR Amplifier) (see note 13)	–0.3	+25
16	OSL	Output Source (LS Amplifier) (see note 13)	–0.3	+25
17	∅R	Reset Pulse	–20	+20
18	R∅DC	Multiplication Register DC Bias	–20	+20
19	R∅2HV	Multiplication Register Clock (see note 14)	–20	+50
20	DG	Dump Gate	–20	+20
21	n.c.	Not Connected		
22	n.c.	Not Connected		
23	SS	Substrate	0	
24	n.c.	Not Connected		
25	n.c.	Not Connected		
26	DD	Dump Drain	–0.3	+25
27	RØ3	Register Clock 3	–20	+20
28	RØ1	Register Clock 1	–20	+20
29	RØ2	Register Clock 2	–20	+20
30	SS	Substrate	0	
31	SØ3	Store Clock 3	–20	+20
32	SØ1	Store Clock 1	–20	+20
33	IØ1	Image Clock 1	–20	+20
34	IØ2	Image Clock 2	–20	+20
35	SS	Substrate	0	
36	IG	Isolation Gate	–20	+20

NOTES

12. Anti-blooming is not available on this device type. However, ABD is used for connection purposes and must be biased as specified.

13. Permanent damage may result if, in operation, OSL or OSH experiences short-circuit conditions.

    An external load is required for each output amplifier as shown in figure 2. For the HR amplifier, this can be a resistor of about 5 kΩ or a constant current type of about 5 mA. For the LS amplifier, the load should be either 3.3 kΩ or 7.5 mA. The on-chip amplifier power dissipation is approximately 30 mW for the HR amplifier and 50 mW for the LS amplifier.

14. The RØ2HV connection has no anti-static gate protection device incorporated. Extreme care must be used with handling.

Maximum Voltages between Pairs of Pins

PIN	CONNECTION	PIN	CONNECTION	MIN (V)	MAX (V)
15	OSH	11	ODH	–15	+15
16	OSL	13	ODL	–15	+15
19	RØ2HV	18	RØDC	–20	+50
19	RØ2HV	27	RØ3	–20	+50
Output Transistor Current (mA)					20

OPERATING CONDITIONS

Typical operating voltages are as given in the table below. Some adjustment within the minimum-maximum range specified may be required to optimise performance.

CONNECTION	PULSE AMPLITUDE OR DC LEVEL (V)		
	Min	Typical	Max
IØ1, 2, 3, 4 high (see note 15)	+5	+7	+9
IØ1, 2, 3, 4 low (see note 15)	–6	–5	–4
SØ1, 2, 3, 4 high (see note 15)	+5	+7	+9
SØ1, 2, 3, 4 low (see note 15)	–6	–5	–4
RØ1, 2, 3 high	+8	+12	+13
RØ1, 2, 3 low	-	0	-
RØ2HV high (see note 2)	+20	+40	+50
RØ2HV low	0	+4	+5
ØR high (see notes 16,17)		+10	
ØR low	-	0	-
RØDC	+2	+3	+5
OG (see note 17)	+1	+3	+5
IG	-	–5	-
SS (see note 18)	0	+4.5	+7
ODL, ODH	+25	+28	+32
RD (see note 17)	+15	+17	+20
ABD	+10	+18	+20
DG low	-	0	-
DG high	+10	+12	+13
DD	+20	+24	+25

NOTES

15. I∅ and S∅ adjustment may be common. The high level may need to be adjusted to achieve correct charge transfer and the low level may need to be separately adjusted to achieve correct inverted mode operation that is uniform across the array.
16. The ∅R high level may be adjusted in common with R∅1, 2, 3.
17. The two amplifiers have common connections between the reset gates (∅R), reset drains (RD) and output gates (OG).
18. The SS voltage may also need to be adjusted to achieve correct inverted-mode operation.
19. An external load is required for each output amplifier. For the HR amplifier, this can be a resistor of about 5 kΩ or a constant current type of about 5 mA. For the LS amplifier, the load should be either 3.3 kΩ or 7.5 mA. The quiescent voltage level on OS is then typically 7V more positive than the voltage used for RD.

DRIVE PULSE WAVEFORM SPECIFICATION

The device is of a 4-phase construction, designed to operate in 2-phase inverted mode. This is achieved by applying common timings to phases ∅1 and ∅2, and phases ∅3 and ∅4 of the image and store sections. The read-out register is basically three-phase. Suggested timing diagrams are shown in Figs. 6 -- 14.

The following are suggested pulse rise and fall times.

Symbol	Description	Min	Typ (see note 20)	Max	Units
T_i	Line transfer time during FT (see note 20)	$2[t_{wi} - t_{oi}]$	1.5	(see note 21)	µs
t_{wi}	Image/store clock pulse width	$3t_{oi}$	1	(see note 21)	µs
t_{oi}	Image/store clock pulse edge overlap	200	250	(see note 21)	ns
t_{ri}	Image/store clock pulse rise time (10 - 90%)		50	$0.3\ t_{oi}$	ns
t_{fi}	Image/store clock pulse fall time (10 - 90%)		50	$0.3\ t_{oi}$	ns
t_{D1}	Image/store clock delay time at start of FT	20	40	(see note 21)	µs
t_{D2}	Delay time, RØ stop to SØ rising	0.1	1	(see note 21)	µs
t_{D3}	Delay time, SØ falling to RØ start	0.3	1	(see note 21)	µs
t_{D4}	Delay time, RØ falling to DG falling	5	20	(see note 21)	µs
t_{D5}	Delay time, DG falling to RØ rising	5	20	(see note 21)	µs
T_{rr}	Register clock period (see note 20)		67	(see note 21)	ns
t_{w1}	Register pulse width, RØ1 (at 50% levels)		$T_{rr}/2$	(see note 21)	
t_{w2}	Register pulse width, RØ2 (at 50% levels)		$T_{rr}/4$	(see note 21)	
t_{w3}	Register pulse width, RØ3 (at 50% levels)		$T_{rr}/4$	(see note 21)	
t_{rr}	Register clock pulse rise time (10 - 90%)	5	10	$T_{rr}/5$	ns
T_{fr}	Register clock pulse fall time (10 - 90%)	5	10	$T_{rr}/5$	ns
t_{or}	Register clock pulse edge overlap (50% levels)	5	10	$T_{rr}/5$	ns
t_{wx}	Reset pulse width (at 50% levels)	10	15	$T_{rr}/4$	ns
t_{rx}	Reset pulse rise time (10 - 90%)	2	5	$T_{rr}/10$	ns
t_{fx}	Reset pulse fall time (10 - 90%)	2	5	$T_{rr}/10$	ns
t_{Dx}	Delay time, ØR falling to RØ2 falling (at 50% levels)	0	5	$t_{w2} - t_{wx}$	ns

NOTES

20. As used for device testing at 15 MHz readout rate.

21. No maximum other than set by system constraints.

22. Total line transfer time for line readout = $t_{D2} + 2t_{wi} - t_{oi} + t_{D3}$

Figure 6: FRAME-TRANSFER SEQUENCE (THROUGH GAIN REGISTER)

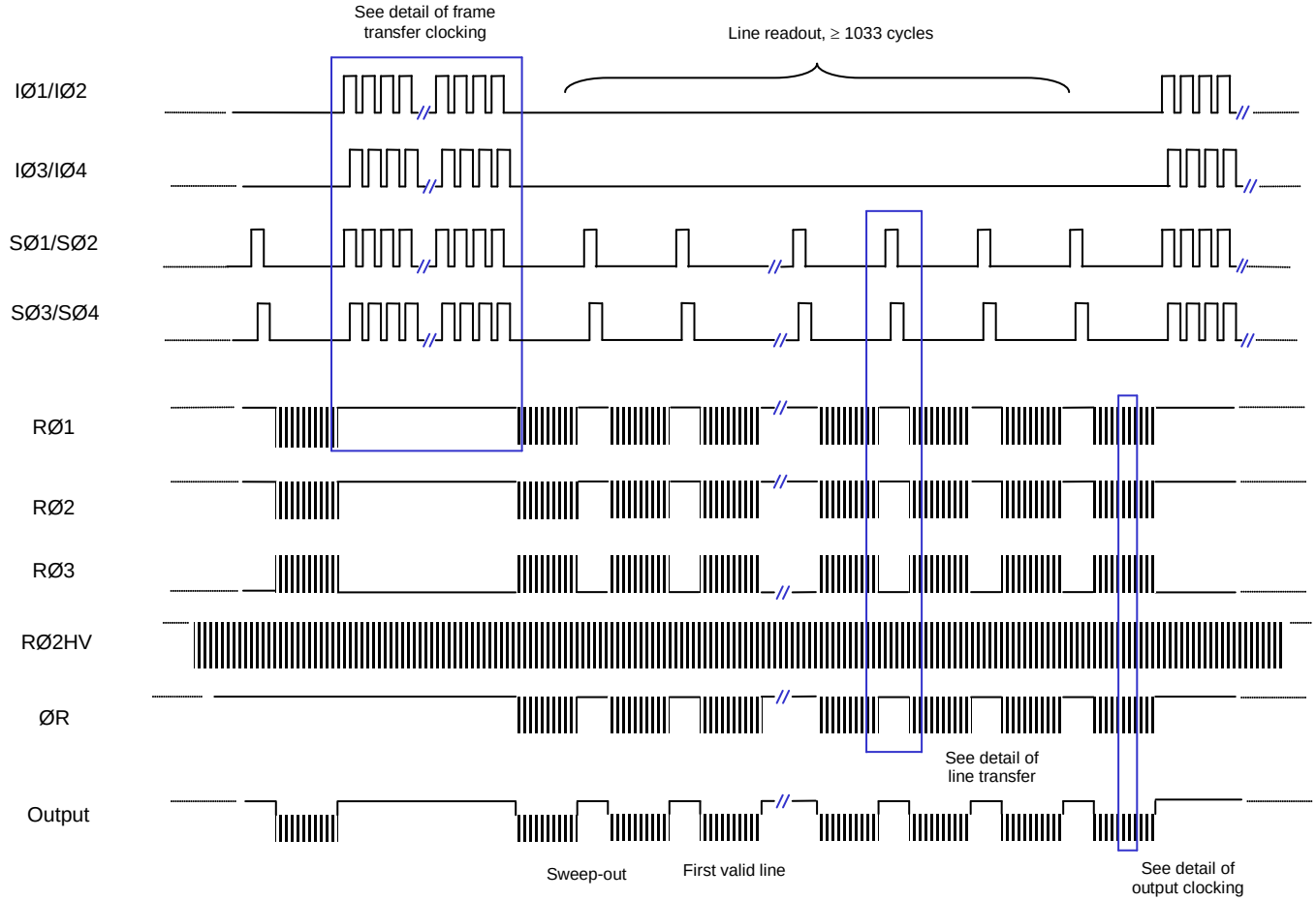


Figure 7: DETAIL OF FRAME-TRANSFER CLOCKING

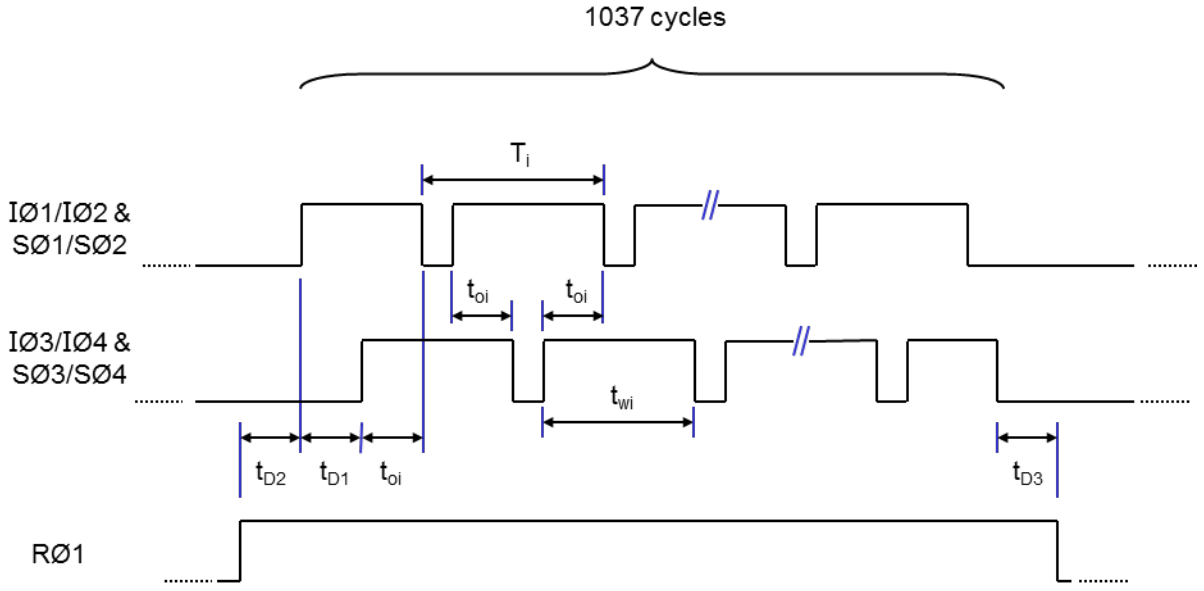


Figure 8: DETAIL OF LINE TRANSFER CLOCKING

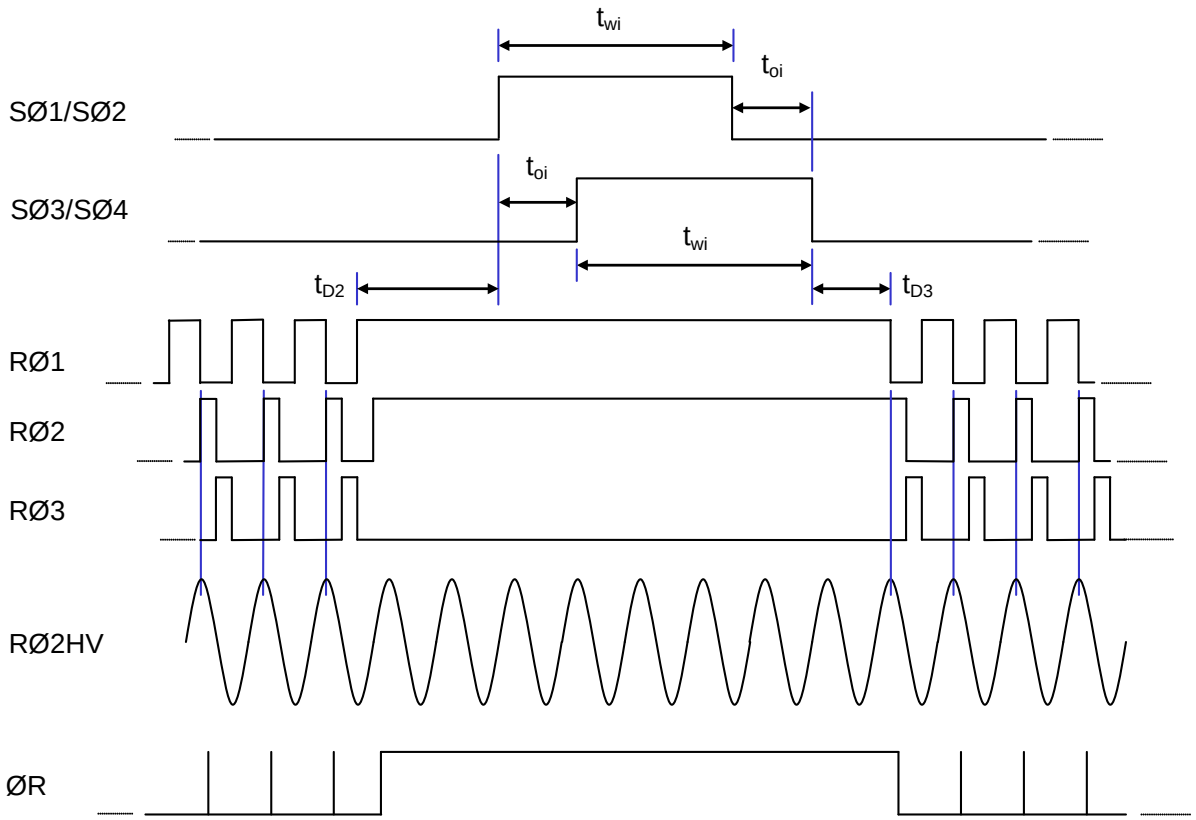
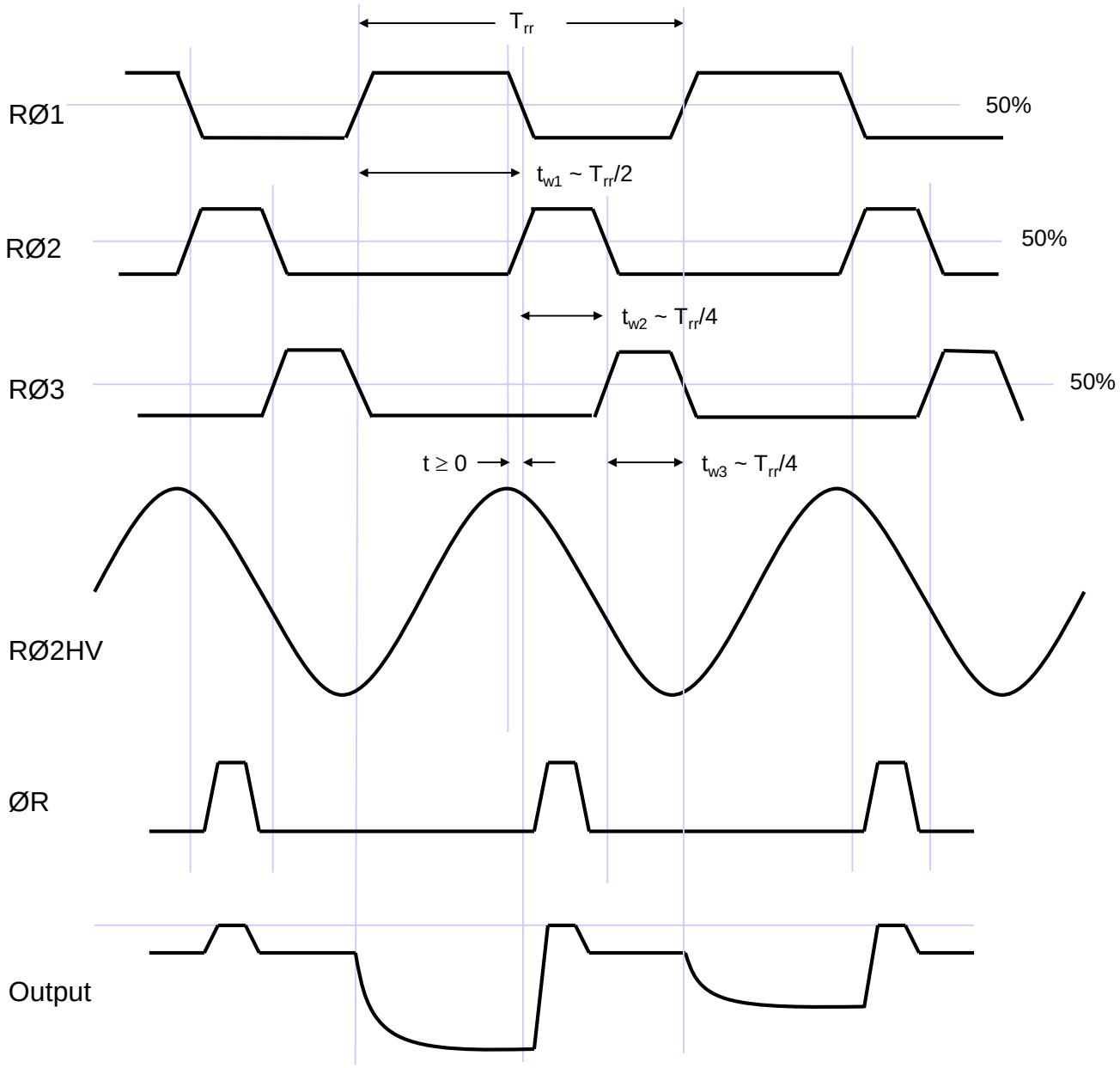


Figure 9: SIGNAL READ-OUT – GENERAL TIMING ARRANGEMENT



NOTES

23. RØ2HV can also be of a trapezoidal pulse shape, as shown in Figure 10 below.
24. The RØ2HV pulse should reach full amplitude before RØ1 starts to fall.
25. The edge times are not critical and could be ~5% of the read-out period.

Figure 10: SIGNAL OUTPUT – ALTERNATIVE TIMING WITH TRAPEZOIDAL RØ2HV

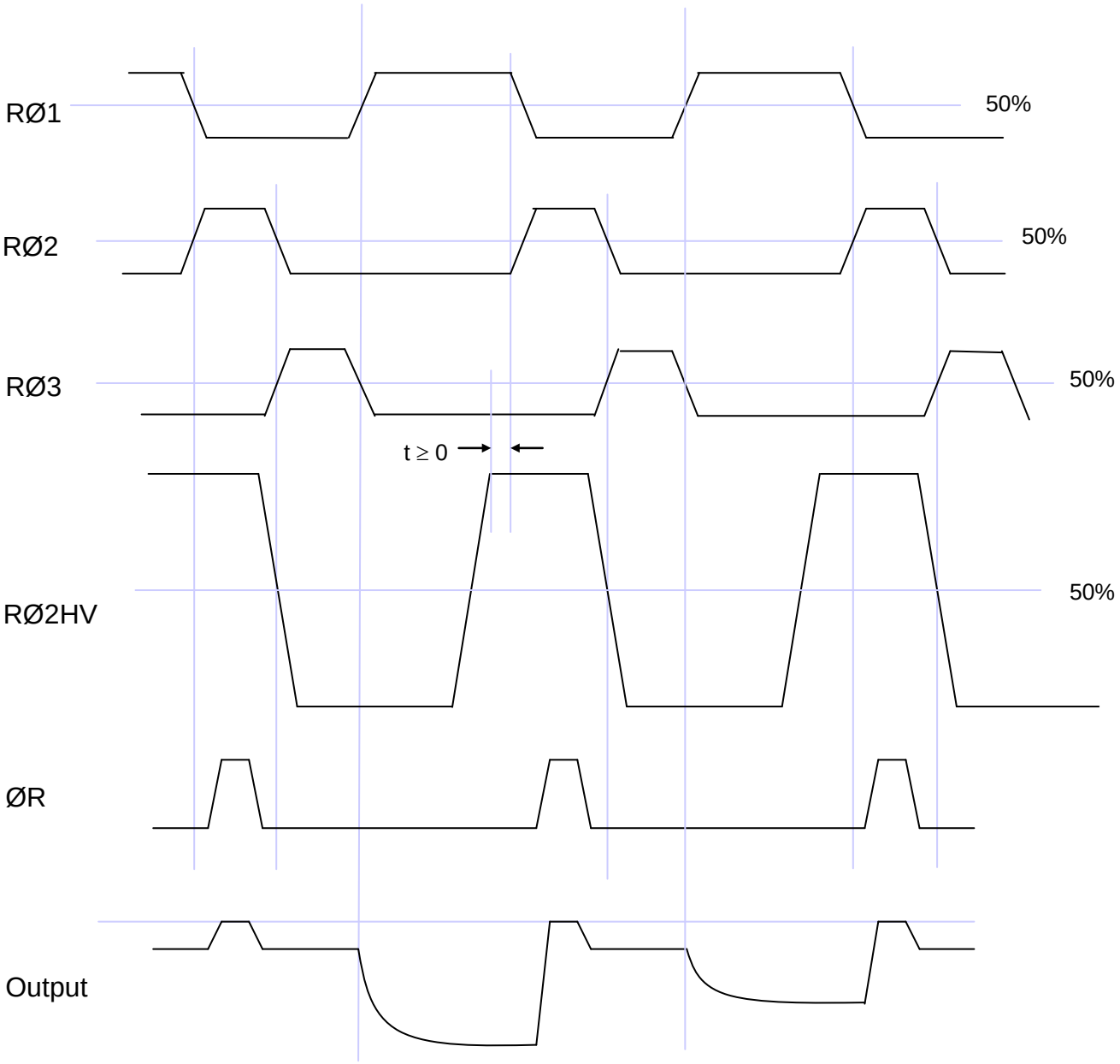
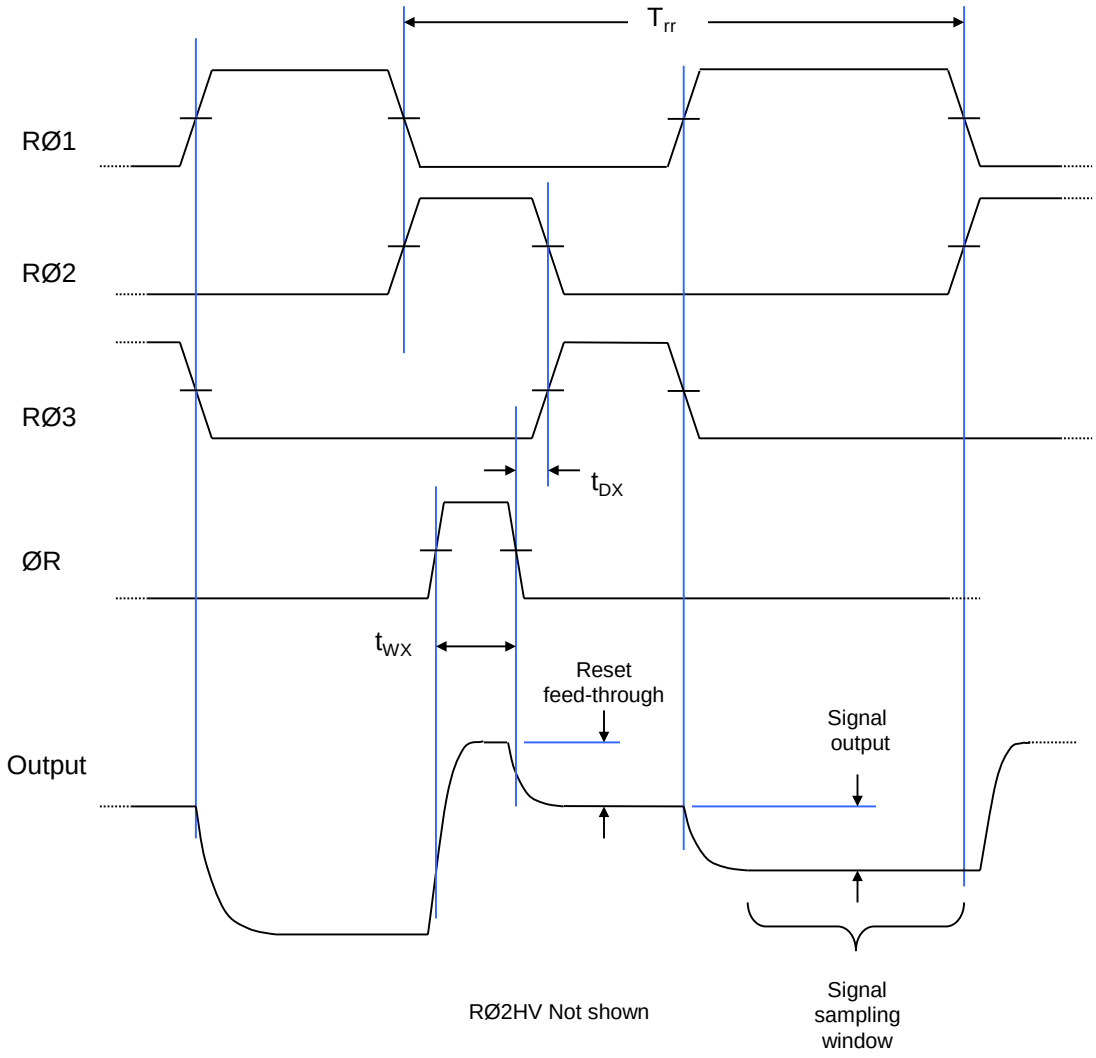


Figure 11: GENERAL RESET TIMING



NOTE

26. To operate through the OSH output amplifier, the R∅1 and R∅2 waveforms should be interchanged and RØ2HV can be held at 0V.

Figure 12: LINE OUTPUT FORMAT (OSH amplifier)

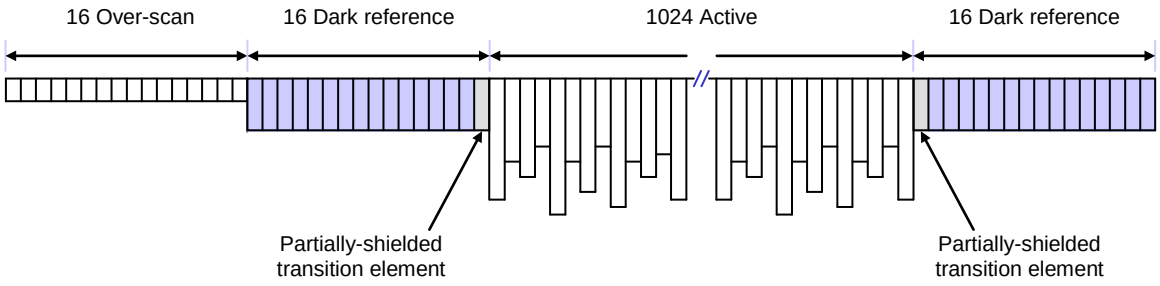
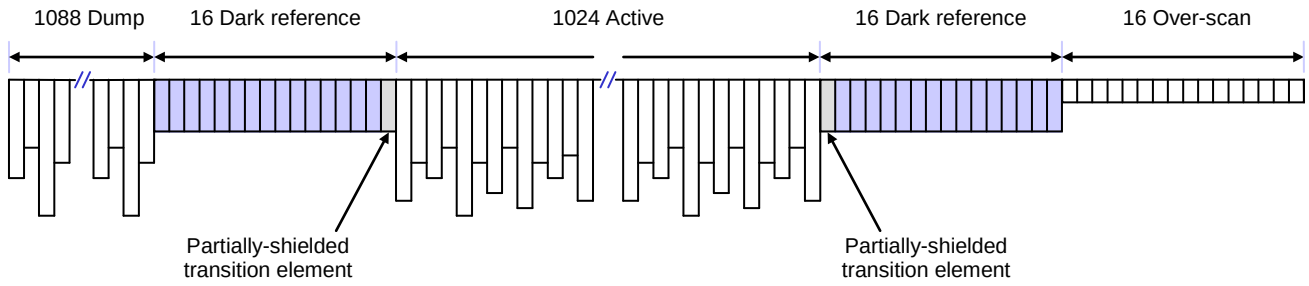


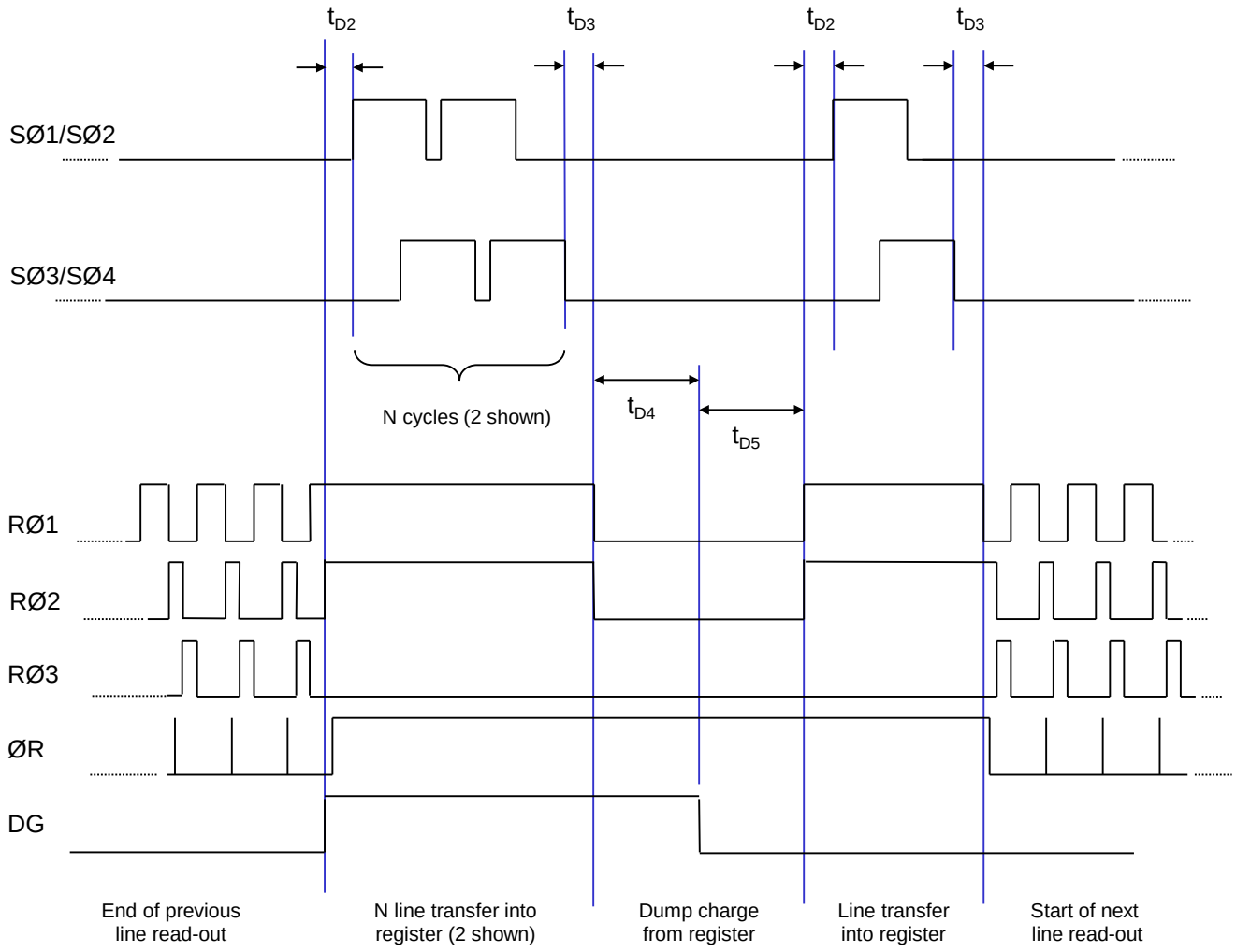
Figure 13: LINE OUTPUT FORMAT (OSL amplifier)



NOTE

27. There is a 1-line propagation delay between transferring a line from the store section to the standard register and reading it out through the OSL output amplifier.

Figure 14: LINE DUMPING – IF REQUIRED



RØ2HV Not shown

DEVICE COSMETIC PERFORMANCE

Grade 1 devices are supplied to the blemish specification shown below.

Note that incorrect biasing of the device may result in spurious dark or white blemishes appearing. These will be eliminated if the biases are adjusted.

Test Conditions

Operating mode	Devices run in 2-phase inverted mode, with an integration time of 100 ms and a read-out rate of 15 MHz.
Sensor temperature	18 ± 3 °C.
Multiplication gain	Set to approximately 1000.
Illumination	Set to give a signal level of approximately 60 e^-/pixel/frame.

BLEMISH SPECIFICATION

Black Columns Black defects are counted when they have a responsivity of less than 80% of the local mean signal at approximately the specified multiplication gain and level of illumination. A black column contains at least 9 contiguous black defects.

White Columns White defects are pixels having a dark signal generation rate corresponding to an output signal of greater than 5 times the maximum specified dark signal level. A white column contains at least 9 contiguous white defects.

SPECIFICATION

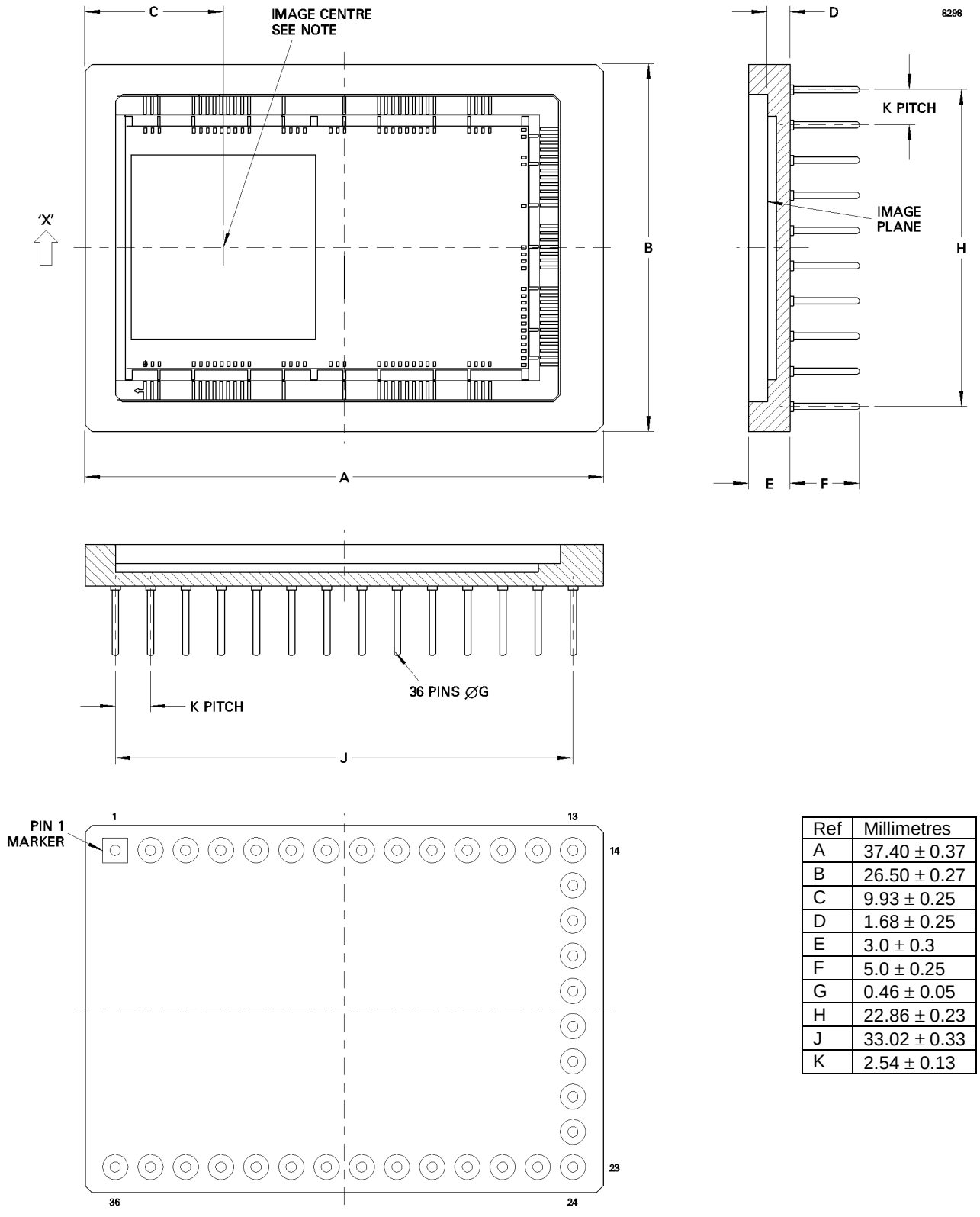
PARAMETER	GRADE 1 SPECIFICATION	GRADE 2 SPECIFICATION
White Columns	0	0
Black Columns	1	6

STORAGE AND OPERATIONTEMPERATURE EXTREMES

	MIN	MAX
Storage temperature (°C)	-200	+100
Operating temperature (°C)	-120	+75
Temperature ramping (°C/min)	-	5

Note: Operation or storage in humid conditions may give rise to moisture on the sensor surface on cooling, causing irreversible damage.

Figure 15: PACKAGE OUTLINE



Ref	Millimetres
A	37.40 ± 0.37
B	26.50 ± 0.27
C	9.93 ± 0.25
D	1.68 ± 0.25
E	3.0 ± 0.3
F	5.0 ± 0.25
G	0.46 ± 0.05
H	22.86 ± 0.23
J	33.02 ± 0.33
K	2.54 ± 0.13

Outline Note

The image centre is aligned centrally in the package in direction 'X' to within a tolerance of ±0.2 mm.