

Yosys Verilog Parsing Error: Unable to Synthesize After Reading File

I encountered an error while using Yosys to read a Verilog file. The steps and the error message are as follows:

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| yosys -- Yosys Open SYnthesis Suite  
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|-----  
Yosys 0.41+126 (git sha1 855ac285f49, g++ 11.4.0-1ubuntu1~22.04 -fPIC -Os)  
  
yosys> read_verilog design.v  
  
1. Executing Verilog-2005 frontend: design.v  
Parsing Verilog input from 'design.v' to AST representation.  
Generating RTLIL representation for module '\top'.  
Generating RTLIL representation for module '\module282'.  
ERROR: Assert 'node->bits == v' failed in frontends/ast/ast.cc:855.
```

After this error, the parsing process is interrupted. I have checked the Verilog file for syntax errors but couldn't find any obvious issues. I am using the latest version of Yosys.