Vivado Hang During Synthesis with Specific Constraints.

I am encountering an issue where Vivado hangs during the synthesis optimizating process. My system is running on Linux, and I'm using Vivado version 2024.1. The commands I use in the terminal are:

vivado -mode tcl

read_verilog rtl.v

synth_design -top top -flatten_hierarchy none -gated_clock_conversion auto -bufg 12 -directive AreaMapLargeShiftRegToBRAM -fsm_extraction gray -resource_sharing on -control_set_opt_threshold 20 -shreg_min_size 11 -max_bram 33 -max_uram 50 -max_dsp 16 -max_bram_cascade_height 10 -max_uram_cascade_height 17 -cascade_dsp force -incremental_mode quick -no_lc -retiming

Vivado hangs during synthesis with these constraints. This suggests a potential issue with Vivado's handling of these specific constraints.