

NXP WIT

RTL DESIGN OF DUAL PORT RAM USING VERILOG

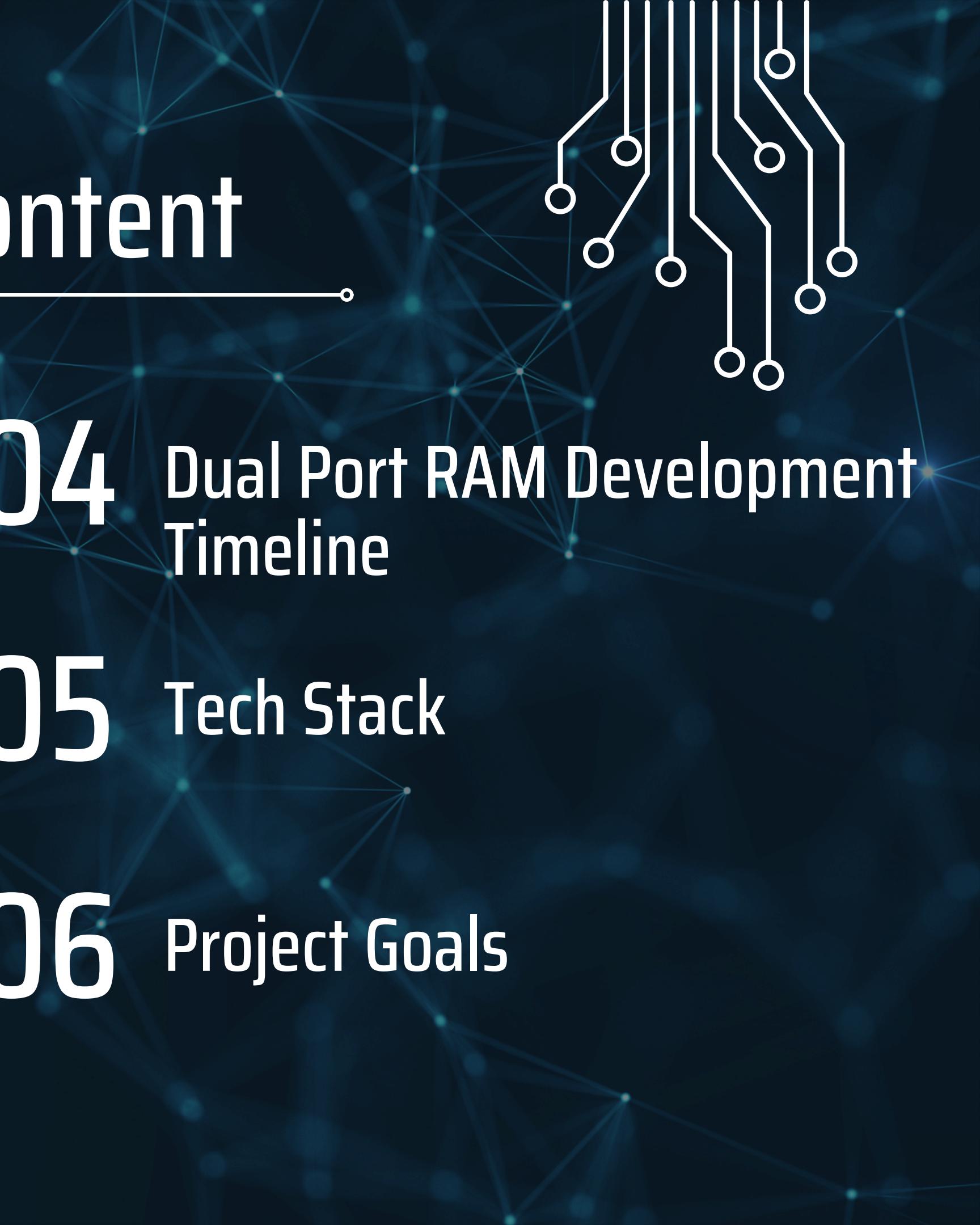
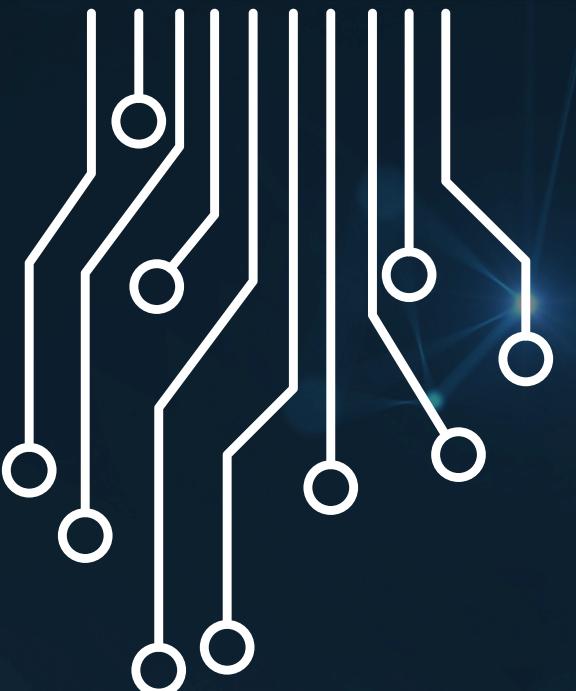


Table Of Content

Our Team

01

Overview

02

Importance in Modern
Industry

03

Dual Port RAM Development
Timeline

04

Tech Stack

05

Project Goals

06

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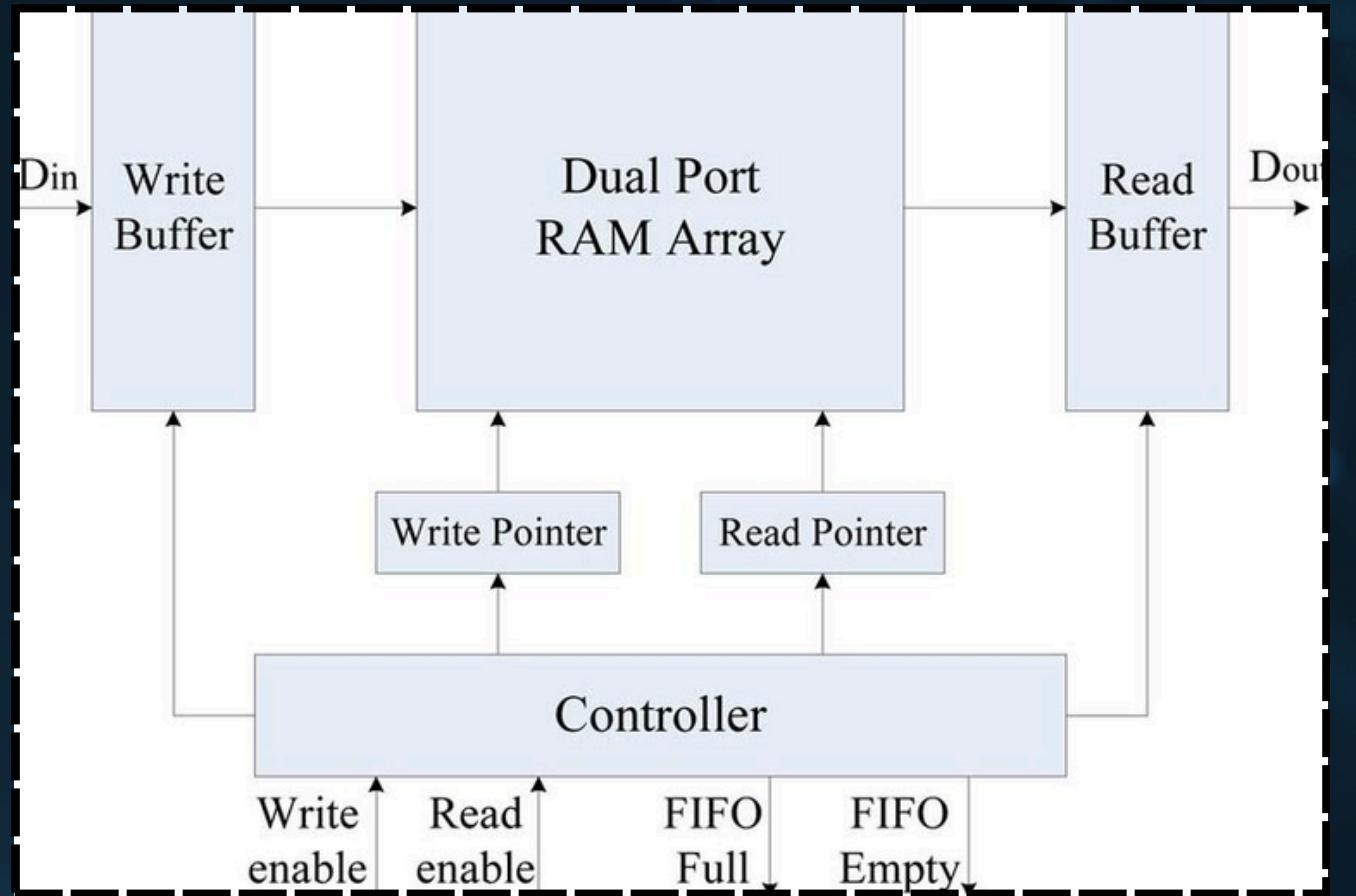
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Overview

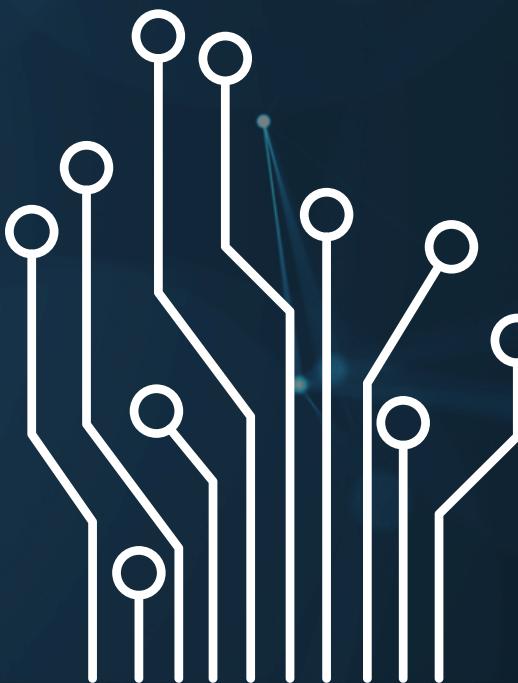


- **Dual Port Architecture**: Allows two independent ports for simultaneous read/write operations, improving data throughput.
- **Key Components**:
 - Memory array for storing data.
 - Address decoders for each port.
 - Data paths for managing input/output.
 - Control logic for read/write operations.

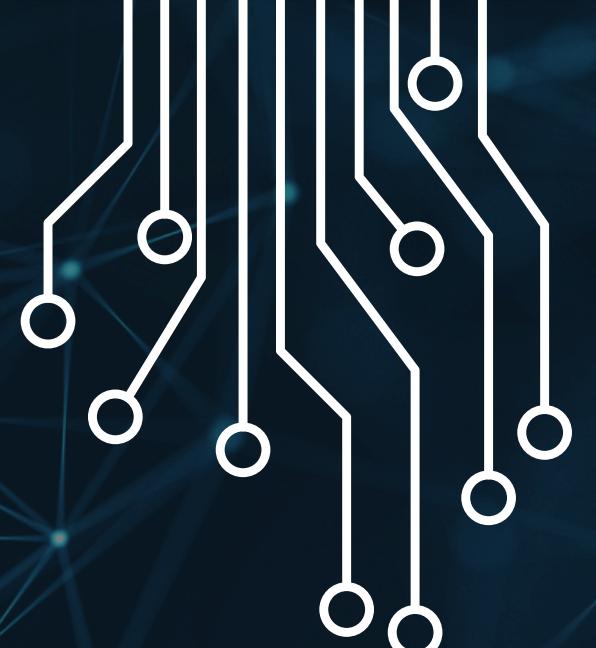


Overview

- **Conflict Handling**: Manages simultaneous access (e.g., both ports writing to the same address) using prioritization or stalling.
- **Synchronous vs Asynchronous**:
Synchronous: Operations happen on clock edges (more predictable).
Asynchronous: Operations occur without a clock (faster but more complex).
- **Applications**: Used in FPGAs, parallel processing, and high-performance data buffering.



Importance in Modern Industry:

- 
- 1. **Increased Throughput**: Enables simultaneous read/write, boosting data handling speed.
 - 2. **Parallel Processing**: Supports multicore CPUs and GPUs for efficient task execution.
 - 3. **FPGA and DSP**: Critical in managing multiple data streams for high-performance applications.

Importance in Industry: in Modern



- **Shared Memory**: Facilitates data sharing between processors or units.
- **Low Latency**: Reduces memory access bottlenecks in real-time systems.
- **Resource Optimization**: Saves space and power in embedded systems.

Dual Port RAM Development Timeline



1. Introduction of Dual Port Architecture:

Enabled two simultaneous read/write operations, improving performance over single-port RAM.

2. Integration in FPGAs (1980s-1990s): Became a key component in FPGA designs, enabling parallel processing and custom logic applications.

3. Synchronous Dual Port RAM (1990s):

Introduction of clocked Dual Port RAM for more predictable and reliable timing in digital system.

Dual Port RAM Development Timeline



4. **True Dual-Port RAM**: Allowed both ports to independently perform read/write operations, enhancing flexibility and throughput.
5. **Scaling with Smaller Technologies (2000s)**: Advancement in semiconductor fabrication technologies, leading to smaller, faster, and more efficient Dual Port RAM cells.
6. **Low-Power Dual Port RAM**: Developed for embedded systems and mobile devices, balancing power consumption with

Tech Stack

- **Verilog HDL** – For coding and implementing the hardware design at the RTL (Register Transfer Level).
- **ModelSim/EDA Playground/Xilinx Vivado** – For simulation and verification of the Verilog code and memory operations..
- **Waveform Viewer** – For visualizing and debugging signal transitions during simulation.
- **Makefiles/Scripts** – To automate synthesis, simulation, and verification steps (if applicable).



Project Goals

- **Simultaneous Access:** Enable two independent memory ports to perform read and write operations concurrently without interference.
- **Efficient Memory Design:** Develop a compact, efficient RTL design for the dual port RAM that meets specified size and performance criteria.
- **Conflict Resolution:** Implement logic to handle potential conflicts when both ports access the same memory address at the same time.
- **Verification and Validation:** Simulate the design using a testbench to ensure correct functionality across all edge cases and scenarios.



Thank You!

