Magnitude of a Complex Number

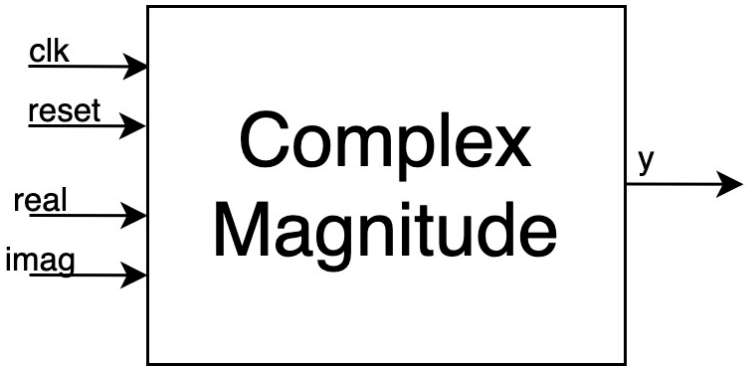
Design a digital circuit that realises the calculus of the magnitude of a given complex number using the following approximated formula:

$$\sqrt{P^2+Q^2} = \max\{|P|,|Q|\} + \frac{1}{2}\min\{|P|,|Q|\} - \frac{1}{16}\left[\max\{|P|,|Q|\} + \min\{|P|,|Q|\}\right]$$

Where P and Q are respectively the real and the imaginary parts and are represented with N bits in 2-complement. Considering a symmetric interval of representation, the values $|P|,|Q|$ are inside the range $[0, 2^{N-1}-1]$.

Use $N = 10$ and evaluate the Mean Square Error (MSE) due to the approximation.

The interface of the circuit to be designed is as follows:



You are requested to deal with the various possible error situations, documenting the choices made.

The final project report must contain:

- Introduction (circuit description, possible applications, possible architectures, etc.)
- Description of the architecture designed (block diagram, inputs/outputs, etc.)
- VHDL code (with detailed comments) to be attached to the report.
- Test strategy (Test-plan) and related Testbench for verification; a detailed, though not exhaustive, verification is required, including error situations and borderline cases of functioning
- Interpretation of the results obtained in the automatic synthesis/implementation on a Xilinx FPGA platform in terms of maximum clock frequency (critical path), elements used (slice, LUT, etc.) and estimated power consumption. Comment on any warning messages.
- Conclusions