```
module FUNC1 (IO, I1, S, out);
        input IO, I1;
        input S;
        output out;
        out = S? I1: IO;
endmodule

module FUNC2 (out,ctl,clk,reset);
        output [7:0] out;
        input ctl, clk, reset;
        reg [7:0] out;
        always @(posedge clk)
```

Unn Fig. B-2