



From Hennessy JL, Patterson DA: Computer architecture: A quantitative approach, ed 6, Cambridge MA, 2018, Morgan Kaufmann.

FIGURE 4.74 The basic structure of the A53 integer pipeline is eight stages: F1 and F2 fetch the instruction, D1 and D2 do the basic decoding, and D3 decodes some more complex instructions and is overlapped with the first stage of the execution pipeline (ISS). After ISS, the Ex1, EX2, and WB stages complete the integer pipeline. Branches use four different predictors, depending on the type. The floating-point execution pipeline is five cycles deep, in addition to the five cycles needed for fetch and decode, yielding 10 stages in total. AGU stands for *Address Generation Unit* and TLB for *Transaction Lookaside Buffer* (See Chapter 5). The NEON unit performs the ARM SIMD instructions of the same name. (From Hennessy JL, Patterson DA: *Computer architecture: A quantitative approach*, ed 6, Cambridge MA, 2018, Morgan Kaufmann.)