



FIGURE e4.14.10 Single-cycle pipeline diagrams for clock cycles 5 (top diagram) and 6 (bottom diagram). In clock cycle 5, **lw** completes by writing the data in MEM/WB into register 10, and **sub** sends the difference in EX/MEM to MEM/WB. In the next clock cycle, **sub** writes the value in MEM/WB to register 11.