```
 EXMEMIR <= IDEXIR; EXMEMB <= IDEXB; //pass along the IR & B register
//Mem stage of pipeline
if (EXMEMop==ALUop) MEMWBValue <= EXMEMALUOut; //pass along ALU result
    else if (EXMEMop == LW) MEMWBValue <= DMemory[EXMEMALUOut>>2];
    else if (EXMEMop == SW) DMemory[EXMEMALUOut>>2] <=EXMEMB; //store
   MEMWBIR <= EXMEMIR; //pass along IR
    // the WB stage
    if ((MEMWBop==ALUop) & (MEMWBrd != 0)) // update registers if ALU operation and destination not 0
        Regs[MEMWBrd] <= MEMWBValue; // ALU operation
        else if ((EXMEMop == LW)& (MEMWBrt != 0)) // Update registers if load and destination not 0
           Regs[MEMWBrt] <= MEMWBValue;
  end
endmodule
```

FIGURE e4.14.1 A Verilog behavorial model for the MIPS five-stage pipeline, ignoring branch and data hazards. (*Continued*)