



**FIGURE B.9.4 Typical organization of a  $4\text{M} \times 8$  SRAM as an array of  $4\text{K} \times 1024$  arrays.** The first decoder generates the addresses for eight  $4\text{K} \times 1024$  arrays; then a set of multiplexors is used to select 1 bit from each 1024-bit-wide array. This is a much easier design than a single-level decode that would need either an enormous decoder or a gigantic multiplexor. In practice, a modern SRAM of this size would probably use an even larger number of blocks, each somewhat smaller.