



FIGURE e4.14.19 Clock cycles 4 and 5 of the instruction sequence on page 4.13-26 with a load replacing sub. The bubble is inserted in the pipeline in clock cycle 4, and then the and instruction is allowed to proceed in clock cycle 5. The forwarding unit is highlighted in clock cycle 5 because it is forwarding data from lw to the ALU. Note that in clock cycle 4, the forwarding unit forwards the address of the lw as if it were the contents of register \$2; this is rendered harmless by the insertion of the bubble. The bold lines are those active in a clock cycle, and the italicized register numbers in color indicate a hazard.