		Time (in clock cycles) ————————————————————————————————————								→
		CC 1	CC 2	CC 3	CC 4	CC 5	CC 6	CC 7	CC 8	CC 9
e: oi	rogram kecution rder n instructions)									
	lw \$10, 20(\$1)	Instruction fetch	Instruction decode	Execution	Data access	Write-back				
	sub \$11, \$2, \$3		Instruction fetch	Instruction decode	Execution	Data access	Write-back			
	add \$12, \$3, \$4			Instruction fetch	Instruction decode	Execution	Data access	Write-back		
	lw \$13, 24(\$1)				Instruction fetch	Instruction decode	Execution	Data access	Write-back	
	add \$14, \$5, \$6					Instruction fetch	Instruction decode	Execution	Data access	Write-back

FIGURE 4.44 Traditional multiple-clock-cycle pipeline diagram of five instructions in Figure 4.43.