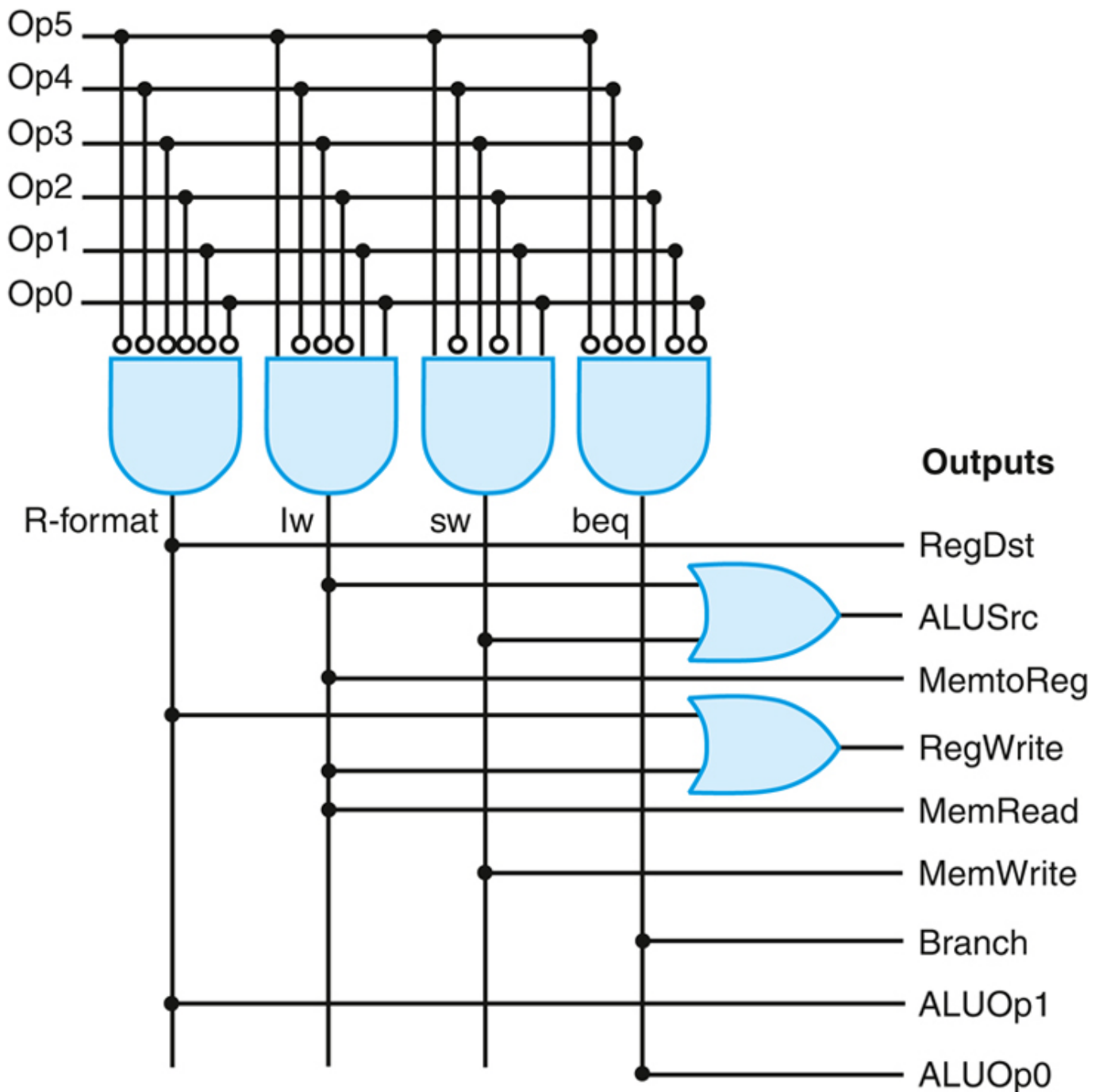**FIGURE D.2.5 The structured implementation of the control function as described by the truth table in Figure D.2.4.** The structure, called a programmable logic array (PLA), uses an array of AND gates followed by an array of OR gates. Th e inputs to the AND gates are the function inputs and their inverses (bubbles indicate inversion of a signal). Th e inputs to the OR gates are the outputs of the AND gates (or, as a degenerate case, the function inputs and inverses). Th e output of the OR gates is the function outputs.