| | ARMv8 | MIPS64 | PowerPC | RISC-V | SPARCv.9 |
|---|---|---|---|---|---|
| Number of condition code bits (integer and FP) | 16 (8 + the inverse) | none | 8 × 4 both | none | 2 × 4 integer, 4 × 2 FP |
| Basic compare instructions (integer and FP) | 1 integer; 1 FP | 1 integer, 1 FP | 4 integer, 2 FP | 2 integer; 3 FP | 1 FP |
| Basic branch instructions (integer and FP) | 1 | 2 integer, 1 FP | 1 both | 4 integer (used for FP as well) | 3 integer, 1 FP |
| Compare register with register/ constant and branch | — | =, not= | — | =, not =, >=, < | — |
| Compare register to zero and branch | — | =, not=, <, <=, >, >= | — | =, not=, <, <=, >, >= | =, not=, <, <=, >, >= |

**FIGURE E.12 Summary of five desktop RISC approaches to conditional branches.** Integer compare on SPARC is synthesized with an arithmetic instruction that sets the condition codes using r0 as the destination.