Instruction class	Instruction fetch	Register read	ALU operation	Data access	Register write	Total time
Load word (Tw)	200 ps	100 ps	200 ps	200 ps	100 ps	800 ps
Store word (SW)	200 ps	100 ps	200 ps	200 ps		700 ps
R-format (add, sub, AND, OR, slt)	200 ps	100 ps	200 ps		100 ps	600 ps
Branch (beq)	200 ps	100 ps	200 ps			500 ps

FIGURE 4.26 Total time for each instruction calculated from the time for each component. This calculation assumes that the multiplexors, control unit, PC accesses, and sign extension unit have no delay.

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