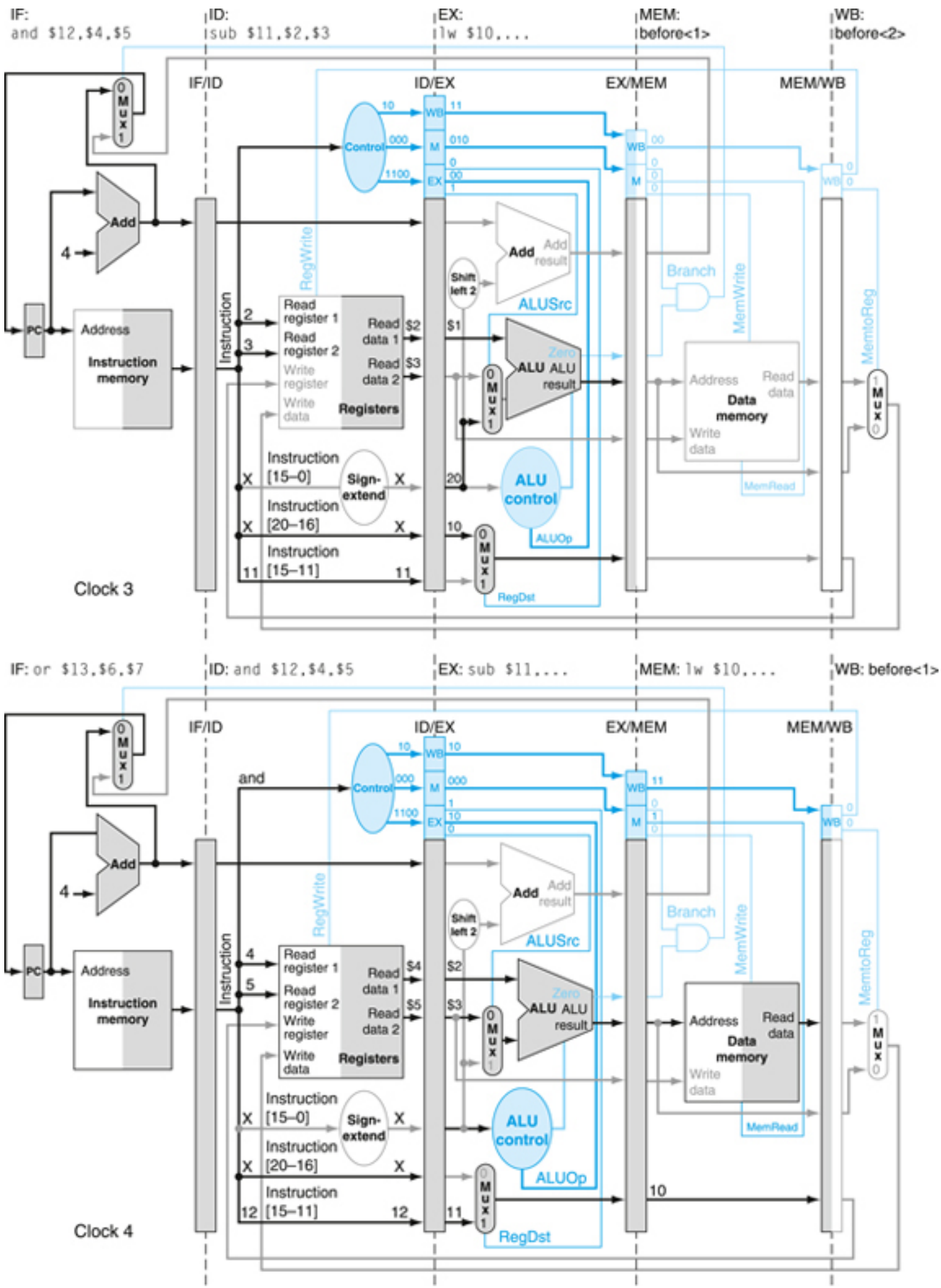

FIGURE e4.14.11 Clock cycles 1 and 2. The phrase "*before* <*i*>" means the ith instruction before lw. The lw instruction in the top datapath is in the IF stage. At the end of the clock cycle, the lw instruction is in the IF/ID pipeline registers. In the second clock cycle, seen in the bottom datapath, the lw moves to the ID stage, and sub enters in the IF stage. Note that the values of the instruction fields and the selected source registers are shown in the ID stage. Hence register $1 and the constant 20, the operands of lw, are written into the ID/EX pipeline register. The number 10, representing the destination register number of lw, is also placed in ID/EX. Bits 15–11 are 0, but we use X to show that a field plays no role in a given instruction. The top of the ID/EX pipeline register shows the control values for lw to be used in the remaining stages. These control values can be read from the lw row of the table in Figure 4.18.