FIGURE e4.14.20 Clock cycles 6 and 7 of the instruction sequence on page 4.13-26 with a load replacing sub. Note that unlike in Figure e4.14.17, the stall allows the lw to complete, and so there is no forwarding from MEM/WB in clock cycle 6. Register $4 for the add in the EX stage still depends on the result from or in EX/MEM, so the forwarding unit passes the result to the ALU. The bold lines show ALU input lines active in a clock cycle, and the italicized register numbers indicate a hazard. The instructions after add are shown as inactive for pedagogical reasons.