```
package cache_def;
  // data structures for cache tag & data

  parameter int TAGMSB = 31;     //tag msb
  parameter int TAGLSB = 14;     //tag lsb

//data structure for cache tag
typedef struct packed {
  bit    valid;                  //valid bit
  bit    dirty;                  //dirty bit
  bit [TAGMSB:TAGLSB]tag;        //tag bits
}cache_tag_type;

//data structure for cache memory request
typedef struct {
  bit [9:0]index;                //10-bit index
  bit    we;                     //write enable
}cache_req_type;

//128-bit cache line data
typedef bit [127:0]cache_data_type;
```

FIGURE e5.12.1 Type declarations in SystemVerilog for the cache tags and data. The tag field is 18 bits wide and the index field is 10 bits wide, while a 2-bit field (bits 3–2) is used to index the block and select the word from the block. The rest of the type declaration is found in the following figure.