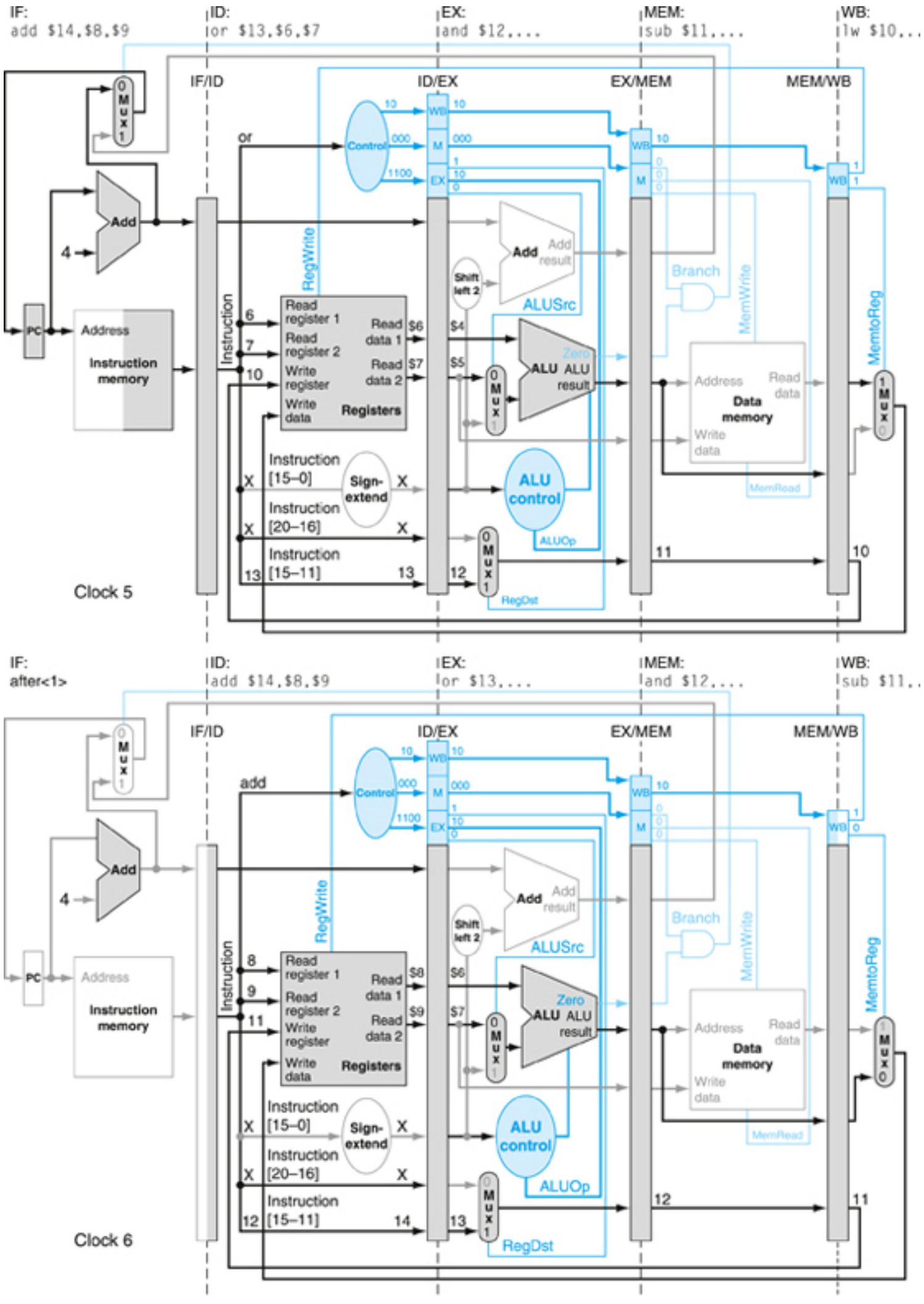

FIGURE e4.14.12 Clock cycles 3 and 4. In the top diagram, lw enters the EX stage in the third clock cycle, adding $1 and 20 to form the address in the EX/MEM pipeline register. (The lw instruction is written lw $10,. . . upon reaching EX, because the identity of instruction operands is not needed by EX or the subsequent stages. In this version of the pipeline, the actions of EX, MEM, and WB depend only on the instruction and its destination register or its target address.) At the same time, sub enters ID, reading registers $2 and $3, and the and instruction starts IF. In the fourth clock cycle (bottom datapath), lw moves into MEM stage, reading memory using the value in EX/MEM as the address. In the same clock cycle, the ALU subtracts $3 from $2 and places the difference into EX/MEM, reads registers $4 and $5 during ID, and the or instruction enters IF. The two diagrams show the control signals being created in the ID stage and peeled off as they are used in subsequent pipe stages.