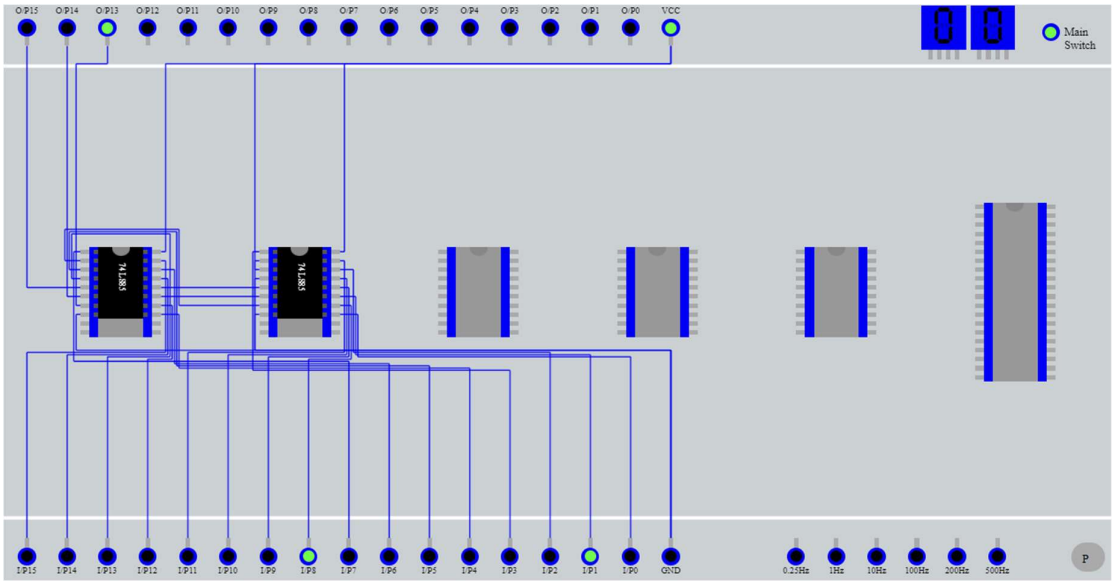
Virtual Lab

Course Name:	**Digital Design Laboratory**	**Semester:**	**III**
Date of Performance:	**09 / 09 / 2024**	**Batch No:**	**D3**
Faculty Name:	**Mansi Kambli**	**Roll No:**	**16010123294**
Faculty Sign & Date:		**Grade/Marks :**	**___/25**

A<B



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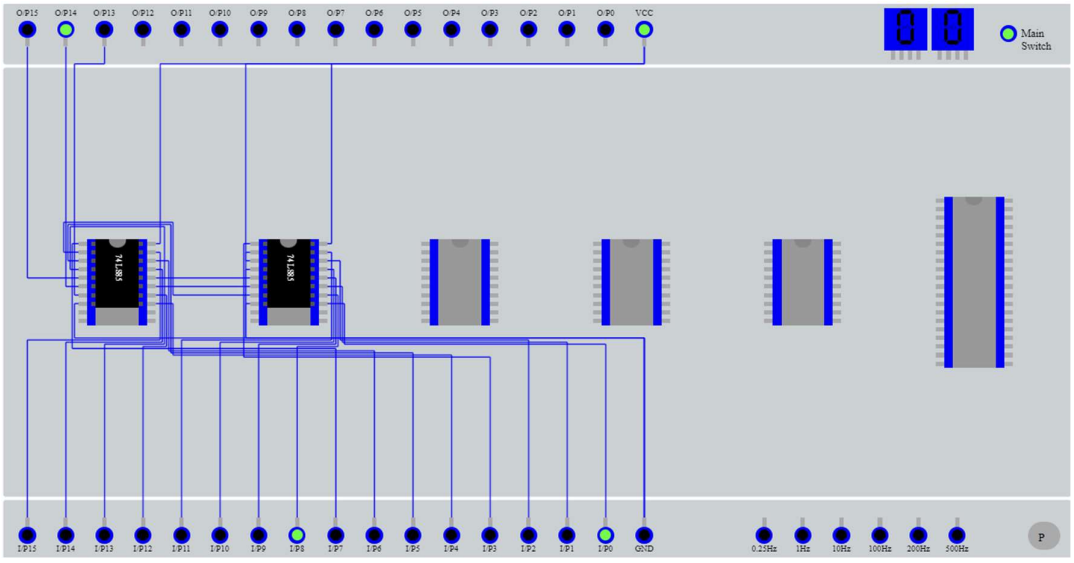

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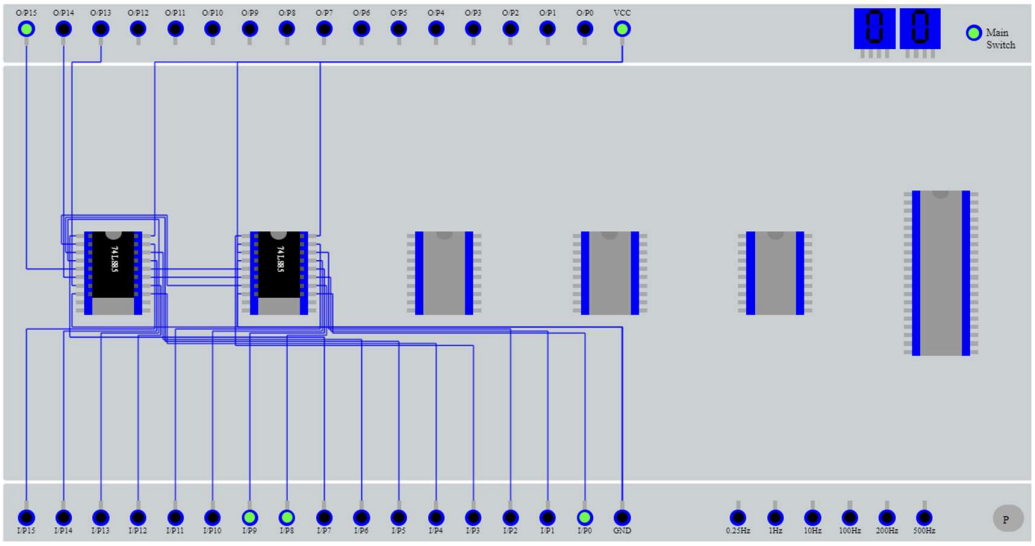
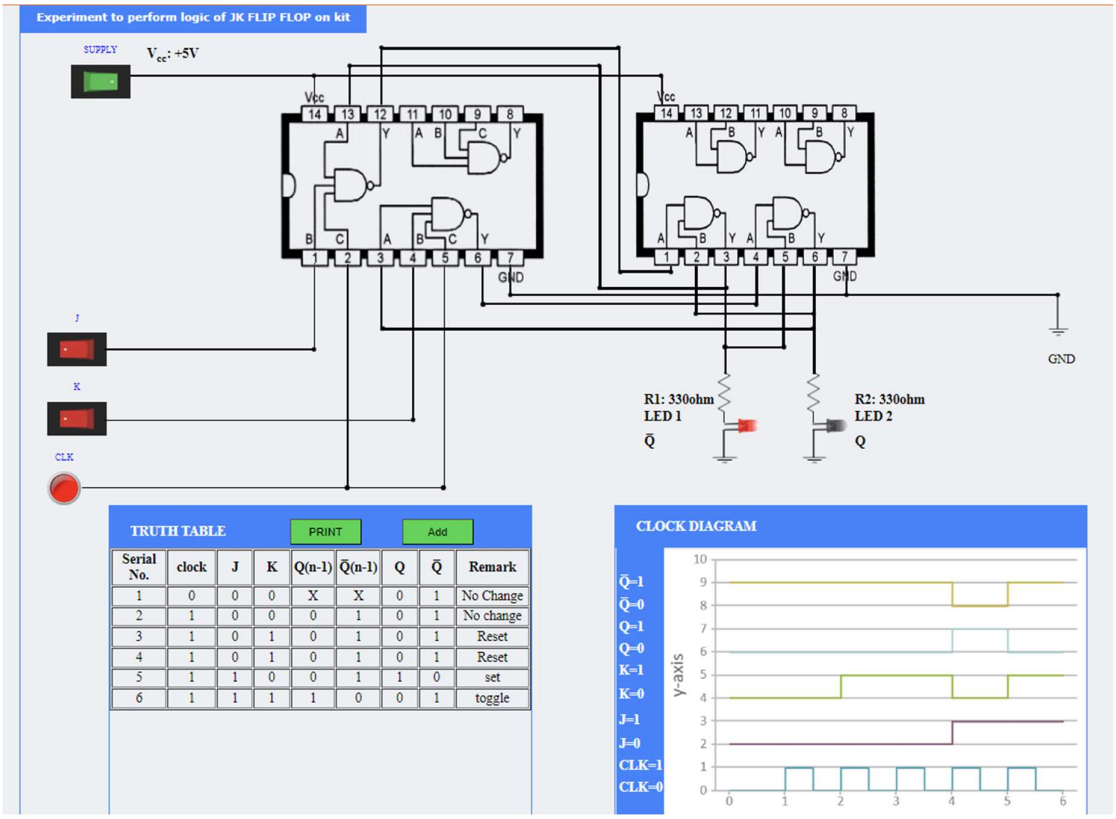


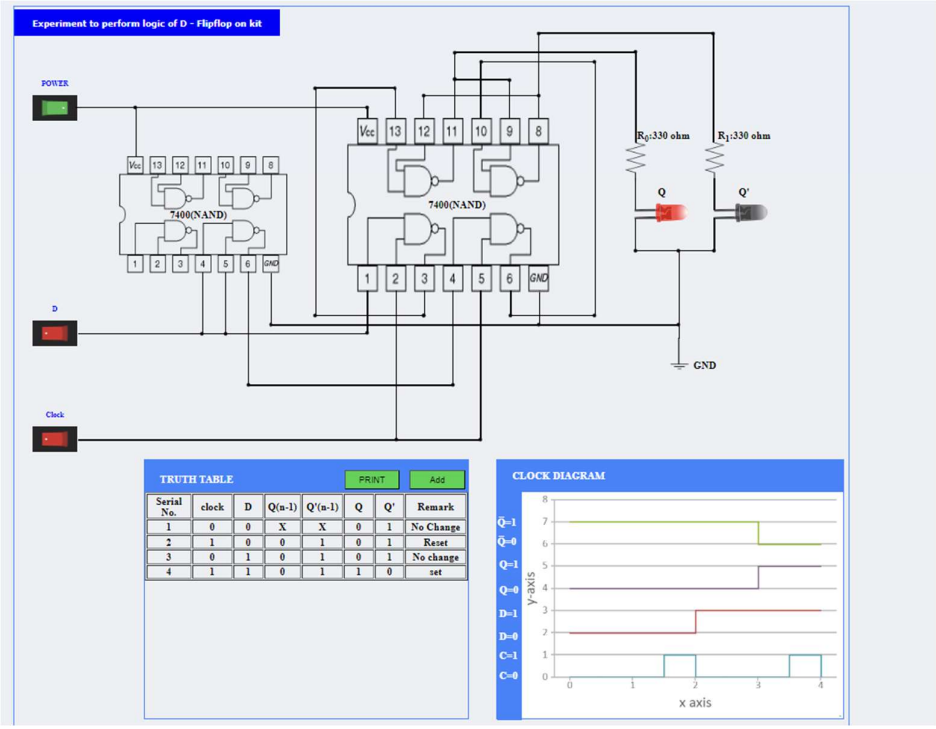
Flip Flops:

JK flip flop

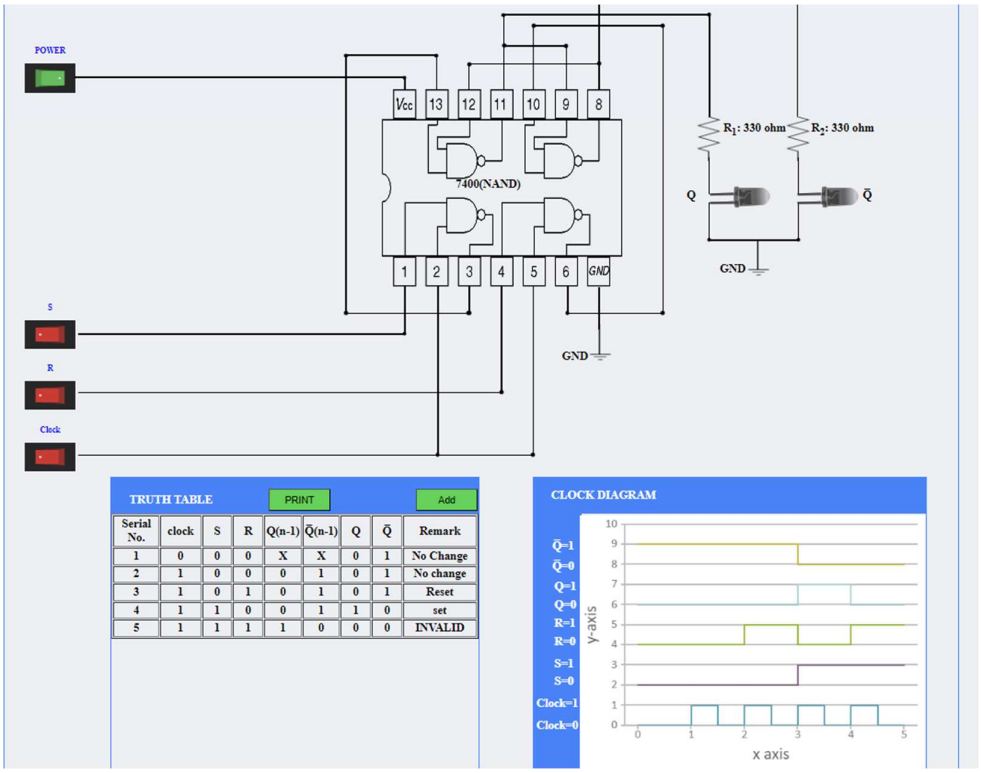


Serial No.	clock	J	K	Q(n-1)	Q̄(n-1)	Q	Q̄	Remark
1	0	0	0	X	X	0	1	No Change
2	1	0	0	0	1	0	1	No change
3	1	0	1	0	1	0	1	Reset
4	1	0	1	0	1	0	1	Reset
5	1	1	0	0	1	1	0	set
6	1	1	1	1	0	0	1	toggle

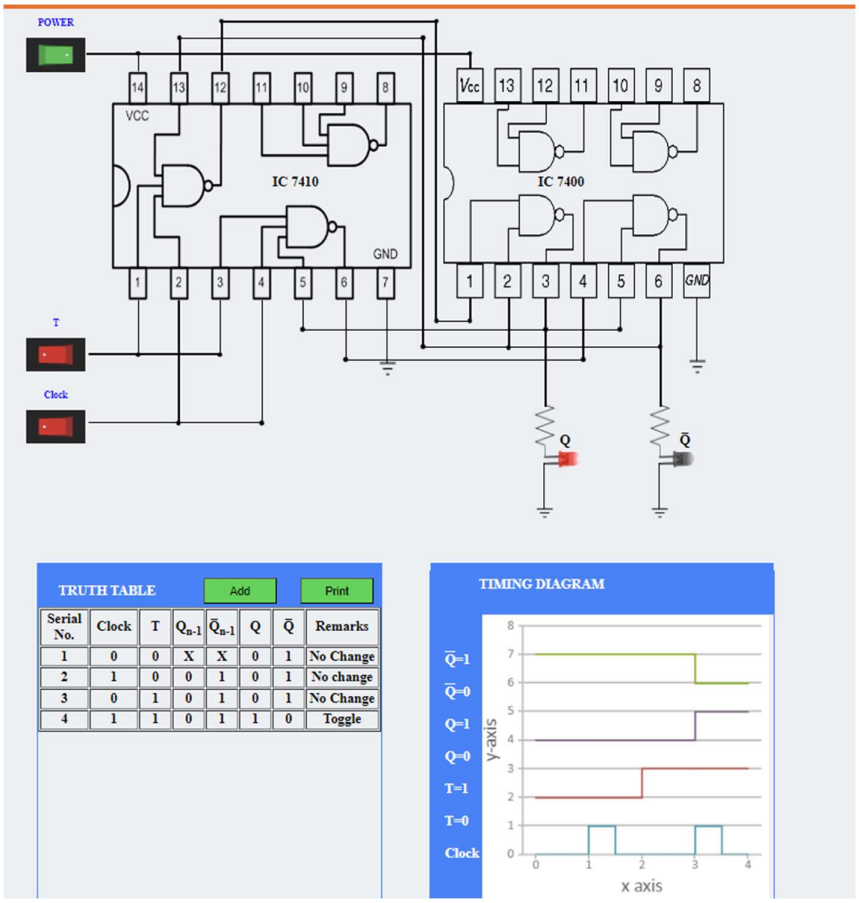
D flip flop



RS Flip Flop



T Flip Flop



TRUTH TABLE

Add Print

Serial No.	Clock	T	Q_{n-1}	$\bar{Q}_{n-1}$	Q	$\bar{Q}$	Remarks
1	0	0	X	X	0	1	No Change
2	1	0	0	1	0	1	No change
3	0	1	0	1	0	1	No Change
4	1	1	0	1	1	0	Toggle