Course Name:	**Digital Design Laboratory**	**Semester:**	**III**
Date of Performance:	**29 / 07 / 2024**	**Batch No:**	**D3**
Faculty Name:	**Mansi Kambli**	**Roll No:**	**16010123294**
Faculty Sign & Date:		**Grade/Marks:**	**___/25**

Experiment No: 2
Title: Binary Adders and Subtractors

Aim and Objective of the Experiment:

To implement half and full adder–subtractor using gates and IC 7483

COs to be achieved:

CO2: Use different minimization technique and solve combinational circuits.

Tools used:

Trainer kits

Theory:

Adder: The addition of two binary digits is the most basic operation performed by the digital computer. There are two types of adder:

- Half adder
- Full adder

Half Adder: Half adder is a combinational logic circuit with two inputs and two outputs. It is the basic building block for the addition of two single-bit numbers.

Full adder: A half adder has a provision not to add a carry coming from the lower order bits when multi-bit addition is performed. for this purpose, a third input terminal is added and this circuit is to add A, B, and C where A and B are the nth order bits of the number A and B respectively and C is the carry generated from the addition of (n-1) order bits. This circuit is referred to as full adder.

Subtractor: Subtraction of two binary digits is one of the most basic operations performed by digital computer .there are two types of subtractors:

- Half subtractor

- Full subtractor

Half subtractor: Logic circuit for the subtraction of B from A where A,B are 1 bit numbers is referred to as half subtract or .the subtract or process has two input and difference and borrow are the two outputs.

Full subtractor: As in the case of the addition using logic gates, a full subtractor is made by combining two half-sub tractors and an additional OR-gate. A full subtractor has the borrow in capability (denoted as BOR_{IN}) and so allows cascading which results in the possibility of multi-bit subtraction.

IC 7483

For subtraction of one binary number from another, we do so by adding 2’s complement of the former to the latter number using a full adder circuit.

IC 7483 is a 16 pin, 4-bit full adder. This IC has a provision to add the carry output to transfer and end around carry output using Co and C4 respectively.

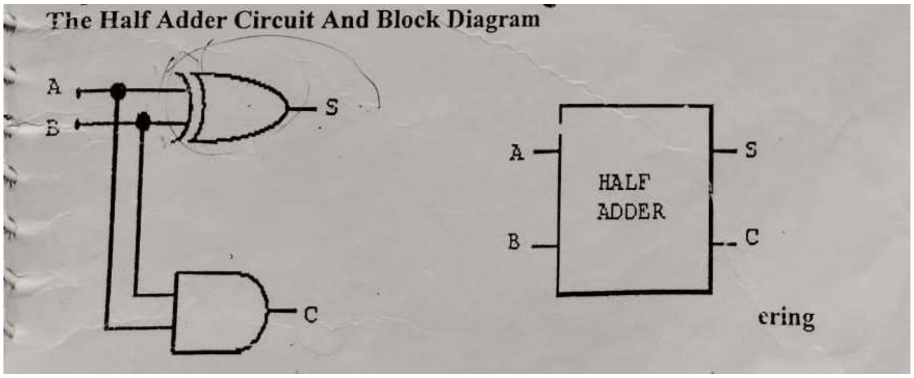
2’s complement: 2’s complement of any binary no. can be obtained by adding 1 in 1’scomplement of that no.

e.g. 2’s complement of $+(10)_{10}$ =1010is

1C of	01
1010	01
	+ 1
$-(10)_{10}$	01
	10

In 2’s complement subtraction using IC 7483, we are representing negative number in 2’s complement form and then adding it with 1st number.

Implementation Details:
Half Adder Block Diagram & circuit



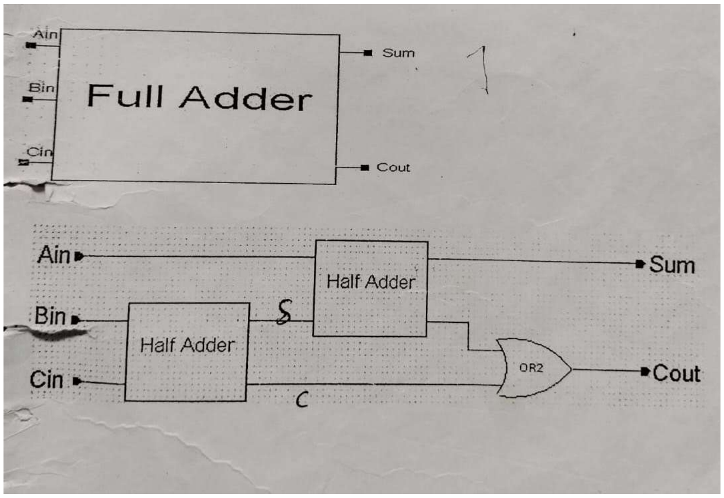
Truth Table for Half Adder

Inputs		Outputs	
A	**B**	**A**	**B**
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

From the truth table (with steps):

A	B	Sum (S)	Carry (C)	Steps for Calculation
0	0	0	0	0 + 0 = 0, Sum = 0, Carry = 0
0	1	1	0	0 + 1 = 1, Sum = 1, Carry = 0
1	0	1	0	1 + 0 = 1, Sum = 1, Carry = 0
1	1	0	1	1 + 1 = 2, Sum = 0, Carry = 1

Full Adder Block Diagram & Circuit



Truth Table for Full Adder

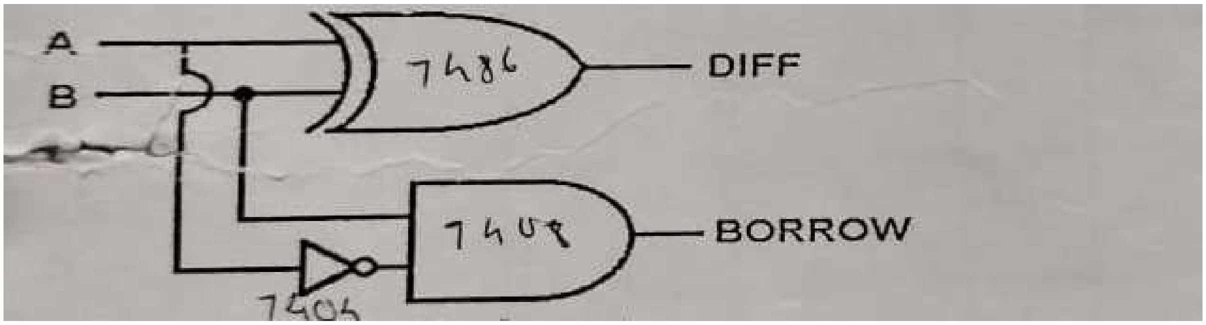
A	B	Cin	S	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

From the truth table (with steps):

A	B	C_{in}	Sum (S)	Carry-out (C_{out})	Steps for Calculation
0	0	0	0	0	0 + 0 + 0 = 0, Sum = 0, Carry-out = 0
0	0	1	1	0	0 + 0 + 1 = 1, Sum = 1, Carry-out = 0
0	1	0	1	0	0 + 1 + 0 = 1, Sum = 1, Carry-out = 0
0	1	1	0	1	0 + 1 + 1 = 2, Sum = 0, Carry-out = 1
1	0	0	1	0	1 + 0 + 0 = 1, Sum = 1, Carry-out = 0
1	0	1	0	1	1 + 0 + 1 = 2, Sum = 0, Carry-out = 1
1	1	0	0	1	1 + 1 + 0 = 2, Sum = 0, Carry-out = 1
1	1	1	1	1	1 + 1 + 1 = 3, Sum = 1, Carry-out = 1

When the sum of the input is 2 or more then carry out is set to 1.

Half Subtractor Block Diagram & Half Subtractor Circuit



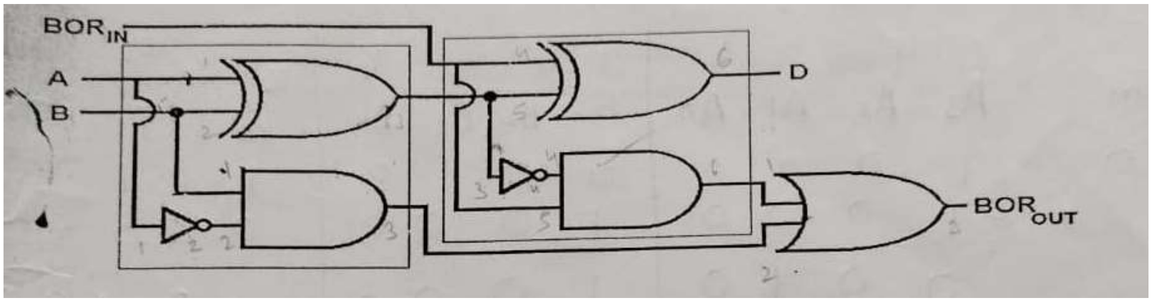
Truth Table for Half Subtractor

A	B	DIFFERENCE (D)	BORROW(Bo)
0	0	0	0
1	0	1	0
0	1	1	1
1	1	0	0

From the truth table (with steps) :

A	B	Difference (D)	Borrow (B_{out})	Steps for Calculation
0	0	0	0	0 - 0 = 0, Difference = 0, Borrow = 0
0	1	1	1	0 - 1 = -1 (borrow 1), Difference = 1, Borrow = 1
1	0	1	0	1 - 0 = 1, Difference = 1, Borrow = 0
1	1	0	0	1 - 1 = 0, Difference = 0, Borrow = 0

Full Subtractor Block Diagram & Full Subtractor Circuit



Truth Table for Full subtractor

A	B	BIN	D	BOROUT
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

.

.

From the truth table (with steps):

A	B	B_{in}	Difference (D)	Borrow (B_{out})	Steps for Calculation
0	0	0	0	0	0 - 0 - 0 = 0, Difference = 0, Borrow = 0
0	0	1	1	1	0 - 0 - 1 = -1 (borrow 1), Difference = 1, Borrow = 1
0	1	0	1	1	0 - 1 - 0 = -1 (borrow 1), Difference = 1, Borrow = 1
0	1	1	0	1	0 - 1 - 1 = -2 (borrow 1), Difference = 0, Borrow = 1
1	0	0	1	0	1 - 0 - 0 = 1, Difference = 1, Borrow = 0
1	0	1	0	0	1 - 0 - 1 = 0, Difference = 0, Borrow = 0
1	1	0	0	0	1 - 1 - 0 = 0, Difference = 0, Borrow = 0
1	1	1	1	1	1 - 1 - 1 = -1 (borrow 1), Difference = 1, Borrow = 1

Example:

1) $7_{10} - 2_{10} = 5_{10}$

7 0111

2 0010

1'C of 2

1101

+ 1

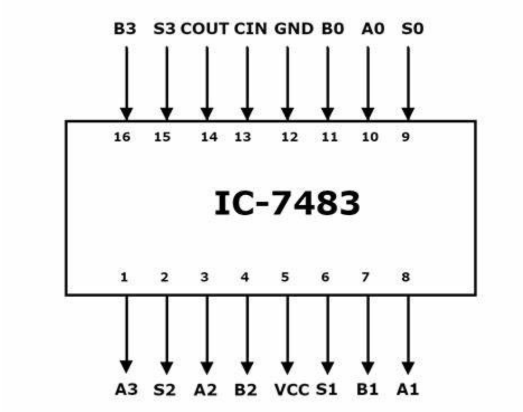
2'C of 2

1110

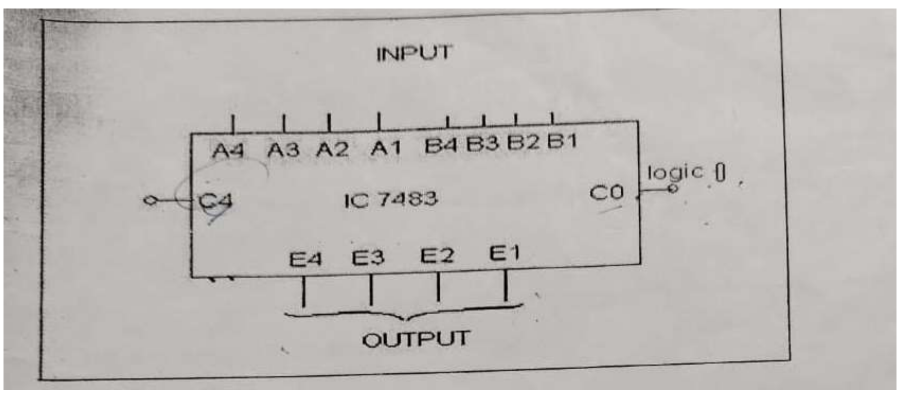
0111 + 1110 1

0101

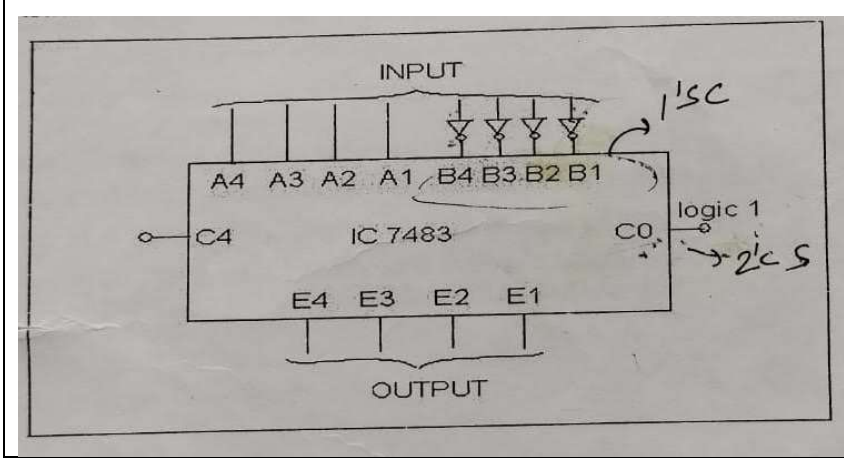
Pin Diagram IC7483



Adder



Subtractor



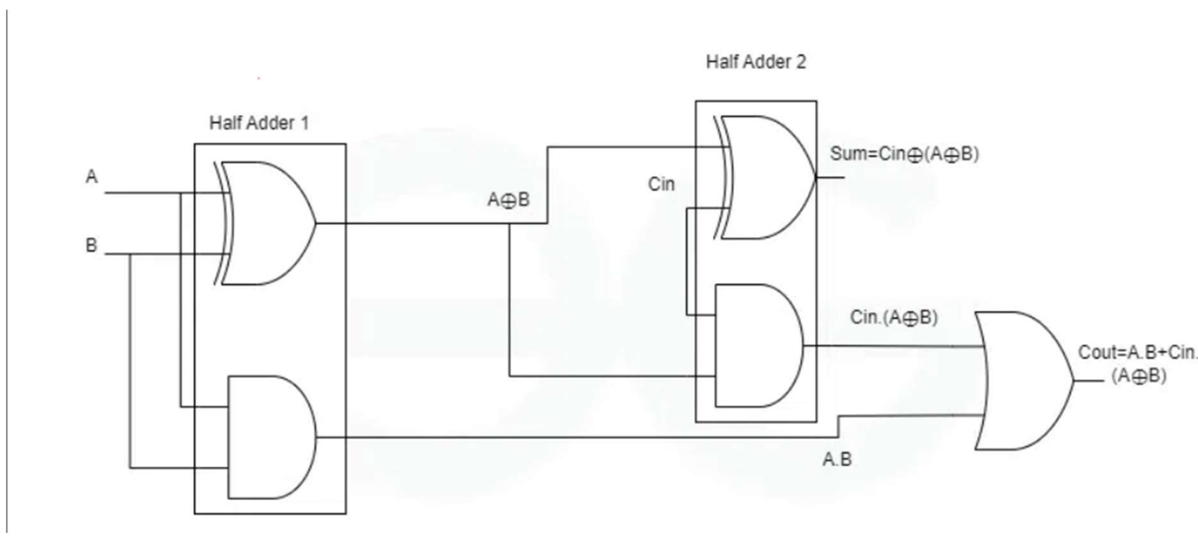
Implementation Details

Procedure:

1) Locate the IC 7483 and 4-not gates block on trainer kit.
2) Connect 1st input no. to A4-A1 input slot and 2nd (negative) no. to B4-B1 through 4-not gates (1C of 2nd no.)
3) Connect high input to Co so that it will get added with 1C of 2nd no. to get 2C.
4) Connect 4-bit output to the output indicators.
5) Switch ON the power supply and monitor the output for various input combinations.

Post Lab Subjective/Objective type Questions:

1. Design a full adder using two half adders.



2. Perform the following Binary subtraction with the help of appropriate ICs:
   a. 6-4
   b. 5-8
   c. 7-9

a) 6 − 4

$6 = (0110)_2$, $4 = (0100)_2$

2's complement of 4 = ~~101~~ → 1's complement = $(1011)_2$

2's complement = $(1100)_2$

on adding

$$\begin{array}{r} 0110 \\ +\ 1100 \\ \hline \cancel{1}0010 \end{array} = \underline{\underline{2}}$$

b) 5 − 8

$5 = (0101)_2$ $8 = (1000)_2$

2's complement of 8 → 1's complement = 0111

2's complement = 1000

adding

$$\begin{array}{r} 0101 \\ +\ 1000 \\ \hline 1101 \end{array}$$

→ 2's compliment of $-\underline{3}$

c) 7-~~8~~9

7 = 0111 9 → 1001

2's complement of 9 = 0111

on adding

$$\begin{array}{r} 0111 \\ +\ 0111 \\ \hline 1110 \end{array}$$

2's complement of 2 ←

Conclusion:

Learned about binary adder and subtractor and also verified using the 7483 ic and learned its connections and application on the DDL kit.

Signature of faculty in-charge with Date: