Course Name:	Digital Design Laboratory	Semester:	III
Date of Performance:	07/10 /2024	Batch No:	D3
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Faculty Sign & Date:		Grade/Marks:	___/25

Experiment No: 7
Title: Asynchronous Counter

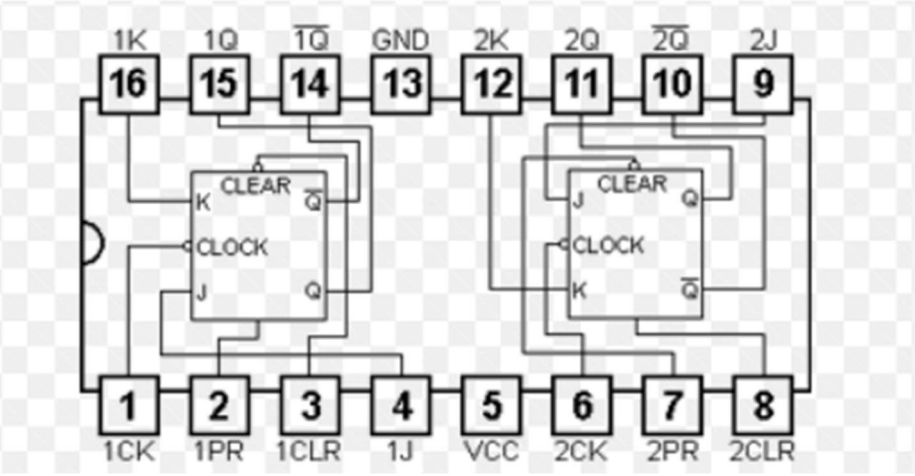
Aim and Objective of the Experiment:
To design and implement 3 bit Asynchronous up counter using JK Flip Flop

COs to be achieved:
CO3: Design synchronous and asynchronous sequential circuits.

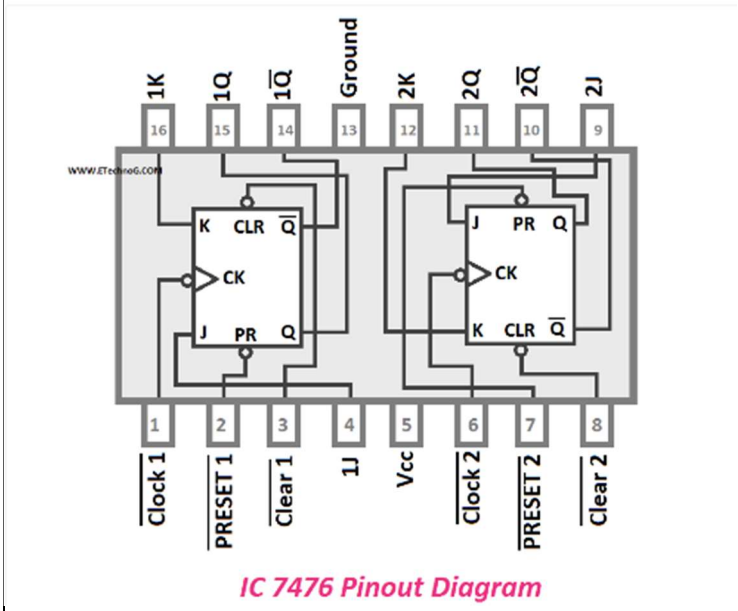
Tools used:
Trainer kits

Theory:

Circuit diagram of 3 bit Asynchronous Up counter using JK FF (IC 7476)



Pin diagram of JK FF (IC 7476)



IC 7476 Pinout Diagram

Implementation Details

Procedure

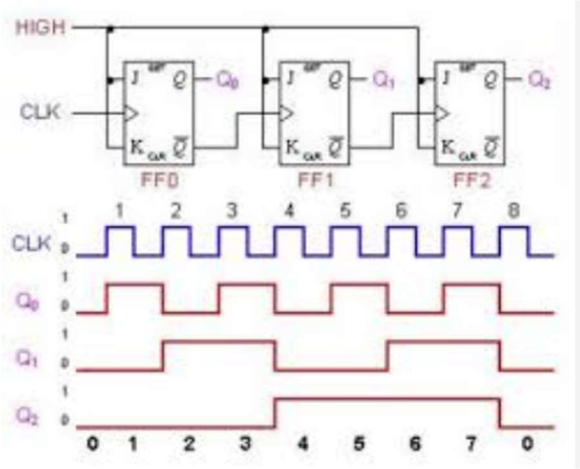
1) Locate IC 7476 JK FF on Digital trainer kit
2) Apply various inputs to appropriate pins as per the circuit diagram of the 3 bit Asynchronous up counter with reference to the pin configuration of the IC.
3) Make sure of Reset and Clear Pins connections with reference to data sheet information.
4) Connect a pulsar switch to the clock input.
5) Verify the working and prepare a truth table.

Post Lab Subjective/Objective type Questions:

1. How JK FF need to be configured to use for counter operation?
   To configure a JK flip-flop (FF) for counter operation:
   J and K inputs: Set both J = 1 and K = 1 for toggling.
   Clock: Connect the flip-flops in a series, with the clock pulse triggering each one.
   Output: Use the Q output of one flip-flop as the clock input for the next to create a ripple counter.
   This setup makes the JK flip-flop toggle states with each clock pulse, counting binary numbers.

2. What changes are required to use the same counter as 3 bit asynchronous down counter?
   To modify a 3-bit asynchronous counter to function as a down counter:
   Invert Q outputs: Instead of feeding the Q output to the clock of the next flip-flop, use the **Q' (NOT Q)** output for the clock input of the next flip-flop.
   Initial state: Set the counter to the maximum value (e.g., 111 for a 3-bit counter) to count down.
   This makes the counter decrement with each clock pulse.

3. Draw the timing diagram of 3 bit Asynchronous up counter.



4. What is mod n concept used in counters?
   The mod-n concept in counters refers to a counter that cycles through **n distinct states** (0 to n-1) before resetting to zero. For example, a mod-4 counter counts 0, 1, 2, 3, and then resets to 0 on the next clock pulse.

5. For Mod-5 counter how many JK FFs are required?
   For a Mod-5 counter, **3 JK flip-flops** are required. This is because 23=82^3 = 823=8 is the smallest number of states greater than or equal to 5, and the extra states (5 to 7) can be reset using additional logic.

Conclusion:

We learned about the working of 3 bit Asynchronous up counter using JK Flip Flop and implemented it using IC on the kit.

Signature of faculty in-charge with Date: