Course Name:	**Digital Design Laboratory**	**Semester:**	**III**
Date of Performance:	**06/11/24**	**Batch No:**	**B2**
Faculty Name:	**Mansi Kambli**	**Roll No:**	**16010123294**
Faculty Sign & Date:		**Grade/Marks:**	**___/25**

Experiment No: 8
Title: 1-bit adder on VHDL

Aim and Objective of the Experiment:
To implement 1-bit adder on VHDL

COs to be achieved:
CO4: Implement digital networks using VHDL

Tools used:
Quartus, ModelSim

Theory:
A 1-bit adder, a fundamental component of digital circuits, performs binary addition of two 1-bit numbers. It utilizes logic gates to generate the sum and carry-out outputs. A half-adder adds two bits without considering the carry from the previous stage, while a full-adder accounts for the carry input. Using VHDL, a hardware description language, the 1-bit adder can be designed as a combinational circuit. VHDL facilitates the creation of a structural and behavioral description of the adder. In practice, this simple unit serves as a building block for constructing larger multi-bit adders, enabling arithmetic operations in microprocessors and digital systems.

Implementation Details
AND Code: and_gate.vhd library ieee;

```
library ieee;
use ieee.std_logic_1164.all;

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entity AND_ent is
port(    x: in std_logic;
         y: in std_logic;
         F: out std_logic
);
end AND_ent;

-----------------------------------------------

architecture behav1 of AND_ent is
begin

   process(x, y)
   begin
      -- compare to truth table
      if ((x='1') and (y='1')) then
            F <= '1';
         else
            F <= '0';
         end if;
   end process;

end behav1;

architecture behav2 of AND_ent is
begin

   F <= x and y;

end behav2;
```
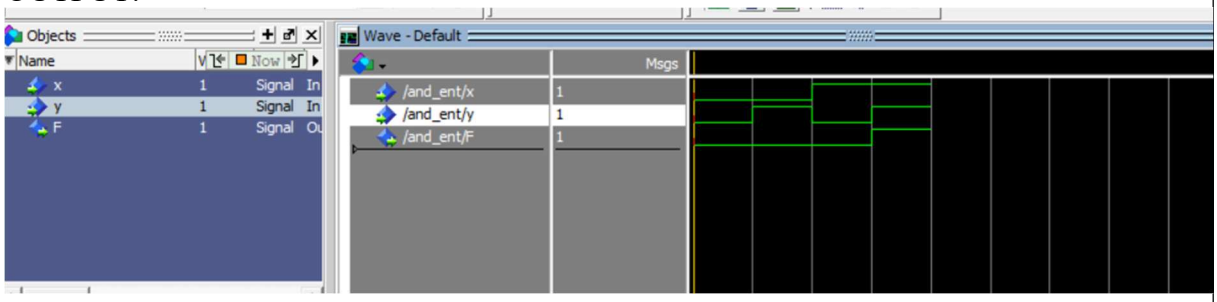
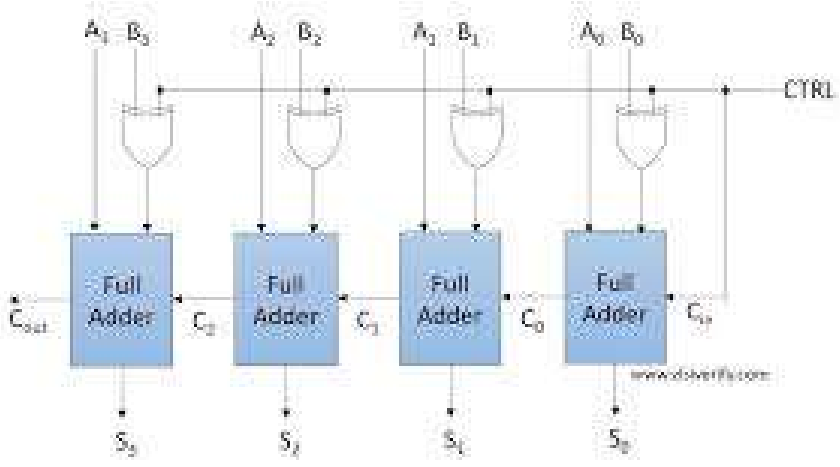

OUTPUT:



Post Lab Subjective/Objective type Questions:

1. How can 1-bit adder be used to implement a 4-bit adder?

A 4-bit adder can be implemented using four 1-bit full adders connected in series, forming a ripple-carry adder. Each 1-bit full adder adds corresponding bits from two 4-bit numbers, along with a carry input. The first adder adds the least significant bits with an initial carry of 0, producing a sum and carry. The carry is passed to the next adder, which processes the next pair of bits, and this process continues until the most significant bits are added. The final adder produces the overall carry-out and the final sum. This structure allows for the addition of two 4-bit binary numbers.



4-Bit Adder Subtractor

2. What is VHDL used for?

VHDL is used to model, simulate, and design digital systems such as integrated circuits (ICs), FPGAs, and other hardware components. It allows engineers to describe the behavior and structure of electronic systems at different abstraction levels, from algorithmic to gate-level implementation. VHDL enables the simulation of hardware behavior before physical implementation, making it essential for verifying designs, reducing errors, and optimizing digital systems in the development process. It is commonly used in industries like telecommunications, computer hardware, and automotive systems for designing complex digital systems.

Conclusion:

In this experiment we learned how to implement circuits/gates using VHDL, ie code/algorithms, We learned how to make a 1 bit adder using code.

Signature of faculty in-charge with Date: