Flip Flops

TRUTH TABLE FOR SR F/F

S	R	QN	QN+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

NO CHANGE

RESET

SET

PROHIBITED STATE

TRUTH TABLE FOR JK F/F

J	K	QN	QN+1
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

NO CHANGE

J VALUE FORWARDED

TOGGLE CASE

TRUTH TABLE FOR T F/F

T	QN	QN+1
0	0	0
0	1	0
1	0	1
1	1	1

NO CHANGE

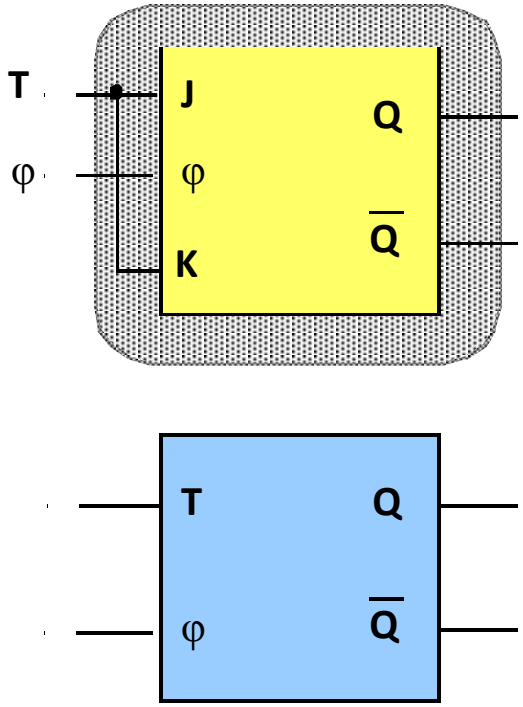
TOGGLE CASE

TRUTH TABLE FOR D F/F

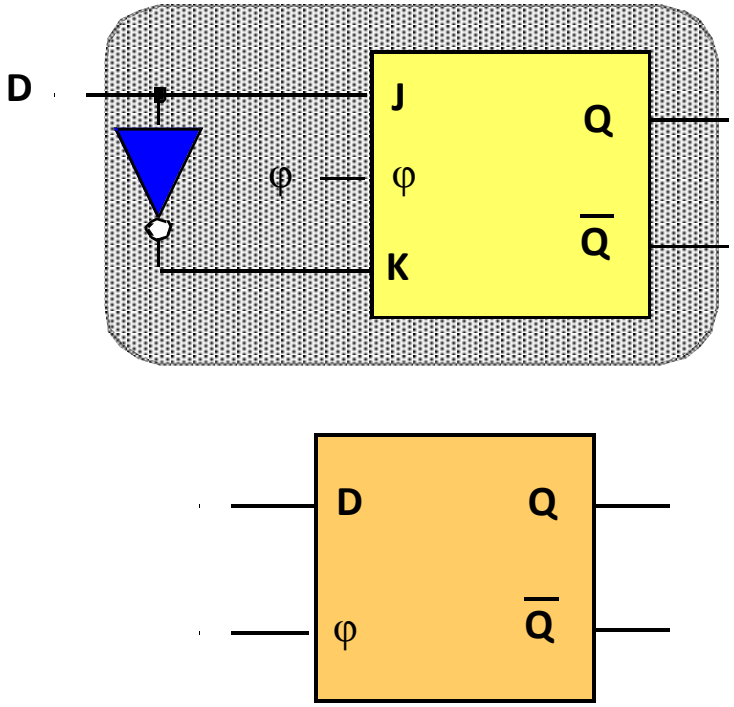
D	QN	QN+1
0	0	0
0	1	0
1	0	1
1	1	1

INPUT VALUE FORWARDED WITH SOME DELAY

Other Flip Flops



Toggle Flip-Flop



Delay Flip-Flop (D-latch)

EXCITATION TABLE FOR F/F

PRESSENT STATE	NEXT STATE	S	R	J	K	T	D
0	0	0	X	0	X	0	0
0	1	1	0	1	X	1	1
1	0	0	1	X	1	1	0
1	1	X	0	X	0	0	1

CONVERSION FROM ONE F/F TO ANOTHER

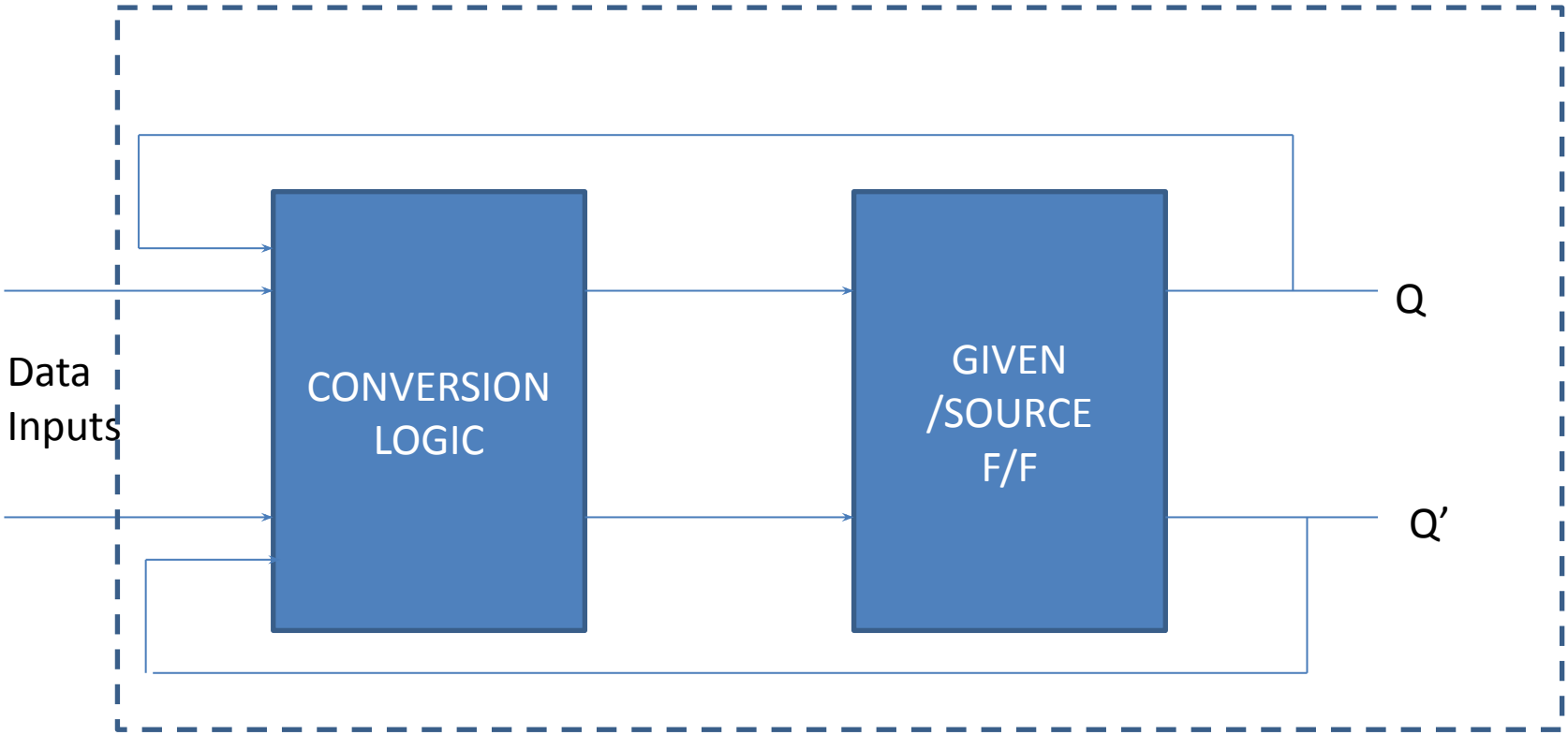
STEP1-Combine the excitation tables for both Flipflops, make a truth table.

The truth table has input values of target f/f as inputs of truth table and Inputs of Given or source f/f as outputs of the truth table.

STEP2-Draw the Kmap for each output & obtain the simplified expression.

STEP3-Implement using logic gates.

CONVERSION FROM ONE F/F TO ANOTHER



CONVERSION FROM SR F/F TO D F/F

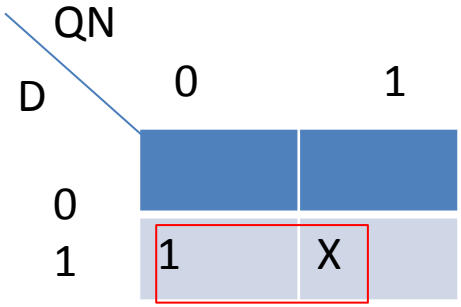
- Truth table for SR to D Conversion

D	PRESENT STATE QN	NEXT STATE QN+1	S	R
0	0	0	0	X
1	0	1	1	0
0	1	0	0	1
1	1	1	X	0

Entries from Excitation Table of D FF

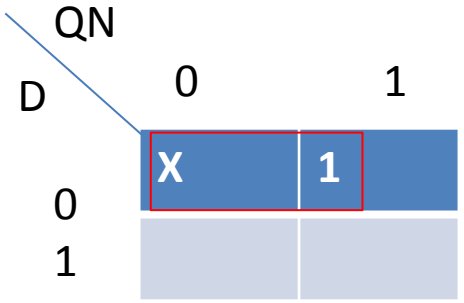
Entries from Excitation Table of SR FF

Kmaps for S&R



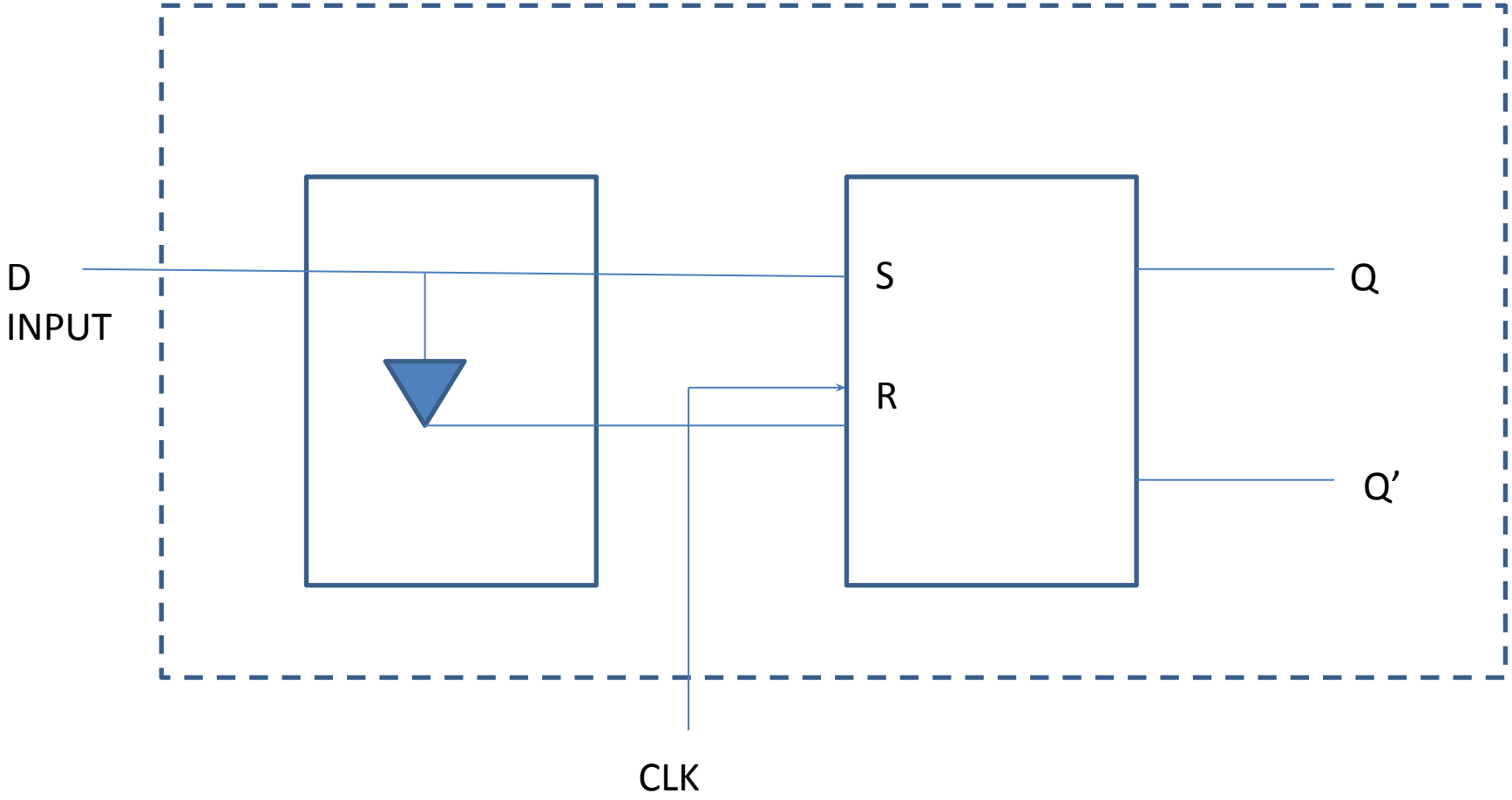
S=D

Kmap for S



R=D’

Kmap for R


D
INPUT
S
R
Q
Q’
CLK

REGISTER

Register is composed of a group of flip flops to store data.

N f/f are used for storing N bit word.

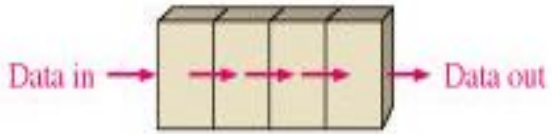
1 f/f can store 1 bit of information

SHIFT REGISTERS

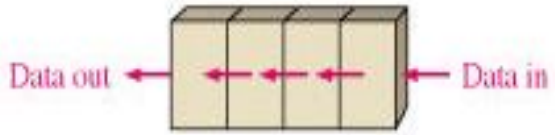
- Shift registers are a type of sequential logic circuit.
- They are a group of flip-flops connected in a chain so that the output from one flip-flop becomes the input of the next flip-flop.
- All flip-flop is driven by a common clock, and all are set or reset simultaneously.

- Shift registers are used for
  - Data Storage
  - Data movement
  - Arithmetic & Logic Operations

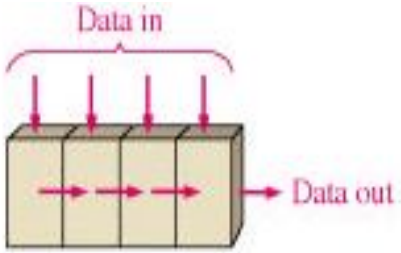
MODES OF OPERATION OF A SHIFT REGISTER



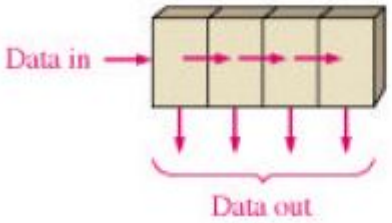
(a) Serial in/shift right/serial out



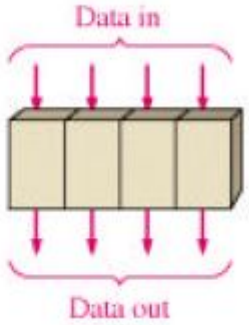
(b) Serial in/shift left/serial out



(c) Parallel in/serial out

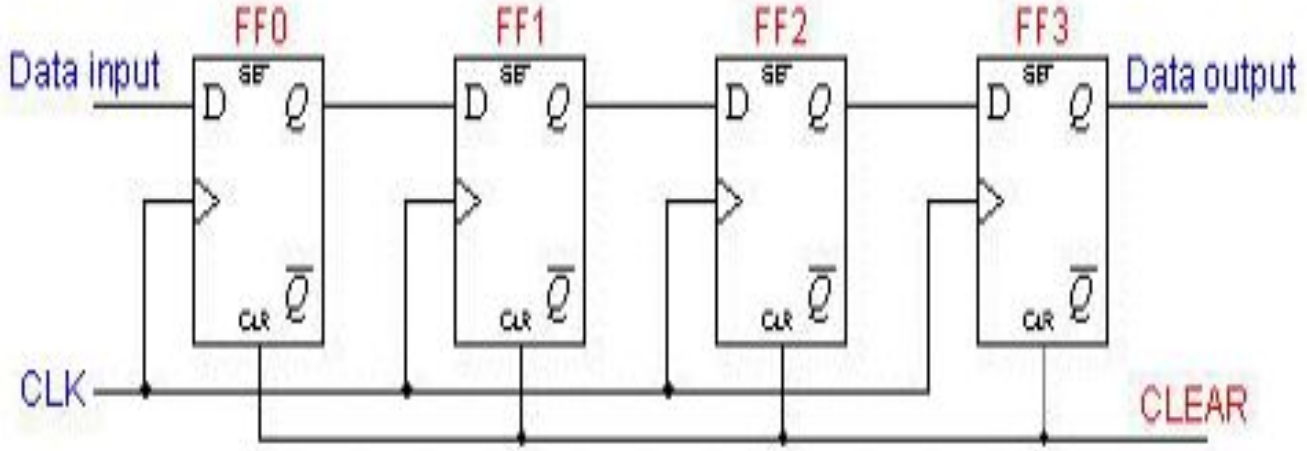


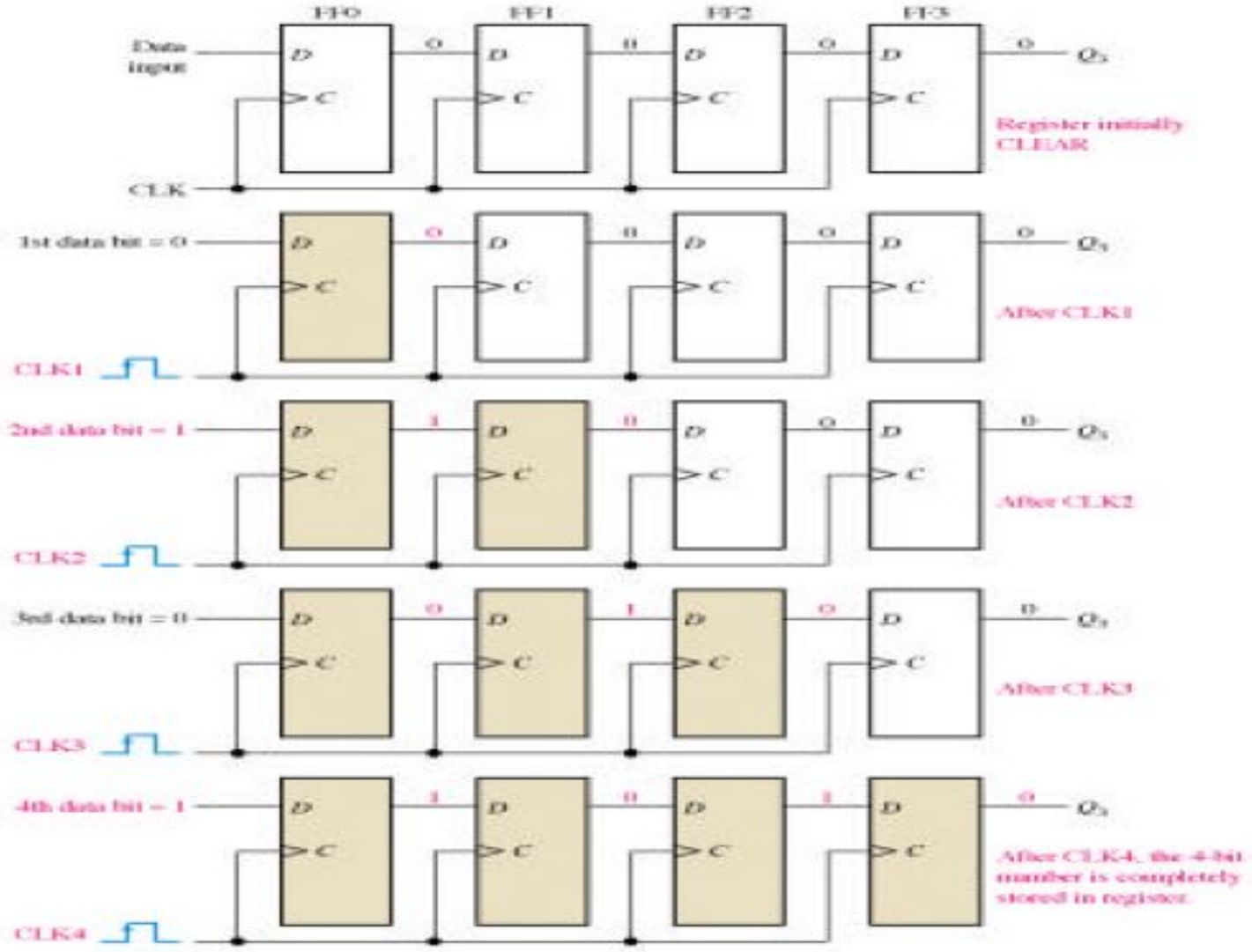
(d) Serial in/parallel out



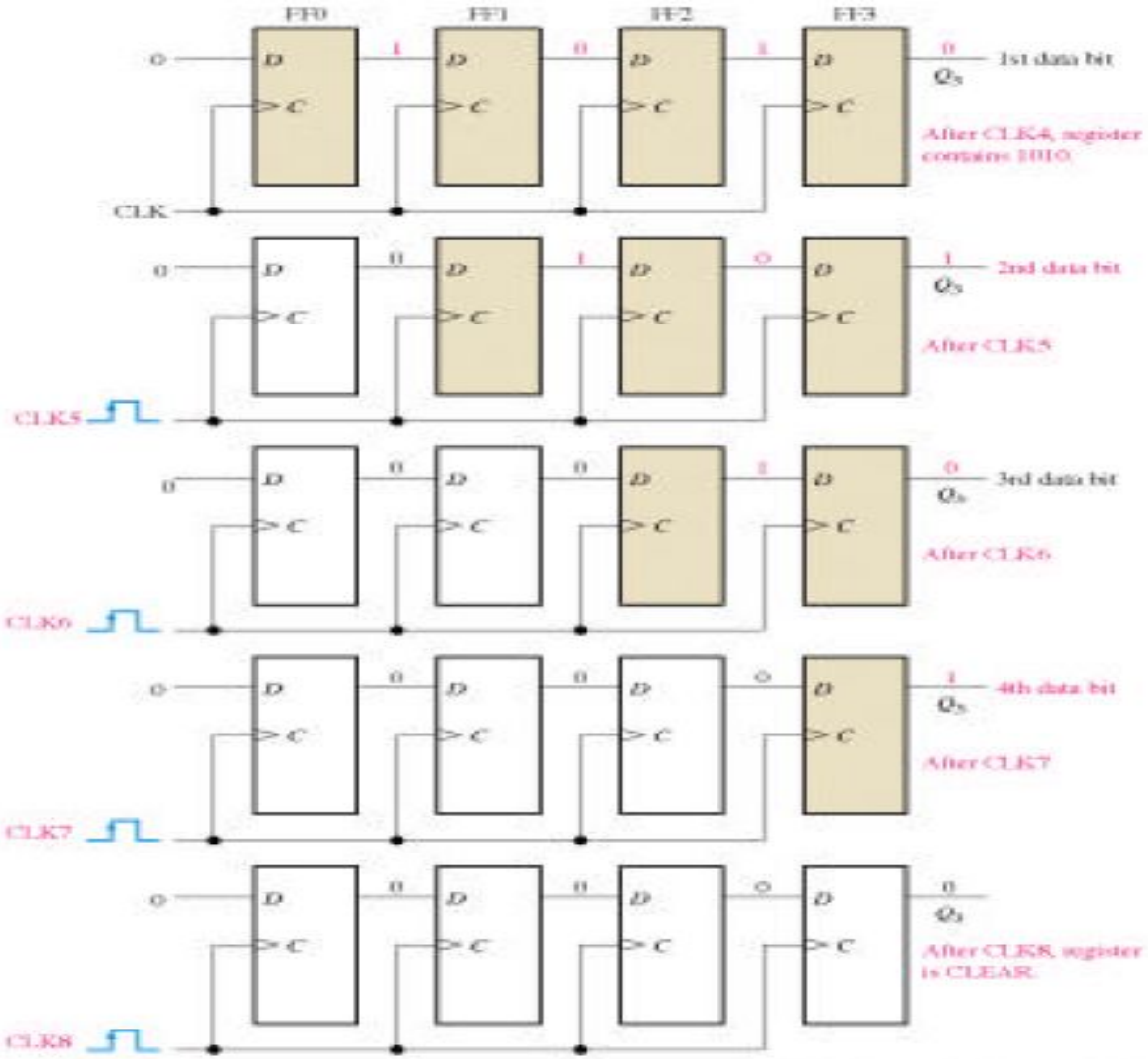
(e) Parallel in/parallel out

SISO(SHIFT RIGHT MODE)



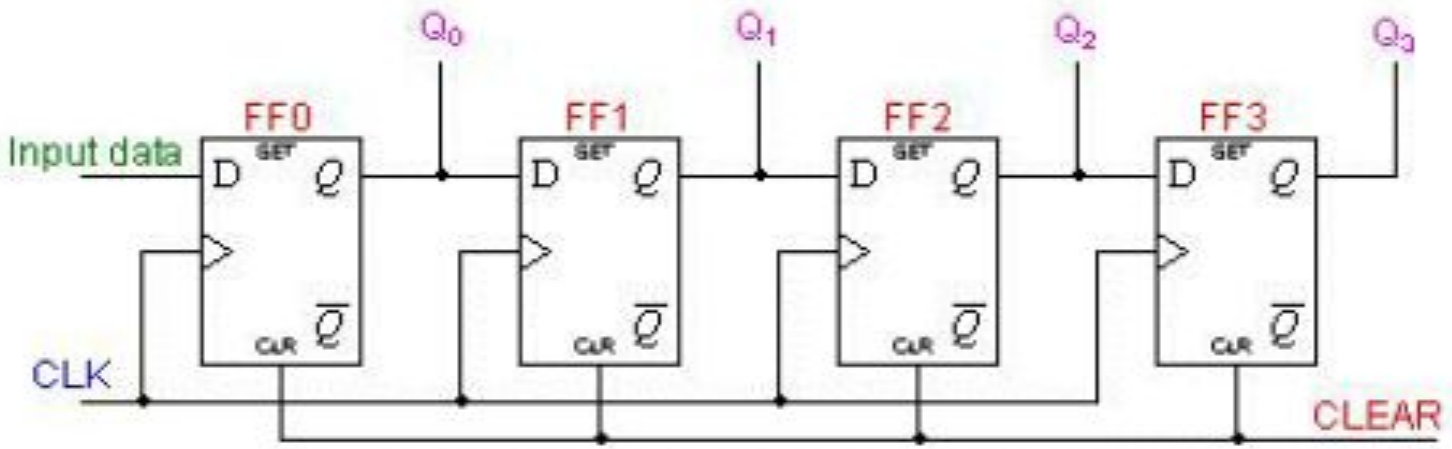


Four bits (1010) being entered serially into the register.

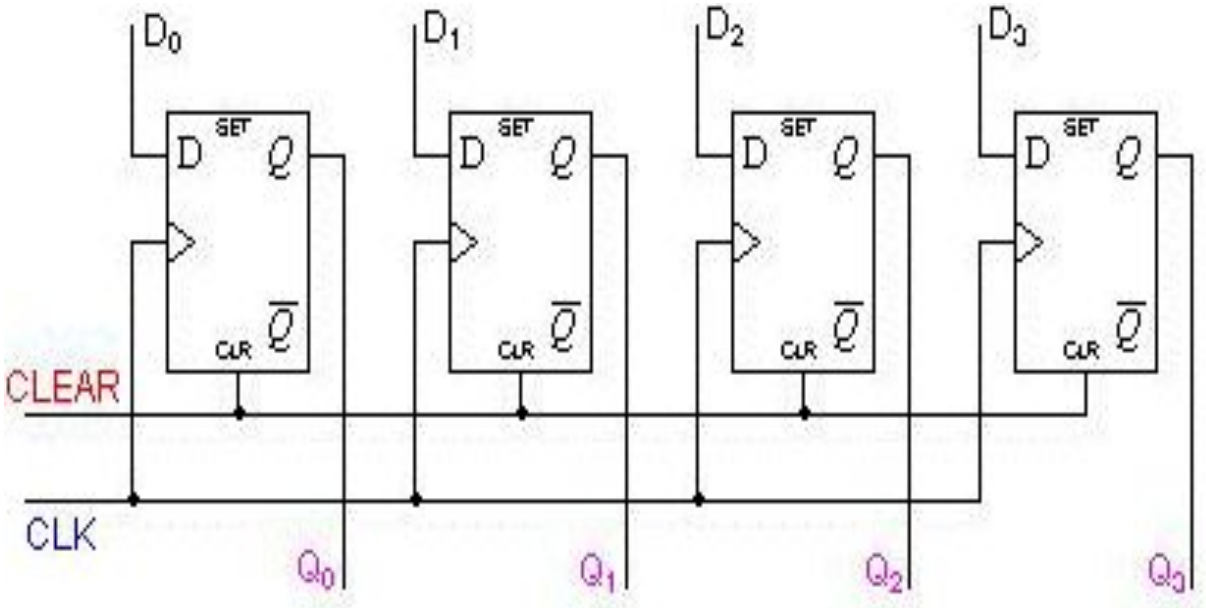


Four bits (1010) being serially shifted out of the register and replaced by all zeros

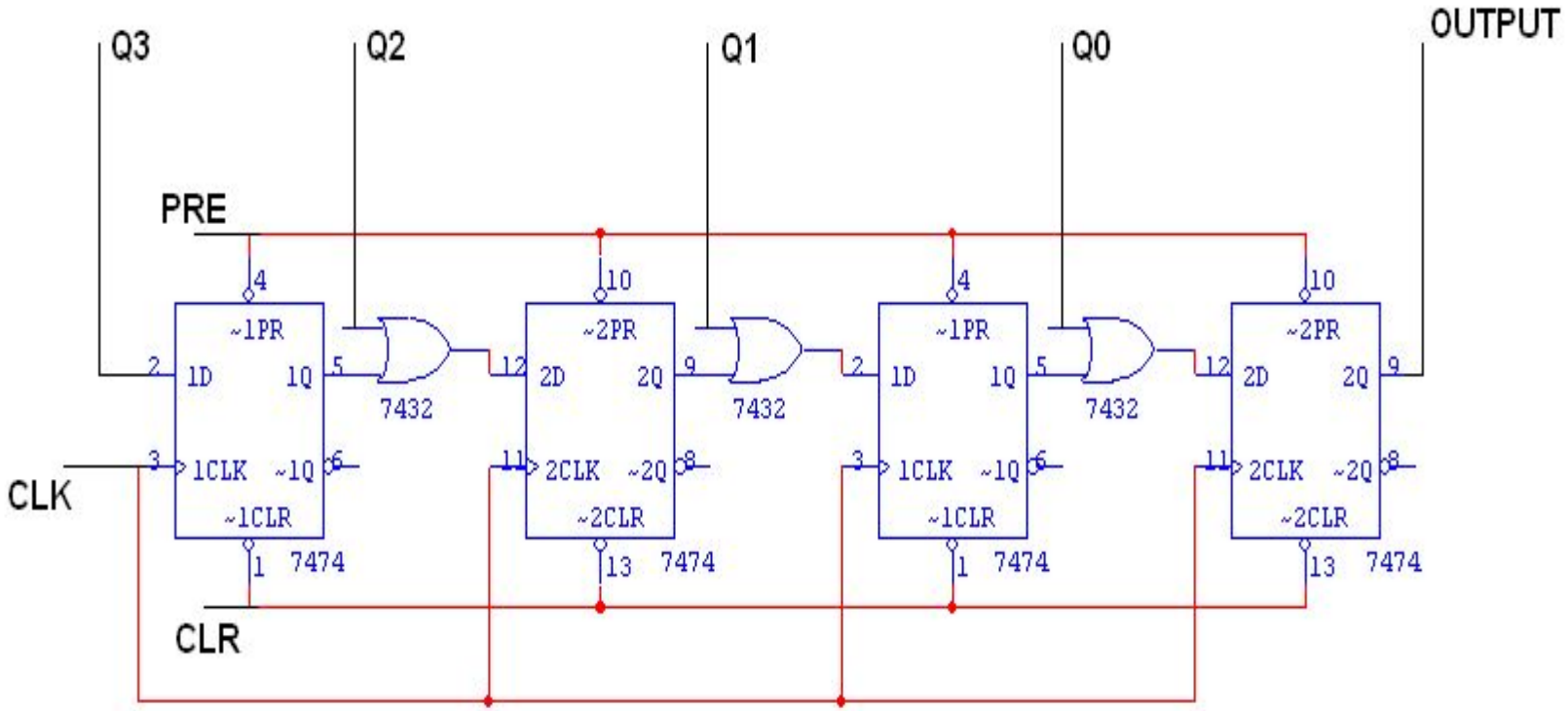
SIPO (SERIAL INPUT PARALLEL OUTPUT)



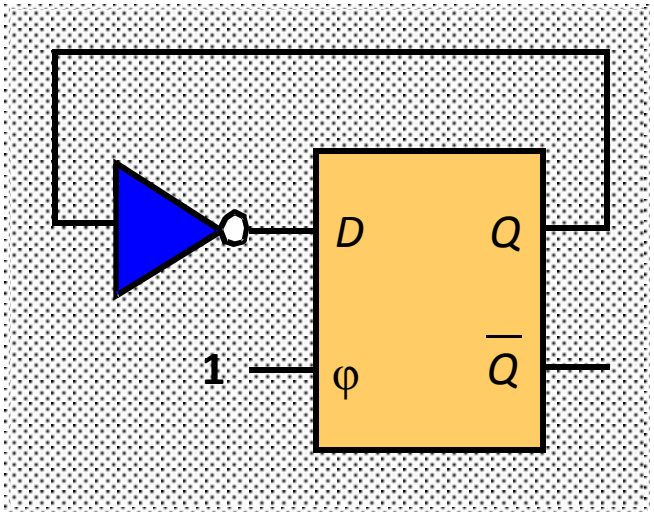
PIPO(PARALLEL IN PARALLEL OUT)

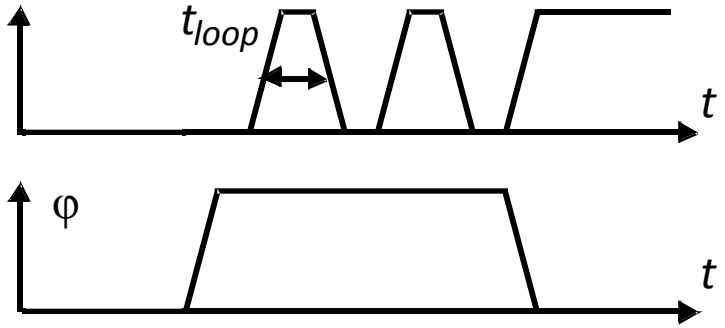


PISO(PARALLEL IN SERIAL OUT)



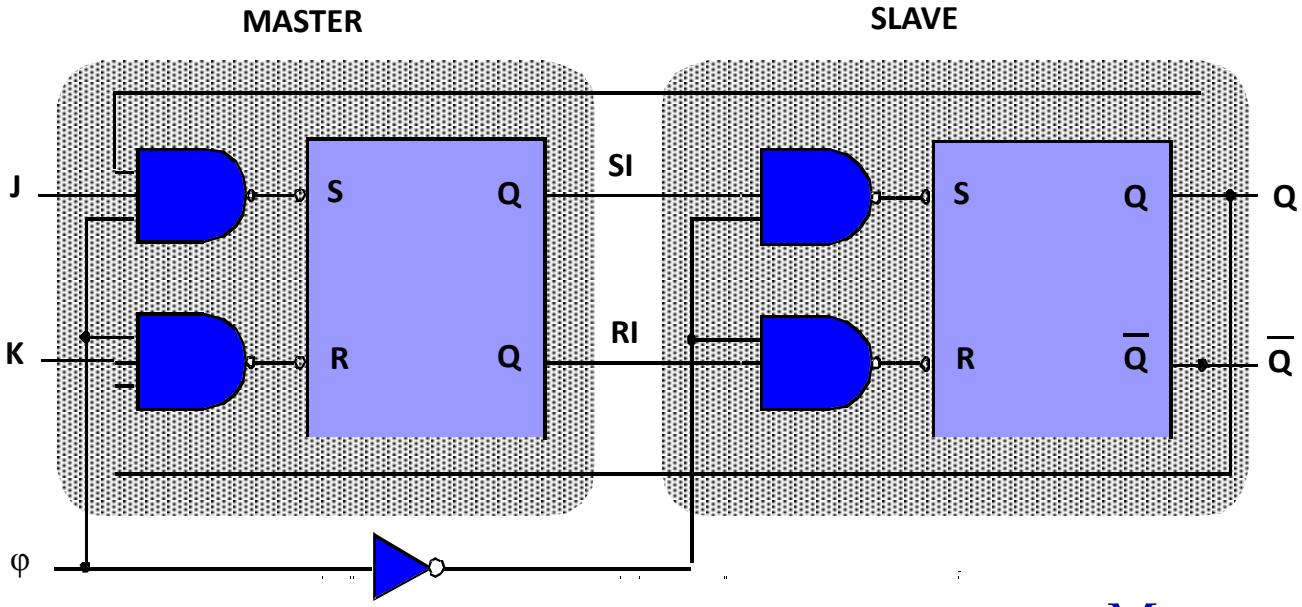
Race Problem

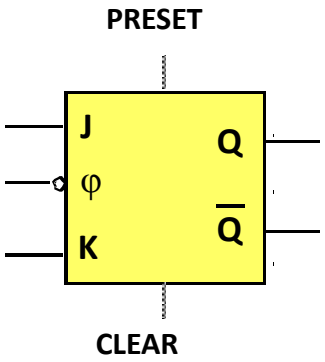




Signal can race around during φ = 1

Master-Slave Flip Flop Implementation





Master transmits the signal to the output during the high clock phase and slave is waiting for the clock to change this prevents race conditions