JOINT INSTITUTE
交大密西根学院

ECE2700J Introduction to Logic Design

Homework 4

Assigned: October 28, 2024

Due: November 4, 2024, 4:00pm

Submit a hard copy before the lecture begins.

1. (25 points) Design a 4-bit up-counter with a `CE` (count enable) and `load` control inputs and an additional output `upper` that outputs a `1` whenever the counter is within the upper half of the counter's range, `8` to `15`, otherwise `0`. Design the counter using MUXes, gates, and D flip flops without any external control signal (reset or set). Model the circuit in Verilog HDL using the aforementioned components. Simulate your Verilog module and show the simulation results as timing diagram.
2. (15 points) Design a 4-bit up/down-counter that has four control inputs: `cnt_up` enables counting up, `cnt_down` enables counting down, `clear` synchronously resets the counter to all 0s, and `set` synchronously sets the counter to all 1s. if two or more control inputs are 1s, the counter retains its current count value. Use a parallel-load register as a building block. Use components to draw schematic. Verilog modeling is not needed.
3. (10 points) Design a circuit that outputs a 1 every 99 clock cycles:
   (a) Using an up-counter with a synchronous clear control input and using extra logic if necessary; (4 points)
   (b) Using a down-counter with parallel load, and using extra logic if necessary; (4 points)
   (c) What are the tradeoffs between the two designs from parts (a) and (b)? (2 points)
   Use components to draw schematic.

NOTE: the following problems are optional and won't be graded.

4. Design a 4-bit down-counter that has three control inputs: `CE` enables counting down, `clear` synchronously resets the counter to all 0s, and `set` synchronously sets the counter to all 1s. Design the counter using MUXes, gates, and D flip flops without any external control signal (reset or set). Model the circuit in Verilog HDL. Simulate your Verilog module.

5. Create a clock divider that converts a 14 MHz clock into a 1 MHz clock. Use a down-counter with parallel load. Clearly indicate the width of the down-counter and the counter's load value. Synchronize any gated clock. Use components to draw schematic.