JOINT INSTITUTE
交大密西根学院

ECE2700J Introduction to Logic Design

Homework 3

Assigned: October 21, 2024

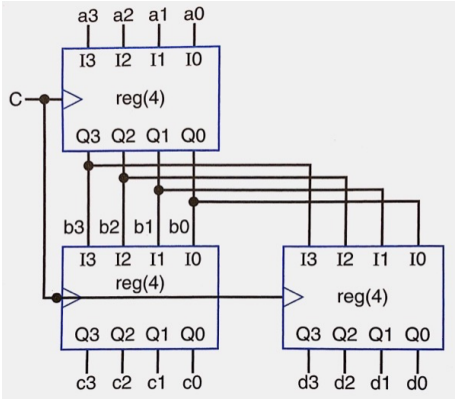
Due: October 28, 2024, 4:00pm

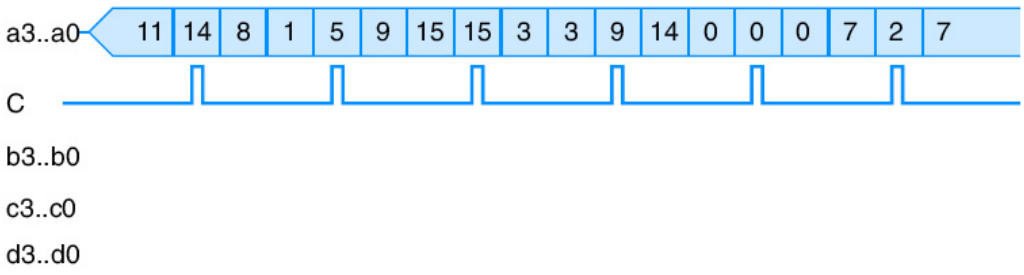
Submit a hard copy before the lecture begins.

***Note**: you may ignore the propagation delays when drawing a timing diagram unless required differently.*

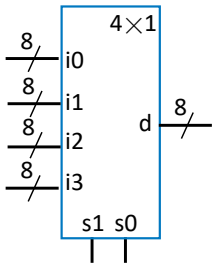
1. (15 points) Design a 4-bit register with an external signal "R_L", such that when R_L = 1, content of the 4-bit register is rotated to the left by 1 bit upon a clock edge (e.g. 1011 becomes 0111), and when R_L = 0, the register works as normal. Use building blocks.

2. (15 points) Consider three 4-bit registers connected as in the figure on right. Assume the initial values in the registers are unknown. Trace the behavior of the registers by completing the following timing diagram.



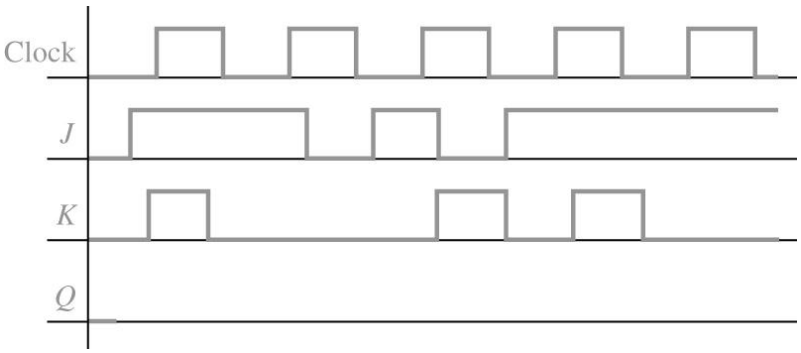


3. (20 points) Describe in Verilog an 8-bit 4-to-1 MUX implemented with 2-to-1 MUXes. Simulate your design with a testbench.

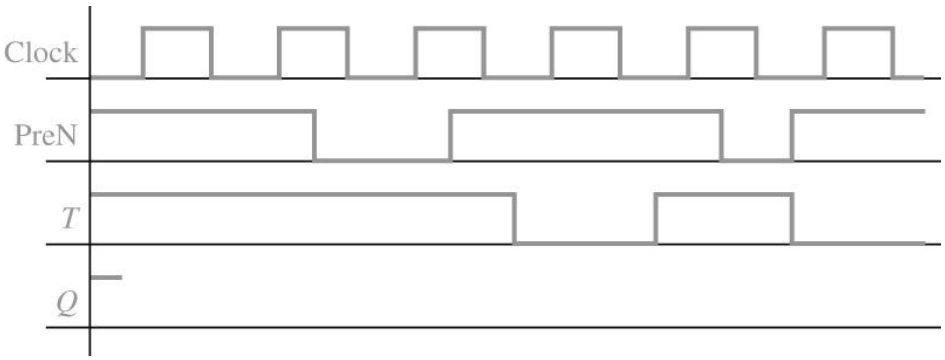


NOTE: the following problems are optional and won't be graded.

4. Model the circuit described in Problem 1 with Verilog HDL. Write a testbench to simulate your design.
5. Fill in the timing diagram below for a falling-edge triggered J-K flip-flop. Assume Q begins at 0.



6. Fill in the following timing diagram for a rising-edge triggered T flip-flop with an asynchronous active-low preset input (PreN, equivalent to set). Assume Q begins at 1.



7. Model the T flip-flop described in above problem in Verilog HDL. Then write a testbench to simulate your designed module and generate the exactly same timing diagram.