

Experiment 2

Terminal Commands:

- gcc -O0 -fno-inline -fno-strict-aliasing {program.c} -o {program.out}
- likwid-perfctr --force -c 0 -g ICACHE ./{program.out} > {output_file.txt}

1. Merging Arrays:

Before:

```
#include <stdio.h>

#define SIZE 3

int val[SIZE];
int key[SIZE];

int main(){
    printf("%d\n",&val);
    printf("%d",&key);
    return 0;
}
```

```
CPU name:   Intel(R) Xeon(R) E-2224 CPU @ 3.40GHz
CPU type:   Intel Coffeelake processor
CPU clock:  3.41 GHz
```

```
6295624
6295640
```

Group 1: ICACHE

Event	Counter	HWThread 0
INSTR_RETIRED_ANY	FIXC0	6289
CPU_CLK_UNHALTED_CORE	FIXC1	25578
CPU_CLK_UNHALTED_REF	FIXC2	20732
ICACHE_64B_IPTAG_ALL	PMC0	6587
ICACHE_64B_IPTAG_MISS	PMC1	1363
ICACHE_64B_IPTAG_STALL	PMC2	3839

Metric	HWThread 0
Runtime (RDTSC) [s]	0.0006
Runtime unhaltd [s]	7.508077e-06
Clock [MHz]	4203.0371
CPI	4.0671
L1I request rate	1.0474
L1I miss rate	0.2167
L1I miss ratio	0.2069
L1I stalls	3839
L1I stall rate	0.6104

After:

```
#include <stdio.h>

#define SIZE 3

struct merge{
    int val;
    int key;
};

int main(){
    struct merge merged_array[SIZE];
    printf("%d\n",&(merged_array->val));
    printf("%d",&(merged_array->key));
    return 0;
}
```

```
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```

```
214476848
214476852
```

Group 1: ICACHE

Event	Counter	HWThread 0
INSTR_RETIRED_ANY	FIXC0	104871
CPU_CLK_UNHALTED_CORE	FIXC1	223456
CPU_CLK_UNHALTED_REF	FIXC2	195818
ICACHE_64B_IPTAG_ALL	PMC0	60587
ICACHE_64B_IPTAG_MISS	PMC1	3675
ICACHE_64B_IPTAG_STALL	PMC2	19023

Metric	HWThread 0
Runtime (RDTSC) [s]	0.0006
Runtime unhalted [s]	0.0001
Clock [MHz]	3889.0075
CPI	2.1308
L1I request rate	0.5777
L1I miss rate	0.0350
L1I miss ratio	0.0607
L1I stalls	19023
L1I stall rate	0.1814

Before Miss Ratio = 20.6%

After Miss Ratio = 6%

2. Loop Interchange:

Before:

```
for (int j=0;j<100;j++){  
    for (int i=0;i<5000;i++){  
        x[i][j]*=2;  
    }  
}
```

```
CPU name: Intel(R) Xeon(R) E-2224 CPU @ 3.40GHz  
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```

Group 1: ICACHE

Event	Counter	HWThread 0
INSTR_RETIRED_ANY	FIXC0	332
CPU_CLK_UNHALTED_CORE	FIXC1	15378
CPU_CLK_UNHALTED_REF	FIXC2	12212
ICACHE_64B_IPTAG_ALL	PMC0	858
ICACHE_64B_IPTAG_MISS	PMC1	493
ICACHE_64B_IPTAG_STALL	PMC2	4022

Metric	HWThread 0
Runtime (RDTSC) [s]	0.0036
Runtime unhaltd [s]	4.512305e-06
Clock [MHz]	4291.5530
CPI	46.3193
L1I request rate	2.5843
L1I miss rate	1.4849
L1I miss ratio	0.5746
L1I stalls	4022
L1I stall rate	12.1145

After:

```
for (int i=0;i<5000;i++){  
    for (int j=0;j<100;j++){  
        x[i][j]*=2;  
    }  
}
```

```
-----  
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-----
```

Group 1: ICACHE

Event	Counter	HWThread 0
INSTR_RETIRED_ANY	FIXC0	6330
CPU_CLK_UNHALTED_CORE	FIXC1	34975
CPU_CLK_UNHALTED_REF	FIXC2	27548
ICACHE_64B_IPTAG_ALL	PMC0	8618
ICACHE_64B_IPTAG_MISS	PMC1	2188
ICACHE_64B_IPTAG_STALL	PMC2	7508

Metric	HWThread 0
Runtime (RDTSC) [s]	0.0031
Runtime unhaltd [s]	1.026273e-05
Clock [MHz]	4326.7561
CPI	5.5253
L1I request rate	1.3615
L1I miss rate	0.3457
L1I miss ratio	0.2539
L1I stalls	7508
L1I stall rate	1.1861

Before Miss Ratio = 57.4%

After Miss Ratio = 25.3%

3. Loop Fusion:

Before:

```
for(int i=0;i<N;i++){
    for(int j=0;j<N;j++){
        a[i][j]=1/b[i][j]*c[i][j];
    }
}
for(int i=0;i<N;i++){
    for(int j=0;j<N;j++){
        d[i][j]=a[i][j]+c[i][j];
    }
}
```

```
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```

Group 1: ICACHE

Event	Counter	HWThread 0
INSTR_RETIRED_ANY	FIXC0	310
CPU_CLK_UNHALTED_CORE	FIXC1	14251
CPU_CLK_UNHALTED_REF	FIXC2	11786
ICACHE_64B_IFTAG_ALL	PMC0	864
ICACHE_64B_IFTAG_MISS	PMC1	478
ICACHE_64B_IFTAG_STALL	PMC2	3211

Metric	HWThread 0
Runtime (RDTSC) [s]	0.0005
Runtime unhaltd [s]	4.181863e-06
Clock [MHz]	4120.5433
CPI	45.9710
L1I request rate	2.7871
L1I miss rate	1.5419
L1I miss ratio	0.5532
L1I stalls	3211
L1I stall rate	10.3581

After:

```
for(int i=0;i<N;i++){  
    for(int j=0;j<N;j++){  
        a[i][j]=1/b[i][j]*c[i][j];  
        d[i][j]=a[i][j]+c[i][j];  
    }  
}
```

```
-----  
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-----
```

Group 1: ICACHE

Event	Counter	HWThread 0
INSTR_RETIRED_ANY	FIXC0	6391
CPU_CLK_UNHALTED_CORE	FIXC1	25428
CPU_CLK_UNHALTED_REF	FIXC2	20874
ICACHE_64B_IPTAG_ALL	PMC0	7255
ICACHE_64B_IPTAG_MISS	PMC1	1283
ICACHE_64B_IPTAG_STALL	PMC2	3204

Metric	HWThread 0
Runtime (RDTSC) [s]	0.0006
Runtime unhaltd [s]	7.461238e-06
Clock [MHz]	4151.5264
CPI	3.9787
L1I request rate	1.1352
L1I miss rate	0.2008
L1I miss ratio	0.1768
L1I stalls	3204
L1I stall rate	0.5013

Before Miss Ratio = 55.3%

After Miss Ratio = 17.6%

4. Blocking: Before:

```
for(int i=0;i<N;i++){  
    for(int j=0;j<N;j++){  
        int r=0;  
        for(int k=0;k<N;k++){  
            r+=(y[i][k]*z[k][j]);  
        }  
        x[i][j]=r;  
    }  
}
```

```
-----  
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CPU type:   Intel Coffeelake processor  
CPU clock:  3.41 GHz  
-----
```

Group 1: ICACHE

Event	Counter	HWThread 0
INSTR_RETIRED_ANY	FIXC0	6378
CPU_CLK_UNHALTED_CORE	FIXC1	27235
CPU_CLK_UNHALTED_REF	FIXC2	22436
ICACHE_64B_IFTAG_ALL	PMC0	6789
ICACHE_64B_IFTAG_MISS	PMC1	1301
ICACHE_64B_IFTAG_STALL	PMC2	3427

Metric	HWThread 0
Runtime (RDTSC) [s]	0.0005
Runtime unhaltd [s]	7.994511e-06
Clock [MHz]	4135.3991
CPI	4.2701
L1I request rate	1.0644
L1I miss rate	0.2040
L1I miss ratio	0.1916
L1I stalls	3427
L1I stall rate	0.5373

After:

```
for(int jj=0;jj<N;jj+=B){
    for(int kk=0;kk<N;kk+=B){
        for(int i=0;i<N;i+=1){
            for(int j=jj;j<min(jj+B,N);j++){
                int r=0;
                for(int k=kk;k<min(kk+B,N);k++){
                    r+=(y[i][k]*z[k][j]);
                }
                x[i][j]=x[i][j]+r;
            }
        }
    }
}
```

```
-----
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-----
```

Group 1: ICACHE

Event	Counter	HWThread 0
INSTR_RETIRED_ANY	FIXC0	5198170
CPU_CLK_UNHALTED_CORE	FIXC1	2331187
CPU_CLK_UNHALTED_REF	FIXC2	1891582
ICACHE_64B_IPTAG_ALL	PMC0	1151711
ICACHE_64B_IPTAG_MISS	PMC1	50706
ICACHE_64B_IPTAG_STALL	PMC2	1800

Metric	HWThread 0
Runtime (RDTSC) [s]	0.0006
Runtime unhaltd [s]	0.0007
Clock [MHz]	4199.9848
CPI	0.4485
L1I request rate	0.2216
L1I miss rate	0.0098
L1I miss ratio	0.0440
L1I stalls	1800
L1I stall rate	0.0003

Before Miss Ratio = 19.16%

After Miss Ratio = 4.4%