Experiment-3 Results

One Level Cache (from Exp. 1):

Components:
L1 Cache, Main Memory

Results:

i) Test 1:

Total Access Sequence = 20
Access Sequence File = cache_replacement_test.txt

Cache Searches: 1021
Cache Hits: 12
Cache Misses: 8
Cache Discards: 0

Main Memory Searches: 8

Total Searches = 1029

ii) Test 2:

Total Access Sequence = 80000
Access Sequence File = access_seq_rand.txt

Cache Searches: 9847167
Cache Hits: 2450
Cache Misses: 77550
Cache Discards: 77425

Main Memory Searches: 77550

Total Searches = 9924717

* Prefetch cache is a combination of ISB and DSB. It fetches 2 adjacent blocks from memory at a time
** Writes occur randomly (currently 20%)

Two Level Cache:

Components:

L1 Cache, Write Buffer, Victim Cache, Prefetch Cache, L2 Cache, Main Memory

Results:

i) Test 1:

Total Access Sequences = 20

Access Sequence File = cache_replacement_test.txt

L1:

Searches: 20
Hits: 8
Misses: 12
Swaps: 8

Write Buffer:

Searches: 42
Hits: 3
Misses: 9

Victim:

Searches: 33
Hits: 1
Misses: 8

Prefetch* Cache:

Searches: 22
Hits: 2
Misses: 6

L2:

Searches: 24
Hits: 0
Misses: 6
Swaps: 1

Main Memory:

Searches: 6

Total Writes** = 7

Total Searches = 147

* Prefetch cache is a combination of ISB and DSB. It fetches 2 adjacent blocks from memory at a time
** Writes occur randomly (currently 20%)

ii) Test 2:

    Total Access Sequence = 80000
    Access Sequence File = access_seq_rand.txt
    L1:

        Searches: 80000
        Hits: 2443
        Misses: 77557
        Swaps: 77432

    Write Buffer:

        Searches: 310115
        Hits: 81
        Misses: 77476
    Victim:

        Searches: 309801
        Hits: 74
        Misses: 77402
    Prefetch* Cache:

        Searches: 618420
        Hits: 158
        Misses: 77244

    L2:

        Searches: 283135
        Hits: 17094
        Misses: 60150
        Swaps: 59150

    Main Memory:
        Searches: 60150

    Total Writes** = 16195
    Total Searches = 1661621

* Prefetch cache is a combination of ISB and DSB. It fetches 2 adjacent blocks from memory at a time
** Writes occur randomly (currently 20%)