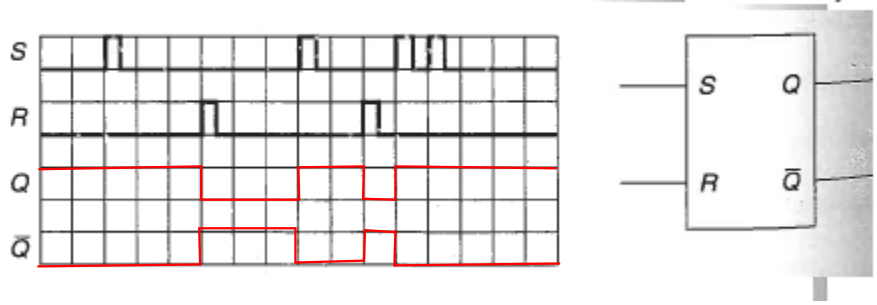
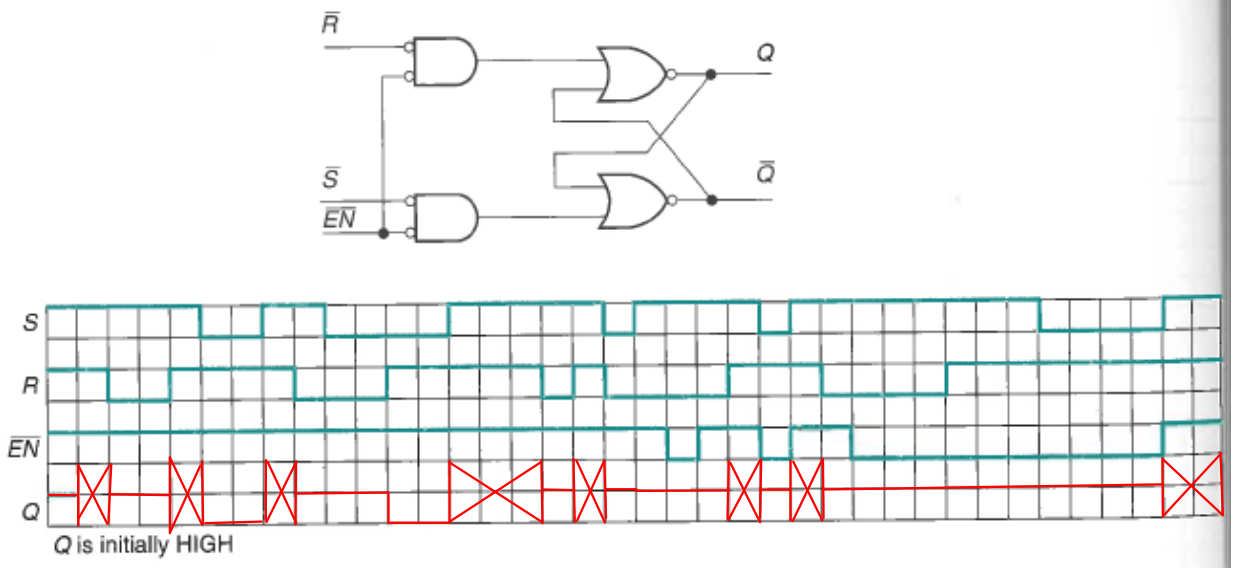
Problem 1:

Complete the timing diagram for the active-HIGH latch shown. The latch is initially set.



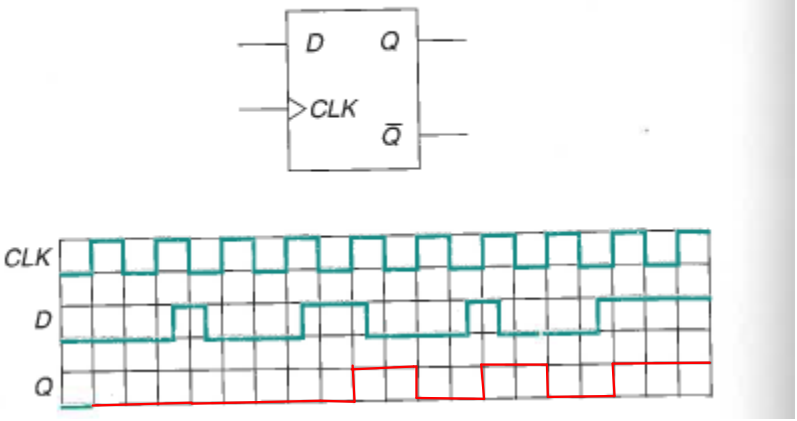
Problem 2: You may have forbidden inputs, just put 'X' for them on the output.

Complete the timing diagram for the gated latch shown in



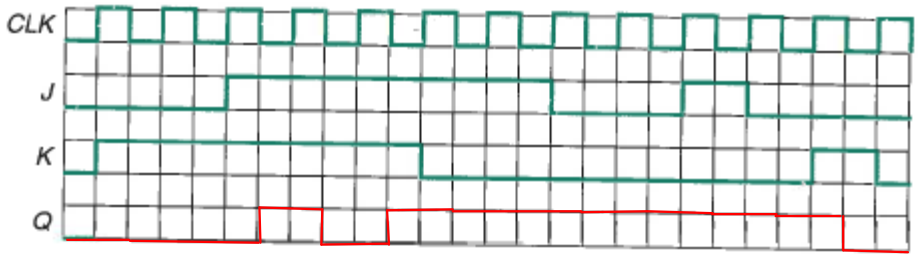
Problem 3:

Complete the timing diagram for a positive edge-triggered D flip-flop if the waveforms shown are applied to the flip-flop inputs.



Problem 4

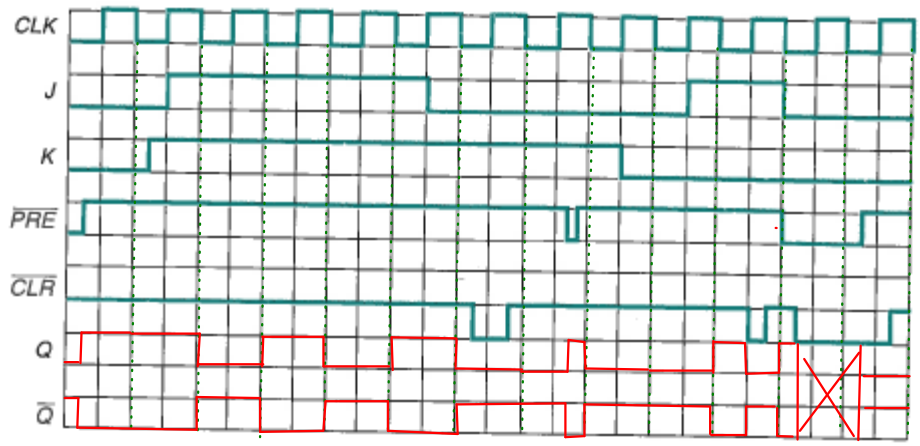
The waveforms are applied to a negative edge-triggered JK flip-flop. Complete the timing diagram by drawing the Q waveform.



Problem 5

You may have forbidden inputs, just put 'X' for them on the output.

The waveforms shown are applied to a negative edge-triggered JK flip-flop. The flip-flop's Preset and Clear inputs are active LOW. Complete the timing diagram by drawing the output waveforms.



Problem 6

The T and CLK waveforms for a positive edge triggered T flip-flop are shown Complete the timing diagram.