Lab 08

Part B – Multiplexed Hexadecimal to 7-Segment

Description

In this lab module, you will combine the functionality of the hexadecimal to 7-segment converter from Lab 06B with the multiplexed display introduced in 08A.

As usual, for this lab module, you will require a PC with a USB-A port to program the FPGA development board.

Procedure

Project Creation

1. Download `lab08b.vhd` and `lab08b.xdc` from Canvas and place them in a new folder titled `lab08b`.
2. Open Vivado and create a new project titled appropriately.
   - For your convenience, the board identifier is `xc7a35tcpg236-1`.
     - You can also find the board with the same options as before: `General Purpose`, `Artix-7`, `cpg236`, `-1`.

Hardware Review and Upload

3. Open the file in the editor, and follow along with the instructor to review the hardware description.
4. `Open Elaborated Design`, review the schematic alongside the instructor, and take screenshots for your report.
5. Run synthesis and implementation and then generate the bitstream to program the device. Then, open the Hardware Manager.
   - Take a screenshot of the resource utilization (LUTs and FFs) to add to your report.
6. Before proceeding, plug the FPGA development board into your computer using the provided Micro-USB to USB-A cable.
7. At the top, in the green banner (or under the `Open Hardware Manager` dropdown) click `Open Target`, then `Auto Connect`.

8. Once the device is connected, select `Program Device` (in either of the locations where `Open Target` was previously).
    - See 06B-handout for troubleshooting steps, or ask the instructor or TA.
9. Click `Program` to upload the bitstream to the FPGA.

Hardware Testing and Analysis

10. Note that there are 16 switches on the board.
    - Each set of four switches are the input of one of the four 7-segment displays.
    - By looking at the XDC and playing with the switches, determine which four switches are the input of which display.
    - In your report, state your answer, and indicate which switch provides the most significant bit of the input.
    - Choose a set of inputs and take a picture of the board.

Deliverables

- Include as part of your **informal report**:
    - A screenshot of the Elaborated Design schematic (Step 4)
    - A screenshot of the FPGA resource utilization (LUTs, FFs) (Step 5)
    - A picture of the FPGA development board (Step 10)
    - Answer to (10)

Outcomes

- Practice working with VHDL.
- Practice using Vivado for hardware synthesis and implementation.
- Practice programming and testing a hardware description on an FPGA development board.
- Understand how a seven-segment display functions.
- Understand the role of multiplexing in the seven-segment display module.