Lab 12

Part A – 4 Bit and 16 Bit CLA Adders

Description

- In this module, you will implement a 4-bit carry-look-ahead adder and then incorporate it into a 16-bit CLA adder to understand how CLA adders are recursively structured.

Procedure

Project Creation

1. Download `lab12a.vhd`, `display_controller.vhd`, `cla_16.vhd`, `cla_4.vhd`, `cla_group_logic.vhd`, `partial_full_adder.vhd`, and `lab12a.xdc` from Canvas and place them in a new folder titled `lab08c`.
2. Open Vivado and create a new project titled appropriately.
   - Initially, include all files **except** `cla_16.vhd`.
   - For your convenience, the board identifier is `xc7a35wtcpg236-1`.
     - You can also find the board with the same options as before: `General Purpose`, `Artix-7`, `cpg236`, `-1`.

Hardware Review, Upload, and Test – 4 Bit CLA Adder

3. Open `lab12a.vhd` in the editor, and follow along with the instructor to review the hardware description of it and the other files.
4. `Open Elaborated Design`, review the schematic alongside the instructor, and take screenshots for your report.
5. Run synthesis and implementation and then generate the bitstream to program the device. Then, open the Hardware Manager.
   - Take a screenshot of the resource utilization (LUTs and FFs) to add to your report.
6. Before proceeding, plug the FPGA development board into your computer using the provided Micro-USB to USB-A cable.
7. At the top, in the green banner (or under the `Open Hardware Manager` dropdown) click `Open Target`, then `Auto Connect`.
8. Once the device is connected, select `Program Device` (in either of the locations where `Open Target` was previously).
   - See 06B-handout for troubleshooting steps, or ask the instructor or TA.

9. Click `Program` to upload the bitstream to the FPGA.
10. For the 4-bit CLA adder, the inputs are the rightmost 8 switches, and the output is on two of the four seven-segment displays
    - One has four bits as normal, but the other is only 0 or 1 since it only represents one bit, the carry-out.
11. Choose a set of inputs and take a picture of the board.

Hardware Review, Upload, and Test – 16 Bit CLA Adder

12. Add `cla_16.vhd` to the project:
    - In the toolbar, click `File`, then `Add Sources`. Alternatively, press `ALT` and `A` simultaneously.
    - If not selected already, check `Add or create design sources`, then click `Next`.
    - The rest of this wizard is identical to the corresponding part of the project creation wizard.
    - Click `Add Files`, then navigate to find `cla_16.vhd`. Once you have added it, click `Finish.`
13. Modify `lab12a.vhd` as follows:
    - Open `lab12a.vhd` by double-clicking on the corresponding entry in the `Sources` subpane of the `PROJECT MANAGER` pane.
    - On line 7, change the generic `G_size` from 4 to 16.
    - Comment out lines 68 to 82.
        - Instead of doing this manually, use your mouse to select all rows of one section, then press `CTRL` and `/` at the same time. This will automatically comment each selected line.
    - Uncomment lines 86 to 111.
        - Use `CTRL + /` in the same way to uncomment these lines. This shortcut toggles line comments on the selected lines, so it can be used in either way.
    - Save the file (`CTRL + S`, or hit the save icon at the top of the editor).
14. `Open Elaborated Design`, review the schematic alongside the instructor, and take screenshots for your report.
15. Run synthesis and implementation and then generate the bitstream to program the device. Then, open the Hardware Manager.
    - Take a screenshot of the resource utilization (LUTs and FFs) to add to your report.
16. Regenerate the bitstream and reupload to the board (repeat Steps 7-9).

17. For the 16-bit CLA adder, the inputs are slightly different:
    - The left and right buttons load the current value of the switches into the addend or augend registers respectively.
        - That is, to add two values, set the first value on the switches, then press the left button. Then repeat for the second value and right button.
    - The output is on all four seven-segment displays, except for the carry-out which is on the leftmost LED.
18. Choose a set of inputs and take a picture of the board.

Deliverables

- Include as part of your **informal report**:
    - Screenshots of the Elaborated Design schematics (Step 4 and 14)
    - Screenshots of the FPGA resource utilization (LUTs, FFs) (Step 5 and 15)
    - Two pictures of the FPGA development board (Steps 11 and 18)

Outcomes

- Understand the recursive structure of a carry-look-ahead adder.
- Practice working with VHDL.
- Practice using Vivado for hardware synthesis and implementation.
- Practice programming and testing a hardware description on an FPGA development board.