Lab 05

Truth Tables and Logic Gates

Description

- In this lab, you will:
  - Learn about:
    1. truth tables and how to represent and structure them, and
    2. the seven basic logic gates and their notations, truth tables, and Boolean expressions.
  - Develop a truth table for a specific problem and describe it in hardware.
  - Practice the full FPGA development and testing process:
    1. writing a VHDL description,
    2. synthesis,
    3. implementation,
    4. programming the FPGA a hardware description, and
    5. live testing on the FPGA development board.
  - Derive the truth tables of the seven basic logic gates experimentally by testing their inputs and outputs on the FPGA.
  - Create your own novel representation for each logic gate.

Procedure

Part A – Truth Tables

- The instructor will introduce truth tables and provide background and a foundation for the rest of the lab.

Part B – Challenge

- Download 05B-handout, `lab05b.vhd`, and `lab05.xdc` from Canvas and complete this module, following along with the instructor.

Part C – Implementing Logic Gates

- Download 05C-handout, `lab05c.vhd`, and `lab05.xdc` from Canvas and complete this module, following along with the instructor.

Part D – More on Logic Gates

- The instructor will discuss the boolean expressions and accepted notations for the seven basic logic gates.

Part E – Novel Gate Representation Activity

- Download 05E-handout from Canvas and complete this module, following along with the instructor.

Deliverables

Lab Report

- Submit an **informal report** including the following:
  - A brief description of each part of the lab
    - For the lecture parts, just briefly summarize what was discussed
  - Part B – 2HB Challenge
    - Completed VHDL description/code
    - Picture(s) of the programmed FPGA development board functioning as a two-high-bit detector
  - Part C – Gate Implementation
    - Elaborated Design schematics
    - Picture(s) of the programmed FPGA development board functioning as multiple gates
    - Filled truth tables for each of the seven basic logic gates
  - Part E – Novel Gate Exercise
    - Pictures of your new notation for each of the seven gates
    - Select one gate and comment on the following factors, comparing your new notation to the accepted one:
      - Sensibility
      - Aesthetics
    - Describe how you have taken ownership of your new logic gate representation, which may include:
      - Your goals in designing your notation
      - What you wanted to change about the accepted notation
      - Any new insights you have acquired from this activity

Outcomes

- Understand truth tables and how they are structured.
- Practice designing hardware to solve a specific problem.

- Practice working with VHDL.
- Practice using Vivado for hardware synthesis and implementation.
- Understand what a constraint file does.
- Understand how to program an FPGA with a hardware description.
- Understand how to test a hardware description on an FPGA development board.
- Know the seven basic logic gates, their visual representations, their truth tables, and the corresponding Boolean equations.
- Be able to self-reflect and evaluate preconceived ideas, thoughts, and accepted solutions (eKSO 1h).
- Take ownership of, and express interest in logic gate representation (eKSO 1l).