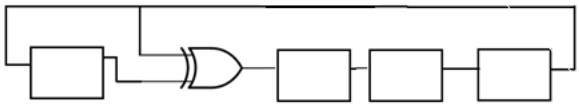
Problem 1

For this problem your task is to design and implement a 3 bit synchronous Gray code counter that goes through the following sequence: 0, 1, 3, 2, 6, 7, 5, 4 and back to 0.

1. Draw the state diagram of this counter.
2. Draw the timing diagram of this counter showing at least 8 clocks.
3. Find the state table using D Flip flops.
4. Simplify the input equations for all the different Flip flops.
5. Draw the hardware as neatly as possible.
6. Can you guess what the special thing about this counter is?

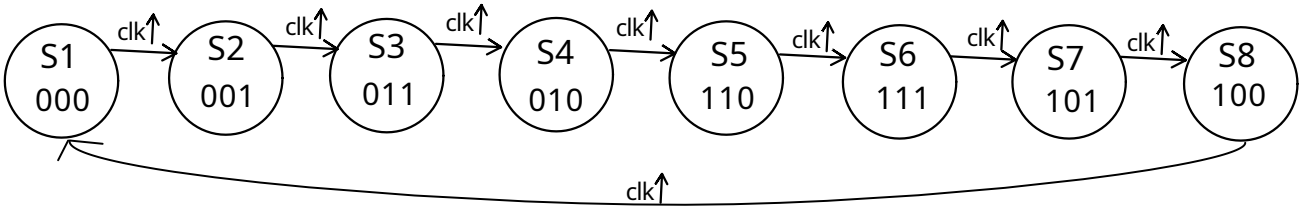
Problem 2

The following Linear Feedback Shift Register (LFSR) is created out of 4 D-Flip Flops that are sensitive to a positive clock edge and a Xor gate

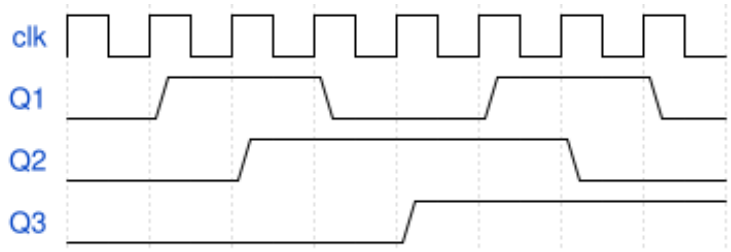


1. Find the state table of this LFSR assuming it was initialized to 1 0 0 0 using asynchronous inputs
2. What will happen if the LFSR was initialized to 0 0 0 0 instead of 1 0 0 0.

1.1:



1.2:



Note: made using WaveDrom.com editor

1.3:

Present State	Synchronous Inputs						Next State
$Q_3Q_2Q_1$	D_3		D_2		D_1		$Q_3Q_2Q_1$
000	0	(R)	0	(R)	1	(S)	001
001	0	(R)	1	(S)	1	(S)	011
011	0	(R)	1	(S)	0	(R)	010
010	1	(S)	1	(S)	0	(R)	110
110	1	(S)	1	(S)	1	(S)	111
111	1	(S)	0	(R)	1	(S)	101
101	1	(S)	0	(R)	0	(R)	100
100	0	(R)	0	(R)	0	(R)	000

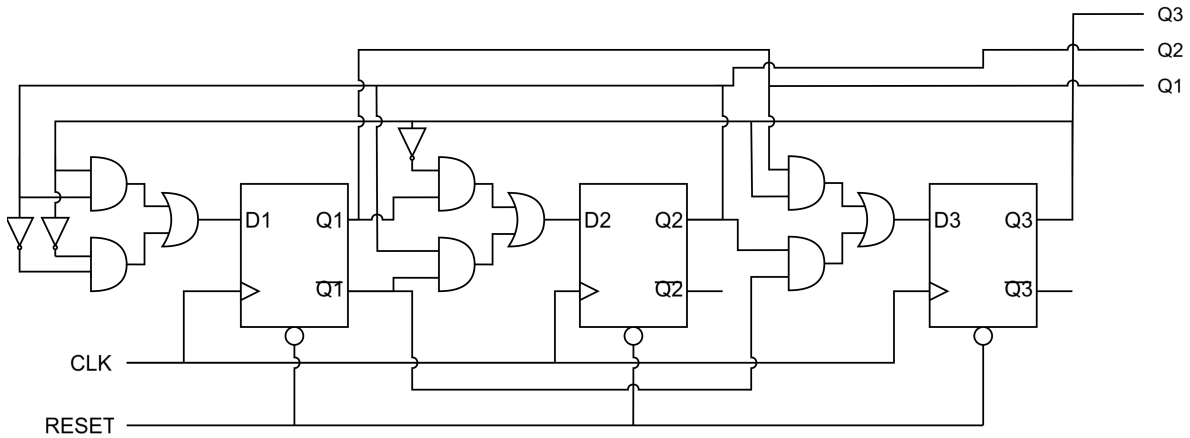
1.4:

$$D_3 = Q_2\overline{Q_1} + Q_3Q_1$$

$$D_2 = \overline{Q_3}Q_1 + Q_2\overline{Q_1}$$

$$D_1 = Q_3Q_2 + \overline{Q_3} \cdot \overline{Q_2}$$

1.5:



1.6: This clock is special because from each current state to the next state, only 1 bit changes. This makes finding the D inputs for each flip-flop easier and faster.

2.1:

Present State	Synchronous Inputs								Next State
$Q_4Q_3Q_2Q_1$	D_4		D_3		D_2		D_1		$Q_3Q_2Q_1$
1000	0	(R)	1	(S)	0	(R)	0	(R)	0100
0100	0	(R)	0	(R)	1	(S)	0	(R)	0010
0010	0	(R)	0	(R)	0	(R)	1	(S)	0001
0001	1	(S)	1	(S)	0	(R)	0	(R)	1100
1100	0	(R)	1	(S)	1	(S)	0	(R)	0110
0110	0	(R)	0	(R)	1	(S)	1	(S)	0011
0011	1	(S)	1	(S)	0	(R)	1	(S)	1101
1101	1	(S)	0	(R)	1	(S)	0	(R)	1010
1010	0	(R)	1	(S)	0	(R)	1	(S)	0101
0101	1	(S)	1	(S)	1	(S)	0	(R)	1110
1110	0	(R)	1	(S)	1	(S)	1	(S)	0111
0111	1	(S)	1	(S)	1	(S)	1	(S)	1111
1111	1	(S)	0	(R)	1	(S)	1	(S)	1011
1011	1	(S)	0	(R)	0	(R)	1	(S)	1001
1001	1	(S)	0	(R)	0	(R)	0	(R)	1000

2.2: All 0s (0 0 0 0) would be 0 in all positions continuously with zero change.