Lab 08

Multiplexed Display and 8-Bit Adder

Description

In this lab, you will build upon the 7-segment display introduced in 06B, and use the improved 7-segment display to view the output of two arithmetic hardware descriptions.

Procedure

Part A – Multiplexed 7-Segment Display

- Download 08A-handout, `lab08a.vhd`, and `lab08a.xdc` from Canvas and complete this module, following along with the instructor.
  - In this module, you will learn about multiplexing and its use for seven-segment displays.

Part B – Multiplexed Hexadecimal to 7-Segment

- Download 08B-handout, `lab08b.vhd`, and `lab08b.xdc` from Canvas and complete this module, following along with the instructor.
  - In this module, you will combine concepts from 06B and 08A.

Part C – 8-Bit Adder/Subtractor on 7-Segment Display

- Download 08C-handout, `lab08c.vhd`, `display_controller.vhd`, `full_adder.vhd`, `half_adder.vhd`, and `lab08c.xdc` from Canvas and complete this module, following along with the instructor.

Part D – 8-Bit Signed Array Multiplier

- Download 08D-handout, `lab08d.vhd`, `display_controller.vhd`, `full_adder.vhd`, `half_adder.vhd`, `adder_9.vhd`, `part_prod_gen.vhd`, and `lab08d.xdc` from Canvas and complete this module, following along with the instructor.

Deliverables

Lab Report

- Submit an **informal report** including the following:
  - Parts A **and** B
    - A screenshot of the Elaborated Design schematic
    - A screenshot of the FPGA resource utilization
    - Pictures of the FPGA development board
    - Answers to handout questions
  - Part C
    - A screenshot of the Elaborated Design schematic
    - A screenshot of the FPGA resource utilization
    - A picture of the FPGA development board
    - Answers to handout questions
    - Testing results
    - Manual verification of functionality
  - Part D
    - A screenshot of the Elaborated Design schematic
    - Screenshots of simulation results
    - A screenshot of the FPGA resource utilization
    - A picture of the FPGA development board
    - Answers to handout questions

Outcomes

- Practice working with VHDL.
- Practice using Vivado for hardware simulation.
- Practice using Vivado for hardware synthesis and implementation.
- Practice programming and testing a hardware description on an FPGA dev. board.
- Practice working with two's complement on an actual piece of hardware.
- Understand how a seven-segment display functions.
- Understand the role of multiplexing in the seven-segment display module.
- Understand how a ripple-carry adder works.
- Understand how an array multiplier works.
- Understand VHDL components, instantiation, and structural connections.