Lab 07

Priority Encoders

Description

In this lab, you will practice more efficient gate implementations from K-Maps, building upon 06C, and also test 8:3 and 16:4 priority encoders on the FPGA development board.

Procedure

Part A – Return of the Two-High-Bit Challenge

- Download 07A-handout and follow along with the instructor.
  - In this module, you will expand upon 06C to practice building efficient gate implementations.

Part B – Gate-Based 8:3 Priority Encoder

- Download 07B-handout, `lab07b.vhd`, and `lab07b.xdc` from Canvas and complete this module, following along with the instructor.
  - In this module, you will learn about the gate-level implementation of an 8:3 priority encoder.

Part C – Multiplexer-Based 8:3 Priority Encoder

- Download 07C-handout, `lab07c.vhd`, and `lab07c.xdc` from Canvas and complete this module, following along with the instructor.
  - In this module, you will learn about an alternative implementation of the 8:3 priority encoder using multiplexers, and compare this with the gate-level implementation.

Part D – Two-Level 16:4 Priority Encoder

- Download 07D-handout, `lab07d.vhd`, `priority_encoder_4.vhd`, and `lab07d.xdc` from Canvas and complete this module, following along with the instructor.
  - In this module, you will work with a 16:4 priority encoder implemented using a two-level hardware structure.

Deliverables

Lab Report

- Submit a ***formal* report** including the following:
  - Part A: an *appendix* including:
    - Pictures of drawn gate implementations
    - Answers to handout questions
  - Parts B **and** C
    - A screenshot of the Elaborated Design schematic
    - A screenshot of the FPGA resource utilization
    - Pictures of FPGA development board
    - Answers to handout questions
  - Parts D
    - A screenshot of the Elaborated Design schematic
    - A screenshot of the FPGA resource utilization
    - Pictures of FPGA development board
    - Answers to handout questions
    - Testing results
    - Manual verification of functionality
  - Remember to consult the *Formal Lab Report Guidelines* on Canvas for other details.
    - The items above are the figures and other information that you should integrate into your report.

Outcomes

- Understand how to derive boolean equations from a truth table using Karnaugh Maps.
- Understand how to transform boolean equations to a "Sum of Product" implementation using NAND gates.
- Understand how to transform boolean equations to a "Product of Sum" implementation using NOR gates.
- Practice working with VHDL.
- Practice using Vivado for hardware synthesis and implementation.
- Practice programming and testing a hardware description on an FPGA development board.
- Understand what a priority encoder does and how it functions.
- Understand the gate-level implementation of an 8:3 priority encoder.
- Understand the multiplexer-based implementation of an 8:3 priority encoder.
- Understand how a 16:4 two-level priority encoder is constructed.
- Understand VHDL components, instantiation, and structural connections.