Lab 13

Comparing Hardware and Prioritizing Metrics

Description

In this lab, you will first investigate and compare two 8-bit multipliers implemented differently than 2LMR from 12C. Then, you will consider how different hardware metrics (including power, complexity, and speed) affect the choice of hardware for a particular application.

Procedure

Part A – 8-Bit Array Multiplier

- In this module, you will synthesize, implement, upload, and test a hardware description for an 8-bit pipelined array multiplier.
- Download 13A-handout and the files listed below from Canvas and complete this module, following along with the instructor.
- Files to download:
  - `lab13a.xdc`
  - `lab13a.vhd`
  - `adder_9.vhd`
  - `display_controller.vhd`
  - `full_adder.vhd`
  - `half_adder.vhd`
  - `part_prod_gen.vhd`
  - `sign_magnitude.vhd`

Part B – 8-Bit Serial Multiplier

- In this module, you will synthesize, implement, upload, and test a hardware description for an 8-bit serial multiplier (one that operates in series, not one contained within a serial transceiver, as before).
- Download 13B-handout and the files listed below from Canvas and complete this module, following along with the instructor.
- Files to download:
  - `lab13b.xdc`
  - `lab13b.vhd`
  - `adder_8.vhd`
  - `controller.vhd`
  - `dataflow.vhd`
  - `display_controller.vhd`
  - `f_abs.vhd`
  - `full_adder.vhd`
  - `sign_magnitude_f.vhd`

Part C – Prioritization Activity

- In this module, you will evaluate three different computing platforms based on six digital design evaluation metrics individually, in pairs, and then in larger groups.
- Download 13C-handout from Canvas and complete this module, following along with the instructor.

Deliverables

Lab Report

- Submit an **informal report** including the following:
  - Screenshots of Elaborated Design schematics (as specified) for Parts A and B
  - Screenshots of FPGA resource utilization for Parts A and B
  - Pictures of the FPGA development board (as specified) for Parts A and B
  - Completed testing spreadsheet from Parts A and B
  - A table evaluating the hardware from Parts A and B based on the criteria outlined in those modules
  - Answers to discussion questions from Parts A and B
  - Your completed spreadsheet from Part C as `.xlsx` or `.pdf`
  - Your individual reflection from Part C

Outcomes

- Practice working with VHDL.
- Practice using Vivado for hardware synthesis and implementation.
- Practice programming and testing a hardware description on an FPGA development board.
- Understand the implementation of a pipelined array multiplier.
- Understand the implementation of a serial multiplier.
- Practice comparing different hardware.
- Practice evaluating competing hardware designs based on a set of metrics.
- Understand ramifications of digital system design decisions (eKSO 2a).