Lab 06

K-Maps and 7-Segment Display

Description

In this lab, you will:

1. learn about the 7-segment display on the FPGA development board;
2. utilize Karnaugh Maps (K-Maps) to derive the gate implementation of the 2-high-bit challenge from Lab 05; and
3. play a game to get more practice with K-Maps.

Procedure

Part A – Gates and Buffers

- The instructor will give a brief lecture on logic switches, LEDs, logic gate enables and inhibits, and tri-state buffers.
  - This content expands upon what you have learned previously about gates in the lecture and in Lab 05.
  - The latter are used in the FPGA development board's I/O pins, so understanding them will be helpful for the lab.

Part B – Hexadecimal to 7-Segment

- Download 06B-handout, `lab06b.vhd`, and `lab06b.xdc` from Canvas and complete this module, following along with the instructor.
  - In this module, you will learn about seven-segment displays and how they are controlled at a fundamental level.

Part C – The Two-High-Bit Challenge Strikes Back

- Download 06C-handout, `lab06c.vhd`, and `lab06c.xdc` from Canvas and complete this module, following along with the instructor.
  - In this module, you will continue working on the two-high-bit detection challenge from Lab 05B, implementing it at the gate level after deriving its boolean equations using Karnaugh maps.

Part D – K-Map Game

- Download 06D-handout from Canvas and complete the K-Map Game.

Deliverables

Lab Report

- Submit an **informal report** including the following:
  - Part B
    - Screenshots of FPGA resource utilization (LUTs, FFs)
    - Screenshots of Elaborated Design
    - Pictures of FPGA development board with functional hardware running
    - Answers to selected discussion questions (see individual handouts)
  - Part C
    - Derived 4x4 K-Map and equations
    - Completed VHDL Code
    - Screenshot of FPGA resource utilization (LUTs, FFs)
    - Screenshot of Elaborated Design
    - Answers to handout questions
  - Part D
    - Scan or picture of completed K-Map Game
    - Sum of Product and Product of Sum implementation drawings and analysis
    - Reflection from handout

Outcomes

- Understand additional applications of gates.
- Understand how tri-state buffers are used to enable FPGA I/O.
- Practice describing truth tables of arbitrary hardware.
- Practice working with VHDL.
- Practice using Vivado for hardware synthesis and implementation.
- Practice programming and testing a hardware description on an FPGA development board.
- Understand how a seven-segment display functions.
- Understand how to derive boolean equations from a truth table using Karnaugh Maps.