Lab 09

Part D – Digital Stopwatch Accuracy

Description

In this lab module, you will build a stopwatch from two different types of counters: one that counts from 0 to 9, and another that divides the 100 MHz clock by 2^{20} (about 1 million).

Procedure

Project Creation

1. Download `d_counter.vhd`, `display_controller.vhd`, `lab09d.vhd`, and `lab09d.xdc` from Canvas and place them in a new folder titled `lab09d`.
2. Open Vivado and create a new project, but only add `d_counter.vhd` for now.
   - For your convenience, the board identifier is `xc7a35tcpg236-1`.
     - You can also find the board with these options: `General Purpose`, `Artix-7`, `cpg236`, `-1`.

Decimal Counter Review and Simulation

3. Open `d_counter.vhd` in the editor, and follow along with the instructor to review the file.
4. `Open Elaborated Design`, review the schematic alongside the instructor, and take a screenshot for your report.
5. Setup the behavioral simulation.
   - In Vivado, from the left side pane, click `Run Simulation`, then `Run Behavioral Simulation`.
   - Minimize the two panes on the left with `Scope` and `Objects` tabs to make the wave view bigger.
   - Optionally, minimize the bottom pane (`Tcl Console/Messages/Log`).
   - Optionally, drag the handle next to `Value` to make the columns larger.
6. Select the signals `count_out`, `q`, and `d` by holding the `Shift` key and clicking the first and last of the three signals, or hold `Ctrl` and click each of them.
   - Right click one of them and select `Radix`.
   - Select `Unsigned Decimal` (make sure to select *unsigned*, not signed).

7. Create a clock on the `clk` signal:
    - Right-click the signal `clk`.
    - Select the `Force Clock...` option.
    - Set the `Leading edge value` to `1` and the `Trailing edge value` to `0`.
    - Keep the `Duty cycle (%)` at 50%.
    - Set the `Period` to `10ns` instead of `100ns`.
8. First, set `reset` to `1`:
    - Right-click the signal `reset`.
    - Select `Force Constant...`.
    - Set a `Force value` of `1`.
9. Force `enable` to `0` similar to how you did for `reset`.
10. Now, run the simulation for `10 ns` by clicking the play button with `(T)` underneath, or pressing `Shift+F2`.
    - While holding `Ctrl`, you can use the mouse scroll wheel to zoom in and out in the waveform view.
    - While holding `Shift`, you can use the mouse scroll wheel to navigate horizontally along the waveform view.
    - If you accidentally close the waveform view, go to `Window` in the toolbar, and click `Waveform`.
11. Next, force `reset` to `0` and `enable` to `1`, then run the simulation repeatedly until you see the values repeat.
12. At this point, take a screenshot of your simulation results for your report.

Stopwatch Review and Upload

13. In the top menu bar, click `File`, then `Add Sources` (or alternatively, press `Alt` and `A` simultaneously on your keyboard).
14. Select the `Add or create design sources` option and click `Next`.
15. Add the other VHDL files you downloaded before (`display_controller.vhd` and `lab09d.vhd`).
16. Click `Finish`.
17. Repeat steps 13 through 16, but select `Add or create constraints` instead, and add `lab09d.xdc` this time.
18. `Open Elaborated Design`, review the schematic alongside the instructor, and take a screenshot for your report.

19. Run synthesis and implementation and then generate the bitstream to program the device. Then, open the Hardware Manager.
    - Take a screenshot of the resource utilization (LUTs and FFs) to add to your report.
20. Before proceeding, plug the FPGA development board into your computer using the provided Micro-USB to USB-A cable.
21. At the top, in the green banner (or under the `Open Hardware Manager` dropdown) click `Open Target`, then `Auto Connect`.
22. Once the device is connected, select `Program Device` (in either of the locations where `Open Target` was previously).
    - See 06B-handout for troubleshooting steps, or ask the instructor or TA.
23. Click `Program` to upload the bitstream to the FPGA.

Stopwatch Accuracy Testing and Analysis, Part 1

24. On the FPGA development board, the GPIO is organized as follows:
    - The seven-segment displays have a decimal point in the middle. By default, they will read `00.00` – this is the readout of the stopwatch in seconds.
    - Of the five buttons, holding down the left button enables the stopwatch, while pressing the right button resets the stopwatch.
25. Bring up a stopwatch application or website on your smartphone or computer.
26. Run both stopwatches for 20 or 30 seconds.
    - Start and stop both the FPGA and your phone/computer stopwatch at the same times. Try to get as close to your chosen time as possible.
27. At this time, take a picture of the FPGA development board for your report.

Improving the Accuracy of the Stopwatch

28. Let us assume that your phone or computer's stopwatch is accurate. You should notice that the stopwatch on the FPGA development board is not quite accurate. Why is this?
29. What applications might be able to use the stopwatch with an accuracy of ± 1 second? List a few.
30. How can the accuracy of the stopwatch be improved? Explain.
31. Would improving the accuracy allow usage in different applications? Explain.
32. Implement an improved, more accurate stopwatch alongside the instructor.
33. Take screenshots of the new Elaborated Design and of the resource utilization.

34. Verify that the improved stopwatch is more accurate by repeating steps 25 to 27, including a new picture.
35. Comment on how much the accuracy of the stopwatch has improved.
36. How many extra LUTs were required to improve the accuracy of the stopwatch?
37. If you were mass producing these stopwatches, would the cost of improving the accuracy be justified by the additional marketability for different applications? Explain.

Deliverables

- Include as part of your **informal report**:
  - A screenshot of the Elaborated Design schematic for `d_counter.vhd` (Step 4)
  - A screenshot of your simulation results for `d_counter.vhd` (Step 12)
  - A screenshot of the Elaborated Design schematic for the whole stopwatch (Step 18)
  - A screenshot of the FPGA resource utilization (LUTs, FFs) for the stopwatch (Steps 19, 33)
  - A picture of the FPGA development board showing the final time for each trial (Steps 27, 34)
  - A screenshot of the portion of the Elaborated Design that changed with the improved stopwatch (Step 33)
  - Answers to handout questions (Steps 28, 29, 30, 31, 35, 36, 37)

Outcomes

- Practice working with VHDL.
- Practice using Vivado for hardware simulation.
- Practice using Vivado for hardware synthesis and implementation.
- Practice programming and testing a hardware description on an FPGA development board.
- Understand VHDL components, instantiation, and structural connections.
- Understand delay flip-flops.
- Understand digital counters.