Lab 11

Serial Communication

Description

In previous labs, you have used the buttons, switches, and LEDs on the FPGA development board as inputs and outputs for the hardware you have tested. However, many hardware descriptions require more than 16 bits of input or output. In this lab, you will learn how to address this with serial communication, and apply it to test the components of the multiplier hardware for the lab project.

Procedure

Part A – Serial Communication

- In this module, you will be introduced to the concepts behind serial communication, and in particular, the serial transceiver hardware we will be using in this lab.
  - Download 11A-presentation.pptx and follow along with the instructor.
    - You are encouraged to keep this on hand, as it will be useful for your project report.

Part B – 64 Bit Two-Level Priority Encoder

- In this module, you will:
  1. setup a program that can communicate using a serial protocol over USB with the FPGA.
     - You can install this program either on your laptop or a lab computer, but the computer you choose to install on must be able to connect to the FPGA normally with Vivado.
  2. synthesize, implement, upload, and test a hardware description for a two-level priority encoder, encapsulated within a serial transceiver.
- Download 11B-handout and the files listed below from Canvas and complete this module, following along with the instructor.

- Files to download:
  - 2LPE Files – for Part B only
    - `mux_generic.vhd`
    - `priority_encoder_8.vhd`
    - `priority_encoder_64_2l.vhd`
  - Transceiver Files – for Parts B, C, and D
    - `basys3_mk8_apex.xdc`
    - `d_flip_flop.vhd`
    - `mk8_apex_64.vhd`
    - `mk8_container_lab11.vhd`
    - `mk8_rx_module.vhd`
    - `mk8_tx_module.vhd`
    - `mk8_xcvr_generic.vhd`
    - `synchronizer_2ff.vhd`

Part C – 64 Bit Two-Level Decoder

- In this module, you will synthesize, implement, upload, and test a hardware description for a two-level decoder, encapsulated within a serial transceiver.
  - You will use the same program for serial communication as in Part B.
- Download 11C-handout and `decoder_generic.vhd` from Canvas and complete this module, following along with the instructor.
  - You will also need all the transceiver files listed above.

Part D – 64 Bit Two-Level Barrel Shifter

- In this module, you will synthesize, implement, upload, and test a hardware description for a two-level barrel shifter, encapsulated within a serial transceiver.
  - You will use the same program for serial communication as in Parts B and C.
- Download 11D-handout and `barrel_shifter_generic.vhd` from Canvas and complete this module, following along with the instructor.
  - You will also need all the transceiver files listed above.

Deliverables

Lab Report

- Submit an **informal report** including the following:
  - Screenshots from Parts B, C, and D.

Outcomes

- Understand the concepts behind serial communication.
- Understand how the serial transceiver used in this lab is structured.
- Practice working with VHDL.
- Practice using Vivado for hardware synthesis and implementation.
- Practice programming and testing a hardware description on an FPGA development board.
- Understand how to use serial communication to test hardware descriptions.
- Learn how to use a serial communication software to send data to and receive data from an FPGA development board.
- Learn how to add an Intellectual Property (IP) Core to a Vivado project.
- Learn how to use an onboard MMCM to generate a faster clock from the base 100 MHz clock on the FPGA development board.