Lab 10

Introduction to Lab Project

Description

This lab serves as an introduction to the final project, which will span the next four labs, including this lab. This project is designed for you to experience a real-world application of the concepts covered in this course.

Encryption is a critical application for modern hardware and software. As available computing power increases, decrypting increasingly large data becomes easier, necessitating the use of ever larger key lengths in encryption techniques, in which integer arithmetic operations are frequent. The third most common integer arithmetic operation, after addition and subtraction, is integer multiplication.

Over the next few labs, you will learn about the different components in the two-level multiplier hardware proposed in the paper "Leveraging a Novel Two-Level Priority Encoder for High-Precision Integer Multiplication" which was written and published by students and faculty from ONU's ECCS department. In the final lab of this project, you will assemble the components to create and test a 64×64 bit two-level multiplier.

Procedure

- For this lab, please consult the associated slide deck, presented in today's lab.

Project Schedule

- 2024-04-02 (Today) – Introduction and high-level Description of Project
- 2024-04-09 – Serial communication and testing multiplier components
- 2024-04-23 – Carry-look-ahead adder: implementation and testing
- 2024-04-30 – "Capstone" combining compnents into hardware; testing and simulation of entire multiplier
- 2024-05-10 – Final report due

Deliverables

Lab 10 Report

- Submit an **informal report** with answers to the following questions:
  1. Why is the two-level multiplier more suitable for high precision as compared to the array multiplier that was covered previously in class?
  2. Why does the delay (in clock cycles) of the two-level multiplier depend on the input?
  3. Why it is important to have a "done" signal in the two-level multiplier?
  4. What is the advantage of using the "fine-coarse" concept in multiple components of the two-level multiplier, including the encoder, decoder, and barrel shifter?
  5. Why is the carry-look-ahead adder essential in this multiplier?
- Your answers will help you write your final project report.

Final Project Report

- Due 2024-05-10 at 11:59 PM (end of dead week)
  - You should work on this throughout the next four labs. Do not wait until the last minute.

- Submit a **formal report** with the following sections:
  - Introduction to project
    - Briefly explain the motivation, background, and applications (you should cite one or more sources for this, which can include the paper mentioned above).
    - This need not be more than half of a page.
  - Methodology
    - Explain how the multiplication algorithm works at a high-level.
    - Describe each of the components of the multiplier (from the block diagram) and their functionality.
      - That is: the two-level priority encoder, decoder, barrel shifter, carry-look-ahead adder, XOR gate, and NOR gate.
    - Describe the serial transceiver and why it is required.
    - Describe what happens in one iteration (clock cycle) of the hardware.
    - Your explanations need not be as technically complex as those of the original paper.
    - You can include any figures provided in the slide deck or original paper in your report. You may also choose to include schematic captures from Vivado's Elaborated Design.
    - This section will replace the typical Procedure section in your formal reports. You do not need to explain the detailed procedure for each of the four labs.
  - Results and Discussion
    - Include your data collected in each lab for all simulations and board testing, as applicable. Comment on your results. Specifically, you should comment on:
      - How expensive is the multiplier as a whole? How does this compare to the findings in the original paper?
      - How expensive is each component? Which is the most expensive?
      - What would you need to do in order to use this hardware for higher input precisions (512+ bits)?
      - Can the hardware be improved? If so, explain how. If not, explain why not.
        - There is no wrong answer, this is just to get you thinking about how the hardware works.

- Conclusion
  - Briefly summarize what you have discussed in the report.
  - Reflect and discuss your thoughts on the lab project. You should answer and explain each of the following:
    - Did the project help your understanding of hardware in general?
    - Did the project effectively utilize most or all of the concepts discussed in this class?
    - Did you find this project useful from the perspective of understanding real-world applications of digital logic?
    - Did you find that you met the learning outcomes for this project?
    - Did you enjoy working on this project?
      - If you did, you may want to consider doing undergraduate research – this project is derived directly from student work, as evidenced by the aforementioned source publication.

Final Project Outcomes

- Practice working with VHDL.
- Practice using Vivado for hardware simulation, synthesis and implementation.
- Practice programming and testing a hardware description on an FPGA development board.
- Understand VHDL components, instantiation, and structural connections.
- Understand the four major components of the two-level multiplier: what they are, how they function, and how the two-level hardware structure is used to optimize them.
  - The major components are the priority encoder, decoder, barrel shifter, and carry-look-ahead adder.
- Understand and be able to compare at least two different integer multiplication methods.
- Understand how serial communication can be performed between a computer and an FPGA development board.
- Understand why serial communication is necessary for high-precision applications.
- Understand a critical real-world application of digital logic.
- Understand how to critically analyze a hardware design.