Lab 09

Timing and Shift Registers

Description

In this lab, you will learn about hardware timing, use a shift register with accumulator, and analyze the accuracy of a digital stopwatch.

Procedure

Part A – Adder/Subtractor Timing

- Download 09A-handout, `full_adder.vhd`, `half_adder.vhd`, `lab09a.vhd`, and `lab09a.xdc` from Canvas and complete this module, following along with the instructor.

Part B – Array Multiplier Timing

- Download 09B-handout, `full_adder.vhd`, `half_adder.vhd`, `adder_9.vhd`, `part_prod_gen.vhd`, `lab09b.vhd`, and `lab09b.xdc` from Canvas and complete this module, following along with the instructor.

Part C – Two-High-Bit Challenge x16

- Download 09C-handout, `full_comparator.vhd`, `half_comparator.vhd`, `comparator_6.vhd`, `half_adder.vhd`, and `lab09c.vhd` from Canvas and complete this module, following along with the instructor.

Part D – Digital Stopwatch Accuracy

- Download 09D-handout, `d_counter.vhd`, `display_controller.vhd`, `lab09d.vhd`, and `lab09d.xdc` from Canvas and complete this module, following along with the instructor.

Deliverables

Lab Report

- Submit an **informal report** including the following:
  - Parts A **and** B
    - A screenshot of the run results for the first failed timing run and the last successful timing run.
  - Part C
    - A screenshot of the Elaborated Design schematic
    - Screenshots of simulation results
  - Part D
    - A screenshot of the Elaborated Design schematics for `d_counter.vhd` and the whole stopwatch
      - Also a screenshot of the part that changes with the improved stopwatch
    - Screenshots of simulation results for `d_counter.vhd`
    - A screenshot of the FPGA resource utilization for the stopwatch
    - A picture of the FPGA development board for each trial (standard and improved)
    - Answers to handout questions

Outcomes

- Practice working with VHDL.
- Practice using Vivado for hardware simulation.
- Practice using Vivado for hardware synthesis and implementation.
- Practice programming and testing a hardware description on an FPGA development board.
- Understand VHDL components, instantiation, and structural connections.
- Understand elements of timing analysis including clock constraints and critical paths.
- Understand shift registers and accumulators.
- Understand delay flip-flops.
- Understand digital counters.