Lab 07

Part C – Mux-Based 8:3 Priority Encoder

Description

In this lab module, you will learn about the gate-level implementation of an 8:3 priority encoder, building upon the concepts covered in the lecture section. This implementation uses several multiplexers in series to determine the output.

As usual, for this lab module, you will require a PC with a USB-A port to program the FPGA development board.

Procedure

Project Creation

1. Download `lab07c.vhd` and `lab07c.xdc` from Canvas and place them in a new folder titled `lab07c`.
2. Open Vivado and create a new project titled appropriately.
   - If you have not memorized how to do this by now, consult a previous lab handout (ex. 06B).
   - For your convenience, the board identifier is `xc7a35tcpg236-1`.
     - You can copy and paste this directly into the search bar in the device select menu.
     - You can also find the board with the same options as before: `General Purpose`, `Artix-7`, `cpg236`, `-1`.

Hardware Review and Upload

3. Open the file in the editor, and follow along with the instructor to review the hardware description.
4. `Open Elaborated Design`, review the schematic alongside the instructor, and take screenshots for your report.
5. Run synthesis and implementation and then generate the bitstream to program the device. Then, open the Hardware Manager.
   - Take a screenshot of the resource utilization (LUTs and FFs) to add to your report.

6. Before proceeding, plug the FPGA development board into your computer using the provided Micro-USB to USB-A cable.
7. At the top, in the green banner (or under the `Open Hardware Manager` dropdown) click `Open Target`, then `Auto Connect`.
8. Once the device is connected, select `Program Device` (in either of the locations where `Open Target` was previously).
   - See 06B-handout for troubleshooting steps, or ask the instructor or TA.
9. Click `Program` to upload the bitstream to the FPGA.

Hardware Testing and Analysis

10. Again, using the eight rightmost switches as the input to the priority encoder, test several different cases and observe the output.
    - The rightmost 3 LEDs are the primary output of the 8:3 priority encoder ($Q_2Q_1Q_0$), while the leftmost LED is the valid bit (V).
11. Verify the functionality. Is the behavior of this hardware the same as the previous hardware?
12. Is one implementation cheaper (gate-based or mux-based), in terms of LUTs, or are they the same? Why do you think this is?

Deliverables

- Include as part of your **formal report**:
  - A screenshot of the Elaborated Design schematic (Step 4)
  - A screenshot of the FPGA resource utilization (LUTs, FFs) (Step 5)
  - Answers to handout questions (Steps 11 and 12)

Outcomes

- Practice working with VHDL.
- Practice using Vivado for hardware synthesis and implementation.
- Practice programming and testing a hardware description on an FPGA development board.
- Understand what a priority encoder does and how it functions.
- Understand the multiplexer-based implementation of an 8:3 priority encoder.