Lab 08

Part C – 8-Bit Adder/Subtractor on 7SD

Description

In this lab module, you will implement and test an 8-bit adder-subtractor on the multiplexed seven-segment display, building upon 08B.

As usual, for this lab module, you will require a PC with a USB-A port to program the FPGA development board.

Procedure

Project Creation

1. Download `lab08c.vhd`, `display_controller.vhd`, `full_adder.vhd`, `half_adder.vhd`, and `lab08c.xdc` from Canvas and place them in a new folder titled `lab08c`.
2. Open Vivado and create a new project titled appropriately.
   - For your convenience, the board identifier is `xc7a35tcpg236-1`.
     - You can also find the board with the same options as before: `General Purpose`, `Artix-7`, `cpg236`, `-1`.

Hardware Review and Upload

3. Open `lab08c.vhd` in the editor, and follow along with the instructor to review the hardware description of it and the other files.
4. `Open Elaborated Design`, review the schematic alongside the instructor, and take screenshots for your report.
5. Run synthesis and implementation and then generate the bitstream to program the device. Then, open the Hardware Manager.
   - Take a screenshot of the resource utilization (LUTs and FFs) to add to your report.
6. Before proceeding, plug the FPGA development board into your computer using the provided Micro-USB to USB-A cable.
7. At the top, in the green banner (or under the `Open Hardware Manager` dropdown) click `Open Target`, then `Auto Connect`.

8. Once the device is connected, select `Program Device` (in either of the locations where `Open Target` was previously).
    - See 06B-handout for troubleshooting steps, or ask the instructor or TA.
9. Click `Program` to upload the bitstream to the FPGA.

Hardware Testing and Analysis

10. The GPIO is organized as follows:
    - The left half of the switches represent the first term (addend or minuend).
    - The right half of the switches represent the second term (augend or subtrahend).
    - The left half of the 7-segment displays show the result of adding the two terms.
    - The right half of the 7-segment displays show the result of subtracting the two terms.
11. What do the bits displayed on the LEDs (`15` and `12`) mean?
12. Is the output of the subtractor displayed in two's complement?
13. Test the inputs in the table below, and record your results.
    - Take a picture of the FPGA development board during one of your tests.
    - Format your results (outputs) as 3 hex digits. Hint: the first digit will only be `0` or `1`.
    - Manually verify that addition and subtraction are performed correctly ("by hand" but does not necessarily have to be on paper).

Input 1	Input 2	Adder Output	Subtractor Output
`2A`	`4B`		
`05`	`10`		
`FF`	`FF`		
`01`	`FF`		

Deliverables

- Include as part of your **informal report**:
  - A screenshot of the Elaborated Design schematic (Step 4)
  - A screenshot of the FPGA resource utilization (LUTs, FFs) (Step 5)
  - A picture of the FPGA development board (Step 13)
  - Answers to handout questions (Steps 11, 12)
  - Testing results (Step 13)
  - Manual verification of functionality (Step 13)

Outcomes

- Practice working with VHDL.
- Practice using Vivado for hardware synthesis and implementation.
- Practice programming and testing a hardware description on an FPGA development board.
- Understand how a ripple-carry adder works.
- Understand VHDL components, instantiation, and structural connections.