ECCS-1721 Digital Logic (Spring 2024)
Exam3

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This exam is *open-notebook* (meaning all of your course materials may be consulted), and the Internet *may be used* to consult information on any of the topics; however, you may not use the Internet or any other means of communication to discuss details of the exam with anyone else ***except the instructor***. AI tools are not allowed. I repeat, **NO form of communication is allowed between students concerning any aspect of the exam**. ***Violating these directions is considered as giving or receiving aid on the exam***. **Please, ask the instructor for clarifications as needed**.

Honor Pledge

(Please copy down the *italicized statement* below on the first sheet you use in writing out your exam and sign before you begin the exam): **[10 pt penalty if omitted!!!]**

I hereby pledge my honor that no aid shall be given nor received during this exam. If I observe any forms of academic misconduct or questionable behavior, I hereby pledge to report it to my instructor.

Student Signature: ______________________________

You need to use separate sheets of paper. Indicate the beginning of each Question of the exam (e.g., Question 1) and be sure to number the answers appropriately. Use the same numbering as this exam.

Question	Score	Out of
1		30
2		20
3		25
4		25
Total		**100**

Question 1 **(30 points)**

For this question your task is to design and implement a 3-bit synchronous counter that goes through the following sequence:1, 6, 2, 5, 3, 4 and back to 1.

1. **(4 points)** Draw the state diagram of this counter.
2. **(4 points)** Draw the timing diagram of this counter showing at least 6 clocks. You can assume any initial value and the transition should happen on a positive clock edge.
3. **(8 points)** Find the transition table using JK Flip flops.
4. **(8 points)** Simplify the input equations for all the different JK Flip flops inputs (J2, K2, J1, K1, and J0, K0) in terms of Q2, Q1, and Q0.
5. **(4 points)** Draw the hardware as neatly as possible.
6. **(2 points)** Can you guess what this counter is trying to emulate?

Question 2 **(20 points)**

Your task in this question is to design a Finite State Machine (FSM) that can detect a sequence of two or more consecutive zeros. An example input/output is shown below:
X= 010011100000011111100111000011001010100000011101001
Z= 000100001111100000001000011100010000001111100000010

1. Design a Moore FSM to achieve this task
    a. **(4 points)** Draw the state diagram
    b. **(4 points)** Write the state table showing the next states and output for every state
    c. **(2 points)** How many Flip-Flops do you need to implement this FSM?
2. Design a Mealy FSM to achieve this task
    a. **(4 points)** Draw the state diagram
    b. **(4 points)** Draw the state table showing the next states and output for every state
    c. **(2 points)** How many Flip-Flops do you need to implement this FSM?

Question 3 **(25 points)**

1. **(5 points)** Minimize the following Mealy FSM, using the standard staircase method. **Hint:** For a Mealy state machine two states are equivalent if their next states and outputs are the same for X=0 and X=1.

Present state	Next state		Output (Z)	
	X=0	X=1	X=0	X=1
A	B	G	0	1
B	A	D	1	1
C	F	G	0	1
D	H	A	0	0
E	G	C	0	0
F	C	D	1	1
G	G	E	0	0
H	G	D	0	0

2. **(2 points)** The following state table represents the FSM after minimization. Draw the state diagram of this FSM.

Present state	Next state		Output (Z)	
	X=0	X=1	X=0	X=1
A	B	G	0	1
B	A	D	1	1
D	G	A	0	0
G	G	D	0	0

3. **(7 points)** Assigning A to 00, B to 01, D to 10, and G to 11, and using Toggle Flip-Flops write the transition table of this FSM.
4. **(8 points)** Using three-input k-maps find the Boolean expressions of T_1, T_0 and Z in terms of Q_1, Q_0 and X.
5. **(3 points)** Draw the hardware diagram of this FSM assuming negative edge triggered Flip-Flops with asynchronous active-low reset.

Question 4 **(25 points)**

1. **(3 points)** The following is the state table of a BCD to Excess 6 FSM. Draw the state diagram of this FSM. Try to Keep the No Carry states (odd states) to the left and the Carry states (even states) to the right.

Present state	Next state		Output (Z)	
	X=0	X=1	X=0	X=1
S0	S1	S1	0	1
S1	S3	S2	1	0
S2	S4	S4	0	1
S3	S5	S4	1	0
S4	S0	-	1	-
S5	S0	S0	0	1

2. **(5 points)** Continue the following testing table to verify that the FSM is working correctly

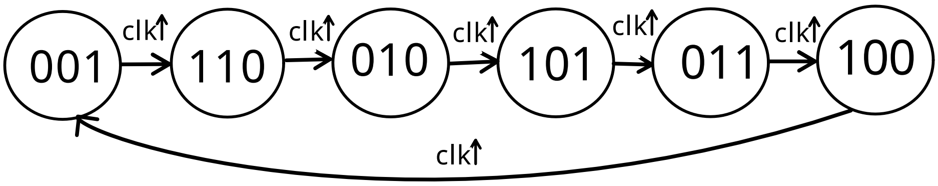
Input sequence				Next state				Output sequence			
t3	t2	t1	t0	t3	t2	t1	t0	t3	t2	t1	t0
0	0	0	0	S0	S5	S3	S1	0	1	1	0
0	0	0	1	S0			S1				
0	0	1	0	S0			S1				
0	0	1	1	S0			S1				
0	1	0	0	S0			S1				
0	1	0	1	S0			S1				
0	1	1	0	S0			S1				
0	1	1	1	S0			S1				
1	0	0	0	S0			S1				
1	0	0	1	S0			S1				

3. **(4 points)** Using Heuristic rules, continue the following state assignment table for the FSM. **Hint:** I partially filled the table to keep your answers as consistent as possible, you should be able to satisfy all the groups in the three rules.

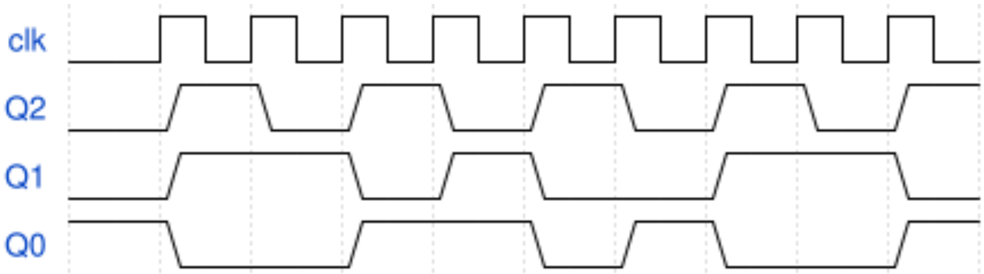
	Q0	
Q2Q1	0	1
00	S0	S1
01		S3
11	X	X
10		

4. **(5points)** Using D Flip-Flops write the transition table of this FSM.
5. **(5 points)** Using four-input K-maps find the Boolean expressions of D2, D1, D0, and Z in terms of Q2, Q1, Q0, and X.
6. **(3 points)** Draw the hardware diagram of this FSM assuming positive edge triggered Flip-Flops with synchronous active-high reset.

1.1:



1.2:



1.3:

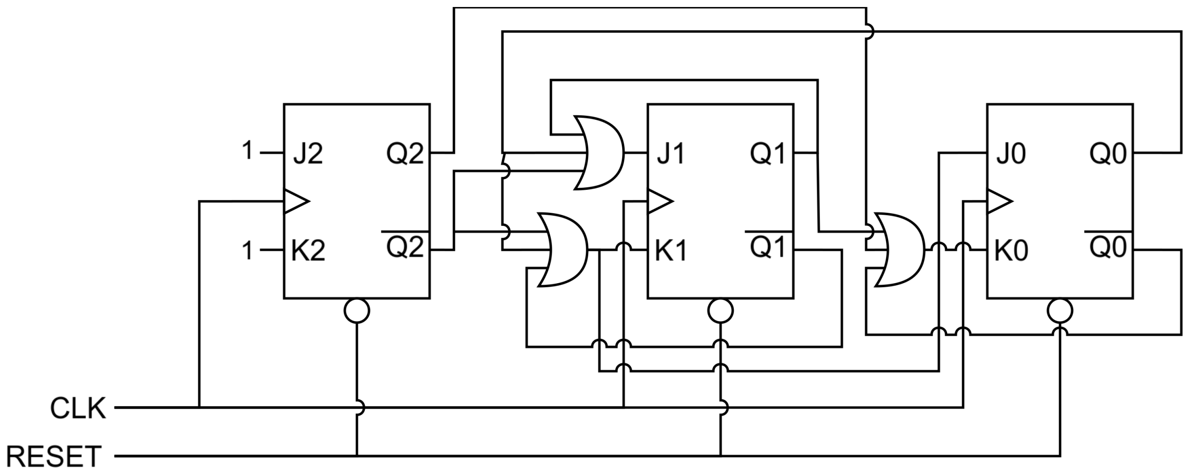
Present State	Synchronous Inputs						Next State
$Q_2Q_1Q_0$	J_2K_2		J_1K_1		J_0K_0		$Q_2Q_1Q_0$
001	11	(T)	11	(T)	11	(T)	110
110	11	(T)	10	(S)	01	(R)	010
010	11	(T)	11	(T)	11	(T)	101
101	11	(T)	11	(T)	10	(S)	011
011	11	(T)	11	(T)	11	(T)	100
100	11	(T)	01	(R)	11	(T)	001

1.4:

$J_2 = 1$ $\qquad J_1 = \overline{Q_2} + Q_1 + Q_0 \qquad K_0 = \overline{Q_2} + Q_1 + \overline{Q_0}$

$K_2 = 1$ $\qquad K_1 = J_0 = \overline{Q_2} + \overline{Q_1} + Q_0$

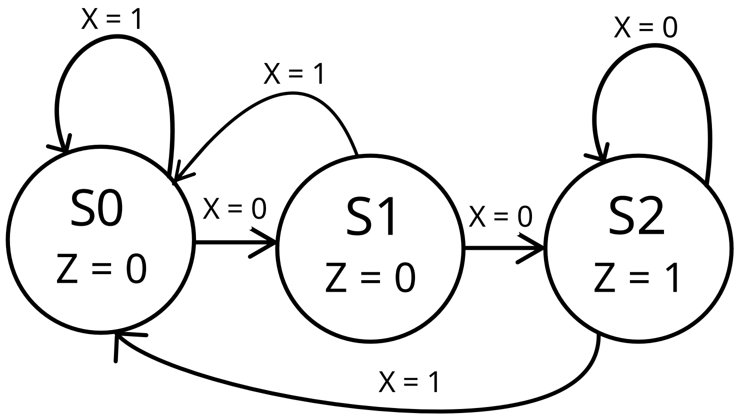
1.5:



1.6:

This counter emulates 1's complement followed by 2's complement.
1's complement -> 2's complement -> 1's complement -> etc.

2.1.a:



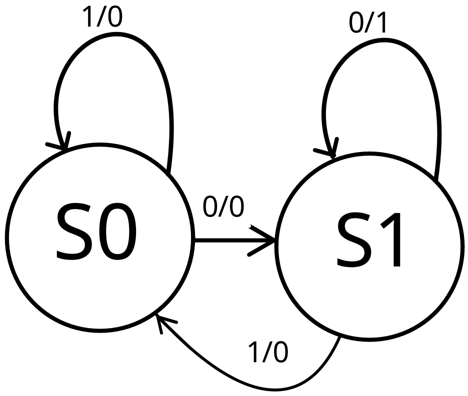
2.1.b:

Present State	Next State X = 0	Next State X = 1	Present Output (Z)
S0	S1	S0	0
S1	S2	S0	0
S2	S2	S0	1

2.1.c:

This state machine would require 2 flip-flops in all assignments.

2.2.a:



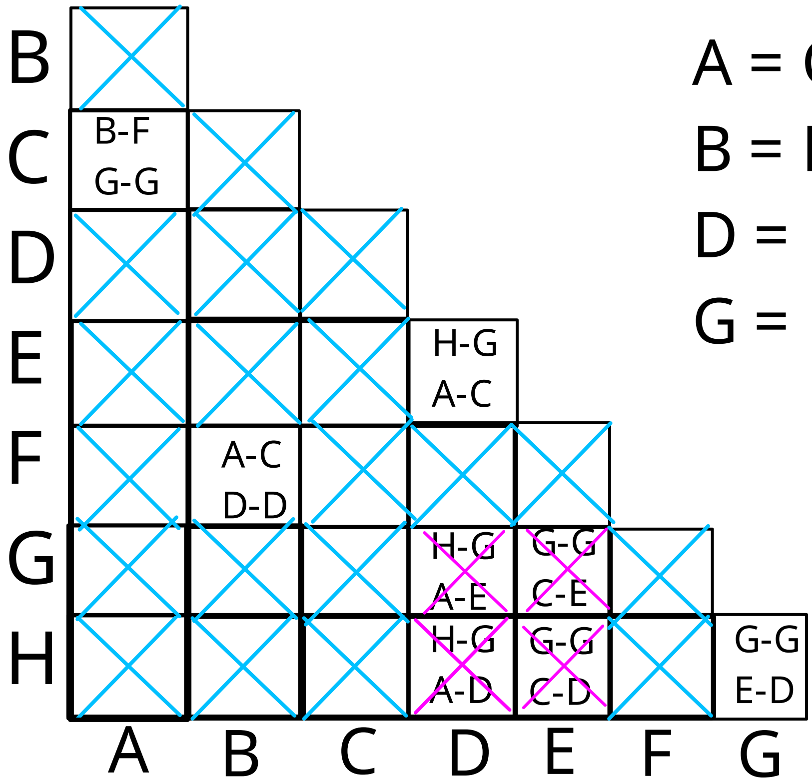
2.2.b:

Present State	Next State X = 0	Next State X = 1	Present Output (Z) X = 0	Present Output (Z) X = 1
S0	S1	S0	0	0
S1	S1	S0	1	0

2.2.c:

This state machine would require 1 flip flop in all assignments.

3.1:



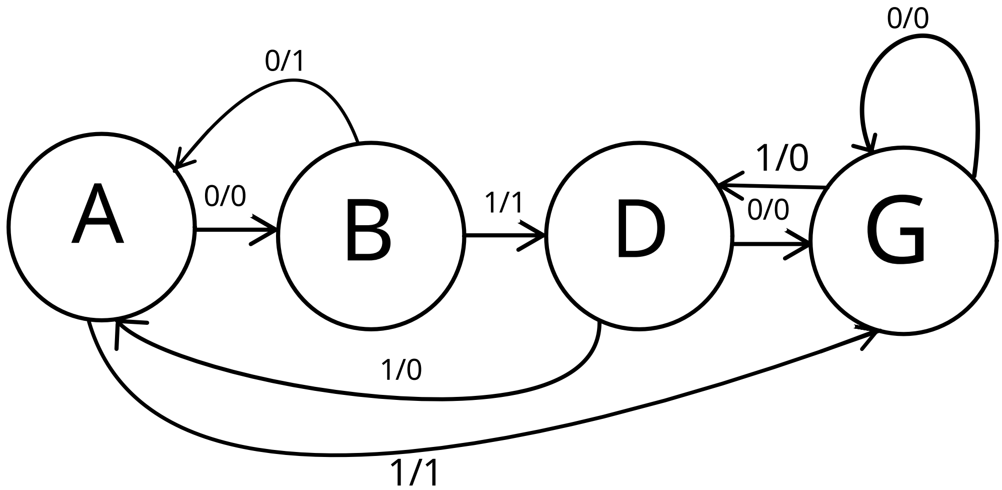
A = C

B = F

D = E

G = H

3.2:



3.3:

	X = 0		X = 1		Output (Z)	
$Q_1^tQ_0^t$	$Q_1^{t+1}Q_0^{t+1}$	T_1T_0	$Q_1^{t+1}Q_0^{t+1}$	T_1T_0	X = 0	X = 1
00	01	01	11	11	0	1
01	00	01	10	11	1	1
10	11	01	00	10	0	0
11	11	00	10	01	0	0

3.4:

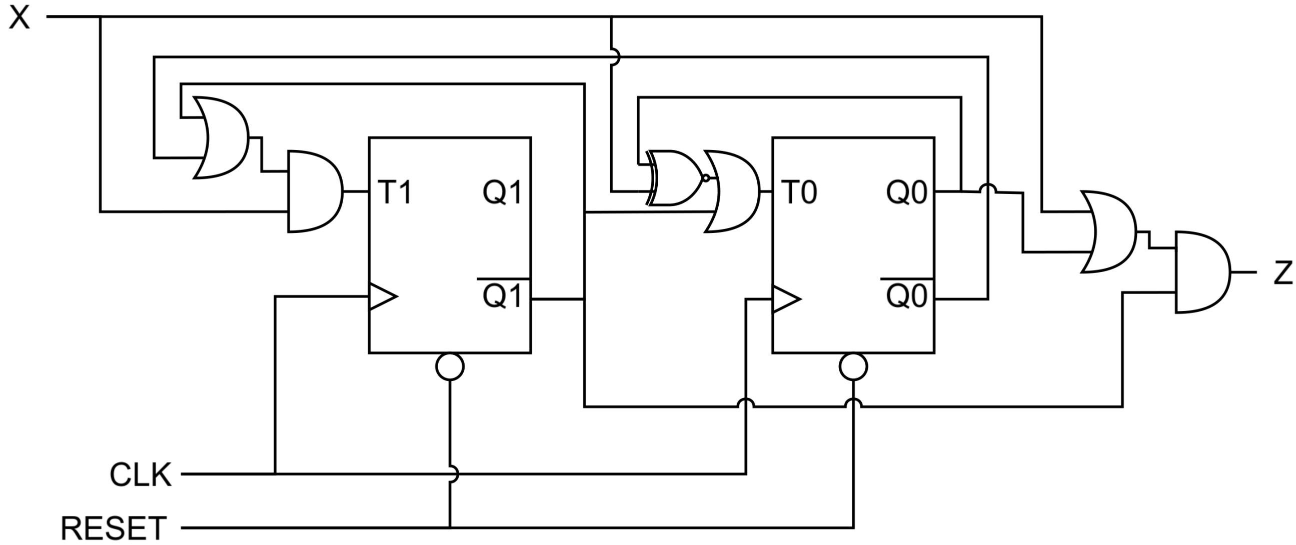
T_1: X \ Q_1Q_0	00	01	11	10
0	0	0	0	0
1	1	1	0	1

T_0: X \ Q_1Q_0	00	01	11	10
0	1	1	0	1
1	1	1	1	0

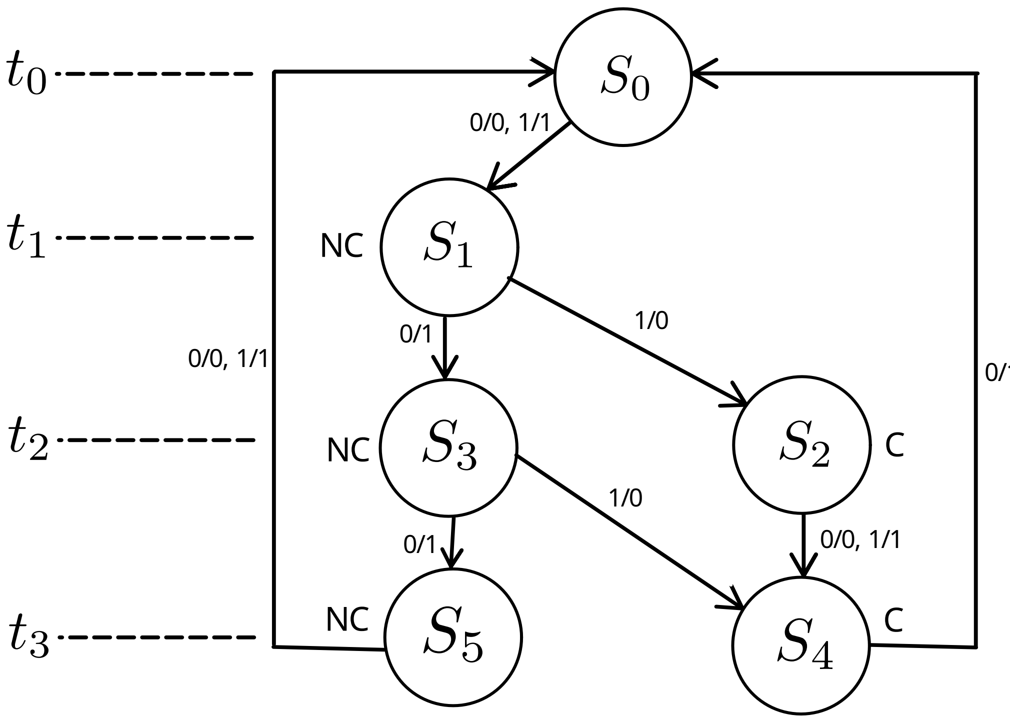
Z: X \ Q_1Q_0	00	01	11	10
0	0	1	0	0
1	1	1	0	0

$$\overline{T_1} = \overline{X} + Q_1Q_0$$
$$T_1 = (X)(\overline{Q_1} + \overline{Q_0})$$
$$T_0 = \overline{Q_1} + Q_0X + \overline{Q_0} \cdot \overline{X}$$
$$T_0 = \overline{Q_1} + \overline{Q_0 \oplus X}$$
$$\overline{Z} = Q_1 + \overline{Q_0X}$$
$$Z = (\overline{Q_1})(Q_0 + X)$$

3.5:



4.1:



4.2:

Input sequence				Next state				Output sequence			
t3	t2	t1	t0	t3	t2	t1	t0	t3	t2	t1	t0
0	0	0	0	S0	S5	S3	S1	0	1	1	0
0	0	0	1	S0	S5	S3	S1	0	1	1	1
0	0	1	0	S0	S4	S2	S1	1	0	0	0
0	0	1	1	S0	S4	S2	S1	1	0	0	1
0	1	0	0	S0	S4	S3	S1	1	0	1	0
0	1	0	1	S0	S4	S3	S1	1	0	1	1
0	1	1	0	S0	S4	S2	S1	1	1	0	0
0	1	1	1	S0	S4	S2	S1	1	1	0	1
1	0	0	0	S0	S5	S3	S1	1	1	1	0
1	0	0	1	S0	S5	S3	S1	1	1	1	1

4.3:

	Q0	
Q2Q1	0	1
00	S0	S1
01	S2	S3
11	X	X
10	S4	S5

4.4:

	X = 0		X = 1		Output (Z)	
$Q_2Q_1Q_0$	$Q_2^{t+1}Q_1^{t+1}Q_0^{t+1}$	$D_2D_1D_0$	$Q_2^{t+1}Q_1^{t+1}Q_0^{t+1}$	$D_2D_1D_0$	X = 0	X = 1
000	001	001	001	001	0	1
001	011	011	010	010	1	0
010	100	100	100	100	0	1
011	101	101	100	100	1	0
100	000	000	-----	-----	1	--
101	000	000	000	000	0	1

4.5:

D_2

Q_2Q_1 \ Q_0X	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	X	X	X	X
10	0	X	0	0

$$D_2 = Q_1$$

D_1

Q_2Q_1 \ Q_0X	00	01	11	10
00	0	0	1	1
01	0	0	0	0
11	X	X	X	X
10	0	X	0	0

$$D_1 = \overline{Q_2 Q_1} Q_0$$

D_0

Q_2Q_1 \ Q_0X	00	01	11	10
00	1	1	0	1
01	0	0	0	1
11	X	X	X	X
10	0	X	0	0

$$D_0 = \overline{Q_2 Q_1 Q_0} + \overline{Q_2} Q_0 \overline{X}$$

Z

Q_2Q_1 \ Q_0X	00	01	11	10
00	0	1	0	1
01	0	1	0	1
11	X	X	X	X
10	1	X	1	0

$$Z = Q_2\overline{Q_0} + \overline{Q_0}X + Q_2X + \overline{Q_2}Q_0\overline{X}$$
$$Z = (\overline{Q_0})(Q_2 + X) + Q_2X + \overline{Q_2}Q_0\overline{X}$$

4.6: