Lab 12

Part B – 64 Bit CLA Adder Over Serial

Description

- In this module, you will synthesize, implement, upload, and test a hardware description for a 64-bit carry-look-ahead adder, encapsulated within a serial transceiver.

Procedure

Project Creation

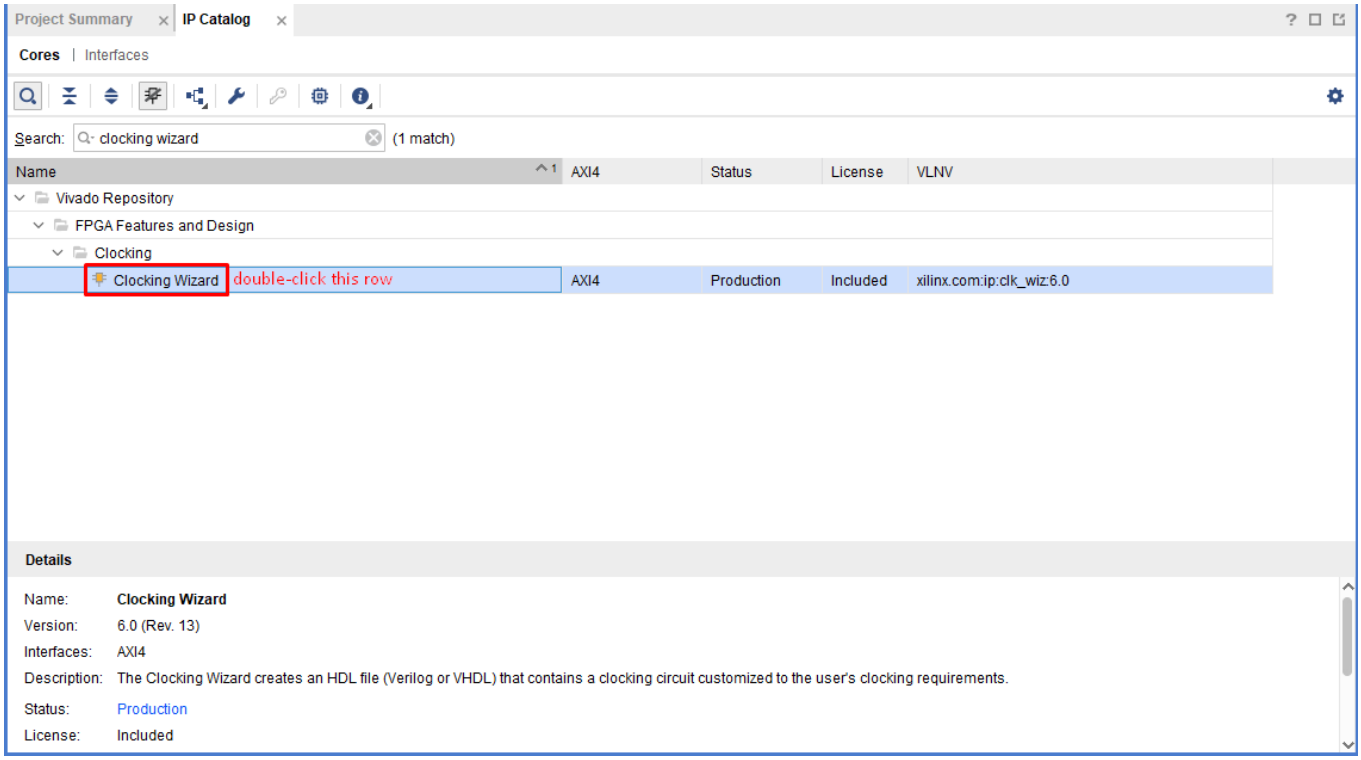
1. Download the files below from Canvas and place them in a new folder titled `lab12b`.
   - CLA Files
     - `cla_pow_4.vhd`
     - `cla_group_logic.vhd`
     - `partial_full_adder.vhd`
   - Transceiver Files
     - `basys3_mk8_apex.xdc`
     - `d_flip_flop.vhd`
     - `mk8_apex_128.vhd`
     - `mk8_container_lab12.vhd`
     - `mk8_rx_module.vhd`
     - `mk8_tx_module.vhd`
     - `mk8_xcvr_generic.vhd`
     - `synchronizer_2ff.vhd`
2. Open Vivado and create a new project titled appropriately.
   - If you have not memorized how to do this by now, consult a previous lab handout (ex. 06B).
   - For your convenience, the board identifier is `xc7a35tcpg236-1`.
     - You can copy and paste this directly into the search bar in the device select menu.
     - You can also find the board with the same options as before: `General Purpose`, `Artix-7`, `cpg236`, `-1`.

3. Enable VHDL 2008 for the `adder : cla_pow_4` file.
    - To do this graphically:
        - In the `PROJECT MANAGER` pane, in the `Sources` subpane, expand the `apex` top-level component, and then its `hw : hw_container` subcomponent.
        - Click on the entry `adder : cla_pow_4`.
        - In the `Source File Properties` subpane below, look for the `Type` property. Click the three dots next to the box containing `VHDL`.
        - In the dialog that opens, expand the dropdown and select `VHDL 2008`.
        - Click `OK`.
    - Alternatively, you can open the `Tcl Console` subpane at the bottom by selecting the corresponding tab, and enter the following command:

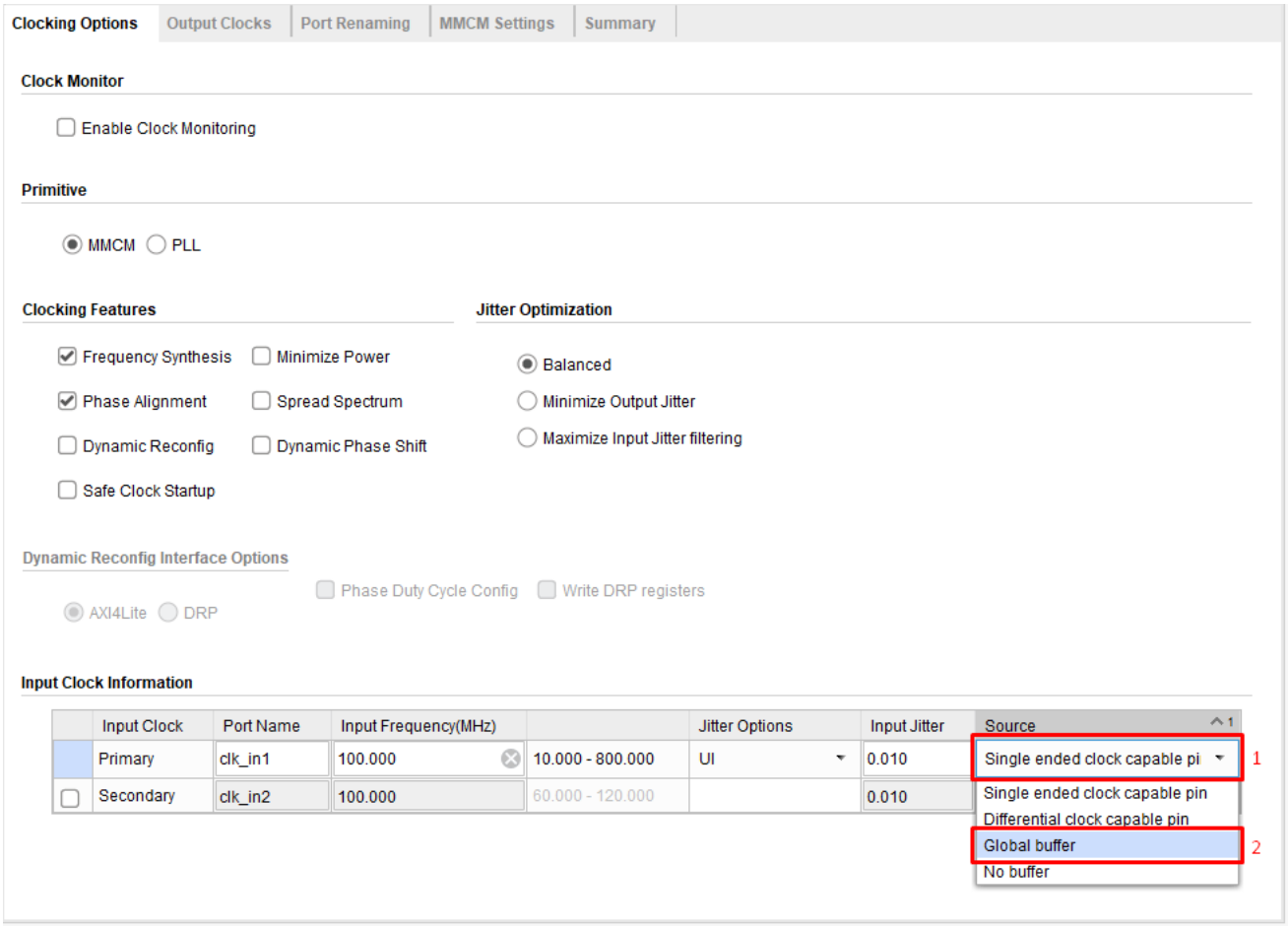
```
set_property file_type {VHDL 2008} [get_files -filter {FILE_TYPE == VHDL}]
```

Adding the Clocking Wizard IP Core

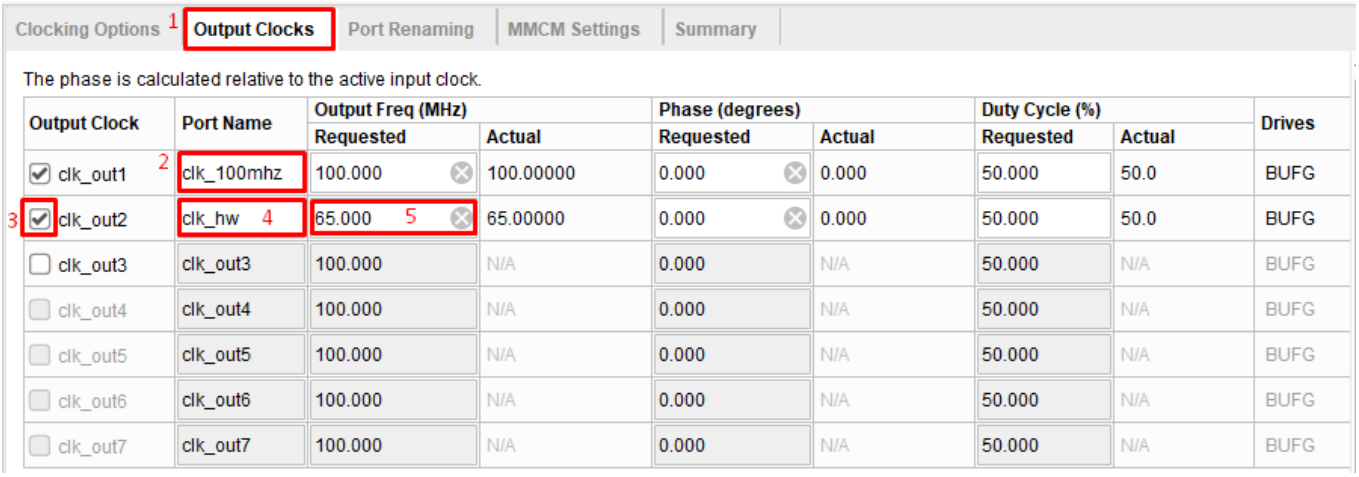
4. On the left sidebar, at the bottom of the `PROJECT MANAGER` dropdown, click on `IP Catalog`.
5. In the search bar, type "clocking wizard", then double-click on the search result for Clocking Wizard.



6. In the clocking wizard dialog that opens, at the bottom under `Input Clock Information`, scroll to the right to reveal the `Source` column of the table. For the value in that column in the row for the "Primary" input clock, click the dropdown and switch it to **Global Buffer**.
    - This step is critical, otherwise implementation will fail!



7. Near the top of the dialog, switch to the Output Clocks tab. Under the `Port Name` column, rename the port `clk_out` to `clk_100mhz`. Check the box in the `Output Clock` column labeled `clk_out2`. Rename the port to `clk_hw` in the `Port Name` column. In the same row, under `Output Freq (MHz)`, change `Requested` to `65.000`.



8. Finally, click `OK` at the bottom right. A dialog may appear, if so, click `Generate`.
   - Note: if you did not properly set up the clock wizard or exited the dialog before setting everything up, do NOT click on the Clocking Wizard entry in the IP catalog again. Instead, double-click the `hw_mmcm : clk_wiz_0` entry in the `Sources` subpane (or alternatively, right-click and select Re-customize IP). This will bring up the correct window for changing the settings on that IP block.

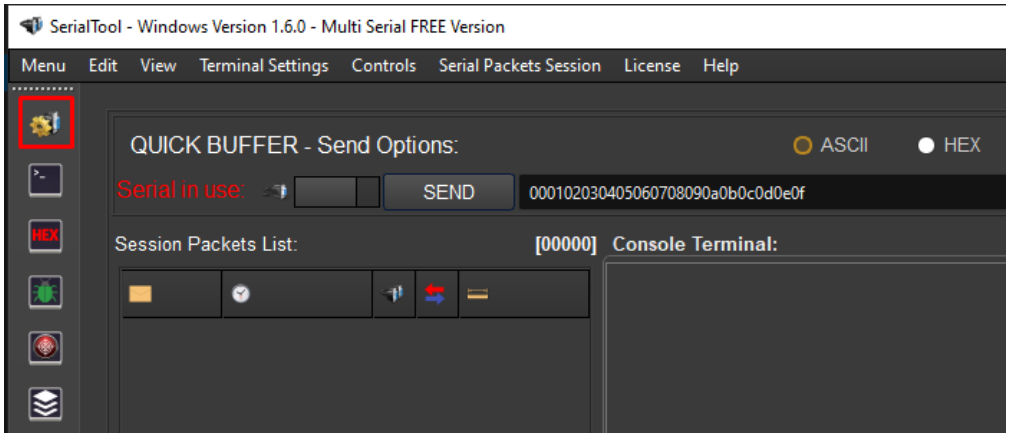
Hardware Review and Upload

9. Follow along with the instructor to briefly review the hardware.
10. `Open Elaborated Design`, review the schematic alongside the instructor, and take screenshots for your report.
    - Take a screenshot of the main schematic (no components expanded).
    - Expand the `hw` block, and then the `adder` block inside it. Take a screenshot of just the adder hardware.
11. Run synthesis, implementation, and bitstream generation. Then, open the Hardware Manager.
    - Take a screenshot of the resource utilization (LUTs and FFs) to add to your report.
12. Before proceeding, plug the FPGA development board into your computer using the provided Micro-USB to USB-A cable.
13. At the top, in the green banner (or under the `Open Hardware Manager` dropdown) click `Open Target`, then `Auto Connect`.

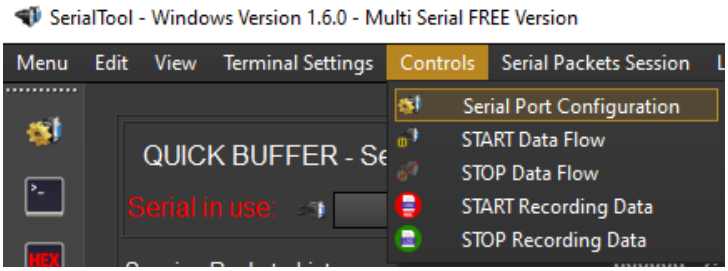
14. Once the device is connected, select `Program Device` (in either of the locations where `Open Target` was previously).
    - See 06B-handout for troubleshooting steps, or ask the instructor or TA.
15. Click `Program` to upload the bitstream to the FPGA.

Enabling Serial Communication

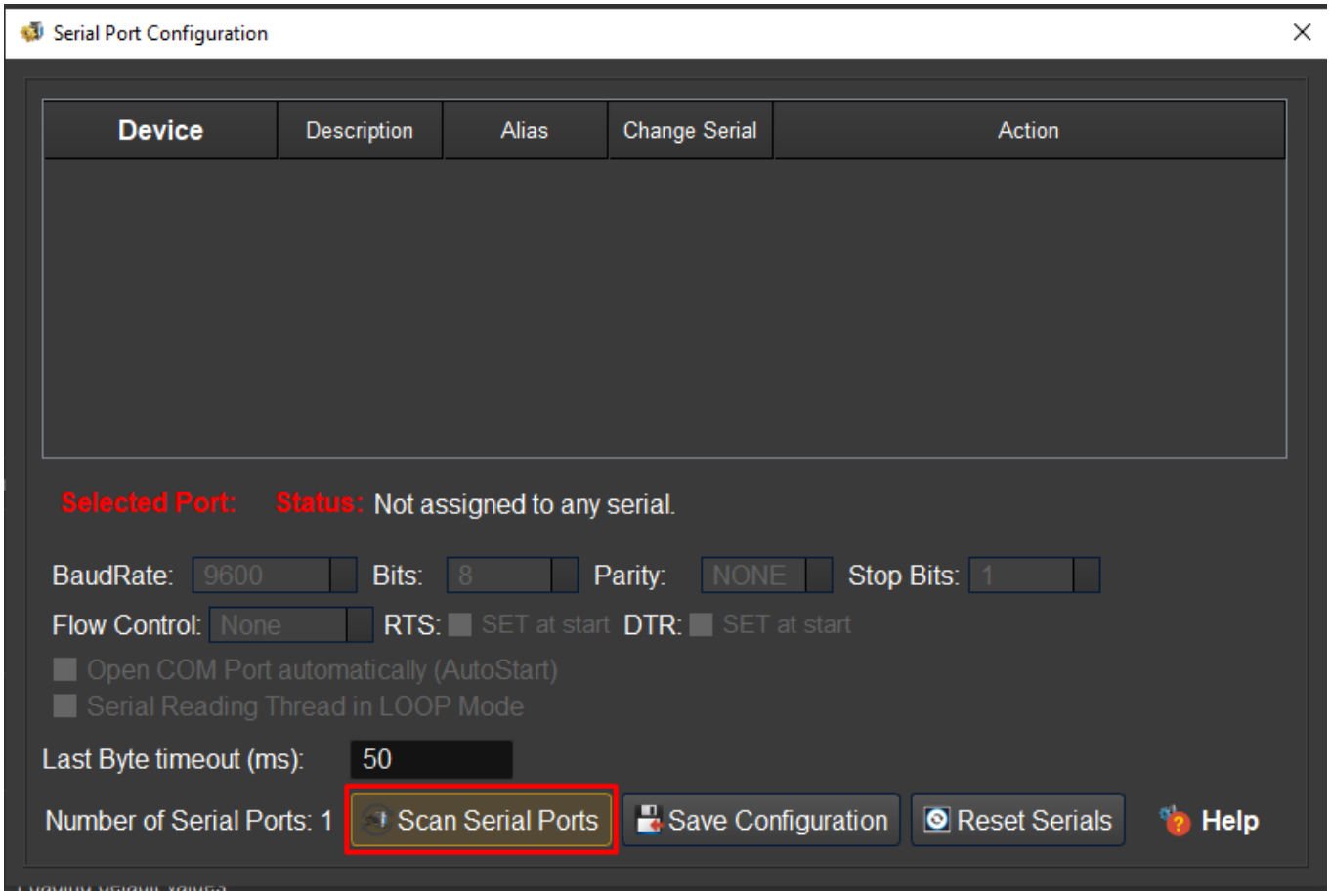
16. Launch SerialTool.
    - You will have to press one of three buttons to start the application.
        - It will tell you which, it is different every time you start it up. This is because the application is freeware.
    - Note that each session (each time you launch the program) is limited to 100 packets. However, this is will not be an issue for the scope of our lab work unless you spam data over the serial connection far beyond what is instructed in this handout.
17. Select the first option on the sidebar (a gear with a serial connector).



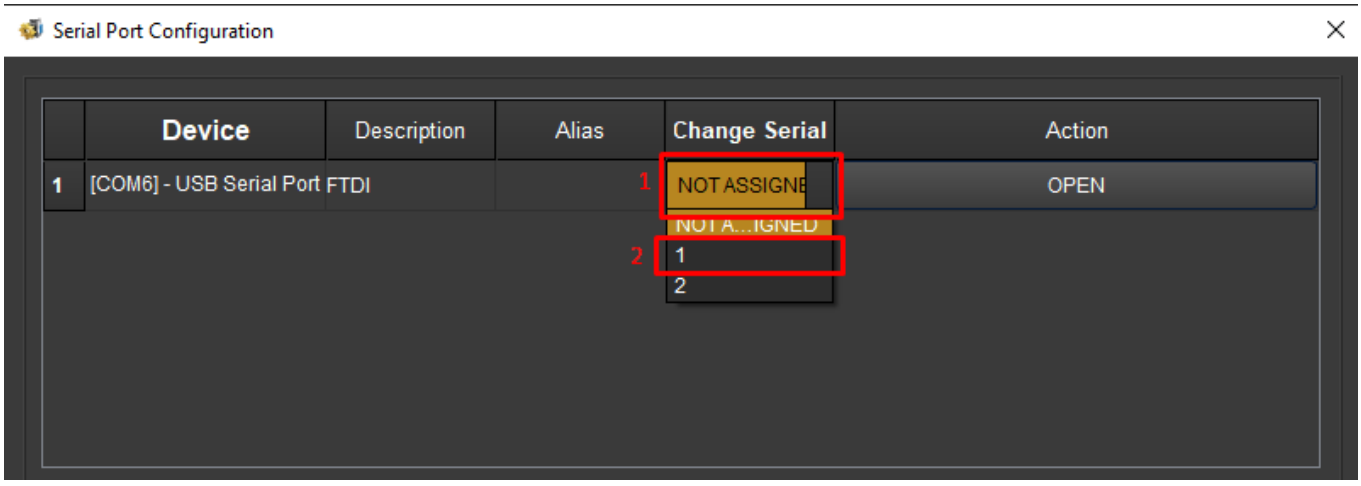
- Alternatively:
    - Top menu bar: `Controls`
    - First option: `Serial Port Configuration`



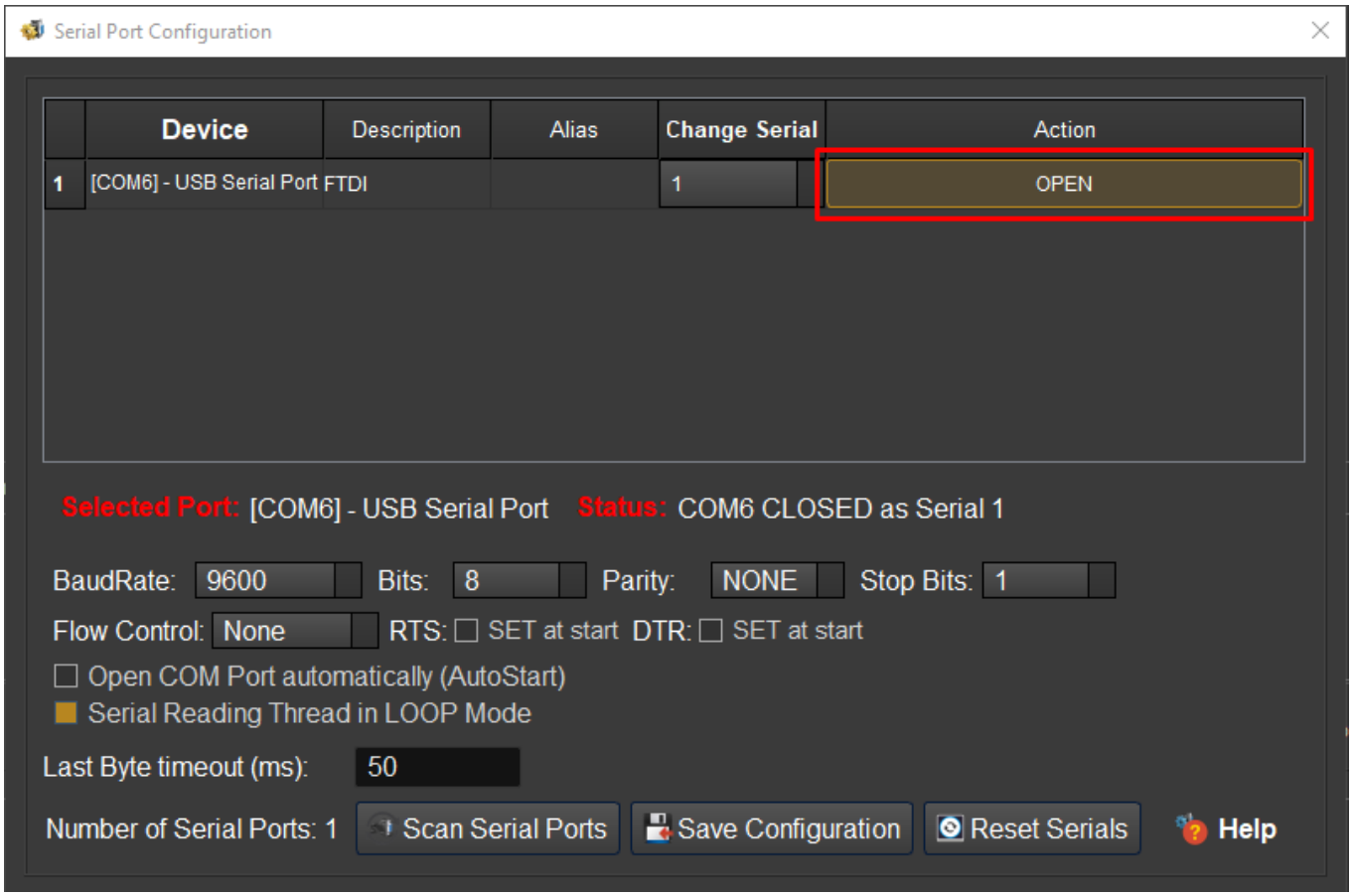
18. At the bottom of the dialog that appears, if no ports are already shown, `Scan Serial Ports`.



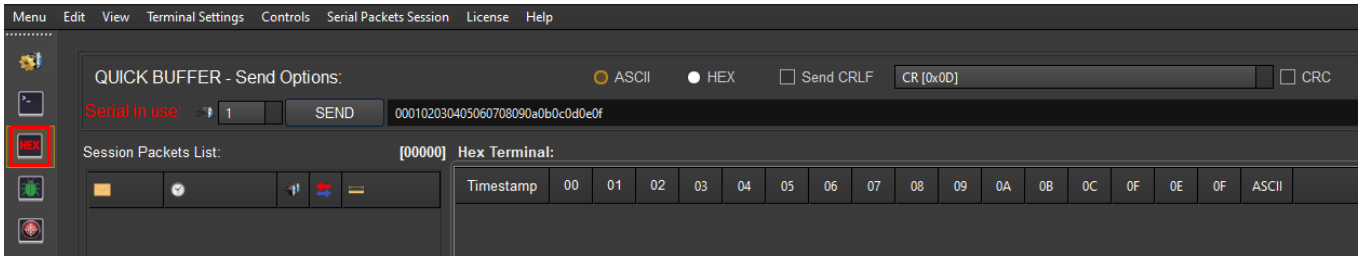
19. A serial port should appear. Click the dropdown that says `NOT ASSIGNED`, then click `1`:



20. Use the following (mostly default) configuration:
    - BaudRate: 9600
    - Bits: 8
    - Parity: NONE
    - Stop Bits: 1
    - Serial Reading Thread in LOOP Mode: Checked
        - This setting is the only one that is not default, you will need to check this box.
            - If you do not, SerialTool will prompt you to do so after the next step.
21. Click `OPEN` on the port:

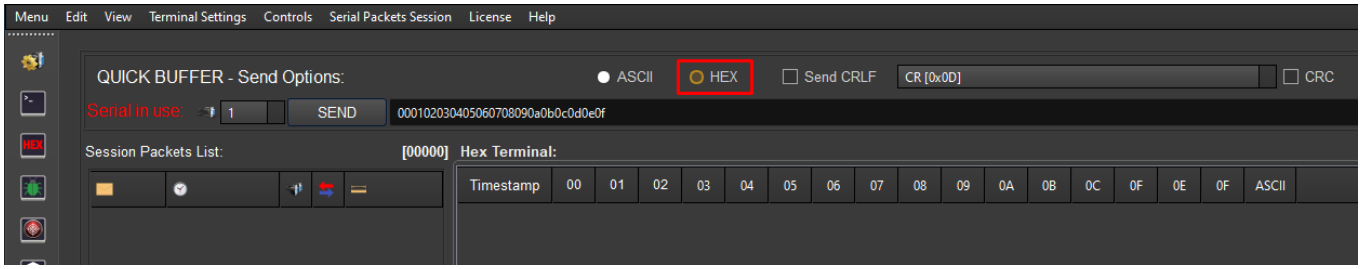


22. Close the dialog box (*not* the serial port!) if it does not disappear automatically.
23. On the sidebar, click the `HEX` terminal button, shown below. Your screen should then appear how it does on the right side of the image below.



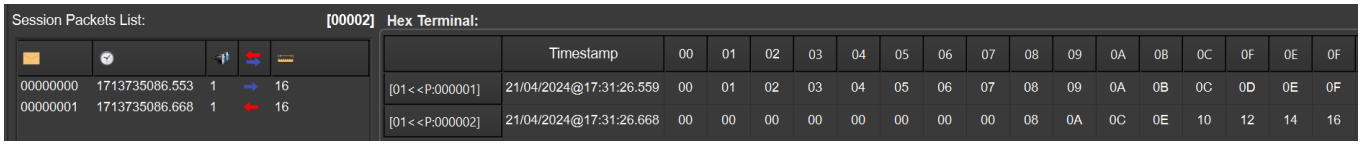
- Alternatively, on the top menu, click `View`, then `Hex Terminal`.

24. Select the `HEX` radio button at the top.



Hardware Testing and Analysis

25. The text box that is by default filled with `000102030405060708090a0b0c0d0e0f` is what you are sending to the FPGA.
26. Press `SEND` to send the data to the FPGA. For the 64-bit carry-look-ahead adder, you should receive a 128-bit response (of at most 65 high bits) that looks like this:



- How to read this:
  - The pane on the left:
    - The blue is transmission and the red is receipt.
    - The decimal number is the timestamp (in unix time).
    - The column labeled with what looks like a ruler is the transmission length, in bytes.
      - For this module, it will be 8.
  - The pane on the right:
    - This will show both incoming and outgoing data.

27. Press the center button (`reset`) to reset the transceiver and prepare it for the next transmission.
28. Repeat for each input below (the first is provided again for you). Do your results match the expected output?
    - Note that everything is in hexadecimal.
    - A template spreadsheet is provided at the following link (make a copy): https://docs.google.com/spreadsheets/d/13vskDKgJuBocyXxhSi5Db3hFf6AFB9sTuGOXItceWrs/edit?usp=sharing

Addend (127..64)	Augend (63..0)	Carry Out (64)	Sum (63..0)
0001020304050607	08090A0B0C0D0E0F	0	080A0C0E10121416
8D8B667EC0A9E8E2	B378F62F36596213	1	41045CADF7034AF5
0000000000000000	0000000000000001	0	0000000000000001
FFFFFFFFFFFFFFFF	0000000000000001	1	0000000000000000
FFFFFFFFFFFFFFFF	FFFFFFFFFFFFFFFF	1	FFFFFFFFFFFFFFFE
8000000000000000	8000000000000000	1	0000000000000000
5555555555555555	AAAAAAAAAAAAAAAA	0	FFFFFFFFFFFFFFFF

29. Take a screenshot of the SerialTool window after testing all the inputs above, to attach to your lab report.

Deliverables

- Include as part of your **informal report**:
  - A screenshot of the Elaborated Design schematic (Step 10)
  - A screenshot of the FPGA resource utilization (LUTs, FFs) (Step 11)
  - A printout of your data spreadsheet (Step 28)
  - A screenshot of SerialTool containing your testing results (Step 29)
  - A brief comment on whether your experimental results match the expected results.

Outcomes

- Practice working with VHDL.
- Practice using Vivado for hardware synthesis and implementation.
- Practice programming and testing a hardware description on an FPGA development board.
- Practice using serial communication to test hardware descriptions by sending data to and receiving data from an FPGA development board.
- Understand the recursive structure of a carry-look-ahead adder.
- Practice working with Intellectual Property (IP) Cores.
- Practice using an onboard MMCM to generate a slower clock from the base 100 MHz clock on the FPGA development board.