Lab 13

Part A – 8-Bit Array Multiplier

Description

- In this module, you will synthesize, implement, upload, and test a hardware description for an 8-bit pipelined array multiplier, adapted from 08D.

Procedure

Project Creation

1. Download the files below from Canvas and place them in a new folder titled `lab13a`.
   - `lab13a.xdc`
   - `lab13a.vhd`
   - `adder_9.vhd`
   - `display_controller.vhd`
   - `full_adder.vhd`
   - `half_adder.vhd`
   - `part_prod_gen.vhd`
   - `sign_magnitude.vhd`
2. Open Vivado and create a new project titled appropriately.
   - For your convenience, the board identifier is `xc7a35wtcpg236-1`.
     - You can also find the board with the same options as before: `General Purpose`, `Artix-7`, `cpg236`, `-1`.

Hardware Review, Upload, and Test – 4 Bit CLA Adder

3. Open `lab13a.vhd` in the editor, and follow along with the instructor to review the hardware description of it and the other files.
4. `Open Elaborated Design`, review the schematic alongside the instructor, and take screenshots for your report as follows:.
   - Take one screenshot of the entire multiplier.
   - Take one screenshot zoomed in to just the `sign_magnitude` hardware component.
5. Run synthesis and implementation and then generate the bitstream to program the device. Then, open the Hardware Manager.
   - Take a screenshot of the resource utilization (LUTs and FFs) to add to your report.

6. Before proceeding, plug the FPGA development board into your computer using the provided Micro-USB to USB-A cable.
7. At the top, in the green banner (or under the `Open Hardware Manager` dropdown) click `Open Target`, then `Auto Connect`.
8. Once the device is connected, select `Program Device` (in either of the locations where `Open Target` was previously).
    - See 06B-handout for troubleshooting steps, or ask the instructor or TA.
9. Click `Program` to upload the bitstream to the FPGA.
10. The GPIO is organized as follows:
    - The left half of the switches represent the first term (multiplicand).
    - The right half of the switches represent the second term (multiplier).
    - The 7-segment displays show the 16-bit result of the multiplication.
11. Make a copy of the template spreadsheet provided at the following link: https://docs.google.com/spreadsheets/d/1LUeCaYJ9kc3Up1m0VH3xfaVEhl34mjmvGhT8vcU10Sg/edit?usp=sharing
    - Test each of the inputs on the board and record your results.
    - During one of your tests, take a picture of the board.
12. Why is the latency different than the throughput in this implementation?

Deliverables

- Include as part of your **informal report**:
    - Screenshots of Elaborated Design schematics (Step 4)
    - Screenshot of FPGA resource utilization (Step 5)
    - A picture of the FPGA development board (Step 11)
    - Completed testing spreadsheet (you will also need Part B) (Step 11)
    - Answer to (12)

Outcomes

- Practice working with VHDL.
- Practice using Vivado for hardware synthesis and implementation.
- Practice programming and testing a hardware description on an FPGA development board.
- Understand the implementation of a pipelined array multiplier.