Chapter 7

Timing Performance of the Data Acquisition System

Achieving a timing precision $\mathcal{O}$ (1 ns) is a pivotal goal for the Data Acquisition (DAQ) at SBND as it is essential for high precision physics analysis. Most importantly, the Cosmic Ray Taggers (CRTs) and PhotoMultiplier Tubes (PMTs) are the two detection subsystems with sufficient timing resolution to resolve the buckets of the Booster Neutrino Beam. Their readout electronics must also have sufficient timing resolution to record the signals with a high level of precision and minimal smearing. It is therefore important to characterise the timing performance of the readout electronics to identify areas of improvement in preparation for the nanosecond goal.

The work undertaken to assess the timing performance of the DAQ electronics is outlined in this chapter. An overview of the timing system at SBND is first given in Section 7.1. The timing characterisation of the CRT and PMT readout electronics are detailed in Section 7.2 and 7.3 respectively. Finally, Sec. 7.4 provides some concluding remarks.

7.1 Timing Reference System of the Data Acquisition

The event building process of the DAQ relies entirely on fragment timestamps to construct a physics event, as was detailed in Sec. 4.2.7. The timestamp generated by each subsystem readout electronic must be generated with a high level of precision and synchronisation. At SBND, the strategy is to utilise the White Rabbit (WR) timing system. It is a collaborative project developed at the European Organisation for Nuclear Research (CERN) and is now a widely-used synchronisation solution in the scientific community [1]. The WR has the capability to offer fully deterministic time transfer with sub-nanosecond accuracy over distances exceeding 80 km. The application of the WR timing system at SBND for time transferring and timestamping is detailed in Sec. 7.1.1 and Sec. 7.1.2 as follows.

7.1.1 Time and Frequency Transfer To Subsystems

Fig. 7.1 provides an overview of the WR timing system at SBND. Starting from the first column of the figure is the Grandmaster switch. It distributes time and frequency to all other slave WR switches within the WR network via optical links. The WR switch has dynamic calibration and thus, is a very reliable and robust delivery system. The system ensures that the Pulse Per Second (PPS), which is 1 Hz, from all slave WR switches are aligned to the Grandmaster's PPS with sub-nanosecond accuracy and tens of picoseconds precision. The Grandmaster switch is also connected to an atomic clock locked to a global navigation satellite system. As a result, the time and frequency distributed by the WR system are derived from the International Atomic Time (TAI) and the Coordinated Universal Time (UTC) format.

At SBND, there are two slave WR switches, as shown in the second column labelled *Servers Hosting Slave Switches*. Each slave switch server hosts a different module of Field programmable gate arrays Mezzanine Card (FMC). The first server contains 2 SVEC-FD modules, which are Fine Delay (FD) cards carried by Simple VME FMC Carrier (SVEC). The second server hosts a single SPEC-TDC module, a Time to Digital Converter (TDC) card carried by a Simple PCIe FMC Carrier (SPEC). The usage of SVEC-FD modules is discussed here, whilst the usage of the SPEC-TDC will be discussed in Sec. 7.1.2 next.

SVEC-FD modules are high precision pulse generators, with 10 ps resolution and time-base accuracy of 2.5 ppm when used within a WR network. They are used to generate frequencies sent to readout electronics to ensure timing synchronisation across all subsystems of the DAQ. There are two types of frequencies: (1) clock as shown by the blue arrow and (2) PPS as shown by the red arrow in Fig. 7.1.

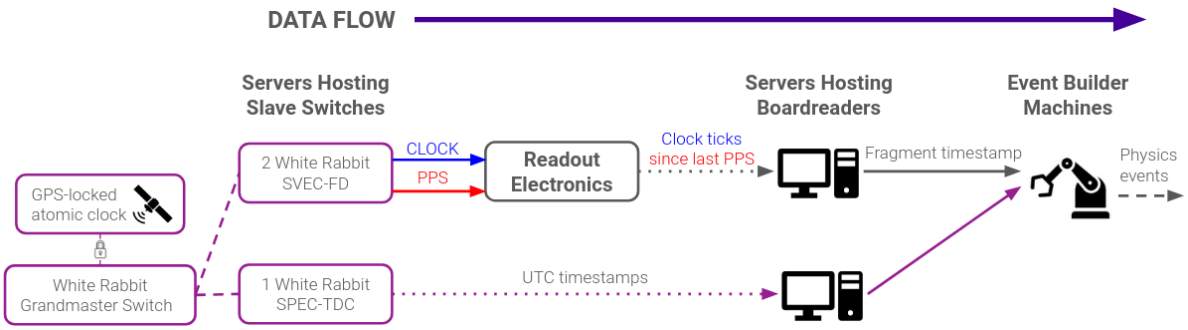


Fig. 7.1 Flow chart showing the distribution of the White Rabbit timing system.

The clock signal provides a *metronome frequency* customised for each readout hardware's internal clocks. This signal behaves as the master clock that the internal clocks of readout electronics can latch onto, thereby maintaining their accuracy and stability over time. The PPS signal provides the *same reference frame* for all readout electronics in the DAQ. All internal clock counters of readout electronics reset upon the arrival of a PPS and thus share the same reference frame as the PPS. Details of the PPS and clock distribution can be found in Appendix C.

Raw data sent from the readout electronics to computer servers, as shown by the dotted grey arrow, contains timing information regarding the arrival time of the trigger at the readout. The timing information at this stage is only the number of clock ticks since last the PPS arrived, and therefore, does not contain sufficient information for event building across multiple subsystems.

To facilitate event building, raw data is packaged into *fragments*, previously detailed in Sec. 4.2.7. The fragment timestamp is in the UTC format, thereby containing timing information about the number of seconds since the Unix Epoch on the 1st of January 1970. This is the *universal* reference frame and allows for direct comparison of fragment timestamps from different subsystems during event building. The number of seconds is generated by the computer servers under the network time protocol with a precision level $\mathcal{O}$(100 ms).

The nanosecond-level of precision of fragment timestamps are derived from the number of clock ticks since the last PPS, generated by internal clocks of each readout electronics. They are converted to the number of nanoseconds since the last whole second using the tick-to-time conversion. This level of precision of fragment timestamp necessitates the event building process, as well as, is stored for downstream reconstruction and analysis.

7.1.2 Precise Timestamping

Also shown in Fig. 7.1, another component of the WR timing system is the SPEC-TDC module. This module can timestamp signals with a precision of 700 ps, and output timestamps in the UTC format. The timestamps can be acquired by the DAQ and be built within a physics event, as shown by the dotted and solid purple arrows.

At SBND, SPEC-TDC is employed to timestamp the arrival time of important signals, recording additional timing information on top of the TPC, PDS and CRT data. This timing information can be leveraged for different physics applications. For instance, it can be used to characterise the timing resolution of the readout electronics. The recorded timestamps can be also used to derive the correction for hardware synchronisation or enable an alternative method to reconstruct the timing of a physics event.

Fig. 7.2 shows the five signals input to the SPEC-TDC. Firstly, two beam signals, shown in blue, provide the status of the BNB beam. The first one is the Booster Extraction Signal (BES), which is an early warning signalling when protons are extracted in the Booster cycles. The second one is the Resistor Wall Monitor (RWM), which measures the instantaneous beam current onto the BNB target. The RWM signal arrives at the SBND detector building almost simultaneously with the beam itself. Additionally, two trigger signals, shown in green, are recorded to monitor the DAQ synchronisation with respect to the triggers. The recorded trigger signals are the flash triggers and the event triggers, which were detailed in Sec. 4.2.5. Finally, clock reset signals for the CRT readout electronics are recorded in the last channel of the SPEC-TDC, as shown in pink.

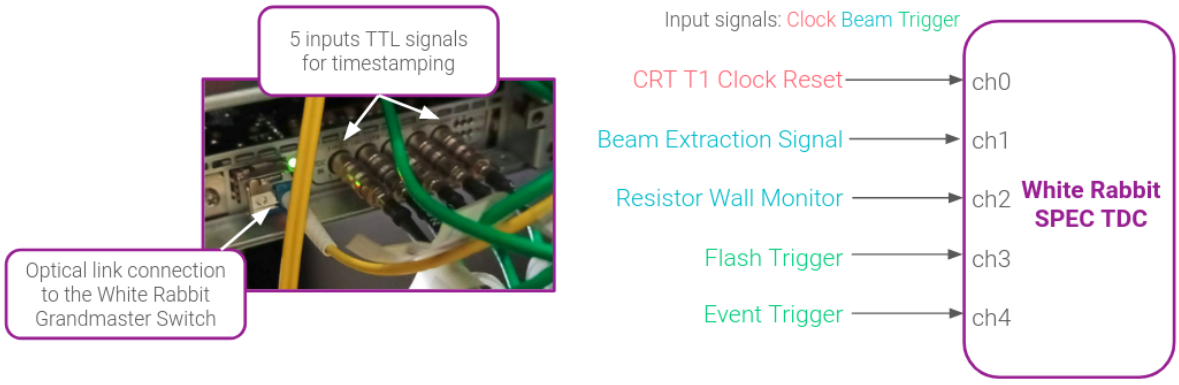


Fig. 7.2 Photograph of the SPEC-TDC module installed at SBND (left) and diagram showing the input signals into the module for timestamping (right).

Two applications of the SPEC-TDC to characterise the timing precision of the readout electronics were explored for the CRT readouts in Sec. 7.2 and the PMT readouts in Sec. 7.3. For the CRT readouts, an alternative timing reconstruction was also derived using the timing information recorded by the SPEC-TDC. For the PMT readouts, the SPEC-TDC timestamps helped validate the timing synchronisation across multiple digitisers.

7.2 Timing Performance of Front End Board Modules

This section provides a description of the characterisation of the timing performance of the CRT readout electronics, Front End Board (FEB) modules, in Sec. 7.2.1 and an alternative timing reconstruction in Sec. 7.2.2.

7.2.1 Evaluation of Internal Clock Resolution

The readout electronics of CRTs are FEB modules, which were detailed in Sec. 4.2.4. Here, the focus is on the precision of the internal clocks of FEB modules. Internal clocks of FEB modules are TDC units with a coarse counter of 4 ns per tick (250 MHz frequency). A high resolution time interpolation method is implemented within the TDC clock cycle to improve the counter to 1 ns per tick [2].

There are two internal clocks per FEB module. The first one is referred to as *T0 clock*, which is reset by the PPS signal therefore its *T0 timestamps* share the same PPS reference frame as all other DAQ readout electronics. The second internal clock is referred to as *T1 clock*, which is reset by a delayed BES signal of the frequency ~ 5 Hz. It produces *T1 timestamps*, referencing the BES signal coincident with the beam arrival time. In addition, FEB modules timestamp the arrival time of reset signals, whether a PPS or a BES and store the timestamps as *T0 or T1 clock reset events*. Each of these reset events is timestamped by both the T0 and T1 clocks, and therefore each has the corresponding T0 and T1 timestamps.

The work to characterise the internet clock was undertaken at Fermilab in 2022 during the commissioning of SBND. It was conducted using a temporary setup called *CRT Sharps*. The CRT Sharps were made up of two sets of CRT panels, where each set of panels was placed upstream and downstream of the SBND detector cryostat, centred on the BNB location. The downstream setup is shown in Fig. 7.3 where 4 CRT panels are arranged orthogonal to each other. Each panel was read out by a FEB module, totalling 8 FEB modules with 4 upstream and 4 downstream. The CRT Sharps was commissioned during the period at which the BNB beam was on. The triggering condition was to have signal coincidences between the

upstream and downstream panels during the beam spill. This was to ensure that the CRT Sharps setup only recorded events produced by muons coming from beam neutrinos and therefore, functioned as a beam telescope. The analysis described below used a dataset recorded by the CRT Sharps during the summer and fall of 2022.

Fig. 7.3 Photograph showing the downstream panels of the CRT Sharps on the back wall of the SBND cryostat.

The T0 clock is characterised using the T0 timestamps of T0 clock reset events. To measure the clock variation, one can simply compare these timestamps with respect to a whole second. An example is shown in Fig. 7.4 for a single FEB module numbered 79. The left plot shows the timestamp variation with respect to the event number to check for clock stability over a period of time. The right plot is a 1D histogram to check for the spread of the distribution. The standard deviation (s.d.) of this distribution is a direct measurement of the T0 clock variation. It is 2.37 ns with a mean of -1.89 ns, indicating that the FEB module 79 consistently received the PPS signal every second to reset its T0 clock. This measurement was repeated for all 8 FEB modules of the CRT Sharps. The T0 clock resolution was found to be $\mathcal{O}$(2 ns), consistent across all FEB modules.

The characterisation of the T1 clock is less trivial since its T1 timestamps do not share the same reference frame with any other readout electronics. The only direct comparison is via T0 timestamps, which contain the T0 clock resolution. The T0 timestamps of T1 clock resets were compared against the SPEC-TDC timestamps of the BES signal since they both measured the same signal and reference to the PPS. This comparison was motivated because the SPEC-TDC has higher precision than FEB internal clocks, 700 ps compared to ~ 1 ns.

The left plot shows the variation with respect to the event number, indicating that the FEB module 79 regularly received BES signals to reset its T1 clock. The right plot shows the 1D histogram of the variation. The s.d. here is not a direct measurement of the T1 clock resolution, however, is expected to be lower than the T0 clock resolution since it is reset more frequently at ~5 Hz. The s.d. is smaller at 1.95 ns and the mean is closer to 0 at -0.443 ns. This measurement was carried out for all FEB modules and the same results were observed.

Moreover, the T1 clock reset events also provide another method to monitor the drift of the T0 clock. This can be done by plotting the variation of T0 timestamps of T1 clock reset

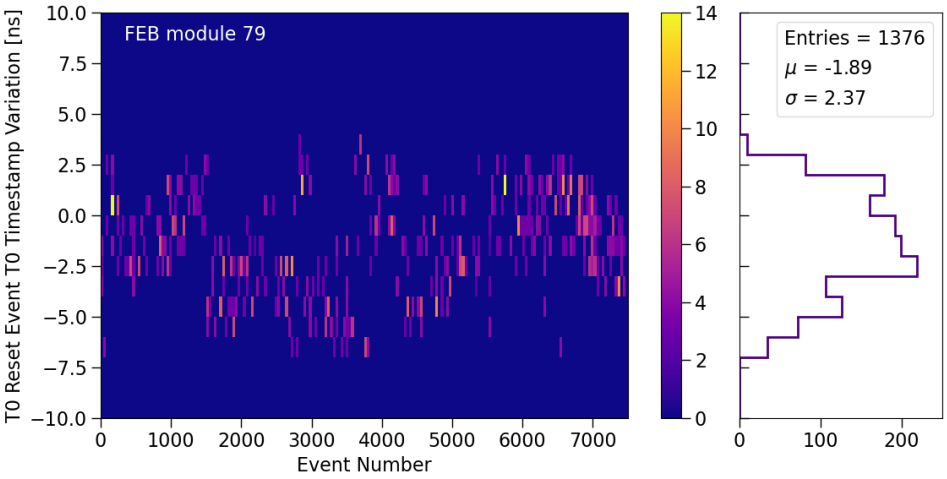


Fig. 7.4 Variation of T0 timestamps of T0 clock reset events with respect to a whole second.

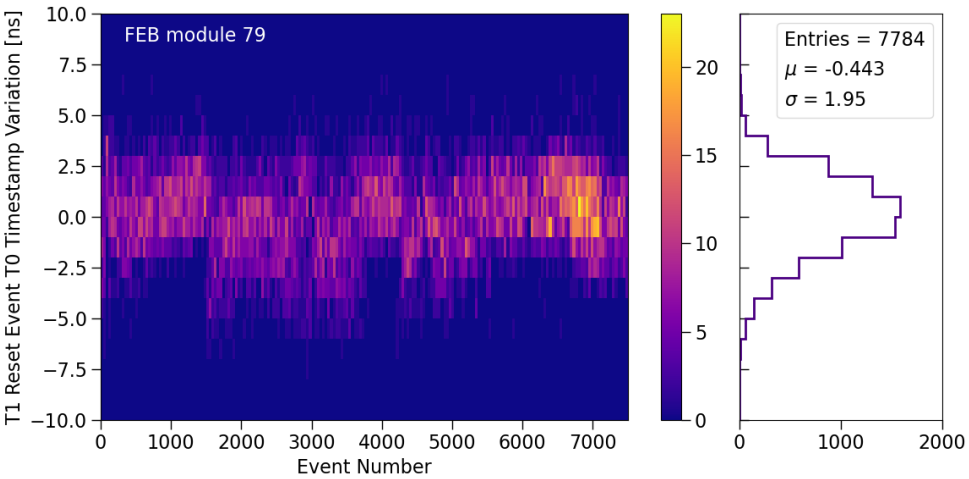


Fig. 7.5 Variation of T0 timestamps of T1 clock reset events with respect to the SPEC-TDC's recorded timestamp of the BES signal.

events as a function of the T0 timestamps, equivalent to when it is generated within the clock cycle. An example is shown in Fig. 7.6 for the FEB module 79. Early in the clock cycle, when T0 timestamps are close to 0 ns, small variations within 2 ns can be seen. However, later in the clock cycle, when T0 timestamps are close to a full second, larger variations up to 7 ns occur. This illustrates that the precision of its T0 timestamp depends on at which point in the clock cycle it is in. It is also possible that the T0 clock counter can overflow and the resulting timestamps are meaningless. This clock drift behaviour is expected to be more prevalent with the T0 clocks than the T1 clocks due to lower reset frequency.

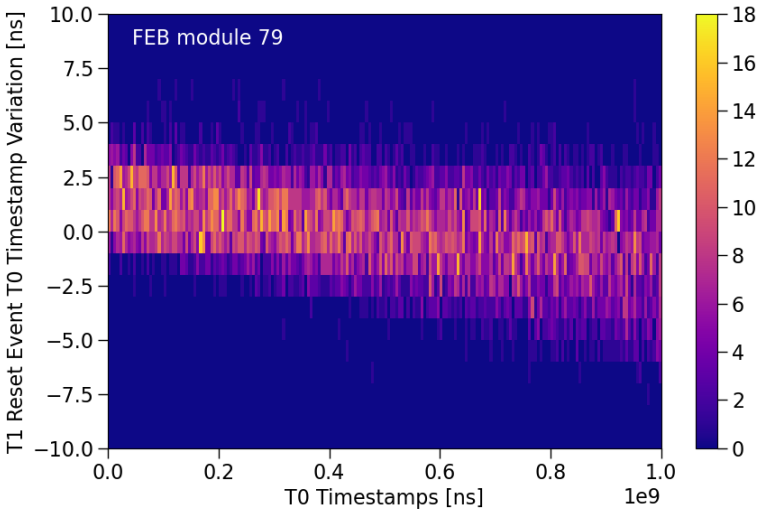


Fig. 7.6 Variation of T0 timestamps of T1 clock reset events as a function of the T0 timestamp.

These plots are useful diagnostic tools to characterise the timing of the FEB modules, including monitoring the magnitude and stability of the T0 and T1 clocks as well as the drift of the T0 clock. It is important to note that the T0 and T1 clocks of the FEB can potentially vary from run to run, and they are very sensitive to external noises. The plots have been reproduced by the CRT working group of SBND during the CRT installation periods and they will also be produced for online monitoring purposes in order to track the clock stability and resolution of the FEB modules.

7.2.2 Alternative Timing Reconstruction

In addition to the timing characterisation, the SPEC-TDC can also provide an alternative timing reconstruction method for events recorded by CRTs. The study here was performed using a data set recorded by the CRT Sharps of ~9000 beam events. The CRT 2D hit time was

reconstructed from coincidental hits of 2 cross scintillator strips, and corrected for cable and propagation delay. The CRT hit time T0 was reconstructed using the T0 timestamp whilst the CRT hit time T1 was reconstructed using the T1 timestamp. Commonly, the timing reconstruction of CRT data only uses the CRT hit time T1 in reference to the beam. Here, the timing reconstruction using CRT hit time T0 instead is presented.

Firstly, the beam spill was reconstructed as shown in Fig. 7.7a and 7.7b using CRT hit time T1 and T0 respectively. The beam spill in Fig. 7.7a was plotted directly using CRT hit time T1 since it is a reference to the BES signal. The plot shows a beam excess to the cosmic background, corresponding to the BNB beam arriving 333 μs after the BES signal and lasting for 1.6 μs. On the other hand, CRT hit time T0 is in the reference frame of the PPS and needs to be corrected to the beam arrival time to reconstruct the beam spill. The correction was done using BES signals recorded by the SPEC-TDC, of which the timestamps are also with respect to the PPS. The beam spill structure acquired from this method shows a good agreement as shown in Fig. 7.7b, where the same beam excess can be seen. It is important to note that the reconstruction of the beam spill only requires a resolution $\mathcal{O}(1\ \mu\text{s})$, which is satisfied by both the T0 and T1 clock resolution $\mathcal{O}(2\ \text{ns})$.

The next step was to reconstruct the substructure of the BNB, made up of 81 Gaussian buckets of width 1.308 ns and separated by 19 ns. Given the limited statistics of the sample to fully plot 81 buckets of a whole beam spill, the buckets were overlaid on top of each other by taking the modulus of 19 ns. The resulting beam buckets using CRT hit time T1

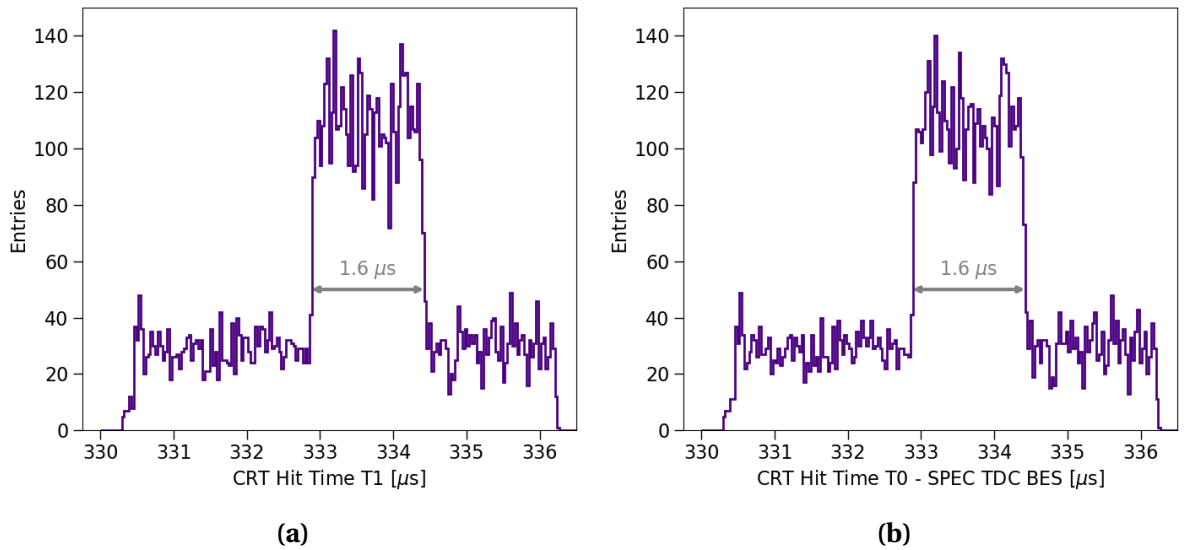
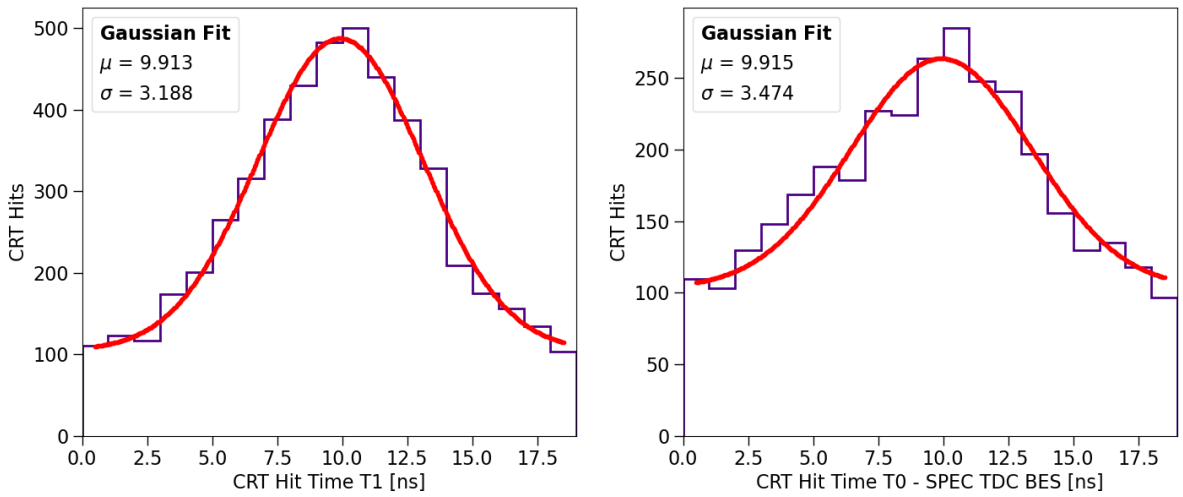


Fig. 7.7 Beam spill reconstructed using (a) CRT hit time T1 and (b) CRT hit time T0 combined with the SPEC-TDC timing information.

and CRT hit time T0 combined with the SPEC-TDC timestamps are shown in Fig. 7.8a and 7.8b respectively. Using the CRT hit time T1, the beam bucket was resolved even with the limited statistics, recovering a Gaussian width of 3.2 ns. However, from the CRT hit time T0 distribution, the Gaussian shape is more smeared out with a larger width of 3.5 ns. This is due to the resolution of the T0 clock being shown to be $\mathcal{O}$(2 ns), which is larger than the width of the beam bucket.



(a) **(b)**

Fig. 7.8 Beam bucket reconstructed using (a) CRT hit time T1 and (b) CRT hit time T0 combined with the SPEC-TDC timing information.

Both the reconstruction of the beam spill and beam bucket demonstrate that the CRT hit time T0 can be utilised together with the SPEC-TDC. This alternative timing reconstruction shows promising early results and certainly has the potential for more improvements. Additionally, this showcases the versatile usages of the SPEC-TDC, where its recorded timestamps can be used in conjunction with other detection subsystems.

7.3 Timing Performance of CAENV1730 Digitisers

Following the timing characterisation of the CRT readout electronics, the next focus is on the PMT readout electronics, CAENV1730SB digitisers. Sec. 7.3.1 provides a description of the CAENV1730's internal clocks. Following that, an evaluation of the timing synchronisation across multiple digitisers is presented in Sec. 7.3.2 and a clock jittering correction method is presented in Sec. 7.3.3.

7.3.1 Internal Clock and Timestamp Structure

A description of the PMT readout electronics, CAENV1730SB digitisers, was provided in Sec. 4.2.4. The internal clock of interest is called REF-CLOCK in the clock domains of CAEN digitiser [3]. The REF-CLK is a clock chain responsible for a synchronous sampling and triggering rate, and thus the timing precision of the CAEN digitiser. The REF-CLK frequency serves as an input to a clock distribution device AD9510, generating three types of frequencies: (1) an ADC sampling clock, (2) a trigger clock and (3) an output clock for external use. The AD9510 device must be programmed for an input frequency to the REF-CLK connector so that all three clock frequencies are phase-locked-loop with the input.

Firstly, the ADC sampling clock has a frequency of 500 MHz. The PMT waveform is therefore sampled with a tick value of 2 ns/tick. Secondly, the trigger clock operates at 125 MHz and is responsible for handling the triggering and synchronisation logic. The trigger clock has a tick value of 8 ns/tick. However, since it is read every two clock cycles, it potentially has a fluctuation of up to 16 ns/tick. Finally, the last clock is a programmable frequency output via the CLK-OUT connector and can be propagated to another CAEN digitiser for synchronisation purposes.

At SBND, CAEN digitisers are configured to use an external clock fed to the REF-CLK with signals from the WR timing system described in Sec. 7.1.1. The clock signal is input to the CLK-IN connector, with frequency depending on the clock synchronisation scheme. This signal behaves as a *metronome frequency* for all three clocks described above. The PPS signal is input to the S-IN connector and is used by the trigger clock. It resets the counter of the trigger clock every second so that the timestamps output by CAEN digitisers share the same reference frame as other readout electronics.

Unlike the timestamp generated by FEB modules or the SPEC-TDC, where it is the number of clock ticks upon receiving a trigger, the timestamp produced by CAEN digitisers is structured differently. Fig. 7.9 illustrates the time structure of a waveform recorded by CAEN digitisers. Upon receiving a trigger at the TRG-IN connected, as shown in grey, there is a latency before the digitiser acting on the trigger, as shown in red. The waveform duration can be any portion pre or post-trigger as shown by the red and blue boxes. For every trigger, the CAEN trigger clock produces a timing object called a trigger time tag. However, the trigger time tag is not instantaneous upon the trigger arrival, it is instead the timestamp value of the last tick on the waveform, as shown in green. Therefore, careful timing reconstruction is needed when decoding the waveforms from CAEN digitisers.

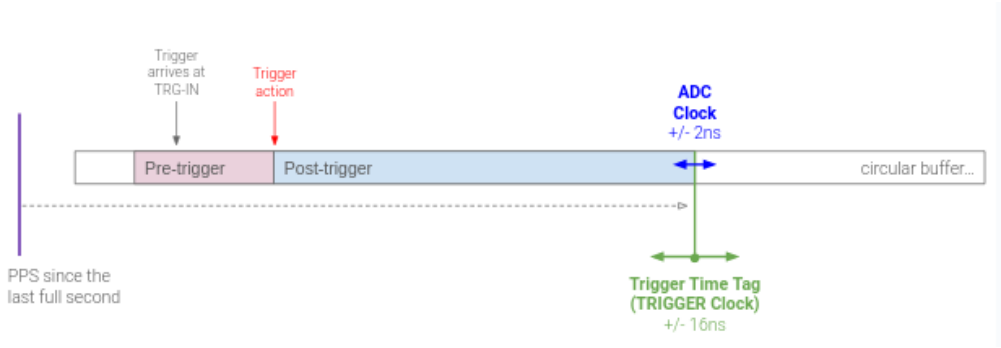


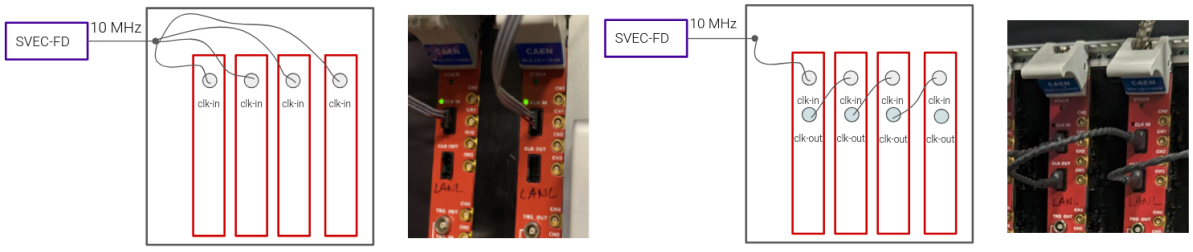
Fig. 7.9 Timing structure of a waveform digitised by CAEN digitisers.

7.3.2 Evaluation of Clock Synchronisation

Multiple CAEN digitisers can be synchronised to behave as if a single digitiser. It is crucially important to record PMT waveforms in synchronisation since they are the key ingredients for timing reconstruction with a resolution $\mathcal{O}$(2 ns) as previously detailed in Sec 6.3.1. The synchronisation can be achieved through two different clock synchronisation schemes: (1) fan out and (b) daisy chain, as shown in Fig. 7.10.

In fan out mode, each digitiser is input with the clock signal set at 10 MHz clock. The 10 MHz was chosen at the time since it is the highest frequency produced by the SVEC-FD card. The clock signal is distributed to a fan out module, and then into the CLK-IN connector of each digitiser. The cable length of each clock signal is identical so that all clock signals arrive at CAEN digitisers at the same time.

In daisy chain mode, the first CAEN digitiser in the daisy chain receives the 10 MHz clock, referred to as the master clock. Its clock is then propagated to the next digitiser in the chain, referred to as the slave clock. The master clock can be precisely programmed with a delay $\mathcal{O}$ (300 ps) to account for cable lengths, ensuring that the master and slave clocks are in phase



(a) Fan Out

(b) Daisy Chain

Fig. 7.10 Diagram illustrating two clock synchronisation schemes, (a) fan out and (b) daisy chain.

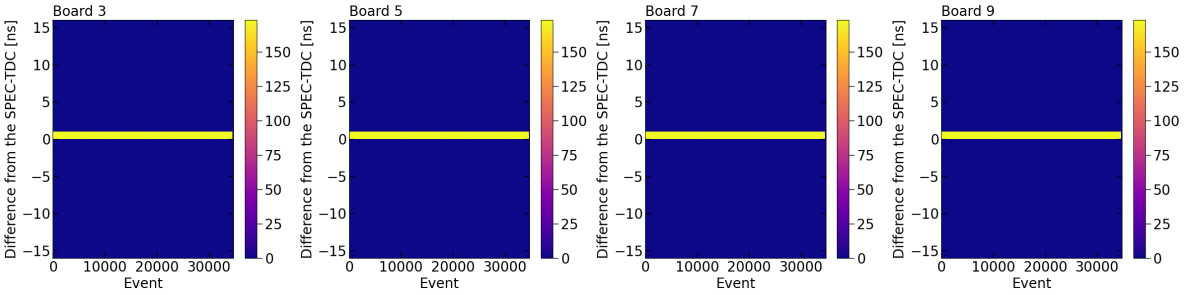
with each other. The clock propagation continues from one digitiser to the next digitiser in the chain, until the last digitiser in the chain is in the same clock phase as the first one.

The timing characterisation study was carried out to determine which clock synchronisation scheme provides the best precision and stability. The setup consisted of 8 CAEN digitisers located in the same VME crate. Each digitiser received an identical trigger with the same cable length so every digitiser was triggered simultaneously. The trigger rate was set as 1 Hz for simplicity.

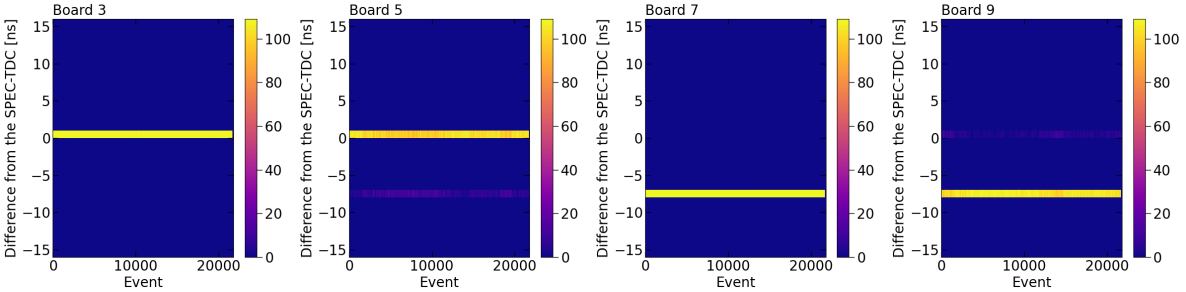
To evaluate the synchronisation of CAEN digitisers, their timestamps of triggered events were directly compared against the same timestamps recorded by the SPEC-TDC since both are referenced to the PPS signal. Similar to the approach with the CRT readout electronics, the SPEC-TDC offers a higher level of precision compared to the CAEN digitiser, 700 ps compared to ~1 ns. For an ideal synchronisation, the timestamps of every triggered event from every digitiser should be identical with respect to each other, and also with respect to the SPEC-TDC after cable correction.

Some results of synchronisation using the daisy chain are shown in Fig. 7.11, depicting the differences of timestamps CAEN digitisers from the SPEC-TDC as a function of the event number. Only 4 out of 8 CAEN digitisers are shown for run 7980 and run 8060, however, similar results were observed for the rest of the digitisers. Run 7980 in Fig. 7.11a demonstrates a perfect synchronisation across all 8 CAEN digitisers. Their differences with respect to the SPEC-TDC are constant at 0 across all the events and all the digitisers. This shows a very good and stable synchronisation. In contrast, run 8060 exhibited some interesting effects as shown in Fig. 7.11b. Firstly, board 5 shows a straddling effect, where the observed differences jitters between 0 and 8 ns. This behaviour could be due to the CAEN trigger clock of the CAEN digitiser being read every 2 clock cycles, introducing some fluctuations. Moreover, board 7, which received a clock signal from board 5 in the daisy chain, drifted by 8 ns. Following that, board 9, receiving clock from board 7, also drifted by 8 ns. This demonstrates that if one clock in the daisy chain drifts, subsequently clocks in the chain will also drift.

The same test was repeated for the fan out fan scheme. Some example results are shown in Fig. 7.12 for run 8178 and run 8196. Firstly, in both of these runs, board 5 shows the same straddling effect, causing timestamps to jitter by 8 ns. The second observation is that the timestamp differences vary randomly between digitisers and across different runs. For instance, the timestamp difference of board 9 is stable at -8 ns in run 8178 but stays at +8 ns in run 8196.

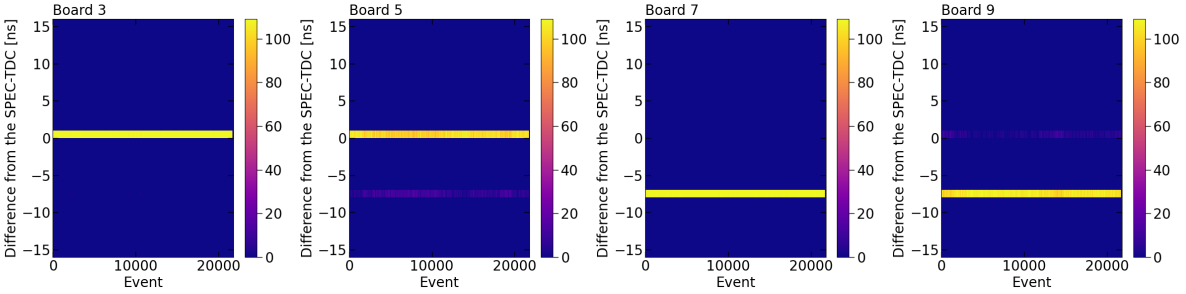


(a) Run 7980

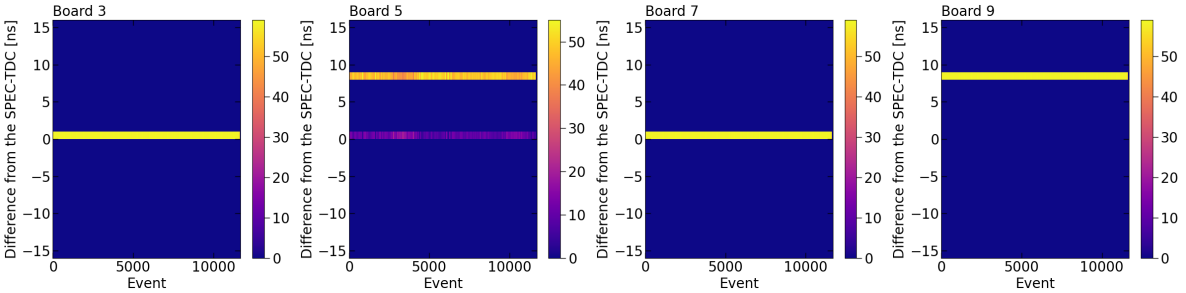


(b) Run 8060

Fig. 7.11 Differences in trigger timestamps between CAEN digitisers and the SPEC-TDC with the CAEN digitisers using the daisy chain clock scheme.



(a) Run 8178



(b) Run 8196

Fig. 7.12 Differences in trigger timestamps between CAEN digitisers and the SPEC-TDC with the CAEN digitisers using the fan out clock scheme.

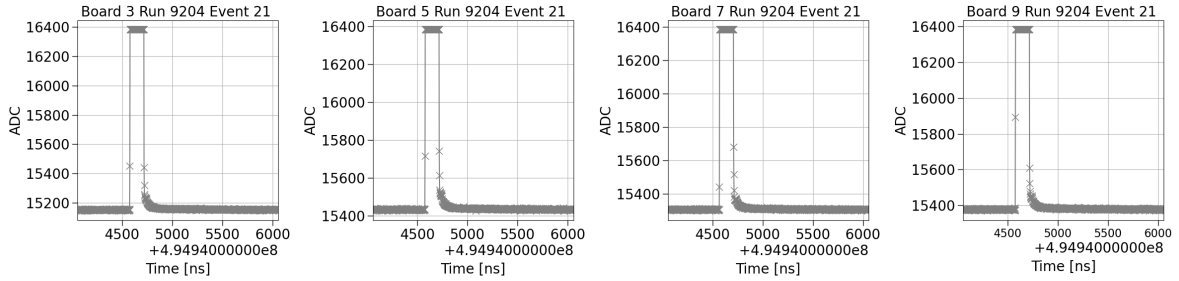
This behaviour is due to the input frequency to the CLK-IN connector set at 10 MHz. As previously explained, the trigger clock is generated by the AD9510 chip, which must be in phase with the input frequency. However, the trigger clock operates at a frequency of 125 MHz, while the input frequency is at 10 MHz. Since these frequencies are not multiples of each other, they cannot be in phase. To generate an out-of-phase frequency, the AD9510 chip latches onto the first rising edge of the input frequency upon the digitiser initialisation. This results in a random phase offset at the beginning of every run, causing the timestamps to vary from run to run and from board to board.

Comparing the two clock schemes, the daisy chain mode offers better synchronisation across the 8 CAEN digitisers compared to the fan out mode. In the daisy chain scheme, only the first CAEN in the daisy chain receives the external 10 MHz clock. The master clock CAEN digitiser will have a random phase offset that is propagated down the daisy chain, resulting in synchronisation across all digitisers. However, the clock drift effect was observed during the testing the daisy chain scheme and therefore, a correction is necessary.

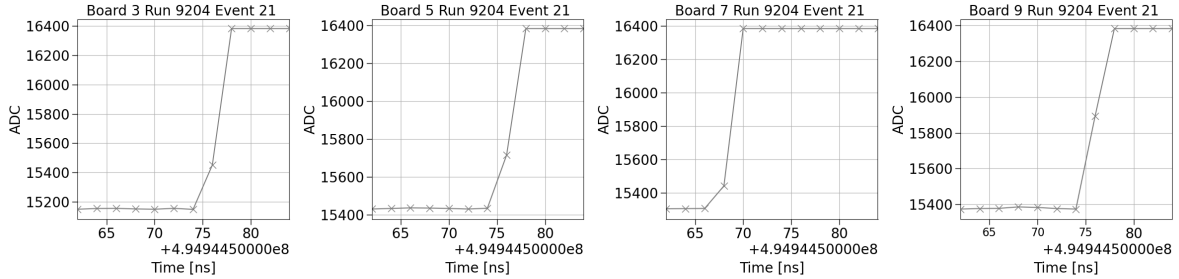
7.3.3 Clock Jittering Correction

To further characterise the timing of the CAEN digitiser, another study was carried out to verify if all 8 CAEN digitisers can digitise waveform in synchronisation with each other $\mathcal{O}$ (1 ns). The same setup was used as described in the previous section, with a new addition of digitising the waveform of the trigger signal in channel 15 of every CAEN digitiser. All the cable lengths were identical so that all trigger signals took the same amount to propagate to the digitisers. The daisy chain clock scheme was also calibrated so that the clock propagation from the master clock to the slave clock was delayed by a precise amount such that their clocks were exactly in phase. This was to ensure that trigger signals were simultaneously timestamped and digitised.

Examples of digitised waveforms of trigger signals are plotted in Fig. 7.13a for four digitisers, where the trigger signals can be seen as a single square wave per digitiser. To examine if trigger signals were digitised simultaneously, zooming into the rising edges of the trigger signals is plotted in Fig. 7.13b. Board 3, 5 and 9 are in synchronisation except for board 7. The rising edge of board 7 is at a different location compared to other boards, showing that its clock jittered. This behaviour although did not occur frequently, was unpredictable and could appear across different events, different runs and different boards. Therefore, a jittering correction was devised to account for clock jittering scenarios.



(a) Full waveforms

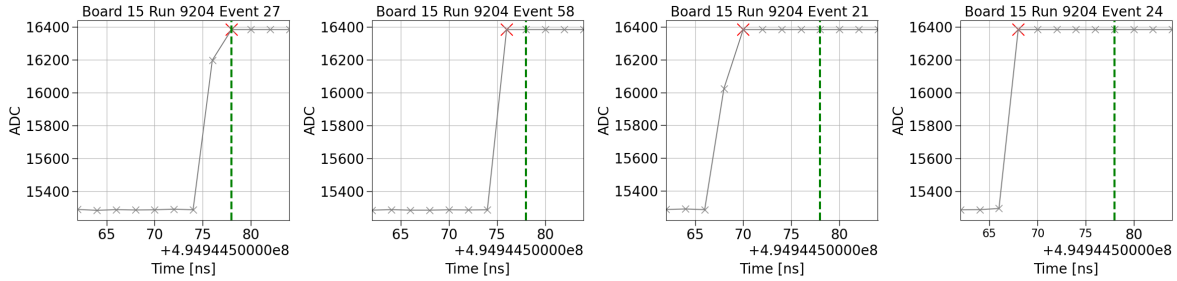


(b) Zoom into the rising edge

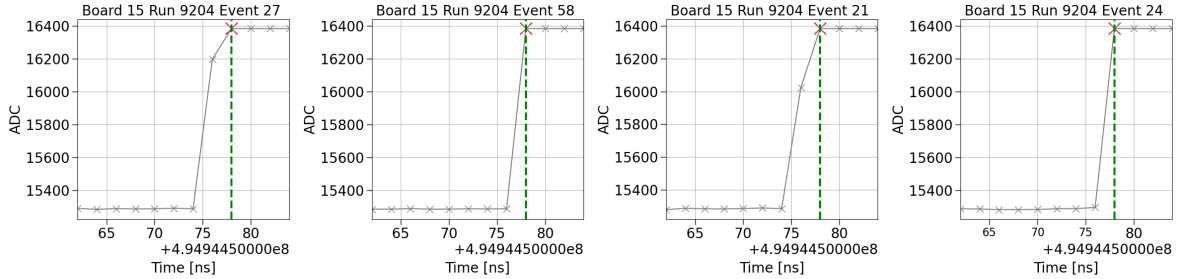
Fig. 7.13 Plots showing (a) full digitised waveforms of trigger signals and (b) zoom into the rising edge.

The timestamp of the rising edge of trigger signals digitised by CAEN digitisers is then compared against the timestamp recorded by the SPEC-TDC of the same trigger signal. This comparison helps the understanding of the clock jittering behaviour of the CAEN digitiser. Three identified cases of jittering are illustrated in Fig. 7.14a. The trigger waveform is plotted in grey, the rising edge is marked with a red cross and the timestamp of the trigger recorded by the SPEC-TDC is plotted as the vertical green line.

In the far left plot, the timestamp of the rising edge and the SPEC-TDC agree with each and hence, the red cross and the green line align. The middle left plot shows the first case of clock jittering of one whole tick, equivalent to 2 ns. This is due to the ADC sampling clock jitters while the triggering clock remains stable, resulting in a different tick value of the rising edge. In the second case, the opposite situation arises such that the tick value of the rising edge is stable however the trigger clock jitters in the step of 8 ns. This is illustrated in the middle right plot, where the rising edge and the SPEC-TDC differ by exactly 8 ns. The last case is the combination of jittering from both clocks. This is shown in the far right plot, where the difference between the rising edge and the SPEC-TDC is equal to the sum of the trigger and ADC sampling clock tick, totalling at 10 ns.



(a) Before Correction



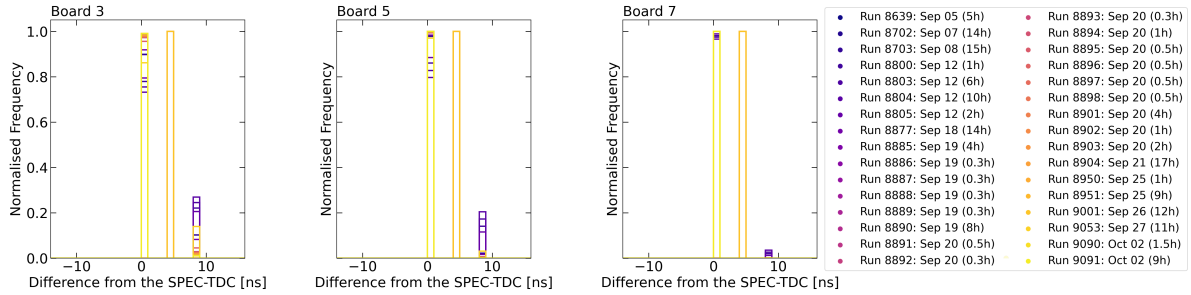
(b) After Correction

Fig. 7.14 Plots showing digitised waveforms of trigger signals zoom into the rising edge (a) before correction and (b) after correction.

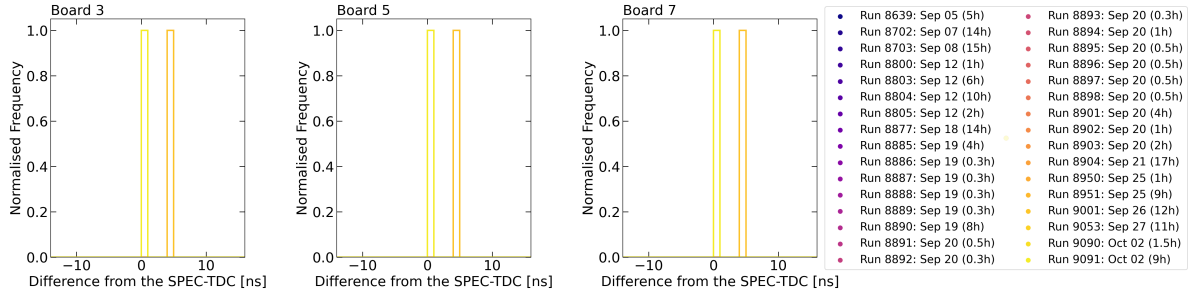
This comparison exercise also demonstrated a possible clock jittering correction. By digitising the trigger signal synchronously on every digitiser, the recorded waveform of the trigger in combination with the SPEC-TDC provides all the necessary information to apply correction. One can simply derive the correction amount by performing the comparison as above. The digitised trigger waveforms after applying correction are illustrated in Fig. 7.14b.

This correction method was validated using multiple runs over one month. Each run duration varied from less than 1 hour up to 10 hours. Fig. 7.15a demonstrated the results conducted on a dataset of 30 runs, showing the 1D histogram of the difference between the timestamp of the rising edge as compared to the SPEC-TDC. The plots are area normalised to compare across different run durations. Before correction, some amount of jittering can be seen across different digitisers, events and runs, with peaks at 4 and 8 ns. The correction was first applied event by event, as shown in Fig. 7.15b. Then, the correction was applied run by run, as shown in Fig. 7.15c. The result is a perfect alignment between the CAEN digitisers and the SPEC-TDC, with their differences forming a single peak at 0 ns.

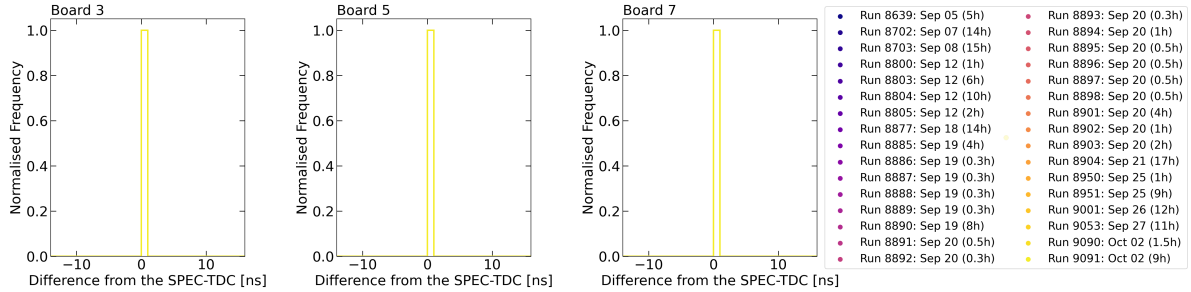
This clock jittering study presented here has resulted in a new hardware proposal at SBND. The proposal is to digitise the trigger signal in channel 15 of every CAEN digitiser



(a) Before correction



(b) After correction event by event



(c) After correction run by run

Fig. 7.15 Differences in trigger timestamps between CAEN digitisers and the SPEC-TDC at each correction step.

as this will provide the necessary timing information for downstream jittering correction. Further adjustment to the proposal includes an additional CAEN digitiser specifically for digitising beam signals. This is vital timing information needed by downstream analysis to reconstruct the BNB substructure as demonstrated by the MicroBooNE collaboration [4].

At the time of writing, several changes have happened to the clock setup of CAEN digitisers. Firstly, further consultation with the CAEN manufacturer led to a new clock synchronisation scheme. A 6.25 MHz clock is now distributed in a fan out mode to every digitiser. Even though it is a lower frequency than 10 MHz, it is a multiple of both the trigger

clock, 125 MHz, and the ADC sampling clock, 500 MHz. The same clock synchronisation study was performed and the digitised trigger waveforms show a good agreement to the SPEC-TDC within 1 ns. This configuration shows an improvement in clock synchronisation and stability than the two methods explored in Sec. 7.3.2. Secondly, digitised waveforms trigger signals, as shown in Fig. 7.13 and 7.14, were evidently saturated. Hardware attenuators were installed, followed by an adjustment of the waveform signal. This ensures to capture of the full shape of the trigger waveforms without damaging the digitisers.

7.4 Concluding Remarks

The timing system at SBND was outlined, detailing the signal distribution to ensure synchronisation across different DAQ subsystems. As part of the timing system, the SPEC-TDC module records extra timing information applicable for versatile usages. The SPEC-TDC has been demonstrated to characterise the timing of the CRT and PMT readout electronics as well as to explore alternative timing reconstruction to reconstruct the beam structure. Most importantly, it was used to examine the clock synchronisation of CAEN digitisers and helped devise a correction method to account for clock jittering. This is a crucial correction as PMT waveforms are the main signals to perform nanosecond timing reconstruction. In the following, the next Chapter 8 will focus on the calibration of the SBND detector, which is another essential step to pin down detector effects affecting physics measurement accuracy.

References

[1] J. Serrano et al., "The White Rabbit Project", in Proceedings of the 12th International Conference on Accelerator and Large Experimental Physics Control Systems, Vol. 1 (2009), p. 93.

[2] A. Aloisio et al., "FPGA implementation of a high-resolution time-to-digital converter", in 2007 IEEE Nuclear Science Symposium Conference Record, Vol. 1 (2007), p. 504.

[3] *730 Digitizer Family 16/8 Ch. 14-bit 500 MS/s Digitizer*, Accessed: 25-02-2023, https://www.caen.it/products/v1730/.

[4] P. Abratenko et al. (MicroBooNE Collaboration), "First demonstration of $\mathcal{O}(1$ ns) timing resolution in the MicroBooNE liquid argon time projection chamber", Phys. Rev. D **108**, 052010 (2023).