# Simulation and Analysis of Multiple Traffic Time-Triggered Ethernet based on OMNeT++

Qinghua Yang
School of Mechanical Engineering and Automation,
Shanghai University
Shanghai, China
yqh_lw@163.com
* Corresponding author: yqh_lw@163.com

Zhen Liu
School of Mechanical Engineering and Automation,
Shanghai University
Shanghai, China
1260212889@qq.com

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***Abstract*—Avionics full-duplex switched Ethernet (AFDX), as the backbone network in civil avionics systems, can transmit event-based device messages. However, with the increase in real-time business requirements of avionics systems, numerous key data need to use clock synchronization at the sender to comprehensively schedule flows of different trigger mechanisms, and expand the high-bandwidth communication architecture to meet Quality of Service (QoS). This paper use OMNeT++ simulator to establish the End System (ES) and switch network topology which adopts clock synchronization on the basis of Time-Triggered Ethernet (TTE). We first simulate the End-to-End Delay of Rate Constrained traffic for each Virtual Link (VL) and compare simultaneously other two approaches to limit the End-to-End latency of AFDX, the results show that the Network Calculus (NC) and Trajectory Approaches (TA) increase in pessimism in most cases. Then we expand the Gigabit network topology of each message scheduling communication paradigm, compared with the traditional AFDX scheduling strategy, and verify that table scheduling can solve Sequence Number (SN) inversion to a certain extent. The experimental results also show that the table scheduling strategy based on time reservation can not only provide time triggered traffic planning establishes transfers to ensure low latency and minimal jitter, while also reducing worst-case end-to-end latency for Rate-Constrained (RC) and Best-Effort (BE) flows.**

***Keywords-AFDX;Simulation; Clock Synchronization; Traffic; Delay Analysis***

## I. INTRODUCTION

AFDX, whose information exchange is based on the Ethernet standard and compliant with the ARINC 664 specification Part 7, breaks the traditional Carrier Sense Multiple Access with Collision Detection (CSMA/CD) network architecture, and uses VLs to allocate bandwidth resources more effectively and reduce communication congestion while simplifying and efficiently Design communication systems on aircraft while meeting the security, redundancy, and reliability requirements for avionics [1]. However, with the deepening of the integration and modularization of avionics systems, and the greatly enhanced requirements for data communication in terms of bandwidth, real-time performance, and reliability, Time-Sensitive Networks (TSN) in the form of resource reservations and Time-Triggered Networks in the form of schedules Real-time determinism of complex services by Ethernet is a future trend. The following TABLE I. compares them in different aspects.

TABLE I. COMPARISON OF DIFFERENT NETWORKING SOLUTIONS

| Network Scheme | Different Networking Solutions | | |
|---|---|---|---|
| | ***AFDX*** | ***TSN*** | ***TTEthernet*** |
| Protocol Features | A380, C919, etc. ARINC664 Bus Standard | Vehicles, Industrial Internet, 5G fronthaul Network Standards | SAE Standard for Hybrid, Critical, Real-Time Applications |
| Synchronization | None | Master-Slave Synchronization | Global/Local Synchronization |
| Redundancy Management | Dual Redundancy | Dual Redundancy | Multiple redundancy |
| QoS | Device Message | Add Multimedia, application data | Add Application Data |
| Bandwidth Rate(Max) | 100Mbps | 1000Mbps | 1000Mbps |

It is found that the new generation of avionics system interconnection technology represented by Time-Triggered Ethernet (TTE) has been typically applied and considered in the integrated electronic system. TTEthernet is a real-time network based on a time-triggered protocol proposed by TTTech [2], which uses the SAE AS6802 protocol [3] to ensure the clock synchronization of each terminal node in the system, and is compatible with ordinary Ethernet, AFDX networks and Time-triggered messages. With TTEthernet bandwidth rates up to 1000Mbps, experiments and analysis by J. F. Suen et al. provide solid evidence that Gigabit solutions are suitable for large-scale integrated avionics systems [4]. Due to its high transmission rate and reliability, the performance of expanding AFDX network is very crucial. For computing worst-case End-to-End delays, H. Bauer et al. combined Network Calculus, Trajectory Approach [5][6] reserves the most stringent computational upper bound for each VL path, which tends to be pessimistic. The simulation method can configure the performance parameters for comparative analysis and make the network characteristics more comprehensive [7], so we considered the simulation method to evaluate the avionics AFDX network. Before transmission, TTEthernet pre-defines a global and unified time planning table according to key business requirements and transmission cycles [8], and then transmits data according to the time plan to ensure that key traffic (TT and RC) will not be transmitted by other non-critical traffic (BE) Preemption, but it does not take into account the impact of special scenarios which is too ideal. J. Yao et al.

proposed a method to integrate critical and non-critical flow, but it preserves the original network bandwidth and better use it for non-critical traffic. O. Hotescu et al. Improves the BE flow guarantee and increases the transmission volume of RC flows in ES by integrating TT scheduling designed using a modified SMT method [9], but it does not analyze the impact of each flow delay.

The main contribution of this paper is to compare different end-to-end delay analysis methods. At the same time, the TTEthernet protocol is used to expand the AFDX communication architecture based on gigabit bandwidth, and the table scheduling of time reservation is improved at the sending terminal system level to reduce the End-to-End delay and jitter which can solve SN inversion for redundant frames. The second part introduces the architecture of time-triggered Ethernet. The third part compares the end-to-end delay of RC traffic evaluated by different methods. The fourth part expands the model to simulate the AFDX-compatible Gigabit real-time network, and analyzes the QoS of various flows.

## II. TTETHERNET ARCHITECTURE OVERVIEW

### *A. Fully Compliant with AFDX*

#### *1) ES*

The terminal system provides an interface between AFDX and the subsystem and its avionics equipment. The terminal system receives the information flow of the avionics equipment in the communication port (sampling and queue), and encapsulates it in the Ethernet protocol and transmits it to AFDX. Therefore, further changes (adding additional networks or BE Ethernet) are possible without modifying the previous AFDX architecture organization as long as there is sufficient bandwidth, traffic shaping to ensure bandwidth constraints allocated to VLs, ES sending arbitrary VL instances, and implement traffic shaping and First Input First Output (FIFO), round-robin scheduling.

#### *2) Switch*

Switch operation is based on a "store-and-forward" model, when frames are received on an input port, the switch starts using filters and scheduling policies such as Static Priority Queuing (SPQ) and then forwards them to the corresponding output ports [1]. Divide switch configuration traffic into RC traffic (pure AFDX TTEthernet), TT traffic and BE traffic, that is, audio and video monitoring traffic. The ability to use time-triggered services, traffic policing to ensure bandwidth limits for VLs can be added.

#### *3) VL*

The path between sender and receiver has a unique VL ID. A VL defines a unidirectional path from one ES to one or more target ES. All VL IDs have the same CT tag, and the VL ID is encoded in the lower two bytes of the destination MAC address. The Maximum Frame Size (MFS) which called Lmax: The ES can accommodate virtual link frames of 64-1518 Bytes. For the shortest time between two frames of each VL, that is, the Bandwidth Allocation Gap (BAG), the End-System traffic shaping function should be able to control the value of the BAG within the range of 1ms to 128ms, generally a power of 2. This limit will be enforced by "BAG policing" in the switch, the RC traffic itself does not guarantee timing or jitter or maintain order of transmission, only determines the bandwidth limit.

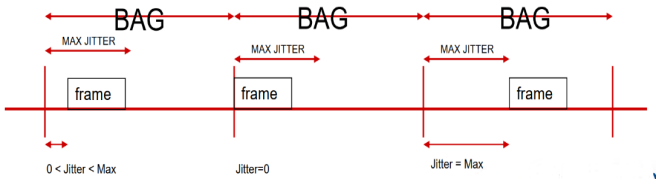


Figure 1. BAG and Jitter

Bounded Maximum Jitter≤500μs [1].

#### *4) Frame structure*

The AFDX frame based on the Ethernet is shown in Figure.2 CT Marker and CT ID is equal to Destination Address which carries the VL.

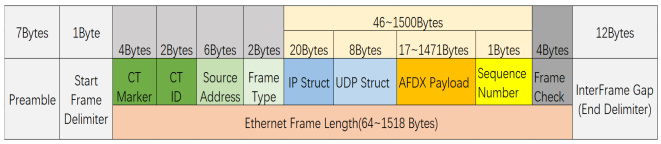


Figure 2. Ethernet Frame

#### *5) Redundancy Management (RM)*

The partition of the sending ES sends a protocol frame with a SN [10], and the SN is incremented in two consecutive frames, and the receiving ES can reconstruct a single sequenced frame before the communication protocol stack below the IP layer. frame stream without duplication. RM is usually placed after the Integrity Checking, and the transfer can only be accepted under the faultless network operation.

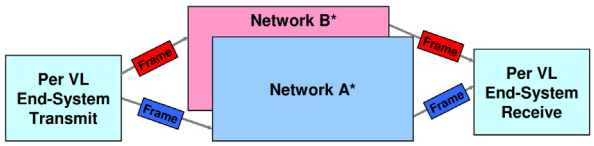


Figure 3. Describe Redundancy

### *B. Clock Synchronization*

#### *1) Synchronization domain*

The components, Synchronization Master (SM) and Compression Master (CM), with a common concept of time are called Synchronization Domains, and usually the SM function is located in the ES and the CM function is located in the switch.

#### *2) Protocol Control Frame (PCF)*

Based on the SAE AS6802 protocol, a PCF is defined to synchronize the local clock of each device. Each TTEthernet component has a local clock, and the time-triggered system periodically resynchronizes these clocks, ensuring that all Time-Triggered communications are delivered as scheduled, and that the sending instant is Time-Triggered with known End-to-End delay and minimal jitter [11]. However, the reception of Time-Triggered frames of these components and the communication between regular Ethernet do not require clock synchronization. PCF is a TTEthernet frame of an

Ethernet frame with a special "Ethertype" field (value 0x891D), in which a communication cycle is a power of 2 times an integration cycle, exchanged between TTEthernet components to establish and keep in sync.

## III. METHOD FOR RC TRAFFIC DELAY ANALYSIS

### A. Clock Model

The time between "ticks" which can be configured is critical to the TTEthernet synchronization. The local clock can be synchronized to an external time reference (such as GPS time), performed by the host CPU to slightly speed up or slow down the local clock without being modified by the application. In order not to completely affect the accuracy of this network topology, we assume that the model clock is ideal.

### B. TTE Component on OMNeT ++

Implementing TTE terminals requires extending the AFDX architecture [12], which combines a message classification module, a scheduler, and a synchronization module. Various classification modules allow to classify received messages according to their type and transmission process, the terminal of this model only sends RC traffic. The role of the scheduler is to send and receive messages according to a messaging plan. AFDX ES under OMNeT++ are shown in the Figure. 4 below.

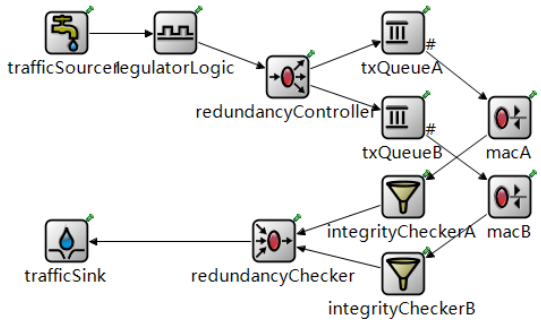


Figure 4. Synchronization Master (ES)

The switch expects frames from the sender within a specific time interval (window), RC traffic frame intervals exceed the BAG, and VL traffic exceeding the limit will be silently suppressed. AFDX Switch are shown in the Figure. 5 below.

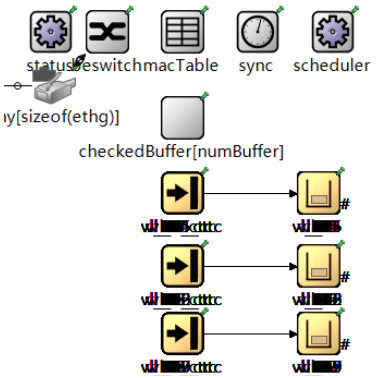


Figure 5. Compression Master (Switch)

### C. Topology Study

#### 1) Model configuration

The parameters configured in each ES initialization file are: MAC address, VL-ID, packet size, port number and BAG, which we modified in [13] for a representative example of a small to medium AFDX configuration network. The network consists of three switches (s1, s2, s3) and thirteen ESs: eight transmitters and three receivers. VL1~VL5 have a BAG=4ms, VL6~VL8 have a BAG=16ms, VL9~VL11 have a BAG=64ms, Lmax of all VL is 500 Bytes. The overall network bandwidth runs at D=100 Mbps and the delay from input to output port of a switch is considered to be a constant t = 16μs.The Network Typology is shown in the Figure. 6 below.

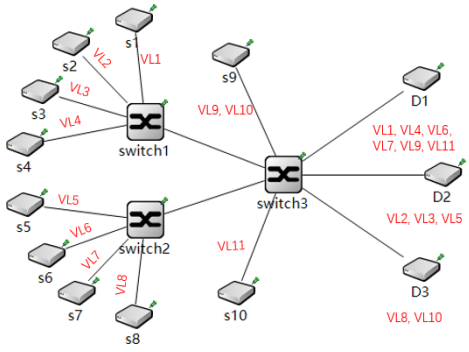


Figure 6. VL on End-to-End System

#### 2) End-to-End delay analysis

The End-to-End delay is the sum of fixed (transmission path) and variable delays [14], the analysis can be expressed in the form of equation (1)

$$D(Fv,Px)=LD(Fv,Px)+SD(Fv,Px)+WD(Fv,Px) \quad (1)$$

The end-to-end delay of a data frame Fv on the VL Px is equal to the sum of transmission delay (fixed delay), switching delay and buffering delay. Among them, LD(Fv,Px) is the transmission delay of the VL, SD(Fv,Px) is the time delay required for the data frame to pass through the switch (16μs), WD (Fv,Px) is the delay in the output buffers of the ESs and Switches. We compared three methods for evaluating the End-to-End latency of AFDX networks [5], and the results are shown in Figure. 7.

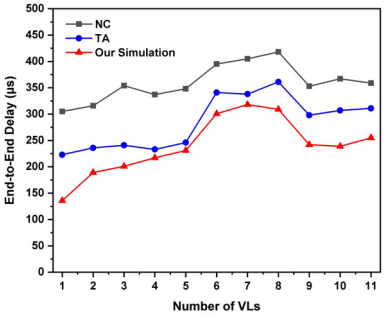


Figure 7. Methods Comparison

*3) Result of comparison*

From Figure.7 we can conclude that the NC considers the worst case of the nodes visited by the flow and the maximum possible jitter introduced by the previously visited nodes. TA outperform NC when network load increases (larger packet size and lower BAG value). But for VL with small packet size, the TA overestimates the worst-case response time, and its pessimism increases. Based on our analysis results for small and medium configurations, it can be seen that the minimum inter-frame delay and frame length directly affect the performance of both methods. In fact, some VLs are sent directly at the input port of the sending ES, without waiting for contention. Finally, in order to simplify the modeling process, we adopt the method of simulation. At this time, the value obtained by the OMNeT++ simulator represents a special scenario, regardless of the final value. In the worst case, this explains the relatively low values obtained by the first two methods.

## IV. EXTEND SIMULATION FOR AVIONICS FRAMES

### *A. Multiple Traffic over Higher Bandwidth*

Traditional AFDX only supports 10/100Mbps transmission. In order to meet the technical parameters and performance of AFDX protocol rules, the simulation method based on TTEthernet can be extended to a Gigabit network to meet the real-time transmission of key traffic and use the remaining bandwidth to transmit video streams. In order to achieve a more optimized QoS, various traffic transmission scenarios described before are achievable [9].

### *B. Improved Table Scheduling Strategy*

In the AFDX network RM, the receiving order may be different from the sending order, and the SN inversion problem is relatively common. According to the analysis in the previous paper [10], the main reasons for the sequence inversion phenomenon in the redundant network are jitter, delay and frame size differences. In order to optimize the resulting potential failures, this paper proposes a table scheduling method based on time reservation:

Scheduling at the terminal system level is mainly divided into three types of traffic. TT traffic (PCF, etc.) has the highest priority, RC traffic has two priorities, and BE traffic will be transmitted in the remaining bandwidth [8]. For critical traffic consider using the SMT method to synthesize global static scheduling of TT streams to reduce the impact of TT messages on RC messages [15].

We improve this model: In the local clock configuration, since clock drift and jitter are not "exactly known", an acceptance window needs to be defined. When the SM transmits a PCF to the CM and hopes to receive it back at the "right time", the TTEthernet component accumulates the transmission delay per PCF, and the receiver can read the total transmission delay in the PCF. The network needs to know the total amount of transmission delay to determine when a frame becomes permanently running synchronously. The recipient can determine the "Earliest Safe" point at which the PCF becomes permanent by subtracting the Eternity Run time (the difference between the Maximum Transmission Delay and the Transmission Delay) from the Reception Time Point. Any critical flow (PCF/TT/RC) is evenly spaced from BAG Reservation (BR) or Column Reservation (CR) [8]and schedules lower priority BE traffic during idle time.

### *C. Topology Study*

*1) Model configuration*

To evaluate the performance of table scheduling on RC stream delivery, network calculus has been used to compute the end-to-end delay bounds of RC streams [8]. We simulate and verify the high-bandwidth AFDX extension traffic in Figure. 8.

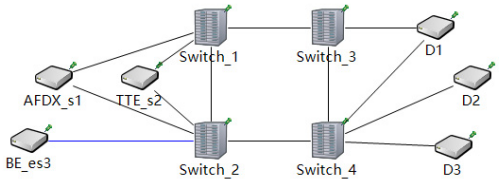


Figure 8. Extend Network Topology

The network configuration consists of 6 end systems and 4 switches. AFDX_s1 only sends RC traffic, and s2 transmits 8 TT streams and 12 RC streams and 1 BE stream. Transmission of BE flows with QoS requirements is carried on the ES (BE_es3). TABLE II. describes the complete set of streams emitted by ES TTE_s2.

TABLE II. MULTIPLE TRAFFIC EMITTED BY TTE_s2

| Table Head | Multiple Traffic | | | | | | |
|---|---|---|---|---|---|---|---|
| | ***PCF_6*** | ***RC_4*** | ***RC_8*** | ***RC_9*** | ***TT_3*** | ***TT_7*** | ***BE*** |
| BAG (μs) | *12000* | *4000* | *16000* | *64000* | *4000* | *4000* | *60* |
| MFS (Bytes) | 64 | 1028 | 516 | 1416 | 523 | 64 | 1518 |

*2) Result discussion*

TABLE III. shows the worst-case End-to-End latency simulation results for the mixed flows emitted by the TTE_s2 allocation.

TABLE III. WORST-CASE END-TO-END DELAY OF MULTIPLE TRAFFIC ON TTE_s2

| Scheduling | Worst-Case End-to-End Delay(μs) | | |
|---|---|---|---|
| | ***TT (PCF)*** | ***RC (VL)*** | ***BE (Video)*** |
| FIFO | 530.78 | 1627.34 | 1628.81 |
| SPQ | 397.66 | 961.97 | 1794.26 |
| TABLE | 329.46 | 358.63 | 430.22 |

According to the standard of ARINC664p7, the worst-case end-to-end delay of VL is higher than that of static priority when FIFO policy is applied at ES level. SPQ allows the use of two priorities to reduce the limitation of VL end-to-end

delay. An offset is introduced between the VLs of the source ES, allowing spreading them out to the switch level. Time-reserved table scheduling greatly reduces latency compared to a table-less static priority scheduling strategy. Typically for an entire network configuration, table scheduling solves the SN problem in RM by reducing transmission delay and jitter. At the same time, it also prevents collisions of RC frames in the first switch. This difference that can be more pronounced on more complex network. The BE stream conforms to the specifications described in Avionics Uncompressed Video Streaming, making better use of the remaining idle bandwidth.

## V. CONCLUSION

In this paper, we study the AFDX-compliant TTEthernet protocol, a deterministic, synchronous, and congestion-free network protocol based on Ethernet technology. Realized the Simulation method of building OMNeT++ model and configuring network parameters, and compared the difference in End-to-End delay between NC and FA methods. The results show that the NC for analyzing worst-case delays is mainly used for avionics network certification, while the TA outperforms NC in most cases. However, it tends to be pessimistic when packets are small, and our simulation approach is more suitable for real-time network performance analysis and design verification.

Aiming at the SN inversion problem which will be translated into End-to-End latency in the AFDX network, the transmission delay difference can be reduced to enhance the jitter estimation. We have added the clock synchronization function to extend the AFDX, and at the same time use gigabit bandwidth to meet the QoS of different traffic. Compared with the original scheduling strategy of the avionics network (FIFO and SPQ), we use a time-reserved table scheduling strategy at the ES level, and use the simulation method to measure the delay of the three types of streams to verify the extended AFDX model. The results show that, compared with the FIFO strategy without priority, SPQ uses two priorities to reduce the End-to-End delay of VL, but it does not optimize the delay of uncompressed video streams in the network, and the table scheduling based on time reservation significantly reduces this boundary. If there is no QoS requirement for video streams, the impact of extending AFDX on the End-to-End delay of VL is limited. In future work, the network allows adding special traffic while switches require more complex scheduling strategies.

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