Simulation and Experiment of AFDX Network Based on OMNeT++

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***Abstract*—With the rapid development of aviation technology, the avionics full duplex switched Ethernet (AFDX) has replaced the traditional avionics transmission bus standards, becoming a new generation of airborne equipment network, which is a major upgrade of civil aircraft integrated avionics system. Because it is difficult to test the real-time and certainty of AFDX network online, it is necessary to study the method of network simulation. This paper establishes the simulation models of AFDX end system, switch and virtual link based on the rate-constrained traffic of TTEthernet in OMNeT++ simulation platform. On the basis of analyzing the functional requirements of different parts and combining with the OMNeT++ platform, the evaluation method of AFDX network simulation is studied emphatically.The influence factors of end-to-end delay of AFDX network are determined by multi-group simulation experiments and on-board function tests. The accuracy of simulation model and the correctness of ARINC664 engineering data analysis based on interface control document (ICD) are verified.**

Keywords—AFDX;TTEthernet, simulation model, end-to-end delay , OMNeT++, airnc664

I. INTRODUCTION

The aviation bus mainly includes MIL-ATD-1553B bus, ARINC429 bus, ARINC629 bus, ARINC 825 bus and ARINC664 bus. MIL-ATD-1553B is the first full-function digital bus for aviation systems and is now used in some military and small aircraft. ARINC429 is the most widely used in aviation bus at present, which has the advantages of simple structure, stable signal transmission and anti-interference number[1]. ARINC664 is a new generation of aviation bus developed on the basis of MIL-ATD-1553B bus and ARINC429 bus, which has the advantages of high bandwidth, low delay and high reliability, and has been widely used in large aircraft such as airbus A380 and boeing 787.

ARINC 664 specification defines an ethernet data network installed on an aircraft, which is developed to Part 1~Part 8. Part 7 defines the avionics full duplex switched ethernet (AFDX) network. Based on the IEEE802.3, AFDX network improves the bus bandwidth, real-time and certainty according to the requirements of avionics [2]. In AFDX networks, end-to-end delay represents the time required for packets to be sent from the sender to the receiver, and is one of the important parameters to evaluate network performance.For any virtual link(VL), end-to-end delay consists of transmission delay, switch delay and buffer delay[3]. The transmission delay describes the time required for the packet to be transmitted on the VL. The switch delay describes the time the packet passes through the switch. And the buffer delay describes the delay of buffers in switches and end systems.

There are three ways to analyze network performance: mathematical modeling analysis, field experiments and network simulation. In general, field experiments not only cost a great deal of manpower and material resources, but also have security risks and are rarely used. In contrast, using network simulation to study the performance of the network can not only reflect the characteristics of the network more comprehensively, but also get more performance parameters. Xin Liu et al. established the network layer model, end system model and process layer model of AFDX system on the OPNET platform[4]. Though the conclusion that AFDX network is a deterministic network is verified by experiments, there is a lack of theoretical analysis in the course of experiments. Song Dong et al. have established a complete AFDX network simulation model using UML diagram[5], but the UML diagram mainly shows the workflow of the AFDX network, but it can not reflect the advantages of the composition and structure of the network.Ding Lina et al. built AFDX network model based on queue theory[6]. The advantage of this method is to greatly restore the way AFDX internal packet storage and scheduling, but if all parts of the network are based on different queue models, not only need to try a lot of models, but also bring trouble to the simulation implementation. Nejla REJEB et al. built AFDX network model based on Time-Triggered-Ethernet(TTEthernet) network[7]. TTEthernet network belongs to deterministic network and provides three types of traffic:time-triggered(TT), rate-constrained(RC), and best effort(BE). Using RC traffic in the network to build a AFDX network model not only simplifies the modeling process, but also brings theoretical support to verify the experimental results. This paper will analyze and verify the real-time and deterministic performance of the AFDX network based on the TTEthernet network model established by Nejla REJEB et al. through simulation and offline analysis of VLs and other experiments.

II. AFDX NETWORK SYSTEM INTRODUCTION

The main components of AFDX network include: end system, switch and VL, as shown in Fig.1. The data frame is transmitted to the switch network through the source end system, and then sent to the destination end system by the switch network, which realizes the data exchange between multiple aviation subsystems[8].

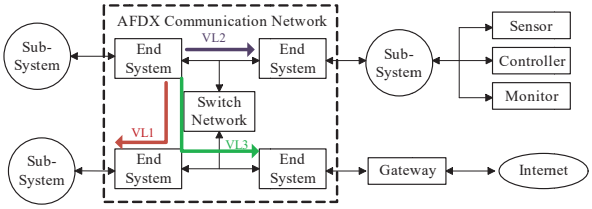

Fig.1. The main components of AFDX network.

A. End System

End system is the interface between aviation subsystem and AFDX interconnection module, the main function is flow shaping, limiting the emergence of burst flow. ARINC664 P7 specified end system communication protocol structure is shown in Fig.2. The design of the end system correspond to the physical layer, the data link layer, the network layer and the transport layer of the OSI reference model respectively.

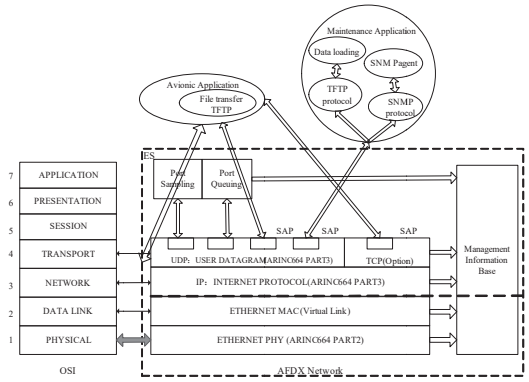

Fig.2. End system protocol structure.

- MAC layer implements VL management and redundancy management (RM) functions. VL management mechanism is responsible for dividing the physical links corresponding to each MAC into multiple independent logical virtual links. RM implements the redundancy processing function of MAC layer data frames.
- IP protocol layer provides the connectionless packet transmission mechanism.This layer mainly realizes the data encapsulation and the slice function, and uses the integrity detection method to guarantee the data integrity. IP package is responsible for adding IP header and tail to the data to form the standard IP packet. Fragmentation function realizes the functions of data partition and data reorganization, so that IP packets with the length greater than 1518 bytes can also be transmitted.
- UDP protocol layer provides the connectionless packet transmission to realize the user datagram protocol. Sampling, queue, and service access point(SAP) protocol ports are provided for users. SAP port is used to AFDX communication between system components and non- AFDX systems.

B. Switch

AFDX switch provides switching path for each end system on the AFDX network to realize data frame forwarding function. Each switch can connect up to 24 end systems, while the switch can cascade to achieve the purpose of AFDX network expansion. The function of the switch is mainly divided into five parts, as shown in figure 3.

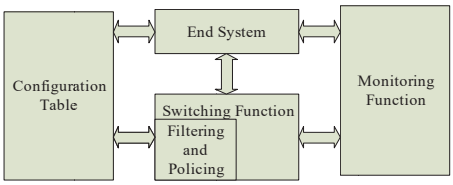

Fig.3. Main functional blocks of AFDX switch.

- Configuration Tables: Completing the configuration of related modules according to the configuration table designed by the AFDX network integrator.
- End System: Following AFDX specification. The only difference is that the end system module of the AFDX switch removes the redundant output function of the frame.
- Switching Function: Realizing the forwarding of frames on AFDX network.
- Filtering & Policing Function: Detecting and filterring the AFDX data frames through the switch, reducing the transmission of invalid network frames and ensuring the network fault control function.
- Monitoring Function: Monitoring the working status of the switch on the network.

C. Virtual Link

The interchange of data frames between end systems in AFDX network is carried out through VLs. VLs can disperse bandwidth resources more effectively and reduce communication conflicts. A VL defines a logically unidirectional connection from a single source end system to multiple destination end systems[9]. Fig.4 depicts three isolated VLs built on a physical communication link.

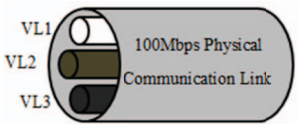

Fig.4. Three isolated VLs built on a physicalcommunication link.

There is a unique ID number for each VL in the AFDX network. AFDX network Ethernet addresses consist of six bytes, where the low 16 bits binary represents the VLID. Because the number of hosts on the plane is limited, and the 16 bits binary is enough to represent so much, the high 32 bits can be filled with 0, as shown in Fig.5. A switch transmits data frames with the same VLID to a preset terminal system.

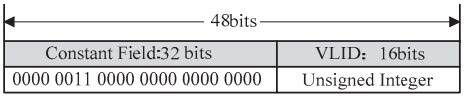

Fig.5. The format of AFDX network destination address.

III. MODELING

OMNeT++ is an object-oriented discrete-time network simulator, which can not only realize the simulation of wired wireless network, but also accurately analyze the performance of complex network. At present, there are many software for network simulation, such as NS3,OPNET and so on. TABLE I gives a simple comparison of these simulation softwares[10].

TABLE I. COMPARISON OF NETWORK SIMULATION PLATFORM

simulators / *parameters*	***OPNET***	***NS3***	***OMNeT++***
Language	C/C++	C++/python	C++/ANDL
License	commercial	Open Source	Open Source
Available Module	Wired, Wireless, Adhoc and WSN.	Wired, Wireless, Adhoc and Wireless Sensor Network (-)Ethernet not available	Wired, Wireless, Adhoc and Wireless Sensor Network (+)Ethernet/TTEthernet available
Extensibility	Very Good	Good	Excellent
Complexity	Complicated	Very Complicated	Simple

The comparison of table I shows that the OMNeT++ platform is not only simple but also well supporting the TTEthernet. Therefore, it is a good choice to use the TTEthernet as the model of the AFDX network for simulation based on OMNET++ software.

A. TTEthernet Model

TTEthernet fully conforms to the standard Ethernet and transparently integrates real-time traffic and standard Ethernet traffic, becoming the most promising real-time network technology[11]. TTEthernet provides three types of traffic: time-triggered(TT) traffic, rate-constrained (RC) traffic and best-effort (BE) traffic.

- TT traffic represents the traffic transmitted according to the time-triggered communication paradigm. TT traffic transmission usually requires time-triggered transmitter system to keep in synchronization[12];
- RC traffic represents the traffic transmitted according to the rate-constrained communication paradigm. Unlike TT traffic, RC traffic does not depend on protocol control frames and is a communication paradigm implemented according to ARINC664 P7. End systems will reshape each RC traffic to ensure minimum time intervals between adjacent data frames. Each switch in the network implements the traffic check function, which can check whether the end system does produce a good sequence of data frames. Those data frames that violate the bandwidth allocation interval (BAG) are discarded by the switch[13].
- BE means traffic transmitted according to the best possible communication paradigm.

B. Clock Model

The basic unit of the clock in the TTEthernet is "tick". The time interval between two ticks is configurable.The clock drift will cause the clock accuracy to be biased. Clock calculations such as formula(1), which is an effective and sufficiently accurate simplification of the clock model.

$$t' = t + \delta * (\Delta t_{Tick} + \Delta t_{Drift}) \quad (1)$$

Where t' is the time of the next event, t is the current simulation time , δ represents the number of planned ticks for a given event , Δt_{Tick} is the duration of a ticks, and Δt_{Drift} is the average drift.

C. End System Model

The end system of AFDX network contains a scheduling module, a synchronization module, a message classification module and a buffer for some cache data frames.

While the structure of the TTEthernet data frame is consistent with that of the AFDX data frame, TTEthernet refined the destination address of the data frame. The 48-bits destination address is divided into two parts: critical traffic marker (CT-Marker) and critical traffic ID (CT-ID), as shown in Figure 7. CT-Marker is used to detect real-time traffic. CT-ID is unique for each data frame, so the VLID of the AFDX network is equivalent with the TTEthernet CT-ID.

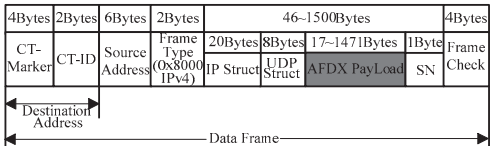

Fig.6. Data frame structure.

Each AFDX end system contains a separate configuration file with the suffix ".ini", which will eventually be included in the entire project's configuration file. The MAC address of the end system, VLID ,the size of data frame, the target port, the time interval generated by the packet and the BAG are all specified in the configuration file.

D. Switch Model

For critical traffic, special consistency checks can be configured in the CTC table of the switch. The main purpose of consistency checking is to confirm whether the data frame has reached the correct port at the correct time and to prevent the system from being corrupted by data frames that do not comply with the time limit and defective data frames. The primary check for RC traffic is the BAG. The switch model of AFDX network also retains only RC traffic.Each switch also has a configuration file with the suffix ".ini". Receiving port, transfer port and BAG just need to be configured.

IV. Analysis of Simulation and Experimental Results

A. Topology of AFDX Network

The AFDX network used in this group simulation is composed of six end systems (s1,s2,s3,D1,D2 and D3) and two switches (switch1 and switch2) as star topology, as shown in Fig.7.

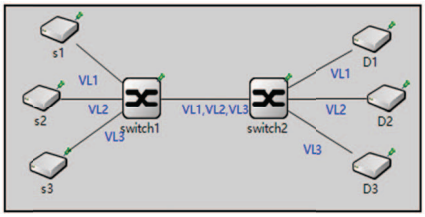

Fig.7. AFDX two-stage switch network topology.

S1,s2 and s3 are source end systems and D1,D2 and D3 are destination end systems. These six end systems form a network with 3 VLs. Where the BAG of VL1 is 4ms, the BAG of VL2 is 32ms and the BAG of VL3 is 128ms. The data frame size for all VLs is 1000 bytes, and all buffers are set to 1024 bytes.

On the output port of switch1, VL1 is always ahead of the VL2 and VL2 always is ahead of the VL3. This setting is also understandable. Since the minimum BAG of the VL1 leads to the maximum network load, the data on the VL1 should be given priority to avoid data accumulation.

B. End-to-end Delay Analysis

The end-to-end delay of VL1,VL2 and VL3 are shown in Fig.8. The simulation time is 50s, the delay of a single switch is 16μs.

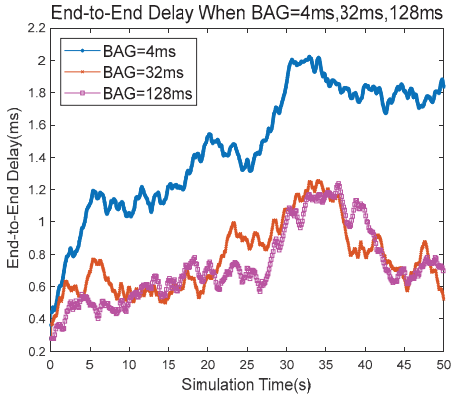

Fig.8. The End-to-End delay of VL1,VL2 and VL3 in AFDX network.

Through graphic analysis, the following conclusions can be drawn:

- The end-to-end delay of the AFDX network is in the range of 0.25~2.1 ms. The end-to-end delay meets the requirements of the ARINC664 protocol for AFDX network delay certainty, and the delay value basically meets the requirements of avionics.
- Different virtual links have different delay characteristics. The total rule is that the delay of VL with smaller BAG is larger. VL1 need more time to process a large number of data frames because VL1 have the smallest BAG. For this reason, the delay of VL1 shown in figure 10 is the largest of the three VLs. Meanwhile, it can be found from the experimental curve that the delay of the VL3 will be greater than the delay of the VL2 in some time, which may be caused by the blocking of the packet in the switch or the unclear priority of the packet.

C. Fixed and Variable Delay Analysis

End-to-end delay can be expressed in the form of formula (3)[14]:

$$D(F_v,P_x) = LD(F_v,P_x) + SD(F_v,P_x) + WD(F_v,P_x) \quad (2)$$

The meaning of this formula is that the end-to-end delay of a data frame F_v on a virtual link P_x is equal to the sum of transmission delay, switch delay and buffer delay. Where $LD(F_v,P_x)$ is the transmission delay of a virtual link, which can be expressed as:

$$LD(F_v,P_x) = nbl(P_x)\times(t_{byte}\times s(F_v)) \quad (3)$$

t_{byte} is the time required to transfer a byte. If the AFDX bandwidth is 100 Mbit/s, t_{byte} =0.08μs. $s(F_v)$is the length of F_v. $nbl(P_x)$ is the number of virtual links across the system.

$WD(F_v,P_x)$ is the delay in the output buffer of the end system and switch, which can be further expressed as:

$$WD(F_v,P_x) = WD(F_v,P_x,e_v) + \sum_{sk\in\varphi_{P_x}} WD(F_v,P_x,sk)) \quad (4)$$

e_v represents the source end system , φ_{P_x} represents the set of switches through a virtual link, $WD(F_v,P_x,e_v)$ represents the delay in output buffering of the source end system, $\sum_{sk\in\varphi_{P_x}} WD(F_v,P_x,sk)$) represents the sum of output buffering delays of the switch.

$SD(F_v,P_x)$ is the time delay required for data frames to pass through the switch and can be further expressed as:

$$SD(F_v,P_x) = nbs(P_x) \times t_d \quad (5)$$

$nbs(P_x)$ means the number of switches and t_d means the delay of a single switch.

From formula (3), it can be seen that the end-to-end delay expression of AFDX network can be divided into two parts. The first part is composed of $LD(F_v,P_x)$ and $SD(F_v,P_x)$, which depends only on the length of the data frame F_v , virtual link P_x and BAG, so this part is also called a fixed part. The second part consists of $WD(F_v,P_x)$, which depends on the dynamic characteristics of the network, so the second part is called a variable part. The fixed part can be obtained by calculation. In order to analyze the experimental law of fixed

part and variable part, a set of experiments is redesigned here to study. The experimental network topology is shown in Fig.9:

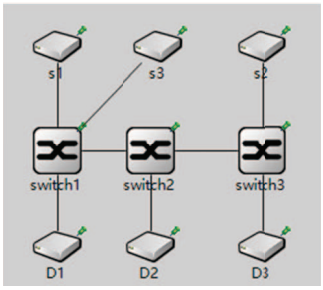

Fig.9. Fixed delay and variable delay analysis.

The BAG for these three virtual links are all 4ms, and the latency of a single switch is 16μs. Fixed and variable delays are shown in TABLE II.

TABLE II. FIXED DELAY AND VARIABLE DELAY ANALYSIS

VL no.	*Frame payload (bytes)*	*The Mean of End-to-end Delay(μs)*	*Fixed delay*		*Variable delay*
			LD(F_v,P_x)(μs)	*SD(F_v,P_x)(μs)*	*WD(F_v,P_x) (μs)*
VL1	100	864.264	8	16	837.597
VL2	1500	1682.455	120	32	1526.952
VL3	400	1694.351	32	48	1609.498

From the experimental data in the above table, it can be found that:

- The end-to-end delay of the VL1 is minimal because both the transmission path of the VL1 and the length of the data frame are minimal;
- The end-to-end delay of VL3 is the largest because VL3 has the longest transmission path;
- The VL2's LD(F_v,P_x) is the largest because the length of data frame on VL2 is the largest.
- By comparing fixed delay with variable delay, it can be found that fixed delay does not occupy the main part in end-to-end delay.

D. Switch Delay Analysis

TABLE III shows the average end-to-end delay and the number of data frames reaching the destionation end systems when the switch delay t_d is equal to 8μs and 16μs. By comparing the datas in table, it can be found that using faster switches can reduce end-to-end delay, because as the switch delay decreases, the fixed delay also decreases in response, so the end-to-end delay decreases.

TABLE III. AVERAGE END-TO-END DELAY WITH DIFFERENT T_D

Switch Delay / *VL Delay(Mean)*	t_d=8μs	t_d=16μs
VL1 Delay(Mean)/ μs	1537.959	1553.959
VL2 Delay(Mean)/ μs	754.866	770.866
VL3 Delay(Mean)/ μs	680.947	696.948

E. VL Engineering Analysis

By monitoring and analyzing VLs, we can understand the nature of the data and transmission protocol of the AFDX network more deeply, and can solve the problems in the network as soon as possible. PCAP is the file storage format of the mainstream packet capture software. By analyzing the datas in the PCAP files, some basic information of the packet and the network running status can be obtained[15]. The common tool of packet capture and analysis is WinPcap, this paper uses the ARINC comprehensive test software developed by the laboratory to carry on the PCAP analysis.

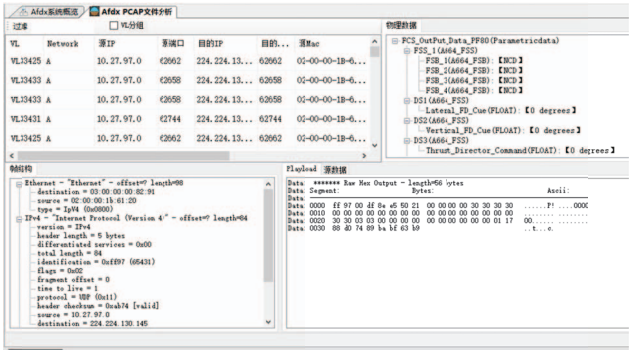

Fig.10. VL engineering analysis.

Because the real-time data is very large, and the transmission speed is very fast, so there are many technical difficulties in the real-time data semantic analysis. This analysis is based on the data packet files saved in the local, to achieve offline analysis. The VLID of this VL analyzed on the figure 12 is 33425, and the packet is sent from the source end system with IP address of 10.27.97.0 through port 62662 to the destination system with IP address of 224.224.13.145. By PCAP analysis, the frame structure and load content of the data frame transmitted on the virtual link can be viewed in detail, and the transmission process of the data frame on the virtual link coincides with the process described in the above simulation experiment.

V. CONCLUSION

ARINC664 is a new generation of bus standard and increasingly applied to aviation systems. AFDX network solves the real-time problem of Ethernet in aviation based on ARINC664 Part7 specification.The simulation model of AFDX end system, switch and virtual link is established based on TTEthernet. The AFDX network is simulated using these models in OMNeT++ environment and the parameters such as switch delay and end-to-end delay are studied to verify the AFDX performance. The simulation results show that the model based on TTEthernet can better reflect the behavior of the AFDX system and provide a reliable reference for further research on AFDX network. Finally, through the PCAP analysis of the AFDX network datas, the description of the AFDX network data structure and data forwarding in the simulation process is verified.

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