DEEC
DEPARTAMENTO DE ENGENHARIA ELETROTÉCNICA E DE COMPUTADORES
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# Projecto de Sistemas Digitais
# Digital System Design

MEEC / MEIC / MEAer – 2015/16 1st Semester

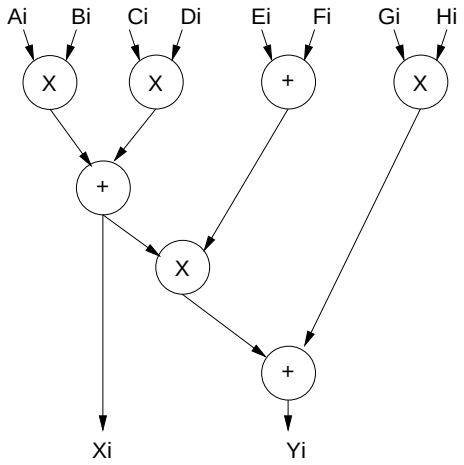
Exam: 2nd call | January 28, 2016 | Duration: 2.5 hours

Individually written exam without consultation

Answer the questions on proper exam sheets identified with name and number.
Justify all your answers and present all the necessary calculations.

## Group I

[7.0] 1. Consider the implementation of an algorithm that computes $Xi$ and $Yi$ described using the following data flow graph:




| Operators 16 bits | | area | $t_p$ (ns) |
|---|---|---|---|
| add, sub, ALU(add, sub) | | 20 | 15 |
| Multiplier (simple) | | 120 | 26 |
| Logic operators | | 10 | 9 |
| Multiplexer 2-to-1 (16-bits) | | 16 | 4 |
| RAM | $t_{setup}$ = 5ns | 800 | 8 |
| Register 16 bits | $t_{setup}$ = 2ns | 50 | 3 |

Consider that all input values are 16-bit integers in 2's complement representation, stored in independent synchronous memories and on each computation new set of input values $(A_i, B_i, \cdots, H_i)$ are read from the memories. Consider also that all buses and operators are 16 bits with the characteristics listed above. All registers are synchronous edge trigger positive of a single clock signal. The outputs values, $X_i$ and $Y_i$ should be stored in a dedicated memory. Get all schedulings for the fastest circuit.

(1.0) (a) Determine, from the DFG, the expression for the computation of $X_i$ and $Y_i$.

(1.5) (b) Considering there is no resource restrictions, get and draw an ASAP scheduling. Which is the minimum number of operators of each type that are required to implement the circuit?

(3.0) (c) Draw a data-path of circuit for the ASAP scheduling of the previous question. Make explicit your biding and register usage. Write the expression to compute the minimum clock period ($T_{min}$) and calculate its value. Identify the outputs, $X_i$ and $Y_i$, that will go to the data-bus of the output memories, as well, all the inputs read from the memory.

(1.5) (d) Get and draw the fastest ALAP scheduling using at most 180 units of area dedicated to operators. How many operators of each type are required to implement the circuit? Considering a clock period of 30 ns, how much is latency and the throughput on each output of the circuit?

[4.5] 2. Consider that we want to implement the following algorithm and there are no hardware restrictions. Assume the same conditions of the previous question regarding the input data size and operators. All values are read from independent memories and the result is store in another memory,

```
for (i=0; i<100; i++) {
    x1 = (A[i] * B[i])  +  (B[i] * C[i]);
    x2 = (A[i] + C[i]);
    Y[i] =  x1 + x2;
}
```

(2.0) (a) Draw a data-path of a circuit that implements the computations **as fast as possible**. Consider that all operators, buses and registers are 16 bits, with the features mentioned above.
How many registers and operators of each types are need?

(1.5) (b) Determine, justifying, which is the maximum clock frequency that can be used on the circuit, its throughput and how many clock cycles are needed to compute all the 100 of Y.

(1.0) (c) If you have access to multipliers with one pipeline level, and your circuit works at 50 MHz, could you improve the computation time of the 100 values of Y. Justify your answer.

## Group II

[1.5] 3. Consider a combinatorial circuit to compute the following formula with signed (2'complement) fix point arithmetic:

$$sol = \frac{X^2 + C}{2}$$

where the $X$ value is given in Q8.8 fix point format and the $C$ value is in Q18.14 format. The circuit should have 3 outputs: `solFull`, the computed value in full precision (i.e., without any lost of precision); `solInt`, the integer part of the solution and `solQ`, the result in Q12.12 format.

Write a complete and full sintetizable VHDL description of the circuit using only one arithmetic operation per instruction based on the following incomplete entity of the circuit (do not forget to complete entity of the circuit):

```
entity solXC is
  port(X       : in   ... ;  -- X value in Q8.8
       C       : in   ... ;  -- C value in Q18.14
       solFull : out  ... ;  -- solution, full precision
       solInt  : out  ... ;  -- integer part of solution
       solQ    : out  ... ); -- solution in Q12.12
end solXC;
```

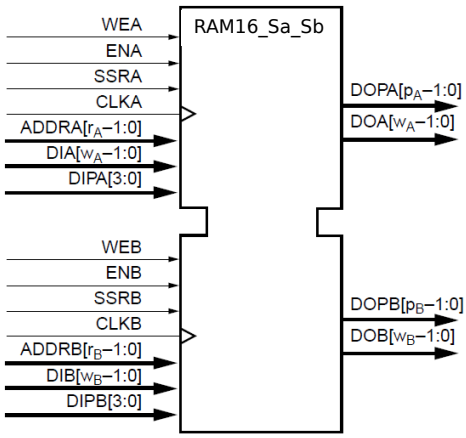
[1.5] 4. Write a complete and full sintetizable VHDL description of an 8 bit counter, `count`, that counts between 7 ($07_{hex}$) and 240 ($A0_{hex}$) inclusive. This counter should have a synchronous `start`, that initialize the counting on the value 44 ($2C_{hex}$), and an `enable` signal that control the counting operation. An example of a counting sequence after a start is: 44, 45,..., 239, 240,7, 8,..., 239, 240, 7, 8,....
Note that all synchronous operations are relative to the rising edge of the clock. Use the following entity for the component architecture you will describe:

```
entity counterInc is
  port (clk, start, enable : in  std_logic;
        count              : out std_logic_vector(7 downto 0));
end counterInc;
```

## Group III

[1.5] 5. Consider the blocks of dual-port RAM in Spartan-3 FPGA that can be configured in the following ways:

| | | Port A | | | | | |
|---|---|---|---|---|---|---|---|
| | | 16Kx1 | 8Kx2 | 4Kx4 | 2Kx9 | 1Kx18 | 512x36 |
| Port B | 16Kx1 | _S1_S1 | | | | | |
| | 8Kx2 | _S1_S2 | _S2_S2 | | | | |
| | 4Kx4 | _S1_S4 | _S2_S4 | _S4_S4 | | | |
| | 2Kx9 | _S1_S9 | _S2_S9 | _S4_S9 | _S9_S9 | | |
| | 1Kx18 | _S1_S18 | _S2_S18 | _S4_S18 | _S9_S18 | _S18_S18 | |
| | 512x36 | _S1_S36 | _S2_S36 | _S4_S36 | _S9_S36 | _S18_S36 | _S36_S36 |



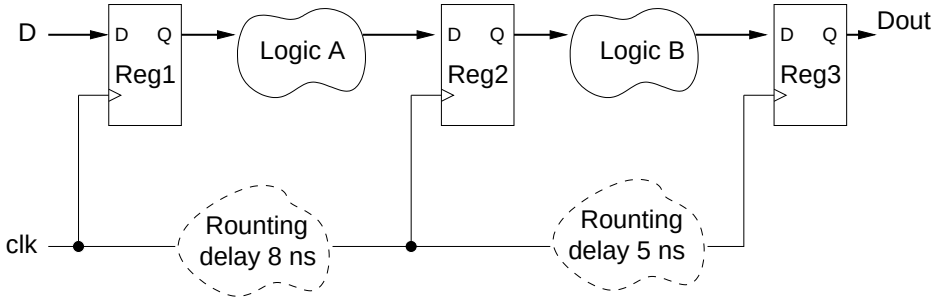

If you use an memory block configured as RAMB16_S1_S36 to implement a CAM (Content Addressable Memory) how many words can be stored in this CAM? Which is the size of each word? Justify your answer by drawing an outline of the necessary interconnections on the reading port.

[1.0] 6. Consider that you want to implement the following logic function:

$$X = \overline{A}BCD + \overline{E}FG\overline{H} + \overline{I}\,\overline{J}KL + M\overline{N}O$$

Identify the minimum number of LUTs and slices needed to implement this function on a Spartan-3 FPGA. Justify you answer by drawing a schematic with the resources used on each slice, how they are interconnected, and which are the inputs signals and the configuration of each used LUT.

[3.0] 7. Consider the following schematic:




in which the circuit elements have the following temporal characteristics:

| | | | |
|---|---|---|---|
| Register: | $t_{setup} = 2ns$ | $t_{hold} = 1ns$ | $t_p = 3ns$ |
| Logic A: | $t_{delayA_{MIN}} = 3ns$ | $t_{delayA_{MAX}} = 12ns$ | |
| Logic B: | $t_{delayB_{MIN}} = 5ns$ | $t_{delayB_{MAX}} = 23ns$ | |

(1.0) (a) Assuming zero delays on the routing of the clock network, determine the minimum clock period for which this circuit can work properly.

(1.0) (b) Consider now the routing delays on the clock network as shown in the figure. Briefly explain if this circuit have clock skew problems. If so, identify which registers are problematic (store wrong results) and why?

(1.0) (c) Explain which are the techniques available to the designer to minimize the clock skew problems on a Xilinx Spartan-3 FPGA.