Projecto de Sistemas Digitais
Digital Systems Design
MEEC/MEAer, 2018/19, 1st Exam

Table 1: Timing characteristics and resource utilization of logic-arithmetic components				
	Area	t_P	t_{SETUP}	t_{HOLD}
16-bit Register	10	2 ns	1 ns	1 ns
BRAM	100	2 ns	1 ns	1 ns
16-bit Adder / Subtractor	16	5 ns		
16-bit Multiplier (simple)	120	14 ns		
16-bit Multiplier (2-stage pipeline: 1 internal register-level)	130	8 ns		
16-bit Divider	500	85 ns		
MUX 2:1 (16-bit data words)	16	3 ns		
MUX 4:1 (16-bit data words)	32	4 ns		
MUX 8:1 (16-bit data words)	64	5 ns		
16-bit logic operators	16	3 ns		

Note: all answers must be properly justified, without which they will not be classified.

1. Consider the following algorithm for quadratic interpolation $P_2(x)$, given 3 points (x_0, y_0), (x_1, y_1), (x_2, y_2) and the 3 functions $L_0(x)$, $L_1(x)$, $L_2(x)$, defined below:

$$L_0(x) = \frac{(x - x_1)(x - x_2)}{(x_0 - x_1)(x_0 - x_2)} \;;\; L_1(x) = \frac{(x - x_0)(x - x_2)}{(x_1 - x_0)(x_1 - x_2)} \;;\; L_2(x) = \frac{(x - x_0)(x - x_1)}{(x_2 - x_0)(x_2 - x_1)}$$

$$P_2(x) = (y_0 L_0(x) + y_1 L_1(x)) + y_2 L_2(x)$$

Consider that the interpolating points (x_i,y_i) are organized on a fixed-sized grid, such that

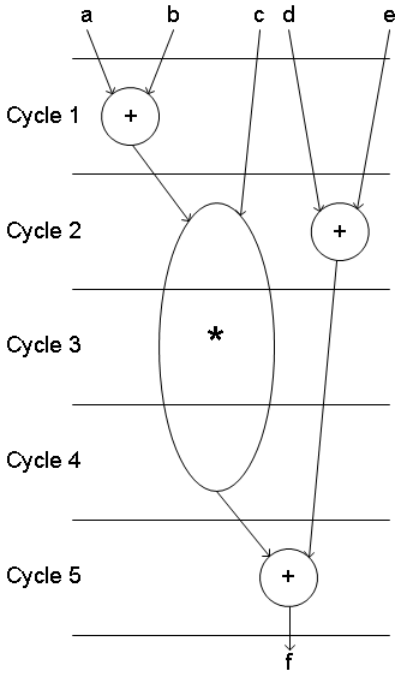
$$x_1 = x_0 + 32 \;;\; x_2 = x_1 + 32$$

a) **[1 val]** Draw the data flow graph corresponding to one quadratic interpolation.

b) **[3 val]** Define a priority list using the critical path as metric.

Consider that the inputs are stored in independent registers, that the arithmetic operators available are 1 multiplier (simple) and 2 adder/subtractors, that one multiplication requires one clock cycle and that 1 addition/subtraction can be performed in half clock cycle.
Obtain a list scheduling using the priority list defined.

2. Consider the schedule defined in the figure, at the right, for a circuit whose datapath is to be implemented with one adder and one multiplier (simple).
   All input values are 16-bit integers in 2's complement representation.
   All operators, buses and datapath registers are 16-bit wide, with the timing/area characteristics shown on the 1st page. All circuit registers must be positive edge-triggered, fully synchronous and be synchronized with a unique global clock.



a) **[3.5 val]** Design the circuit datapath in order to achieve the best possible performance (given the constraints indicated).
   Indicate the number of registers and multiplexers required.
   Draw the block diagram of your datapath.
   Estimate the area occupied, the minimum clock period, and the latency for your design.
   Justify all the bindings and sharing of resources.

b) **[2 val]** Draw the state diagram of the control unit of the circuit for the datapath designed in (a).
   Define an output-based state assignement, in order to eliminate the output logic of the finite state machine. Justify.

3. Consider that you want to design a circuit, on a Xilinx Artix-7 device, to calculate the output sequence of a symmetric FIR filter, **<u>as fast as possible</u>**:

$$y_k = \sum_{i=0}^{(N-1)/2} h_i \cdot (x_i + x_{N-i})$$

Consider that N=31, that $\mathbf{h_i}$ are 16-bit fixed-point numbers in Q2.14 format, and that $\mathbf{x_i}$ are 8-bit fixed-point numbers in Q5.3 format.

The $\mathbf{h_i}$ elements are stored in one independent 18 Kb block RAM, and the $\mathbf{x_i}$ elements are stored in one other independent 18 Kb block RAM. Both BRAMs are configured in ***simple dual-port mode***.

All operators, buses and registers must be sized in order to avoid the existence of *overflows*.

All registers must be positive edge-triggered and be synchronized with a unique global clock. Select the most adequate logic-arithmetic components listed on table 1, and use the timing characteristics indicated in the table to estimate the performance of your circuit.

a) **[2 val]** Define the representation format required for the elements **y**.
Define the organization in memory (elements $\mathbf{h_i}$ and $\mathbf{x_i}$) and the configuration of the RAMB18E1 blocks in order to maximize the throughput of your circuit.
Justify.

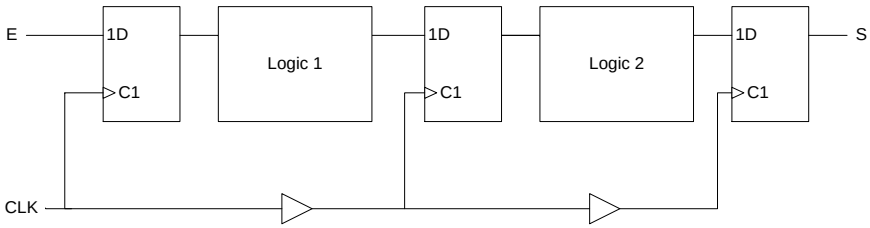
b) **[2 val]** Design the circuit datapath in order to achieve the target performance.
Draw the block diagram of the data unit.
Specify the dimensions of all operands, buses, and registers.
Indicate the throughput and the latency of the circuit you propose.
Justify.

c) **[2 val]** Specify the VHDL architecture of the arithmetic component to perform the operation PI = HI × (XI0 + XI1). Complete the specification below of its input / output ports. Dimension all operators and buses in order to preserve maximum accuracy in the calculations and avoid overflows.

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.NUMERIC_STD.ALL;

entity addm is
  Port ( hi : in  std_logic_vector ( ??? );
         xi0, xi1 : in  std_logic_vector ( ??? );
         pi : out  std_logic_vector ( ??? ));
end addm;

architecture behavioral of addm is

???

begin

???

end behavioral;
```

d) **[1 val]** Consider now that the component in c) will be implemented using only DSP48E1 blocks.
How many DSP48E1 blocks will be required? Justify.

4. Consider the following circuit.



The circuit components have the following timing characteristics:

t_{PFF}=4ns; t_{SETUP}=2ns; t_{HOLD}=1ns;

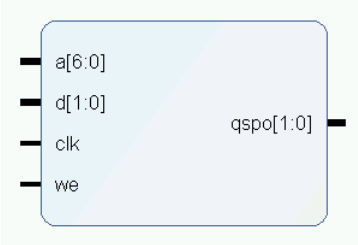
$t_{PLOG1max}$=7ns; $t_{PLOG1min}$=2ns; $t_{PLOG2max}$=11ns; $t_{PLOG2min}$=5ns;

a) **[1 val]** Estimate the minimum clock period for the circuit to work correctly, considering the *buffers* in the clock network "ideal" ($t_{Pbuffers}$=0ns). Justify.

b) **[0.5 val]** What will be the minimum clock period required for the circuit to work correctly if there exists clock skew ($t_{Pbuffers}$=3ns)? Justify.

c) **[0.5 val]** Estimate the WHS (Worst Hold Slack) of the circuit, considering the clock skew ($t_{Pbuffers}$=3ns). Justify.

5. Consider a 112×2 single port RAM implemented with the Distributed Memory Generator.



[1.5 val] Explain how this distributed memory is implemented in Artix-7 devices, indicate which physical resources it is mapped to, and estimate how many resources are required.