DEEC
DEPARTAMENTO DE ENGENHARIA ELETROTÉCNICA E DE COMPUTADORES
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Projecto de Sistemas Digitais
Digital System Design

MEEC / MEIC / MEAer – 2015/16 1st Semester

Exam: 1st call | January 11, 2016 | Duration: 2.5 hours

Individually written exam without consultation

Answer the questions on proper exam sheets identified with name and number.
Justify all your answers and present all the necessary calculations.

Group I

[7.0] 1. It is intended to implement the algorithm defined on the following pseudo-code to compute a series of values for Z.

```
repeat {
   W = (A_i * B_i) + (C_i * D_i) ;
   X = (E_i + F_i) + G_i ;
   Y = (W * E_i) * X ;
   Z_i = Y/2
} unitl (X < 314);
```

Operators 16 bits		area	t_p (ns)
add, sub, ALU(add, sub)		20	16
Multiplier (simple)		120	25
Logic operators		10	8
Multiplexer 2-to-1 (16-bits)		16	4
RAM	t_{setup} = 5ns	800	7
Register 16 bits	t_{setup} = 2ns	50	3

Consider that all input values are 16-bit integers in 2's complement representation, stored in independent synchronous memories and on each loop iteration a new set of input values $(A_i, B_i, \cdots, F_i)$ are read from the memories. Consider also that all buses and operators are 16 bits with the characteristics listed above. All registers are synchronous edge trigger positive of a single clock signal. The output value should be stored in a dedicated memory. Get all schedulings for the fastest circuit.

(1.0) (a) Draw the data flow graph of the computation for the given algorithm.

(1.5) (b) Considering a clock period of 18ns, get and draw an ASAP scheduling. Which is the minimum number of operators of each type that are required to implement the circuit? How much is the latency of the circuit?

(1.5) (c) Considering that each operation takes one clock cycle of 30ns. Get and draw the fastest ALAP scheduling using at most 2 multipliers, 1 ALU and 1 logic operator. How much is latency and the throughput of the circuit?

(3.0) (d) Draw a data-path of circuit for the ALAP scheduling of the previous question. Make explicit your biding and register usage. Write the expression to compute the minimum clock period (T_{min}) and calculate its value. Identify the output Z_i, that will go to the data-bus of the output memory, and the stop condition signal.

[4.5] 2. Consider that you have to design a circuit to compute the value of *polyAccum* as:

$$polyAccum = \sum_{i=1}^{500} (A * X_i^2 + B * X_i + Y_i)$$

(3.0) (a) Draw a data-path of a circuit that implements the computation **as fast as possible** with minimum hardware. How many registers and operators of each types are need?
Consider there are no hardware restrictions and all operators, buses, and registers are 16 bits with the features mentioned in the previous question. All used registers must be edge trigger positive with a single clock. All X_i, Y_i values are read from a memory, the constants A, B are stored in registers and the results will be stored in another memory.

(1.5) (b) Determine, justifying, which is the maximum clock frequency that can be used on the circuit, its throughput (regarding a polynomial computation) and how many clock cycles are needed to compute all the 500 accumalted values on *polyAccum*.

Group II

[1.5] 3. Consider a combinatorial circuit to compute the determinant of a 2×2 matrix using the following formula with signed fix point arithmetic:

$$det\left(\begin{bmatrix} A & B \\ C & D \end{bmatrix}\right) \quad = \quad A \times D \; - \; B \times C$$

where the elements of the main diagonal (A and D) are given in Q9.3 fix point format, the B element is in Q8.6 format and the C is in Q8.4 format. The circuit should have 3 outputs: `detFull`, the determinant of the matrix with full precision (i.e., without any lost of precision); and `detInt` and `detFrac` that should output just the integer and factional part of the determinant, respectively.

Write a complete and full sintetizable VHDL description of the circuit using only one arithmetic operation per instruction based on the following incomplete entity of the circuit (do not forget to complete entity of the circuit):

```
entity detMat2 is
  port(A    : in  ...; -- A element in Q9.3
       B    : in  ...; -- B element in Q8.6
       C    : in  ...; -- C element in Q8.4
       D    : in  ...; -- D element in Q9.3
       detFull : out ...;  -- matrix determninat, full precision
       detInt  : out ...;  -- integer part of determninat
       detFrac : out ...); -- fractional part of determninat
end detMat2;
```

[1.5] 4. Write a complete and full sintetizable VHDL description of a 16 bit cnt with an asynchronous `clear` and an `enable` signal that control the counting operation. There is also input signal, `add3`, that determine if the counter is incremented by 3, when this signal is `'1'`, or incremented by 1, otherwise.
Note that all synchronous operations are relative to the rising edge of the clock, and your synthesized circuit should not have more the 16 one-bit register (i.e., flip-flops). Use the following entity for the component architecture you will describe:

```
entity counter13 is
  port (clk, clear, enable, add3 : in  std_logic;
        count                    : out std_logic_vector(15 downto 0));
end counter13;
```

Group III

[1.5] 5. Consider that you want to determine when the output of a 16 bit counter,`count`, reach the excat value of $1841_{dec} = 0731_{hex}$. Identify the minimum number of LUTs and slices needed to implement this comparator on a Spartan-3 FPGA. Justify you answer by drawing a schematic with the resources used on each slice, how they are interconnected, and which are the inputs signals and the configuration of each used LUT.

[1.0] 6. Consider that on a Spartan-3 FPGA a dual-port RAM16_S9_S36 is instantiated as a ROM initialized with the values identified by the following INIT parameters:

```
INIT_00 => X"3C26205E7D28D71598CD956F20FAC43A7861541583C2F3F29B7A5185FFE60313",
INIT_01 => X"99BCD9C4E4E40E7000034040CC7AC6ABED8D97B24A24DF26D3119BAFBBCABEFE",
INIT_02 => X"0000000000000000000000000000000000000000000000000000000000000000",
        .  .  .
INIT_3F => X"0000000000000000000000000000000000000000000000000000000000000000"
```

What are the values read from this memory in port A at address 2 ($DO_A[2]$) and in port B at address 1 ($DO_B[1]$)? Justify your an answer.

[1.5] 7. In the Xilinx synthesis tools for FPGAs the default encoding for finite state machines (FSMs) is One-Hot encoding. Explain how this encoding is implemented and why is this the default encoding for FPGA instead of a more compact one (e.g. Binary or Gray).

[1.5] 8. Consider the VHDL description of the `max_store` circuit, a register that only stores a new value if it is greater then the current stored value. When this circuit is synthesized the following warning is reported:

```
WARNING:PhysDesignRules:372 - Gated clock. Clock net newclk is sourced
    by a combinatorial pin. This is not good design practice.
```

Explain the reason for this warning and why this is not a good design practice. Describe how can you solve this problem in this circuit without changing its functionality (do not write VHDL code).

```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.std_logic_unsigned.all;

entity max_store is
  port (clk, rst : in  std_logic;
        D        : in  std_logic_vector(15 downto 0);
        Q        : out std_logic_vector(15 downto 0));
end max_store;

architecture problem of max_store is
  signal iQ     : std_logic_vector(15 downto 0);
  signal newclk : std_logic;
begin
  newclk <= '1' when (D > iQ) and (clk = '1') else '0';
  process (newclk, rst) is
  begin  -- process
    if newclk'event and newclk = '1' then
      if rst = '1' then
        iQ <= (others => '0');
      else
        iQ <= D;
      end if;
    end if;
  end process;
  Q <= iQ;
end architecture problem;
```