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Project 3 Experiment Report

CS 4290

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Our goal for the experiment was to find the optimum configuration for a pipeline for each trace. An optimum configuration can be considered to have the best possible IPC with the lowest resource utilization. The list of resources we have for the pipeline are Functional Units in the form of ALU, MUL, LSU, reservation stations per FU which forms the Scheduling Queue, number of physical registers, and buses in the form of fetch width. Since MUL itself is a pipelined hardware, we can assume it is a complicated and the most expensive resource in the pipeline, LSU will come next and then ALU. Reservation stations and physical registers will mostly be in a form of registers, and buses in the form of Fetch Width will be the cheapest. Considering our "expensiveness" of each of our resources, we will look for the optimum configuration for each of our traces.

Cachesim –

The best possible IPC under our restraints for cachesim_gcc is 1.839. There are 30 configurations which achieves an IPC of 1.839. All of the 30 configurations have 3_1_3 or 3_2_3 ALU, MUL, LSU units. The most expensive resource we have are the MUL functional units so we can choose units which have 3, 1, 3 Functional Units. Then of the 12 configurations that are left, we can check the physical registers and reservation stations. There are 4 configurations which have 64 pregs and 4 or 8 reservation stations per Functional Units. 2 of the configurations, 64_4_8_3_1_3 and 64_8_8_3_1_3 (P_F_S_A_M_L), have high stall cycles due to PREGs and have considerably more registers so we can eliminate them. We are left with 64_8_4_3_1_3 and 64_4_4_3_1_3. As the configuration with 64_4_4_3_1_3 is just a little more optimized, we can say that this is the optimal configuration for Cachesim.

Bfs –

The best possible IPC under our restraints for bfs_2 is 1.443. If we look for configurations that is over 1.437 which is well over our restraint of 90% of the best IPC, we have 17 configurations. All of the 17 configurations have 3_1_3 or 3_2_3 ALU, MUL, LSU units. And with the same logic as in Cachesim, we can eliminate all of the configurations with 2 MUL units which leaves us with 8 configurations. If we check the physical registers and reservation units, we can consider configurations with 64_8_8_3_1_3, 64_8_4_3_1_3 and 96_8_4_3_1_3. The configuration 64_8_8_3_1_3 has a considerable amount of stall cycles due to PREGs compared to the other two so it can be eliminated. 64_8_4_3_1_3 has 32 less registers compared to the other configuration however, the other configuration 96_8_4_3_1_3 has ~3500 less clock cycles compared to the configuration with 64 physical registers. Considering 3500 clock cycles can stack up if the trace is repeated many times, we can say that 96_8_4_3_1_3 is the optimal configuration for Bfs.

Perceptron –

The best possible IPC under our restraint for perceptron_gcc is 2.015. If we look for configs over 2.008 which again is over the 90% of the best IPC, we have 18 configurations. All of the configs have 3_1_3 or 3_2_3 ALU, MUL, LSU units and we can eliminate 9 configs which have 2 MUL units. If we check the physical registers and reservation units, we can consider configurations with 64_8_8_3_1_3, 64_8_4_3_1_3, 96_8_4_3_1_3, 64_8_2_3_1_3 and 96_8_2_3_1_3. 96_8_2_3_1_3 has the exact same simulation outputs as 64_8_2_3_1_3 so it can be eliminated as it has more registers. With the rest of the 4 configurations, 64_8_8_3_1_3 has the lowest cycle and the highest IPC, 2.015, so we can say that 64_8_8_3_1_3 is the optimal configuration for Perceptron.

Tiled –

The best possible IPC under our restraint for tiledmm is 1.48. If we look for configs over 1.477, we have 48 configurations. We can eliminate every configs which have 2 MUL units and we are left with 24 configurations. Among the 24 configurations, we have 6 configs which only have 2 ALU units. All of the 6 configurations has the second best IPC of 1.477 with the same amount of cycles. Therefore, the cheapest among the 6 configurations is 64_8_4_2_1_3. However, when we consider the configuration 64_8_2_3_1_3, the IPC is the best possible which is 1.480 and has ~4000 less cycles. It is a matter of decision to think whether 1 ALU unit is considered more expensive than a higher IPC and less cycles. However, I believe the ~4000 cycles is considerable so we can say that 64_8_2_3_1_3 is the optimal configuration.