MULTICORE CACHE COHERENCE: A UVM-Based Study of Quad-Core MESI Coherence

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Abstract

This project presents the design and verification of a quad-core L1 cache coherence system based on the snooping MESI (Modified, Exclusive, Shared, Invalid) protocol. The system ensures cache coherence in a shared-memory multicore environment while addressing key challenges such as transient states, race conditions, and arbitration fairness. Universal Verification Methodology (UVM) is employed to simulate and validate the architecture, ensuring correctness under diverse inter-core interaction scenarios. The verification process focuses on detecting coherence violations, validating bus arbitration fairness, and testing the functionality of critical components, including the L1 cache and arbiter. Simulation results confirm the system's ability to maintain coherence and fairness under varying conditions, offering a robust framework for future multicore cache designs.