National Taiwan Normal University
Department of Computer Science and Information Engineering
CSU0029, Homework 5

1 Information

1. The assignment is worth 100 points.
2. Individual work.
3. Due at 12:00 on 6/6, i.e., Tuesday noon.
4. When asked, use a scientific notation, i.e., show a value in the form $m \times 10^n$, where $1 \leq |m| < 10$ and n is an integer.
5. If any fractional part, round to the second decimal place.
6. Submit the assignment to the course website.
7. Write the assignment in English or Chinese MS Word or PDF format.

2 Contents

1. (20 points) A memory system has 1M words. Each word is an 8-bit byte. The memory is organized into blocks of 8 words each. The cache has 256K words, organized into cache lines of 8 words each. The memory cache is organized into 4-way set associative cache. Which of the following statements are true ?
   (a) 13 bits are needed for cache set address.
   (b) 4 bits are for Tag.
   (c) 21 bits are needed to address all words.
   (d) 17 bits are needed to address all blocks.
   (e) None of the above.
2. (20 points) For a typical disk without considering queuing delay, the average seek time is 5 milliseconds, and the transfer rate is 2M-bytes per second. The disk rotates at 600 RPM (Revolution Per Minute), and the controller overhead is 0.5 millisecond. Determine the average time to read a 1792-bytes sector.
3. (20 points) A virtual memory system often implements a TLB to speed up the virtual-to-physical address translation. A TLB has the following characteristics. Assume each TLB entry has a valid bit, a dirty bit, a tag, and the page number. Determine the exact total number of bits to implement this TLB.
   - It is direct-mapped.
   - It has 16 entries.
   - The page size is 4 Kbytes.
   - The virtual address space is 4 Gbytes.
   - The physical memory is 1 Gbytes.
4. (20 points) Assume that the miss rate of an instruction cache is 3% and the miss rate of the data cache is 6%. If a processor has a CPI of 4 without any memory stalls and the miss penalty is 100 cycles for all misses. Assume the frequency of all loads and stores is 30%. How much faster a processor will run with a perfect cache that never missed.

5. Consider a virtual memory system with the following characteristics:

   - Page size of 64 KB= 2^{16} bytes.
   - Page table and page directory entries of 8 bytes per entry.
   - Inverted page table entries of 16 bytes per entry.
   - 31 bit physical address, byte addressed.
   - Two-level page table structure (containing a page directory and one layer of page tables).

   (a) (10 points) What is the size (in number of address bits) of the virtual address space supported by the above virtual memory configuration?

   (b) (10 points) What is the maximum required size (in KB, MB, or GB) of an inverted page table for the above virtual memory configuration?