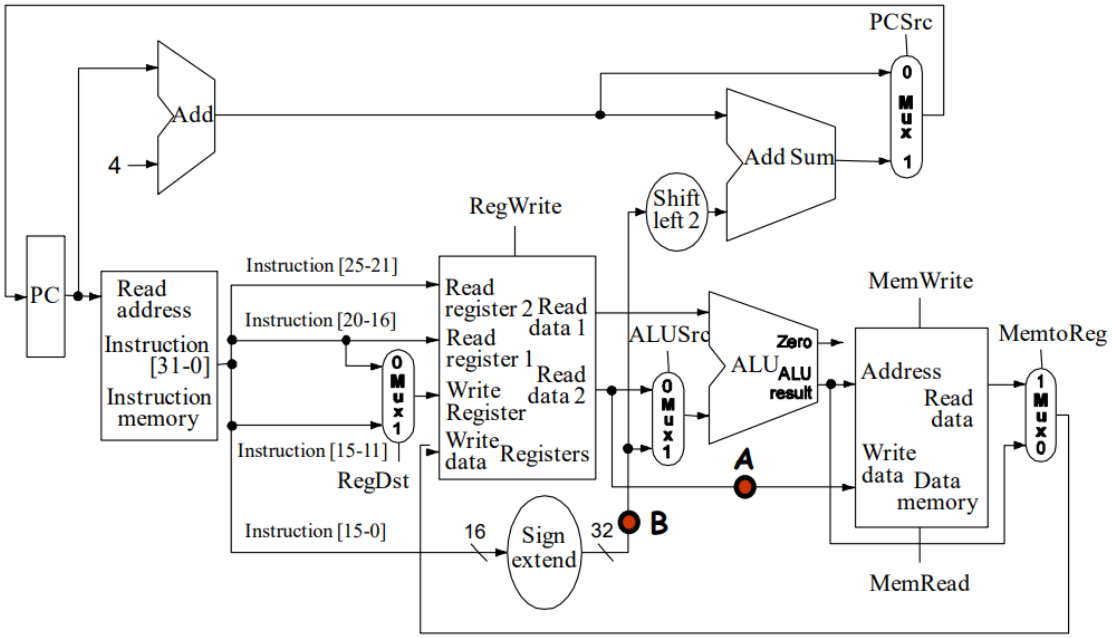
National Taiwan Normal University
Department of Computer Science and Information Engineering
CSU0029, Homework 4

1 Information

1. The assignment is worth 100 points.
2. Individual work.
3. Due at 12:00 on 5/18, i.e., Thursday noon.
4. When asked, use a scientific notation, i.e., show a value in the form $m \times 10^n$, where $1 \leq |m| < 10$ and n is an integer.
5. If any fractional part, round to the second decimal place.
6. Submit the assignment to the course website.
7. Write the assignment in English or Chinese MS Word or PDF format.

2 Contents

1. (20 points) For the Single-Cycle MIPS CPU shown below, which of following statements are correct?



(A) If the path labeled A has been cut, the instructions add, slt, and sw still can run correctly.

(B) If the path labeled B has been cut, the instructions lw, sw and beq may fail.

(C) If the control signal ALUsrc is stuck on 0, the instructions lw, sw, and beq may fail to run correctly.

(D) If the control signal RegDst is stuck on 0, the instructions lw and sw still can run correctly.

(E) If the control signal MemToReg is stuck on 1, the instructions add, sub, lw, and slt may fail to run correctly.

2. (25 points) The execution of an instruction can be divided into five parts: instruction fetch (IF), register read (RR), ALU operation (EX), data access (MEM), and register write (RW). The following Table 1 shows the execution time of each part for several types of instructions, assuming that the multiplexors, and control unit have no delay.

	Instruction fetch	Register read	ALU operation	Data access	Register write
Load word (lw)	200 ps	100 ps	200 ps	200 ps	100 ps
Store word (sw)	200 ps	100 ps	200 ps	200 ps	
R-format (add, sub, and, or, slt)	200 ps	100 ps	200 ps		100 ps
Branch (beq)	200 ps	100 ps	200 ps		

If instructions are to be executed in a pipelined CPU with five pipeline stages, IF, RR, EX, MEM, RW where the pipeline stages execute the corresponding operations mentioned above.

(i) What is the cycle time of the pipelined CPU? What is the maximum working frequency?

(ii) What is the latency of executing the load-word instruction (lw) in the pipelined CPU?

(iii) What is the latency of executing the add instruction (add) in the pipelined CPU?

(iv) What is the maximum throughput of the pipelined CPU?

3. (10 points) A group of students were debating the efficiency of the five-stage pipeline when one student pointed out that not all instructions are active in every stage of the pipeline. After deciding to ignore the effects of hazards, they made the following five statements. Which one is correct ?

   (A) After jumps, branches, and ALU instructions to take fewer stages than the five required by the load instruction will increase pipeline performance under all circumstances.

   (B) Trying to allow some instructions to take fewer cycles does help, since the throughput is determined by the clock cycle; the number of pipe stages per instruction affects both latency and thus throughput.

   (C) You cannot make ALU instructions take fewer cycles because of the write-back of the result, but branches and jumps can take fewer cycles, so there is some opportunity for improvement.

   (D) Instead of trying to make instructions take fewer cycles, we should explore making the pipeline longer, so that instructions take more cycles, but the cycles are shorter. This could improve performance.

4. (25 points) Please answer "Yes" or "No" for pipeline hazards:

   (A) A control hazard occurs due to the need to determine the proper instruction to fetch in the MEM stage of a pipeline processor.

   (B) A control hazard occurs due to the need to determine the proper instruction to fetch in the IF stage of a pipeline processor.

   (C) "Forwarding" is a common technique to relieve the control hazards.

   (D) Data hazards arise from the dependence of one instruction on an earlier one that is still in the pipeline.

   (E) Generally speaking, a pipeline hazard happens when the next instruction cannot execute in the following clock cycle.

(A)	(B)	(C)	(D)	(E)

5. (20 points) Consider a MIPS processor with five-stage (i.e., IF, ID, EX, MEM, WB) pipeline. Suppose the processor has separate instruction and data memories. The hazard detection and forwarding units are also employed. Assume there is no structural hazard. There is also no cache miss. Find the number of clock cycles required by the pipeline for the execution of each of the following sequences.

(a)
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add R3, R2, R1;
add R4, R10, R3;
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(b)
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lw  R6, 12(R4);
add R8, R10, R6;
add R12, R6, R8;
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