計算機結構-hw05

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Question 1

> A memory system has 1M words. Each word is an 8-bit byte. The memory is organized into blocks of 8 words each. The cache has 256K words, organized into cache lines of 8 words each. The memory cache is organized into 4-way set associative cache. Which of the following statements are true?
>
> (a) 13 bits are needed for cache set address.
>
> (b) 4 bits are for Tag.
>
> (c) 21 bits are needed to address all words.
>
> (d) 17 bits are needed to address all blocks.
>
> (e) None of the above.

c: Total number of words in the memory is 1M. To address 1M locations, log2(1M) = 20 bits

Answer: A B D

Question 2

> For a typical disk without considering queuing delay, the average seek time is 5 mil- liseconds, and the transfer rate is 2M-bytes per second. The disk rotates at 600 RPM (Revolution Per Minute), and the controller overhead is 0.5 millisecond. Determine the average time to read a 1792-bytes sector.

Answer:

- Seek Time = 5 ms
- Rotational Delay = (1 / 600) / 2 = 0.1 sec / 2 = 100 ms / 2 = 50 ms
- Transfer Time = 1792 / 2 million = 0.000896 sec = 0.896 ms
- Controller Overhead = 0.5 ms

Total Time = Seek Time + Rotational Delay + Transfer Time + Controller Overhead = 5 ms + 50 ms + 0.896 ms + 0.5 ms = 56.396 milliseconds

Question 3

> A virtual memory system often implements a TLB to speed up the virtual-to-physical address translation. A TLB has the following characteristics. Assume each TLB entry has a valid bit, a dirty bit, a tag, and the page number. Determine the exact total number of bits to implement this TLB.
>
> • It is direct-mapped.
>
> • It has 16 entries.
>
> • The page size is 4 Kbytes.
>
> • The virtual address space is 4 Gbytes.
>
> • The physical memory is 1 Gbytes.

Answer:

- Valid Bit and Dirty Bit: 2*16 = 32 bits
- Tag: 6 bits per entry, for 16 entries, 16 * 16 = 256 bits
- Page Number: 18 bits per entry, for 16 entries, 18 * 16 = 288 bits

Total number of bits: 32 bits (valid and dirty bits) + 256 bits (tag) + 288 bits (Page Number) = 576 bits

Question 4

> Assume that the miss rate of an instruction cache is 3% and the miss rate of the data cache is 6%. If a processor has a CPI of 4 without any memory stalls and the miss penalty is 100 cycles for all misses. Assume the frequency of all loads and stores is 30%. How much faster a processor will run with a perfect cache that never missed.

Answer:

- Orignal:
    - Instruction fetches: 0.03 * 100 = 3 cycles(stall)
    - Data loads / stores: (stall) = 0.30 * 0.06 * 100 = 1.8 cycles(stall)

  Total miss penalty: 3 cycles + 1.8 cycles = 4.8 cycles

  CPI with memory stalls: 4 cycles + 4.8 cycles = 8.8 cycles

- Perfect:

  Only base CPI: 4 cycles

Speedup = Total CPI with original cache / Total CPI with perfect cache

8.8 / 4 = 2.2

Question 5

> Consider a virtual memory system with the following characteristics:
>
> • Page size of 64 KB= 2^16 bytes.
>
> • Page table and page directory entries of 8 bytes per entry.
>
> • Inverted page table entries of 16 bytes per entry.
>
> • 31 bit physical address, byte addressed.
>
> • Two-level page table structure (containing a page directory and one layer of page tables).

> What is the size (in number of address bits) of the virtual address space supported by the above virtual memory configuration?

Answer:

- Offset: 16 bis
- Page Table: 64KB / 8 = 2^13 page table entries, 13 bits
- Page Directory: 64KB / 8 = 2^13 page directory entries, 13 bits

Total virtual address bits = Offset bits + Page Table bits + Page Directory bits

16 + 13 + 13 = 42 bits

> What is the maximum required size (in KB, MB, or GB) of an inverted page table for the above virtual memory configuration?

Answer:

Number of frames = Physical memory size / Page size = 2^31 bytes / 2^16 bytes = 2^15

Inverted page table size = Number of frames * Size per entry = 2^15 * 16 bytes = 2^19 bytes = 512 KB