Top View

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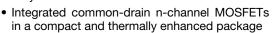
Common Drain Dual N-Channel 30 V (S1-S2) MOSFET

PRODUCT SUMMARY	
V _{S1S2} (V)	30
$R_{S1S2(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.00450
$R_{S1S2(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.00695
Q _g typ. (nC) ^g	14
I _{S1S2} (A) ^a	101
Configuration	Common drain

Bottom View

FEATURES

- TrenchFET® Gen IV power MOSFET
- Very low source-to-source on resistance

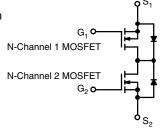




- 100 % R_g and UIS tested
- · Optimizes circuit layout for bi-directional current flow
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- · Battery protection switch
- Bi-directional switch
- · Load switch



ORDERING INFORMATION	
Package	PowerPAK 1212-8SCD
Lead (Pb)-free and halogen-free	SiSF06DN-T1-GE3

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{S1S2}	30	.,,	
Gate-source voltage		V _{GS}	+20 / -16	V	
Continuous drain current (T _J = 150 °C)	T _C = 25 °C		101		
	T _C = 70 °C	1 . 🗀	81		
	T _A = 25 °C	I _{S1S2}	28 b, c	Α	
	T _A = 70 °C	1	22 ^{b, c}		
Pulsed drain current (t = 100 μs)		I _{S1S2M}	190		
	T _C = 25 °C		69.4		
Maximum power dissipation	T _C = 70 °C		44.4	14/	
	T _A = 25 °C	P _D	5.2 ^{b, c}	W	
	T _A = 70 °C	1	3.3 b, c		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) c			260		

THERMAL RESISTANCE RATIN	IGS				
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	t ≤ 10 s	R_{thJA}	19	24	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	1.4	1.8	C/VV

Notes

- a. $T_C = 25 \,^{\circ}C$
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 10 s
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8SCD is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- f. Maximum under steady state conditions is 63 °C/W
- g. Single MOSFET



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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static			•			
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30	-	-	V
Gate-source threshold voltage	V _{GS(th)}	$V_{S1S2} = V_{GS}, I_D = 250 \mu A$	1	-	2.3	V
Gate-source leakage	I _{GSS}	$V_{S1S2} = 0 \text{ V}, V_{GS} = +20 \text{ V} / -16 \text{ V}$	-	-	± 100	nA
Zana mata walta na alumin awamant		V _{S1S2} = 30 V, V _{GS} = 0 V	-	-	1	
Zero gate voltage drain current	I _{DSS}	V _{S1S2} = 30 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15	μA
On-state drain current ^a	I _{S1S2(on)}	V _{S1S2} ≥ 10 V, V _{GS} = 10 V	20	-	-	Α
Duain accurac on atata vaciatanas 3	Б	V _{GS} = 10 V, I _{S1S2} = 7 A	-	0.00344	0.00450	Ω
Drain-source on-state resistance ^a	R _{S1S2(on)}	V _{GS} = 4.5 V, I _{S1S2} = 5 A	-	0.00536	0.00695	
Forward transconductance ^a	9 _{fs}	V _{S1S2} = 10 V, I _{S1S2} = 35 A	-	115	-	S
Dynamic ^{b, c}						
Input capacitance	C _{iss}		-	2050	-	pF
Output capacitance	Coss	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	855	-	
Reverse transfer capacitance	C _{rss}		-	40	-	
Tabella de alemana		$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 5 \text{ A}$	-	30	45	
Total gate charge	Q_g		-	14	21	0
Gate-source charge	Q_{gs}	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 5 \text{ A}$	-	6.1	-	nC
Gate-drain charge	Q_{gd}		-	2.8	-	
Gate resistance	R_g	f = 1 MHz	0.2	1.1	2.2	Ω
Turn-on delay time	t _{d(on)}		-	18	36	
Rise time	t _r	$V_{DD} = 15 \text{ V}, R_L = 3 \Omega, I_{S1S2} \cong 5 \text{ A},$	-	10	20	
Turn-off delay time	t _{d(off)}	$V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	35	70	
Fall time	t _f		-	10	20	
Turn-on delay time	t _{d(on)}		-	30	60	ns
Rise time	t _r	$V_{DD} = 15 \text{ V}, R_L = 3 \Omega, I_D \cong 5 \text{ A},$	-	60	120	
Turn-off delay time	t _{d(off)}	$V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	35	70	
Fall time	t _f		-	20	40	
Drain-Source Body Diode Characteristi	cs ^c					
Continuous source-drain diode current	I _{S1S2}	T _C = 25 °C	-	-	60	_
Pulse diode forward current	I _{S1S2M}		-	-	190	Α
Body diode reverse recovery time	t _{rr}		-	34	51	ns
Body diode reverse recovery charge	Q _{rr}	$I_F = 5 \text{ A, di/dt} = 100 \text{ A/µs,}$	-	25	50	nC
Reverse recovery fall time	t _a	T _J = 25 °C	-	17	-	
Reverse recovery rise time	t _b		-	17	-	ns

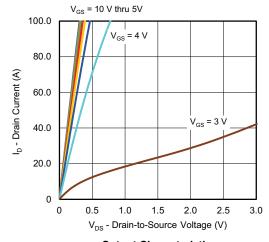
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. On single MOSFET

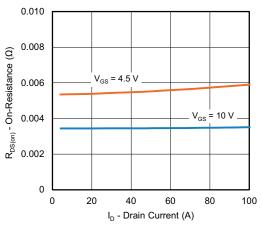
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



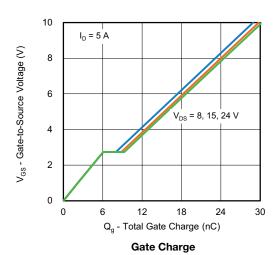
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

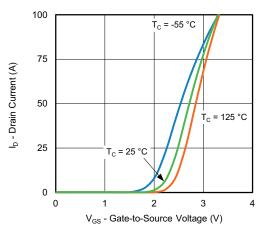


Output Characteristics

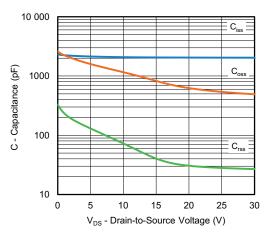


On-Resistance vs. Source Current and Gate Voltage

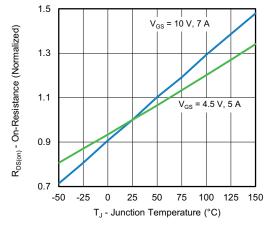




Transfer Characteristics



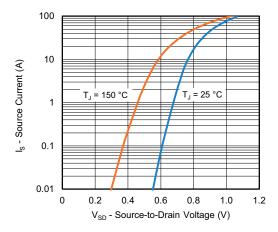
Capacitance



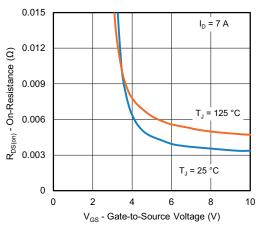
On-Resistance vs. Junction Temperature



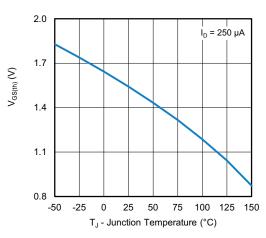
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



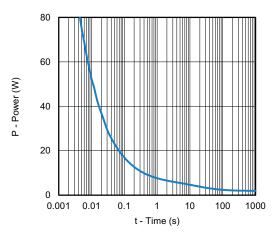
Source-Drain Diode Forward Voltage



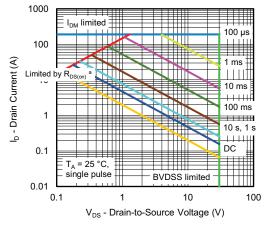
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



Single Pulse Power, Junction-to-Ambient



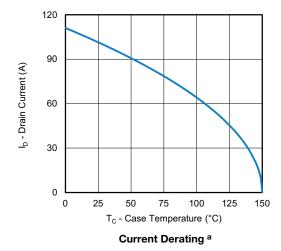
Safe Operating Area, Junction-to-Ambient

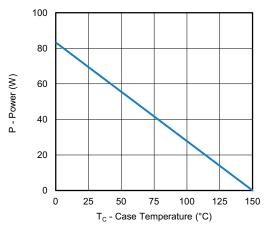
Notes

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





Power, Junction-to-Case

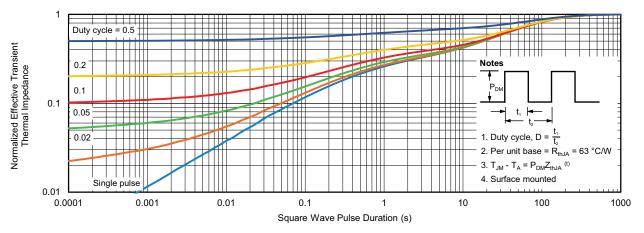
Notes

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

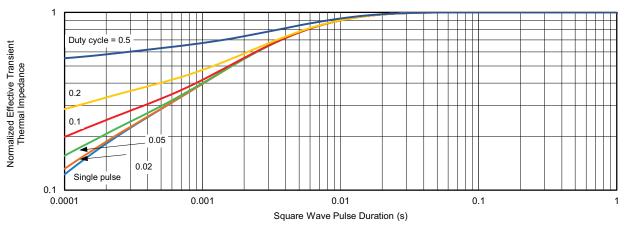


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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient

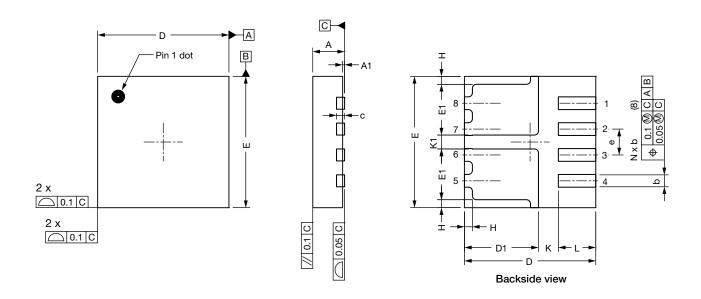


Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?77407.

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PowerPAK® 1212-8S CD with Flip Chip

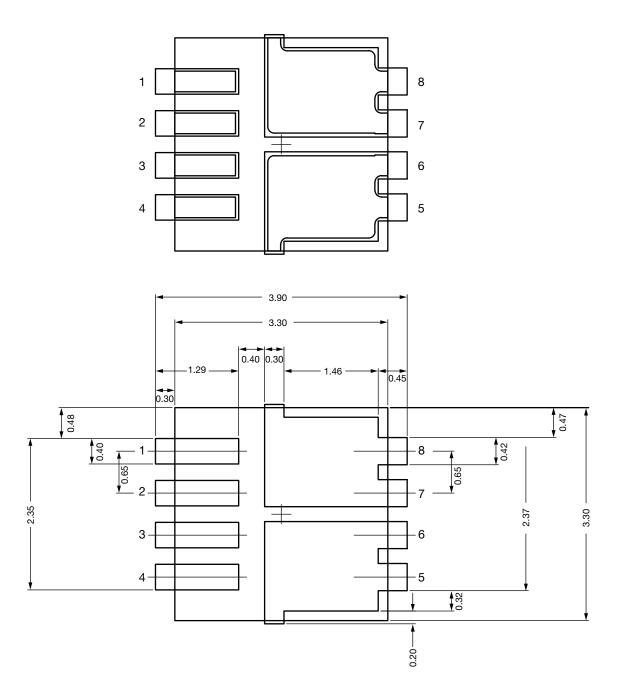


DIM. MIN.	MILLIMETERS			INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	0.70	0.75	0.80	0.027	0.029	0.031	
A1	0	0.02	0.05	0	0.001	0.002	
b	0.27	0.32	0.37	0.011	0.013	0.015	
С	-	0.20 ref.	-	-	0.008 ref.	-	
D	3.20	3.30	3.40	0.126	0.130	0.134	
D1	1.76	1.86	1.96	0.069	0.073	0.077	
E	3.20	3.30	3.40	0.126	0.130	0.134	
E1	1.18	1.28	1.38	0.046	0.050	0.054	
е	0.60	0.65	0.70	0.024	0.026	0.028	
K		0.50 typ.			0.020 typ.		
K1	0.35 typ.			0.014 typ.			
Н	0.10	0.20	0.30	0.006	0.008	0.010	
L	0.84	0.94	1.04	0.033	0.037	0.041	

DWG: 6061



Recommended Land Pattern PowerPAK® 1212-8S CD





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