Features

- Electrically Programmable PLL for multiple applications
- Wide Ranges of Input and Output Frequency for diverse clocking needs
- Uses core supply voltage only – best suited for portable and low power products
- Implemented with Analog Bits' proprietary architecture
- Fully integrated inside customer-specified IO ring
- Occupies no core area
- Low power consumption
- Spread Spectrum tracking capability
- Requires no additional on-chip components or band-gaps, minimizing power consumption
- Excellent jitter performance with optimized noise rejection

General Description

Analog Bits' Wide Range PLL addresses a large portfolio of applications, ranging from simple clock de-skew and non-integer clock multiplication to programmable clock synthesis for multi-clock generation. The PLLs are designed for digital logic processes and use robust design techniques to work in noisy SoC environments, such as high speed communication to low power consumer to memory interfaces.

The PLL macro is implemented in Analog Bits' proprietary architecture that uses core and 2.5V IO devices driven at core voltage only. The PLL resides inside the IO ring that includes two analog power supply pads, occupying no core area. In order to minimize noise coupling and maximize ease of use, the PLL incorporates a proprietary ESD structure, which is proven in several generations of processes. Eliminating band-gaps and integrating all on-chip components such as capacitors and ESD structures, helps the jitter performance significantly and reduces stand-by power. The PLL macro fits into any standard IO pad pitch and can be implemented in either staggered or in-line IO pad ring configurations.

PLL Operational Range

Description	Symbol	Min	Typ	Max	Units
Input Frequency	F_{REF}	10		133	MHz
Post-Divide Reference Frequency (see NOTE3)	F_{PFD}	10		133	MHz
VCO Frequency	F_{VCO}	400		800	MHz
Output Frequency	F_{OUT}	10		400	MHz
Output Duty Cycle	t_{DO}	45		55	%
Lock Time	t_{LOCK}			50	µs
Reset Time	t_{RESET}	1			µs
Maximum Long Term Jitter (see NOTE2)	LTJ	±2% Divided-Ref Period, >=100ps			
Maximum Cycle to Cycle Jitter (see NOTE2)	CCJ	±2% Output Period, >=100ps			
Total area of macro (excluding bond pad area)	A		0.02		sq. mm
Chip core area requirement	CA		0		sq. mm
Total Power (unloaded)	I_{DD}		0.8		mA
Output Load (see NOTE4)	C_L			100	fF
Operational Voltage (Digital)	V_{DIG}	0.99	1.1	1.32	V
Operational Voltage (Analog)	V_{ANA}	0.99	1.1	1.32	V
Operational Temperature	T_{OP}	-40	25	125	C

NOTE1: These specifications represent predicted performance of a typical integration. Actual performance will depend on the actual environment the PLL is incorporated into. Reasonably quiet power supplies and stable reference clock are assumed.
NOTE2: Lower jitter specs are available on request.
NOTE3: External feedback delay should be less than half of the post-divided Reference period.
NOTE4: EM limited by max frequency at max voltage and max temperature.

Table 1: PLL Operational Range

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PLL Functional Specification

The phase-locked loop (PLL) block is provided as a drop-in functional block that fits in typical standard IO rings (TSMC IO ring or 3rd party IP vendor IO ring). The PLL accepts a wide range of input frequencies and can produce a wide range of output frequencies, as detailed in Table 1. Several control bits are provided to configure the desired operating mode of the PLL, and these are detailed in Table 2. The logical features and data flow of the PLL are illustrated in the block diagram of Figure 1.

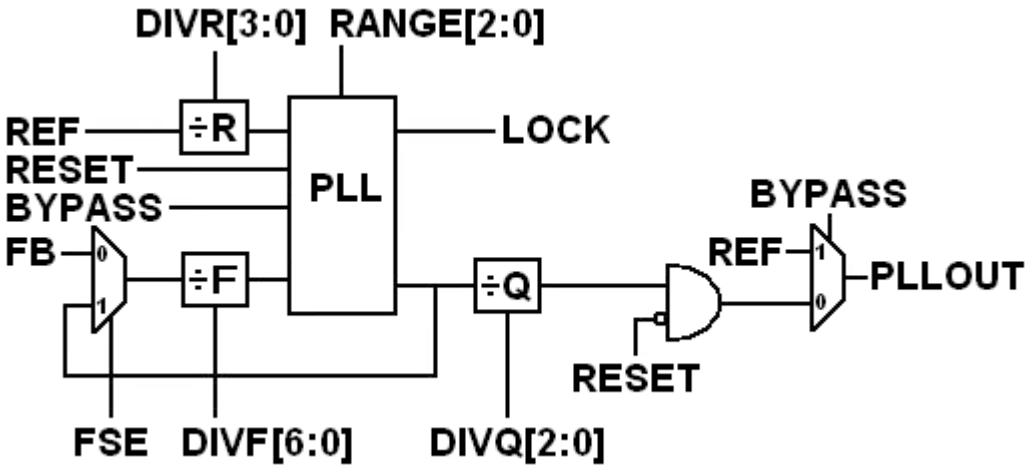


Figure 1: PLL Block Diagram

Pin	Usage	Limitations
DIVR[3:0]	Reference Divider Value (binary value + 1 : 0000 = ÷1)	Both REF and post-divide REF must be within the range specified in Table 1
DIVF[6:0]	Feedback Divider Value (binary value + 1 : 000000 = ÷1)	VCO must be within the range specified in Table 1
DIVQ[2:0]	Output Divider Value (2^ binary value) 001 = ÷2, 010 = ÷4, 011 = ÷8, 100 = ÷16, 101 = ÷32, 110 = ÷64	Settings must maintain the PLL operational ranges specified in Table 1. Valid divider values are 2, 4, 8, 16, 32, and 64.
FSE	Chooses between internal and external input paths: 0 = FB pin input 1 = internal feedback	FB should be tied off (high or low) and not left floating when FSE is high. FB should connect directly or through clock tree to PLLOUT when FSE is low.
RANGE[2:0]	PLL Filter Range 000=BYPASS 100=40-65MHz 001=10-16MHz 101=65-100MHz 010=16-25MHz 110=100-133MHz 011=25-40MHz 111=Not Valid	This sets the PLL loop filter to work with the post-reference divider frequency. Choose the highest valid range for best jitter performance, or optimize with post-silicon characterization.

Table 2: PLL Configuration Controls

LOCK: A LOCK signal is provided to indicate that the PLL has locked on to the incoming signal. LOCK asserts HIGH to indicate that the PLL has achieved frequency lock with a good phase lock. Note that in the case of jittery source clock or feedback tree it is possible the LOCK does not assert because the phases do not match perfectly. It is recommended that LOCK is only used for test and system status information, and is not used for critical system functions without thorough characterization in the host system.

RESET: A RESET control is provided to power down the PLL core and reset it to a known state (low).

BYPASS: A BYPASS signal is provided which both powers-down the PLL core and bypasses it such that PLLOUT tracks REF. BYPASS has precedence over RESET. It is recommended that either BYPASS or RESET are asserted until all configuration controls are set in the desired working value, and the power supply and reference clock are stable within operating range, and the feedback path is functional. Either BYPASS or RESET may be used for power-down IDDQ testing.

Control Signal Table for PLL Output and Power State

BYPASS	RESET	PLLOUT	POWER
0	0	Normal Operation	ON
0	1	Low	OFF
1	X	Tracks REF input	OFF

Table 3: Control Signal Table for PLL Output and Power State

PLL Pin Description

Pin	Type	Function
VDDA	Pad	Analog Power (1.1V)
VSS	Pad	Analog Power
VDD	Ring	Core Power tapped directly from IO ring
VSS	Ring	Core Power tapped directly from IO ring
PLLOUT	Output	PLL Output
LOCK	Output	Lock Indicator Output
RESET	Input	PLL Internal Reset (active HIGH)
BYPASS	Input	PLL Bypass enable (active HIGH)
REF	Input	Reference Clock
FB	Input	Feedback Clock
FSE	Input	Selects source of feedback input (see Table 2)
DIVR[3:0]	Input	Reference Divider Value (see Table 2)
DIVF[6:0]	Input	Feedback Divider Value (see Table 2)
DIVQ[2:0]	Input	Output Divider Value (see Table 2)
RANGE[2:0]	Input	PLL Filter Range (see Table 2)
Note: All input port pins have antenna diodes		

Table 4: PLL Pin Description

Deliverables and EDA Design Views

EDA Design View	Function
GDSII stream file	Layout available to support specified IO pitch for between 5 to 10 metal layers
CDL/Spice netlist	For LVS usage
LEF Views	Place & Route and floor plan, pin caps, number of metal layers.
Datasheet with application notes	Specification of PLL functionality, operational limits and usage help
Verilog (.v)	Behavioral model, functional black box models
Synopsys (.lib)	Timing model files

Table 5: List of Deliverables

APPLICATION NOTE:
Additional General PLL Usage Guidelines

PLL Normal Operation Procedure

1. All operation should commence from the reset or bypass state (RESET=1 or BYPASS=1) with the reference clock running stably and the clock feedback path intact.
2. Set normal operating mode (RESET=0 and BYPASS=0).
3. Wait the specified lock time.
4. It is normal for the LOCK signal to come high before the specified lock time, and may glitch as jitter is acquired. This shows that the PLL has achieved a lock, but it will continue adjusting itself to a more perfect operating point. In a jittery environment, it is possible that LOCK will not assert, but this does not mean that the PLL is not working.
5. To leave normal operating mode, assert RESET or BYPASS.

PLL Special Usage Considerations

1. Note that it is normal for the PLL to overshoot its target frequency during the locking time, so it is recommended that any logic on the output clock domain is held in reset until the specified lock time is complete.
2. Note that the jitter and duty cycle for the output clock of the PLL are what appear at the output of the PLL, but not necessarily at the output of any subsequent clock distribution tree. A common integration oversight is to assume that there will be little or no clock degradation through the distribution tree, whereas it is often a substantial load on the timing budget. Placing a PLL near where the clock is needed (e.g. in the middle of a DDR bus) can help reduce such clock distribution costs.

PLL Characterization Considerations

There is a limit to how precisely a PLL can be characterized on-chip; namely, the jitter picked up between the PLL and any off-chip probe point. However, there are many PLL characteristics which can still be tested. Of interest are:

- Functional Range
- Power Supply Noise Immunity
- Substrate Noise Immunity
- Loop Characteristics

Functional Range

Of primary importance is, does the PLL work; if so, over what range?
To test, set up the part so that a generated clock can be viewed at the pins. Start toggling the input reference clock, and watch the output. Try for many frequencies at the high and low limits, and at various operating voltages and temperatures.
Of particular interest, (even though this is often a test of circuitry outside the PLL such as the clock distribution tree or output buffer), take the input clock up to a high frequency such that the PLL no longer works, and then bring it back down to normal operating frequency. Does the PLL still work; if not, what is the upper frequency limit? Does it have sufficient margin to normal operating range?

Power Supply Noise Immunity

Ideally this would be done with a characterization load board that has an analog power supply filter equal to that of the product board.
Set the PLL at normal operating conditions, and modulate the power supply with some voltage noise (eg +-20%) at a frequency, and measure the output jitter. Of particular interest are T(min) and T(max) of any single cycle, and the maximum phase offset of input to output. Scan the noise frequency low and high. Usually there is some mid-range, somewhere less than F(ref), at which the PLL is most sensitive to noise.

Substrate Noise Immunity
There are two ways to test substrate noise immunity. In a production chip, use heavy duty test vectors to create noise, preferably asynchronous (e.g. pseudo random switching rather than a short repeating loop). Do measurements for T(min) T (max), and maximum offset.
In a test chip without a real-world type noise generator, repeat the power-supply noise test, but put the voltage noise between analog VSS and common VSS. Be sure to keep the peak test voltage << +/- 0.5V.

Loop Characteristics
With the PLL in lock, skip one input cycle and watch the output of the PLL. It should slow down and gradually move to relock at a 360-degree retarded phase. How long does it take? (Typically, 10 to 100 cycles). How much, if at all, does it overshoot (note that a small amount of overshoot is acceptable). Does the output ring a lot? If so, how attenuated is one ring to the next (no ring, or small energy loss between rings may not be optimal, depending on the application). How much was the initial phase shift in the cycle following the skipped cycle? How long was the slowest cycle during this relock?

PLL Production Test Suggestions

Generally the primary PLL datapath is functionally tested with every test the whole chip passes - it quickly becomes apparent if there is not a correct clock. Note that much (often most) of the active area of the PLL is analog in nature, so to help detect significant manufacturing defects with production tests it is required to stress the PLL in ways which may help uncover such defects.

Loop Stability Test
Test the PLL at a lower-than-spec frequency. For instance, if a PLL was designed to run with a minimum operating frequency of 100MHz in and 400MHz out, then test it at 90MHz in and 360MHz out and see if it works OK. This may be repeated at multiple extreme voltage and temperature corners, or additional frequency or voltage margin may be used to compensate for lesser test corners (e.g. tested always at typical temperature, not hot and cold).

Noise Margin Test
Test the PLL at a higher-than-spec frequency. For instance, if a PLL was designed to run with a maximum operating frequency of 100MHz in and 400MHz out, then test it at 110MHz in and 440MHz out and see if it works OK. This may be repeated at multiple extreme voltage and temperature corners, or additional frequency or voltage margin may be used to compensate for lesser test corners (e.g. test always at typical temperature, not hot and cold).

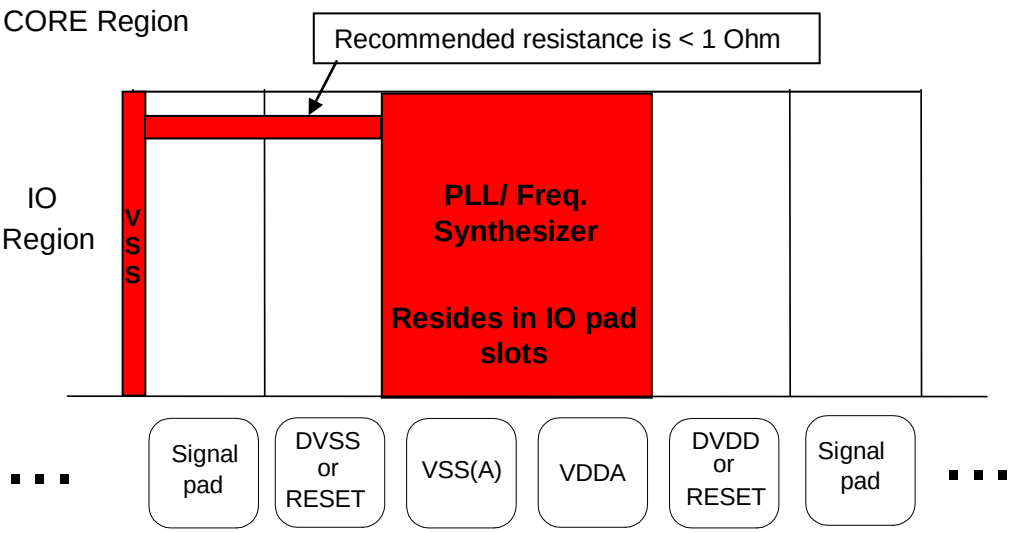
Additional Logic Test
Due to the relatively simple datapath, very good coverage of the logical paths is achieved with simple tests. If the PLL is tested in all functional configurations then that is sufficient to show that the logic works. However, if the number of functional configurations is too large to test, then select a set tests which have each control pin at a 1 and at a zero. For instance, if one test has a divider control bus setting at 01111111 then do another test at 1000000. This way all functions will be validated. At a minimum each PLL divider should be tested at its maximum divide value in at least one production test, to ensure the full coverage of each register element.

APPLICATION NOTE:
Layout and Connectivity Guidelines

- Keep any asynchronous noise generator or sources away from PLLs (e.g. DAC).
- The digital power supply is the primary source of cycle-to-cycle jitter, so the quieter the better.
- Two or more PLLs can be placed next to each other as long as they have their own dedicated analog power supplies
- Place power pads or ground pads or static signals on either side of the PLL for best noise performance
- Place core power pads and ground pads near the PLL for signal integrity and ESD performance
- PLL includes ESD protection for VDDA. ESD protection for core power supply should be provided externally (e.g. in a core VDD pad).
- A core VSS pad should be located less than 1 Ohm away from the PLL (see diagram below)
- This PLL abuts to a customer-specified IO library
- No breaker cells or spacer cells are required
- No power cuts or signal cuts are required
- The digital power is supplied by the digital IO rings and core VSS is connected for ESD purposes
- No manual strapping is required to power pins
- PLL macros use up to M3, so M4 + layers of IO ring do route on top of macros
- If you would like to share the power-pins for multiple PLLs, or abut to a non-standard IO ring, or other customized options, then please contact Analog Bits
- **There will be two connections to the IO pads, the two analog power pins.**

The specs in this document assume that the two power pads are brought outside the package and connected to quiet (filtered) power supplies. (See “APPLICATION NOTE: PCB Mounted Analog Power Supply Filter for PLL Usage”).

Refer to the following drawing for illustration



NOTE: Bond pads shown are for illustrative purposes. Implementation can be based on wirebond (staggered or inline) for both peripheral and CUP style bond pads, or direct to bumps on flip-chip package.

APPLICATION NOTE:
PCB mounted Analog Power Supply Filter for PLL usage

To achieve a reasonable level of long term jitter, it is vital to deliver an analog-grade power supply to the PLL. Typically an R-C or R-L-C filter is usually used, with the "C" being composed of multiple devices to achieve a wide spectrum of noise absorption. Although the circuit is simple, there are specific board layout requirements if it is to work at all.

The series resistance of this filter is limited for DC reasons; generally we like to see <<5% voltage drop across this device under worst-case conditions. High quality series inductors should not be used without a series resistor lest a high gain series resonator is created.

To achieve good low-frequency cut off there should be an electrolytic capacitor in the filter design. As the filter also needs to sustain its attenuation into moderately high frequencies, so there will additionally be at least one non-electrolytic capacitor in parallel. The leads of the high frequency capacitor(s) must be kept short. In some applications the electrolytic capacitor is not required, but it is better to have a space for in on the board which you later leave vacant, rather than have a jittering PLL and no-where to put the cap. Cursory analysis suggests that a third, very high frequency, capacitor should help reduce noise – but experimental data has not shown any jitter benefit in real applications.

Board layout around the high-frequency capacitor and the path from there to the pads is critical. It is vital that the quiet ground and power are treated like analog signals.

The power (vdd) path must be a single wire from the IC package pin to the high frequency cap, then to the low frequency cap, and then through the series element (e.g. resistor) then to board power (vdd). The distance from the IC pin to the high frequency cap should be as short as possible.

Similarly, the ground (vss) path should be from the IC pin to the HF cap, to the LF cap, with the distance from IC pin to HF cap being very short. Modern PLLs will have the DC ground connection made on chip, so the external ground connection must not be connected to PCB ground. With some older designs, where the DC ground connection is not on-chip, a trace would be run from the LF cap to board ground, near the vdd connection – be aware of this difference if converting an old board design.

In all applications, **the power and ground traces should be short, and run close and parallel** as far as is possible, with large spacings to adjacent traces. **On no account should any connection be made from VDDA or VSS(A) to board power planes**; only connect as described above.

Package Considerations

The wiring from the on-chip PLL to the power supply filter includes traces inside the package, all the way to the bond pads. Where possible, the in-package wiring should follow the guidelines for the PCB, being short and parallel and not connected to any other power supplies.

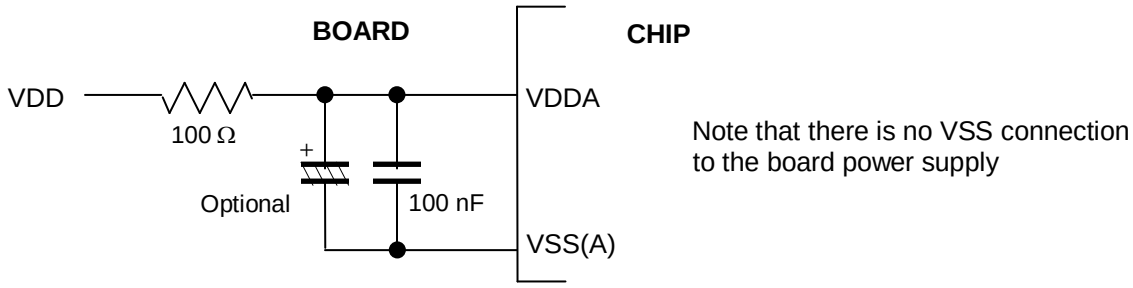
Real World Component Selection

Throughout the attenuating frequency range, there should be no resonant non-absorptions. This means that the series element will either be a resistor or a very poor (i.e. resistive) inductor.

Having got the series element with the most impedance as we can, the filter requires the highest value HF capacitor we can find in a small package (often 100nF). In applications with a low PLL reference frequency and environment with significant low frequency components, it is often beneficial to add a large value capacitor such as an electrolytic which fits nicely on the board (often 22uF).

Example Schematic

This schematic represents both the circuit and the device placement.
The component values are only illustrative.



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