bus

File: bus.kicad_sch

power

File: power.kicad_sch

buffers

File: buffers.kicad_sch

TMS9995CPU

File: TMS9995CPU.kicad_sch

GALS

File: GALS.kicad_sch

bus sharing

File: bussharing.kicad_sch

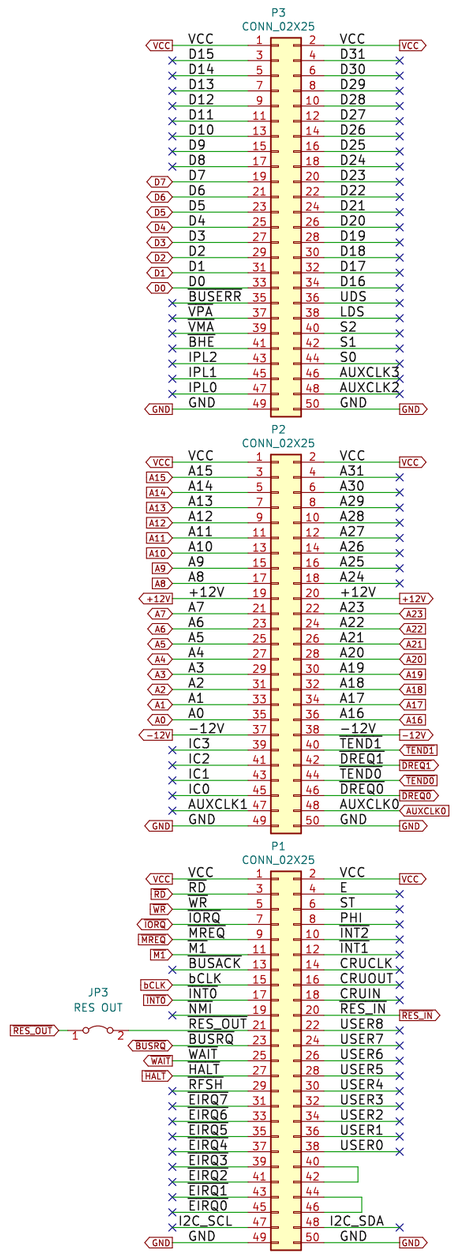
IO

File: io.kicad_sch

Sheet: /
File: processor.tms9995.kicad_sch

**Title: Duodyne TMS9995 CPU board**

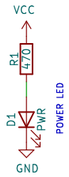
| | | |
|---|---|---|
| Size: B | Date: 2025-03-31 | **Rev: V1.1** |
| KiCad E.D.A. kicad (6.0.11) | | Id: 1/8 |



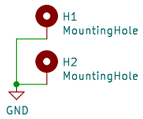

Sheet: /bus/
File: bus.kicad_sch

**Title: Duodyne TMS9995 CPU board**

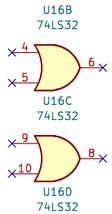
| | | |
|---|---|---|
| Size: B | Date: 2025-03-31 | **Rev: V1.1** |
| KiCad E.D.A. kicad (6.0.11) | | Id: 2/8 |

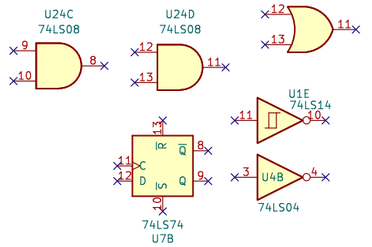


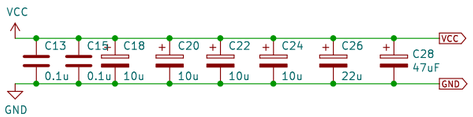





SPARE GATES

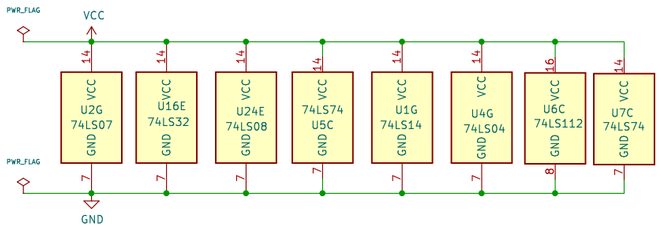


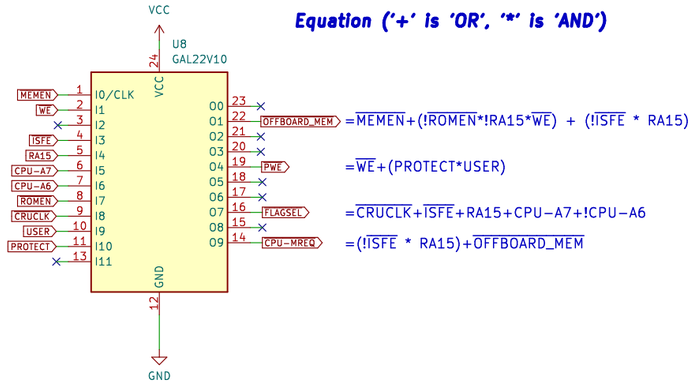







| | | |
|---|---|---|
| Sheet: /power/ | | |
| File: power.kicad_sch | | |
| **Title: Duodyne TMS9995 CPU board** | | |
| Size: B | Date: 2025-03-31 | **Rev: V1.1** |
| KiCad E.D.A. kicad (6.0.11) | | Id: 4/8 |

# TMS9995 MEM GAL22V10




***Equation ('+' is 'OR', '*' is 'AND')***

$$\overline{OFFBOARD\_MEM} = \overline{MEMEN} + (!\overline{ROMEN} * !RA15 * \overline{WE}) + (!\overline{ISFE} * RA15)$$

$$\overline{PWE} = \overline{WE} + (PROTECT * USER)$$

$$FLAGSEL = \overline{CRUCLK} + \overline{ISFE} + RA15 + CPU-A7 + !CPU-A6$$

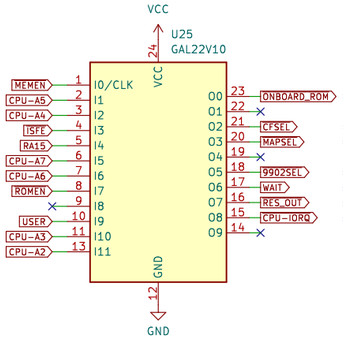
$$\overline{CPU-MREQ} = (!\overline{ISFE} * RA15) + \overline{OFFBOARD\_MEM}$$

The memory map is shown in the table below.

| Memory Address | Mapped To |
|---|---|
| >0000 – >7FFF | ROM when enabled, otherwise RAM |
| >8000 – >EFFF | RAM |
| >F000 – >F0FB | TMS 9995 internal RAM |
| >F0FC – >FDFF | RAM |
| >FE00 – >FE03 | CF card ATA registers |
| >FE10 – >FE13 | CPU RESET |
| >FE40 – >FE4F | Memory mapper registers 0–15 |
| >FEB0 – >FEBF | Offboard IO (ports $80–$FF) |
| >FFF0 – >FFF9 | RAM |
| >FFFA – >FFFF | TMS 9995 internal RAM |

# TMS9995 IO GAL22V10

| CRU Address | Mapped To |
|---|---|
| >0000 – >003F | TMS 9902 registers |
| >0040 – >007F | Control signal latch (further details here) |
| | (Plus processor internal CRU bits) |




$$\overline{ONBOARD\_ROM} = \overline{MEMEN} + \overline{ROMEN} + RA15$$

$$\overline{CFSEL} = \overline{MEMEN} + \overline{ISFE} + !RA15 + CPU-A7 + CPU-A6 + USER + CPU-A5 + CPU-A4 + CPU-A3$$

$$\overline{MAPSEL} = \overline{MEMEN} + \overline{ISFE} + !RA15 + CPU-A7 + CPU-A6 + USER + CPU-A5 + CPU-A4$$

$$\overline{9902SEL} = !\overline{MEMEN} + \overline{ISFE} + RA15 + CPU-A7 + CPU-A6 + USER$$

$$\overline{WAIT} = !\overline{ONBOARD\_ROM} + !CFSEL$$

$$\overline{RES\_OUT} = \overline{MEMEN} + \overline{ISFE} + !RA15 + CPU-A7 + !\overline{CPU-A6} + USER + !CPU-A5 + CPU-A4 + CPU-A3 + CPU-A2$$

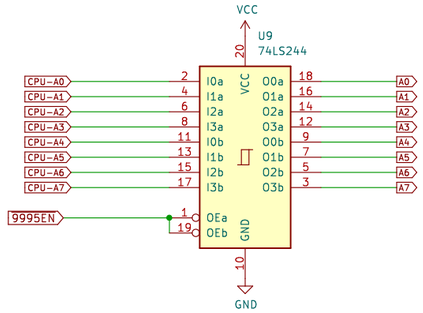
$$\overline{CPU-IORQ} = \overline{MEMEN} + \overline{ISFE} + !\overline{CFSEL} + !MAPSEL + !\overline{9902SEL} + USER + !RA15$$

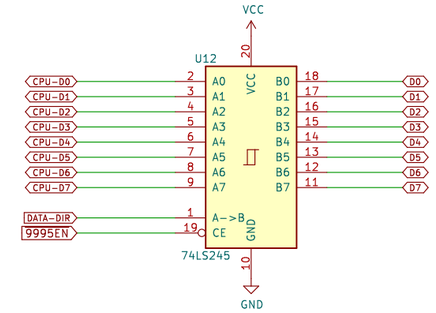
Sheet: /GALS/
File: GALS.kicad_sch

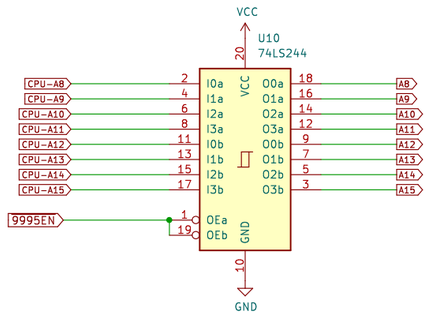
**Title: Duodyne TMS9995 CPU board**

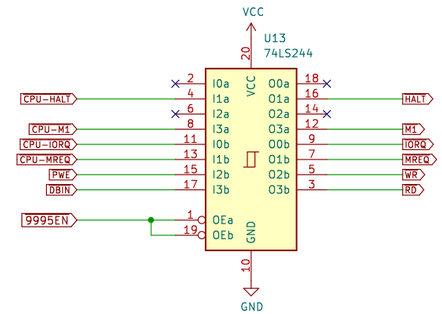
| Size: B | Date: 2025-03-31 | **Rev: V1.1** |
|---|---|---|
| KiCad E.D.A. kicad (6.0.11) | | Id: 5/8 |

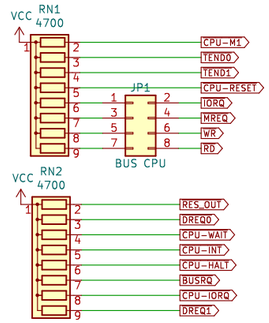
Z80 BUS INTERFACE

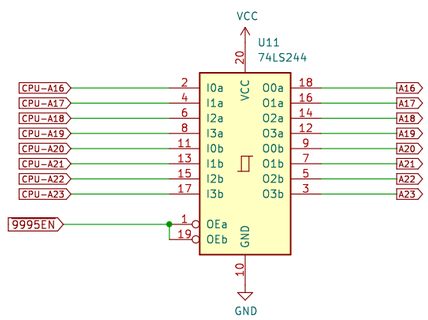


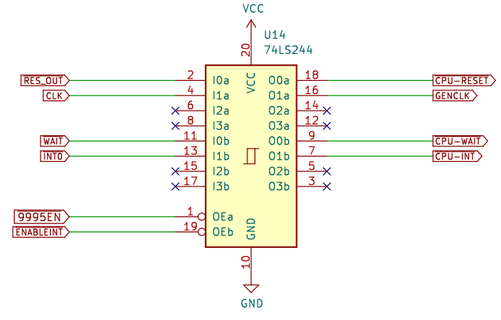



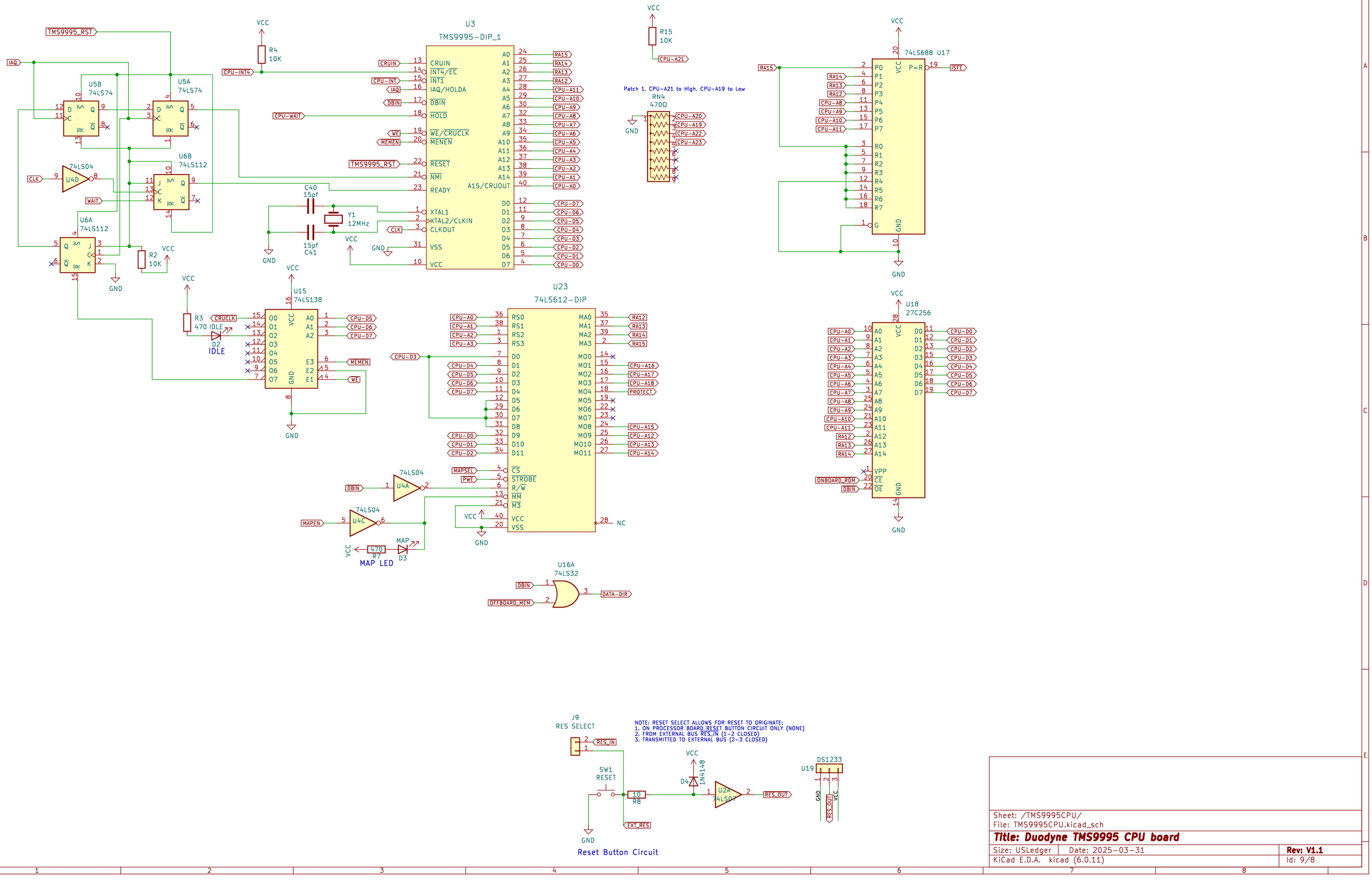



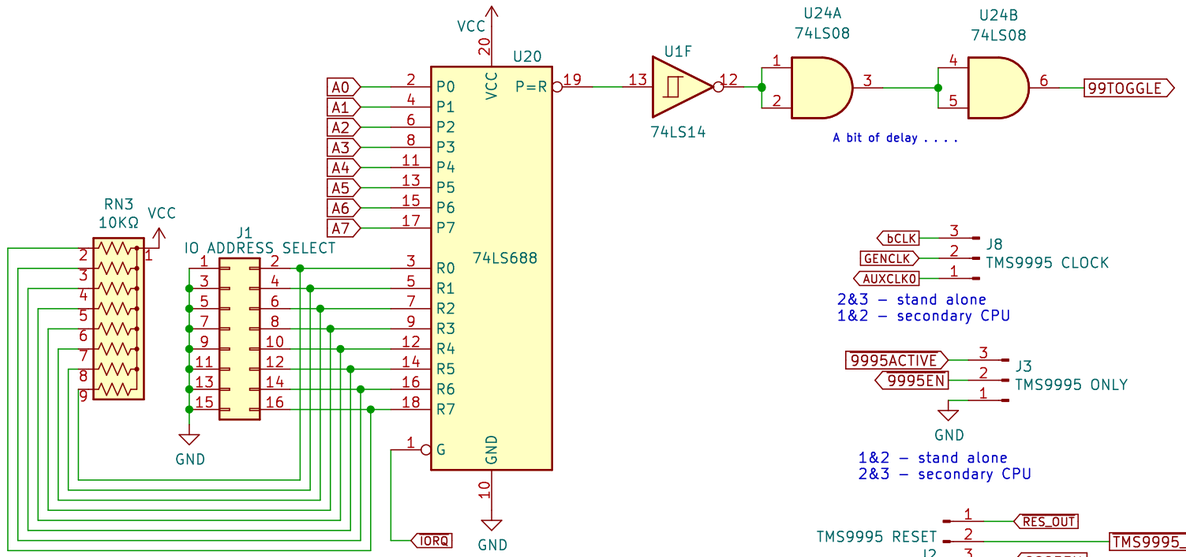

Sheet: /buffers/
File: buffers.kicad_sch

**Title: Duodyne TMS9995 CPU board**

| Size: B | Date: 2025-03-31 | **Rev: V1.1** |
|---|---|---|
| KiCad E.D.A. kicad (6.0.11) | | Id: 6/8 |



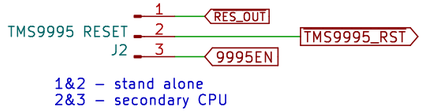

| | |
|---|---|
| Sheet: /TMS9995CPU/ | |
| File: TMS9995CPU.kicad_sch | |
| **Title: Duodyne TMS9995 CPU board** | |
| Size: USLedger | Date: 2025-03-31 |
| KiCad E.D.A. kicad (6.0.11) | Id: 9/8 |

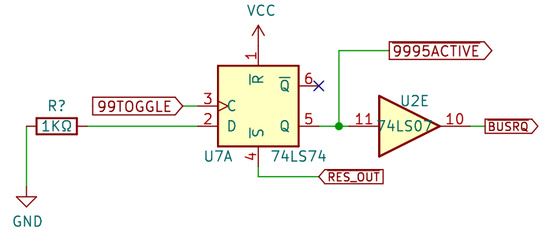


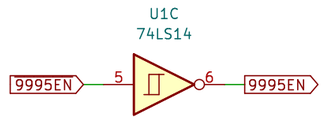


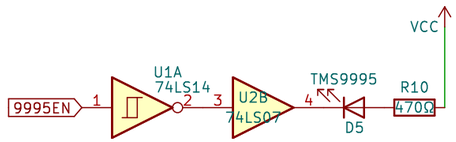




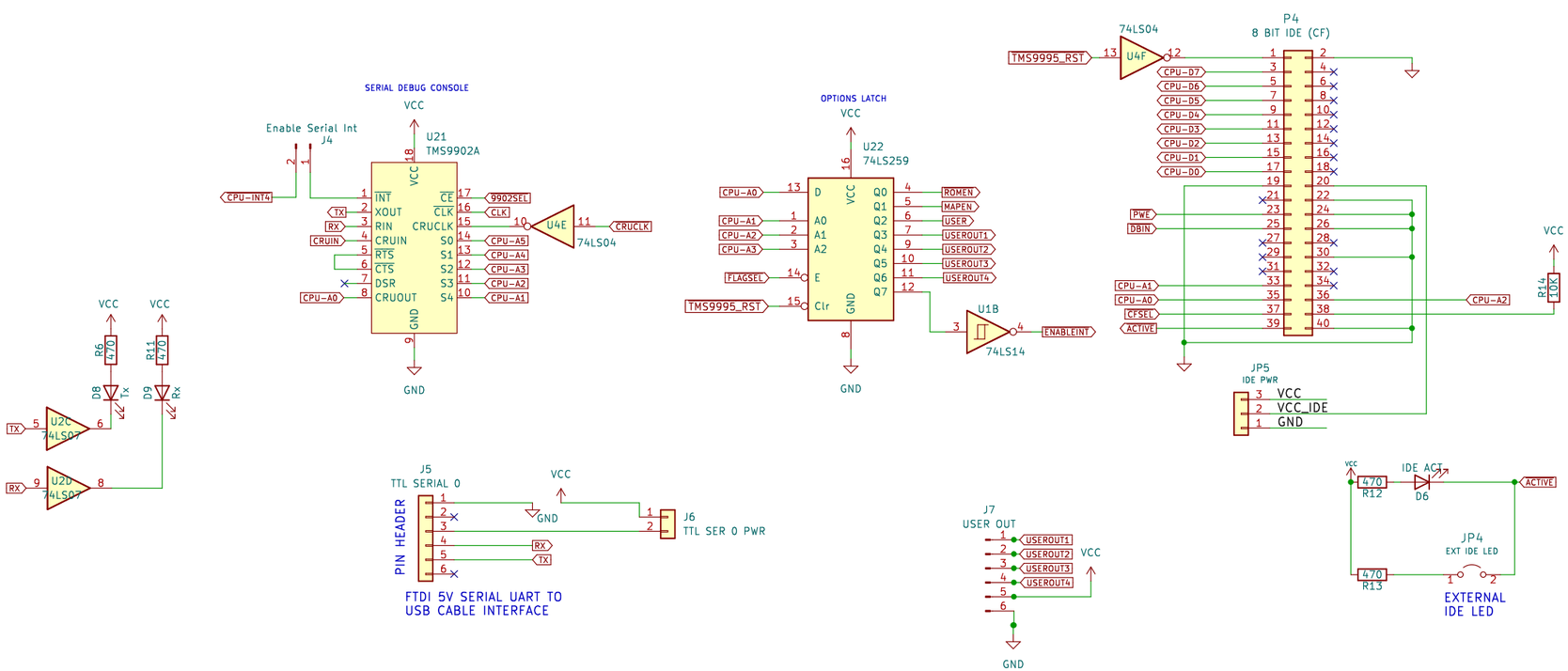




Sheet: /bus sharing/
File: bussharing.kicad_sch

**Title: Duodyne TMS9995 CPU board**

| | | |
|---|---|---|
| Size: A4 | Date: 2025-03-31 | **Rev: V1.1** |
| KiCad E.D.A. kicad (6.0.11) | | Id: 9/8 |




| | |
|---|---|
| Sheet: /IO/ | |
| File: io.kicad_sch | |
| **Title: Duodyne TMS9995 CPU board** | |
| Size: B | Date: 2025-03-31 |
| KiCad E.D.A. kicad (6.0.11) | Id: 11/8 |
| | **Rev: V1.1** |