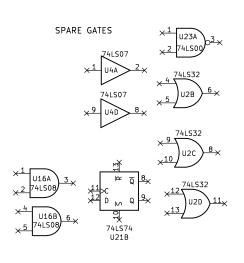
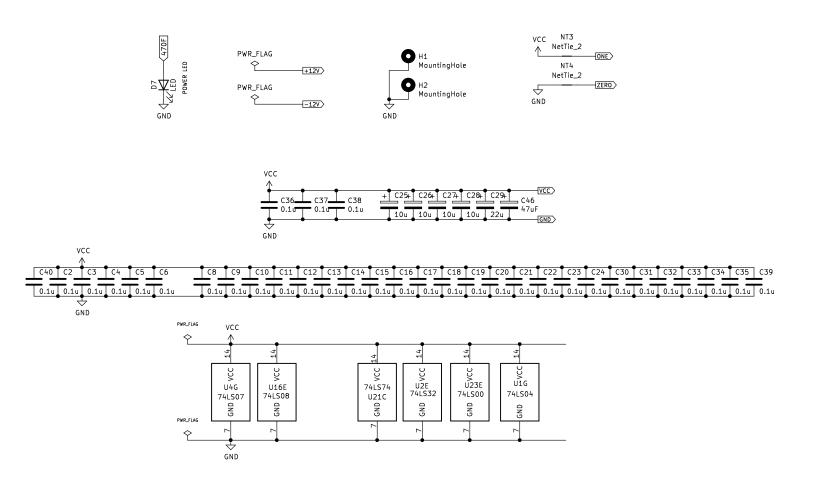
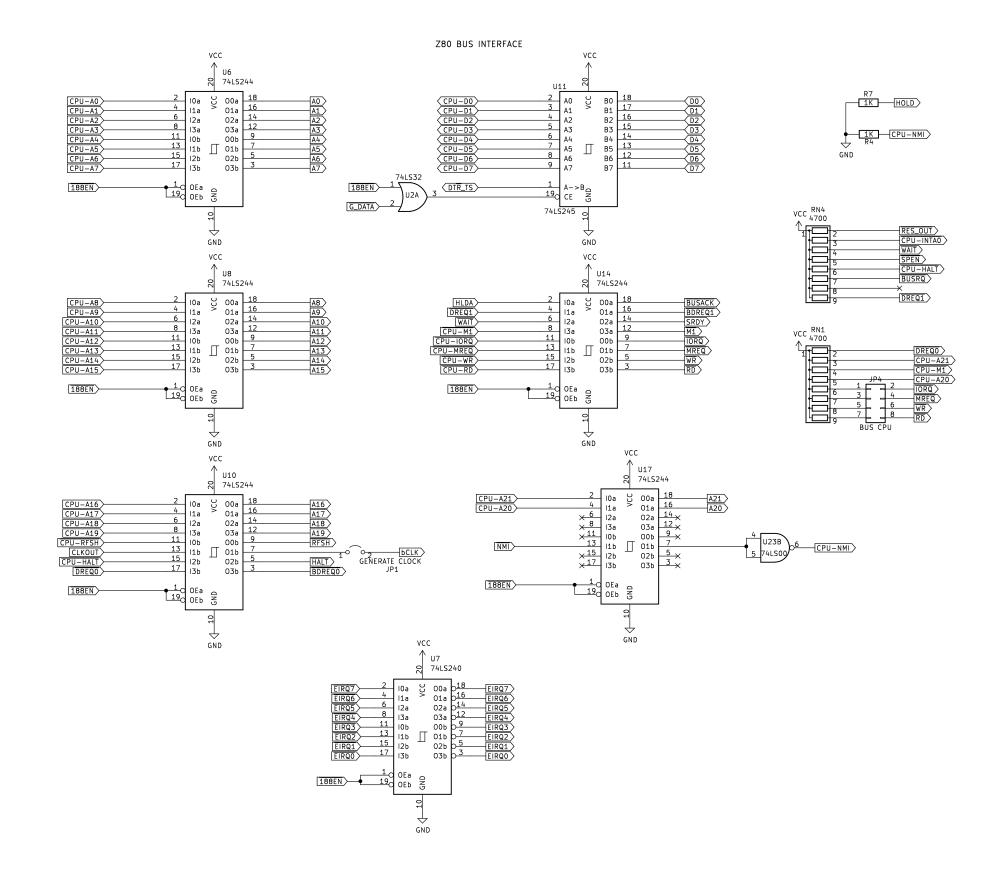
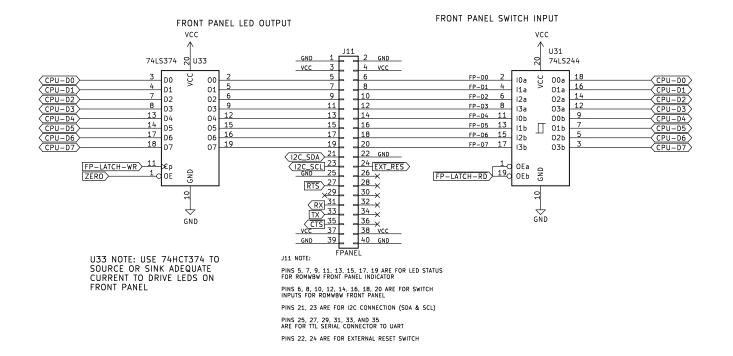
bus	power	buffers	fpanel
File: bus.kicad_sch 80C188CPU	File: power.kicad_sch Memory	File: buffers.kicad_sch bus sharing	File: fpanel.kicad_sch mapper
80C188CPU	Memory	bus sharing	mapper
File: CPU_80C188.kicad_sch	File, Mamazu kinad ash		
FIRE: CFU_OUCTOO.KICAG_SCN	File: Memory.kicad_sch	File: bussharing.kicad_sch	File: mapper.kicad_sch

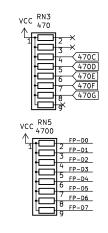
P3	(05
VCC VCC 1 CONN_02	- 2 VCC
VCC D15 3	4 D31 ×
× D14 5	6 <u>D30</u> ×
$\stackrel{\sim}{\times} \stackrel{D13}{{\longrightarrow}} \stackrel{7}{{\longrightarrow}} \stackrel{\cdot}{\longrightarrow} $	8 D29 X 10 D28 X
× D12 9 1 11 11 11	12 D27 ^
^ D10 13 °	1/ D36
× D10 15 15 15 15	16 D25 ×
× D8 17	18 D24 ^
D7 D/ 19 .	20 D23 ×
D6 D6 21 .	22 D22 ×
D5 D5 23 .	24 D21 ×
D3 27 '	26 D20 × 28 D19 ×
D2 30 .	30 D18 ^
D1 31	32 D17 ×
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	34 D16 ×
-X BUSERR 35	36 UDS ×
× VPA 37	38 LDS ×
× VMA 39 → BHE 41	40 S2 × 42 S1 ×
^ IPI 2 //3 "	44 S0 ×
^ IDI 1 /E	46 AUXCLK3
× IPLO 47	48 AUXCLKZ
GND GND 49	50 GND GND
P2	<u> </u>
CONN_02	(25
VCC VCC 1	2 VCC VCC
A15 A15 3 .	4 A31 ×
A14 5 A14 5 A13 7	6 A30 × 8 A29 ×
A13 A12 .	10 428
A12 A11 11	13 427
A11 A10 13	14 A26 ×
A9 15	16 A25 ×
A8 17 .	118 A24 V
(+12V) +12V 19	20 +12V +12V
A7 A6 A6 23	22 A23 × × × × × × × × × × × × × × × × × × ×
A0 A5 25 .	36 A21 ^
Δ3 Λ4 27 F	128 A20 AZI
A4 A3 29	30 A19 A19
A2 A2 31 .	32 A18 A18
A1 33 .	34 A17 A17
A0 A0 35	36 A16 A16 A16
-12V 37 IC3 39	38 -12V -12V -12V
^ IC2 //1	LAS DEFOIL A
× IC1 43	44 TENDO DREQ1
Ç ICO 45 █	46 DREQO PRECO
× AUXCLK1 47	48 AUXCLKU
GND 49	50 GND GND
P1	
CONN_02:	- 2 VCC
VCC DD 7	2 VCC VCC
IKD WD	6 ST
IORQ TORQ 7	8 PHI ×
MREQ MREQ 9	10 INT2 ^
M1 11 .	I12 INI1
BUSACK 13	14 CRUCLK CRUCUX
bCLK bCLK 15	16 CRUOUT 18 CRUIN X
	20 DES IN A
RES_OUT PUCPS	22 USER8 KES_IN
BUSRQ 23	24 USER7 X
WAIT WAII 25	26 USER6 X
HALT HALI 27	28 USER5 X
RFSH RFSH 29 EIRQ7 31	30 USER4 × 32 USER3 ×
FIDOS 77	Z/ LICED2 ^
FIDOS 75	Tage IISEP1 ^
FIRQ4 37	38 USERO ×
FIRQ3 EIRQ3 39	40
FIRO2 EIRUZ 41	42
FIRO1 EIRU1 43	44
EIRQO LICC SCI 45	46 48 12C_SDA (12C_SDA)
LIZC_SCL CND 40	TEO CND IZC_SDA
GND GND 49	50 GND GND

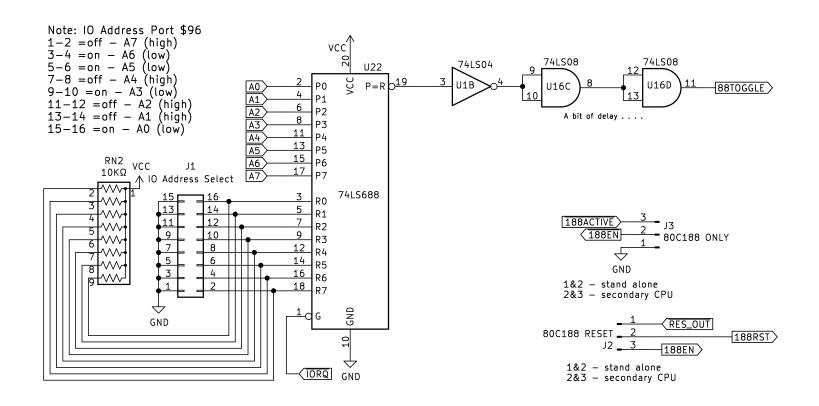


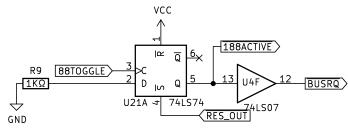


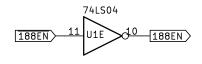




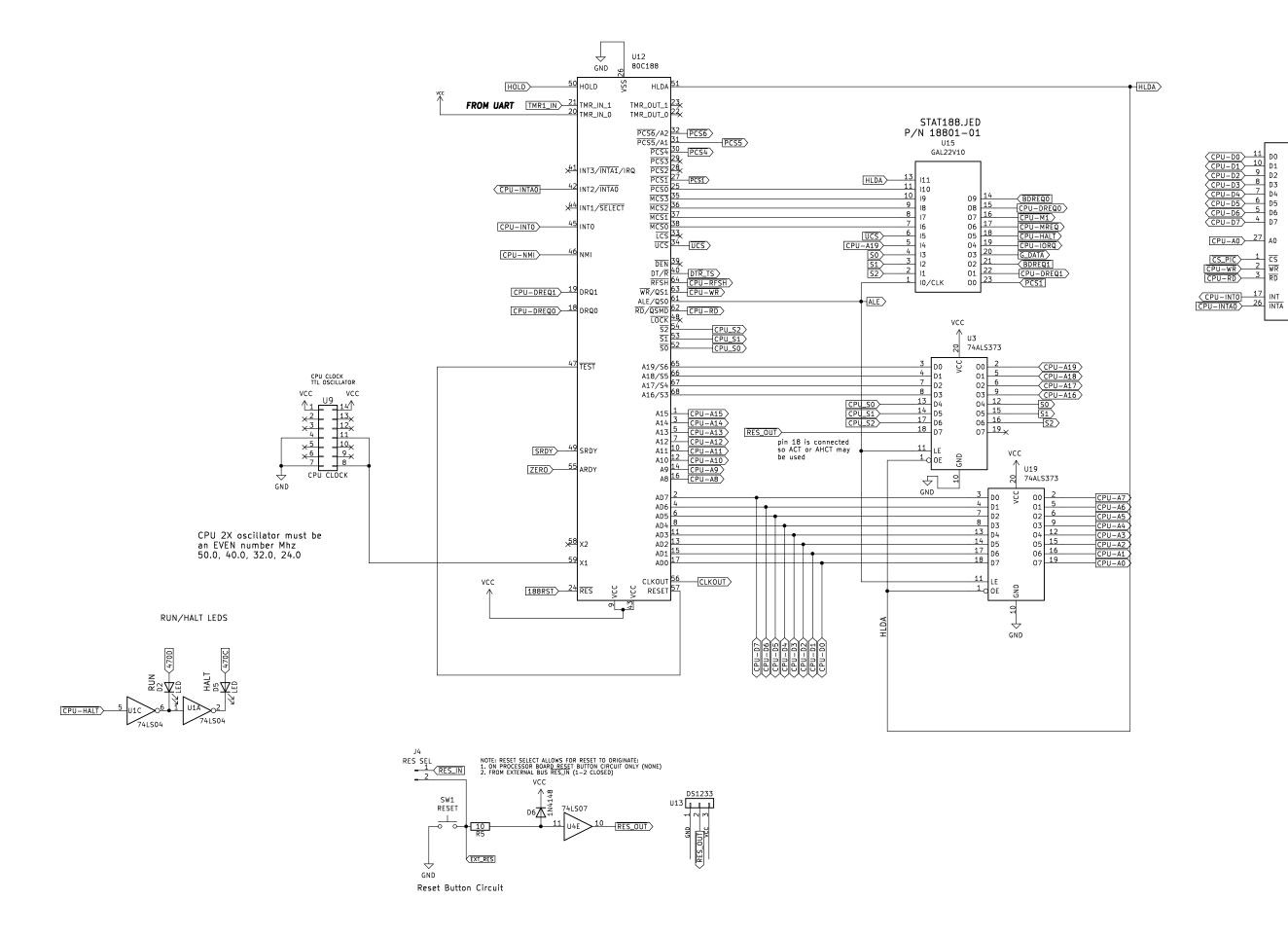








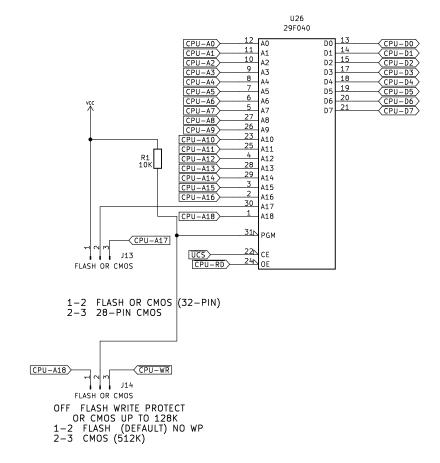




vcc ↑ U5 8259

 $\begin{array}{c|c} \text{CASO} & \begin{array}{c} 12 \\ \text{CAS1} \\ \text{CAS2} \end{array} & \begin{array}{c} 13 \\ \text{15} \\ \end{array} \\ \end{array}$

SP/EN 16 SPEN



ROM

FLASH 39SF010 (128K) ALTERNATES: 39SF020, 29F020, 29F010 39SF040, 29F040 (512K) NOT RECOMMENDED

CMOS 27C010 (128K, 32pin) ALTERNATE 27C020 28pin: 27C512(64K), 27C256(32K)

DEFAULT CHIP: 39SF010 (128K FLASH) DEFAULT JUMPERS: 1-2, 1-2 (BOTH) 29F040 SHOWS ALL PIN ASSIGNMENTS

