bus

File: bus.kicad_sch

power

File: power.kicad_sch

buffers

File: buffers.kicad_sch

fpanel

File: fpanel.kicad_sch

65816CPU

File: 65816CPU.kicad_sch

GALS

File: GALS.kicad_sch

bus sharing

File: bussharing.kicad_sch

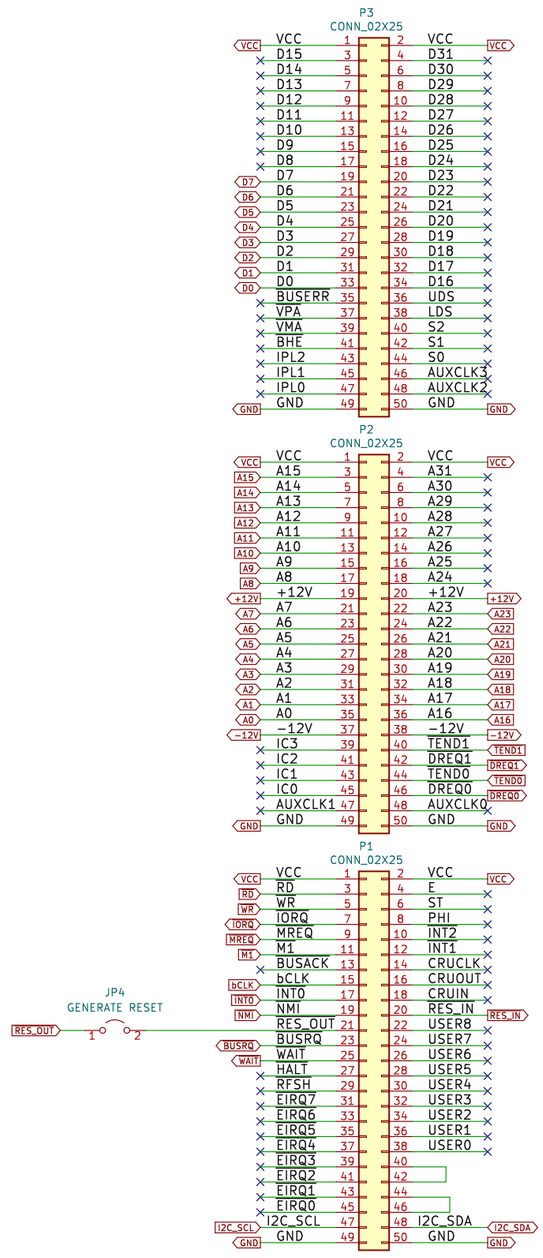
mapper

File: mapper.kicad_sch

Sheet: /
File: processor.65816.kicad_sch

Title: Duodyne 65265 CPU board

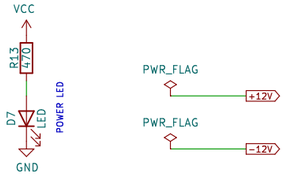
Size: B	Date: 2025-04-12	**Rev: V0.5**
KiCad E.D.A. kicad (6.0.11)		Id: 1/9

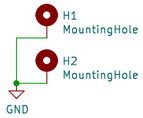


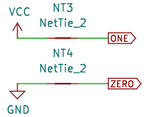
Sheet: /bus/
File: bus.kicad_sch

Title: Duodyne 65265 CPU board

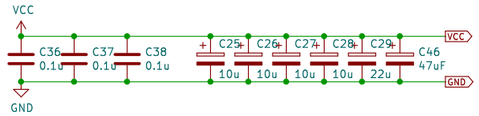
Size: B	Date: 2025-04-12	**Rev: V0.5**
KiCad E.D.A. kicad (6.0.11)		Id: 2/9

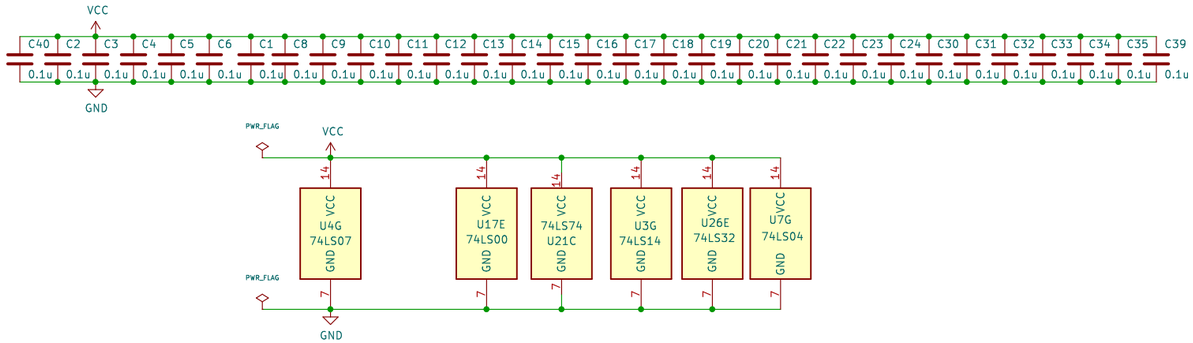


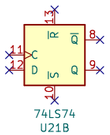


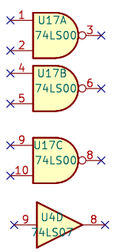


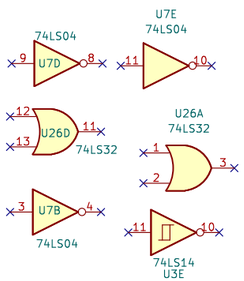
SPARE GATES

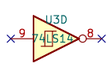






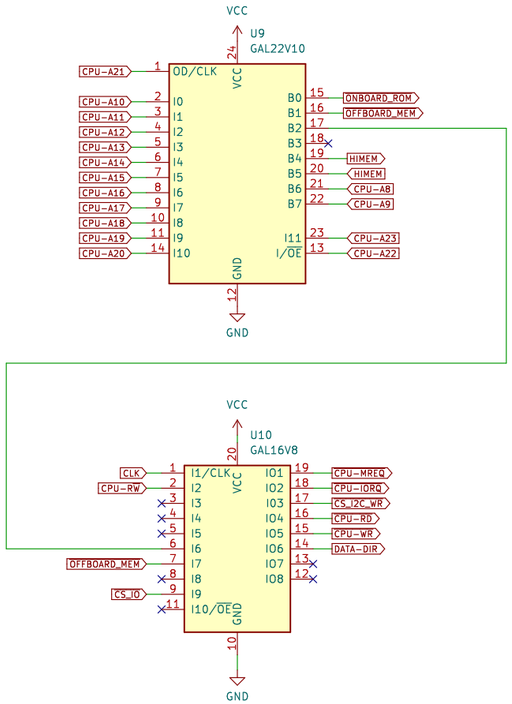






Sheet: /power/	
File: power.kicad_sch	
Title: Duodyne 65265 CPU board	
Size: B	Date: 2025-04-12
KiCad E.D.A. kicad (6.0.11)	Id: 4/9

Rev: V0.5

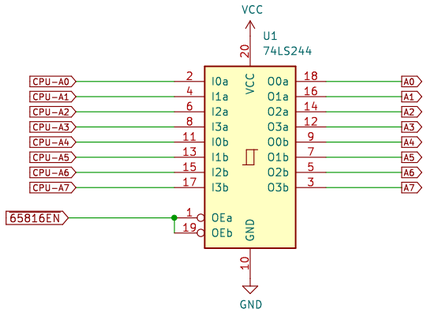


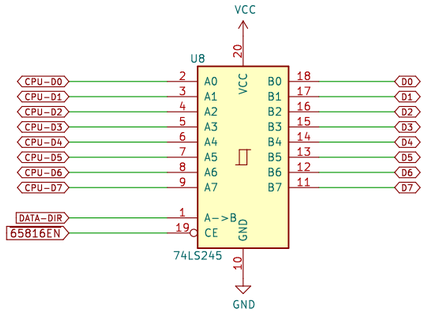
Sheet: /GALS/
File: GALS.kicad_sch

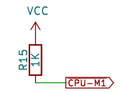
Title: Duodyne 65265 CPU board

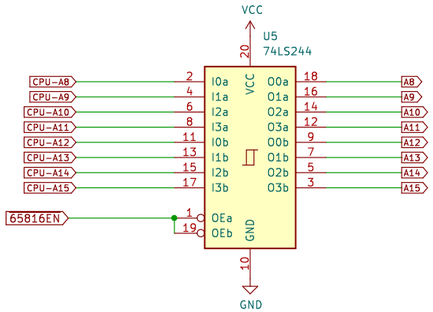
Size: B	Date: 2025-04-12	**Rev: V0.5**
KiCad E.D.A. kicad (6.0.11)		Id: 5/9

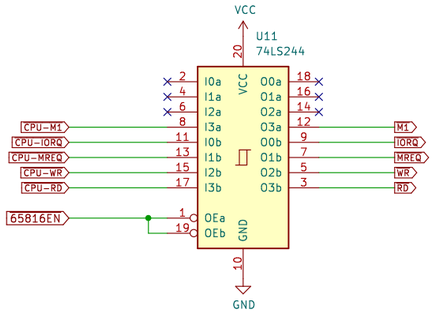
Z80 BUS INTERFACE

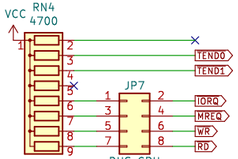


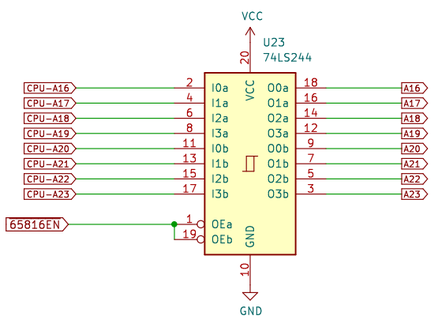


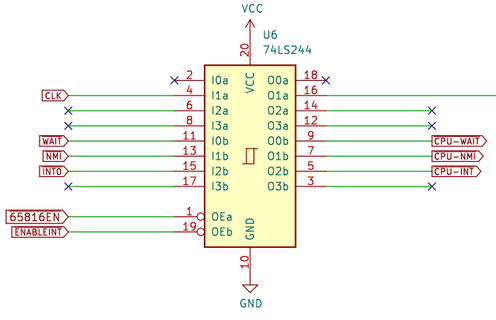


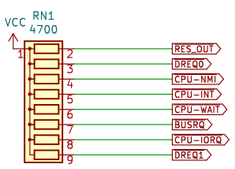








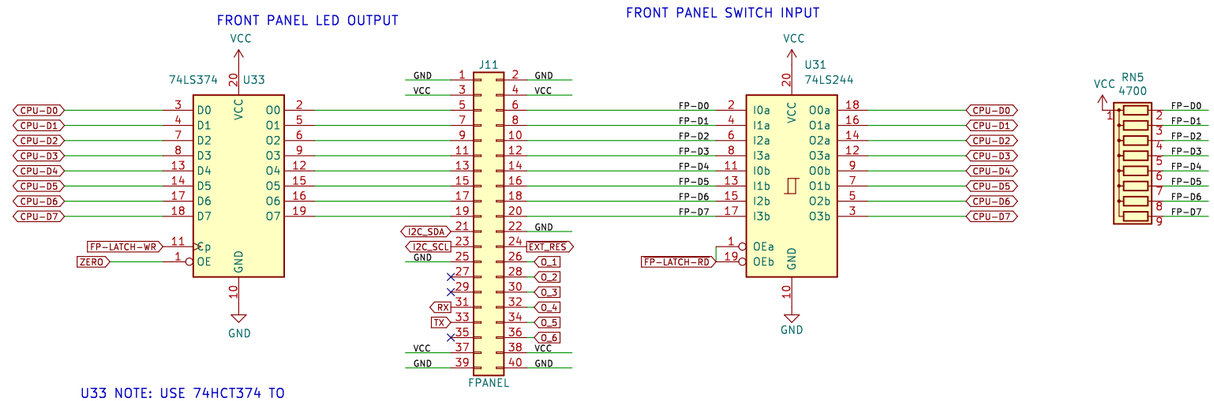




Sheet: /buffers/
File: buffers.kicad_sch

Title: Duodyne 65265 CPU board

Size: B	Date: 2025-04-12	**Rev: V0.5**
KiCad E.D.A. kicad (6.0.11)		Id: 6/9



U33 NOTE: USE 74HCT374 TO SOURCE OR SINK ADEQUATE CURRENT TO DRIVE LEDS ON FRONT PANEL

J11 NOTE:

PINS 5, 7, 9, 11, 13, 15, 17, 19 ARE FOR LED STATUS FOR ROMWBW FRONT PANEL INDICATOR

PINS 6, 8, 10, 12, 14, 16, 18, 20 ARE FOR SWITCH INPUTS FOR ROMWBW FRONT PANEL

PINS 21, 23 ARE FOR I2C CONNECTION (SDA & SCL)

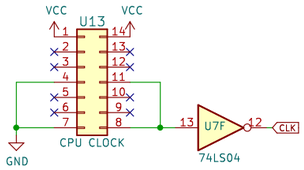
PINS 25, 27, 29, 31, 33, AND 35 ARE FOR TTL SERIAL CONNECTOR TO UART

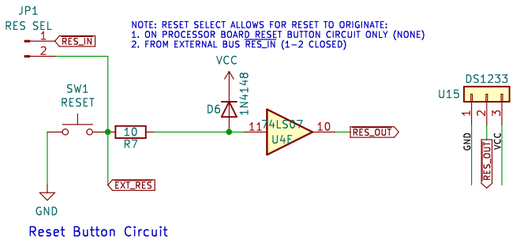
PINS 29, 37 ARE FOR SERIAL VCC POWER ENABLE

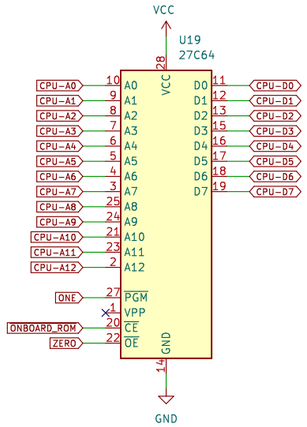
PINS 22, 24 ARE FOR EXTERNAL RESET SWITCH

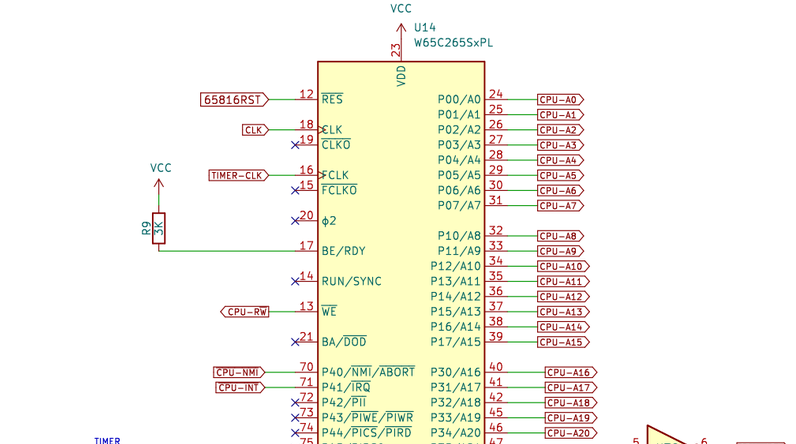
PINS 26, 28, 30, 32, 34, 36 are aux output bits from option register

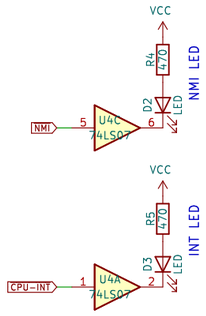
Sheet: /fpanel/		
File: fpanel.kicad_sch		
Title: Duodyne 65265 CPU board		
Size: B	Date: 2025-04-12	**Rev: V0.5**
KiCad E.D.A. kicad (6.0.11)		Id: 8/9









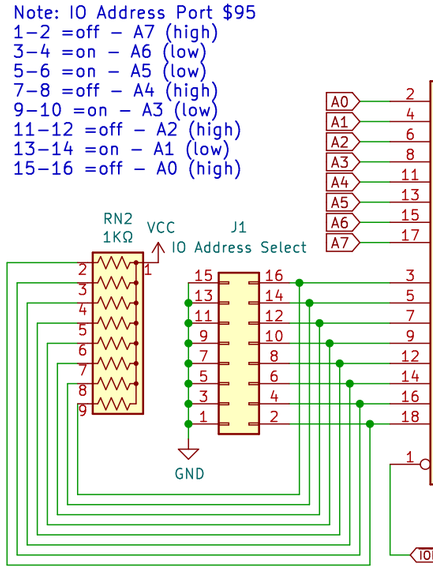


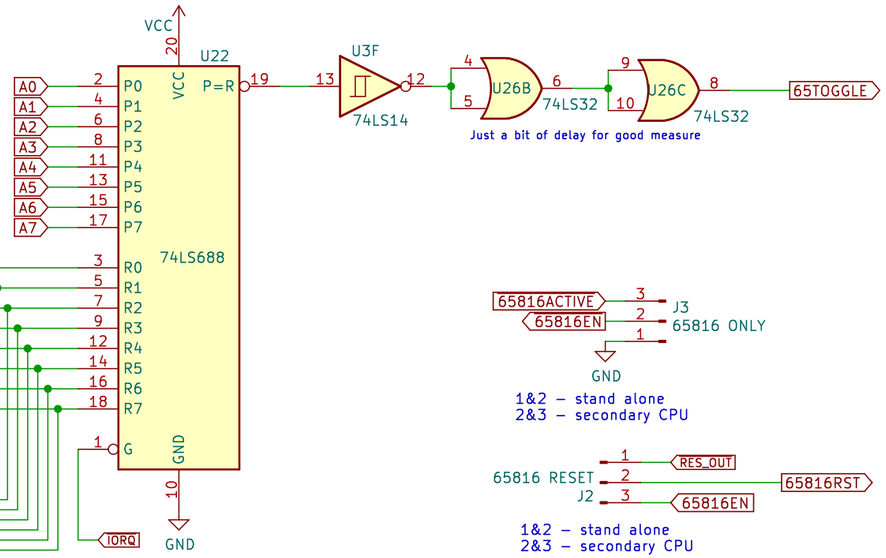
Sheet: /65816CPU/
File: 65816CPU.kicad_sch

Title: Duodyne 65265 CPU board

Size: USLedger	Date: 2025-04-12	**Rev: V0.5**
KiCad E.D.A. kicad (6.0.11)		Id: 9/9

Note: IO Address Port $95
1–2 =off – A7 (high)
3–4 =on – A6 (low)
5–6 =on – A5 (low)
7–8 =off – A4 (high)
9–10 =on – A3 (low)
11–12 =off – A2 (high)
13–14 =on – A1 (low)
15–16 =off – A0 (high)

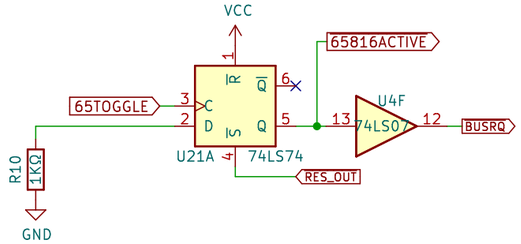


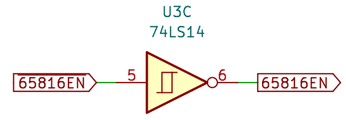


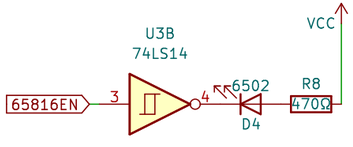
Just a bit of delay for good measure

1&2 – stand alone
2&3 – secondary CPU

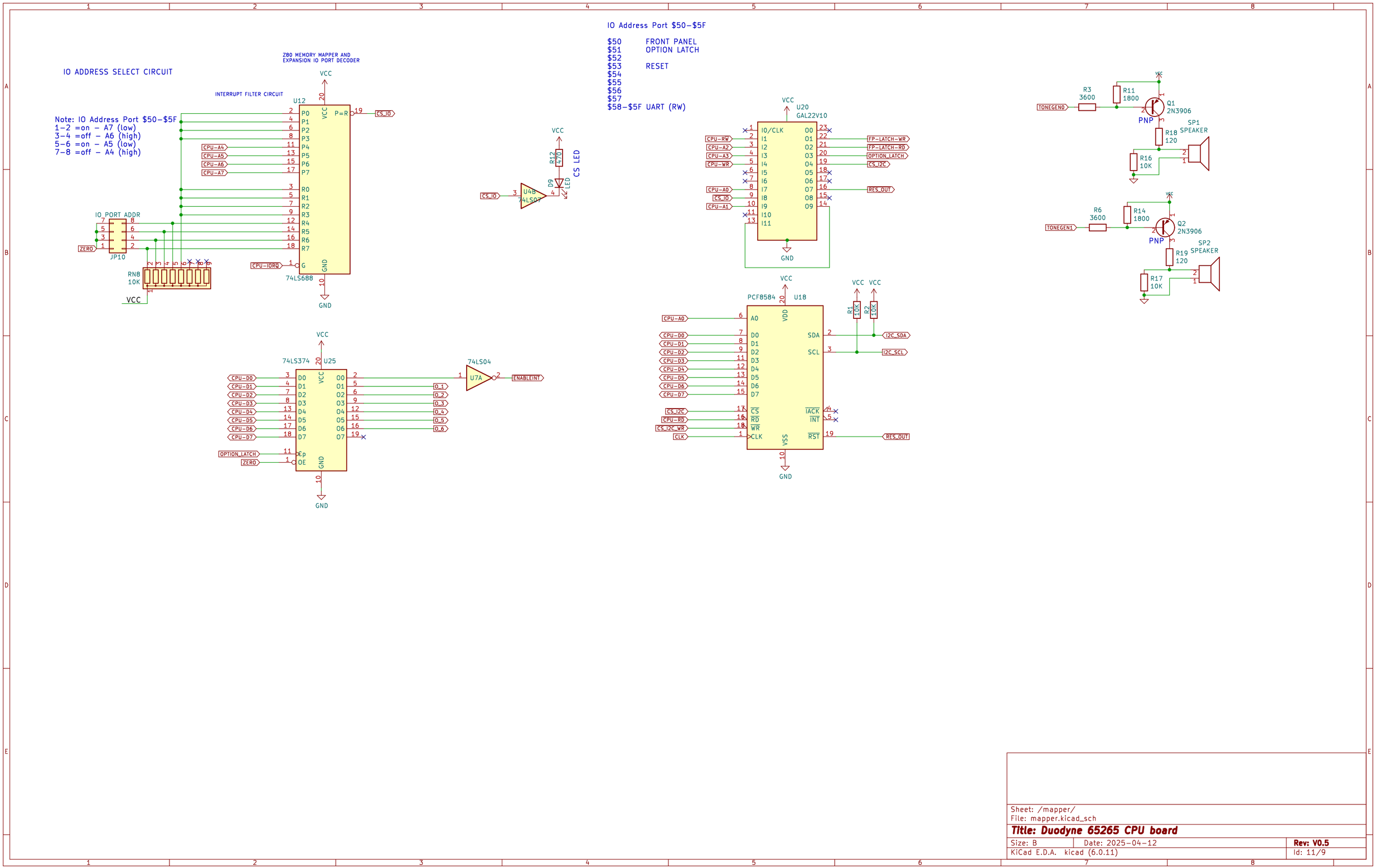
1&2 – stand alone
2&3 – secondary CPU







Sheet: /bus sharing/		
File: bussharing.kicad_sch		
Title: Duodyne 65265 CPU board		
Size: A4	Date: 2025–04–12	**Rev: V0.5**
KiCad E.D.A. kicad (6.0.11)		Id: 9/9


IO ADDRESS SELECT CIRCUIT
Z80 MEMORY MAPPER AND EXPANSION IO PORT DECODER
INTERRUPT FILTER CIRCUIT
Note: IO Address Port $50-$5F
1-2 =on - A7 (low)
3-4 =off - A6 (high)
5-6 =on - A5 (low)
7-8 =off - A4 (high)
IO Address Port $50-$5F
$50 FRONT PANEL
$51 OPTION LATCH
$52
$53 RESET
$54
$55
$56
$57
$58-$5F UART (RW)
U12
74LS688
IO_PORT_ADDR
JP10
RN8
10K
VCC
GND
CS_IO
CPU-IORQ
CPU-A4
CPU-A5
CPU-A6
CPU-A7
U4B
74LS07
R12
470
D9
LED
CS LED
U20
GAL22V10
IO/CLK
CPU-RW
CPU-A2
CPU-A3
CPU-WR
CPU-A0
CPU-A1
FP-LATCH-WR
FP-LATCH-RD
OPTION_LATCH
CS_I2C
RES_OUT
PCF8584
U18
CPU-D0
CPU-D1
CPU-D2
CPU-D3
CPU-D4
CPU-D5
CPU-D6
CPU-D7
CS_I2C
CPU-RD
CS_I2C_WR
CLK
SDA
SCL
IACK
INT
RST
R1
10K
R2
10K
I2C_SDA
I2C_SCL
74LS374
U25
74LS04
U7A
ENABLEINT
OPTION_LATCH
ZERO
R3
3600
R11
1800
Q1
2N3906
PNP
SP1
SPEAKER
R18
120
R16
10K
TONEGEN0
R6
3600
R14
1800
Q2
2N3906
SP2
SPEAKER
R19
120
R17
10K
TONEGEN1
Sheet: /mapper/
File: mapper.kicad_sch
Title: Duodyne 65265 CPU board
Size: B
Date: 2025-04-12
Rev: V0.5
KiCad E.D.A. kicad (6.0.11)
Id: 11/9