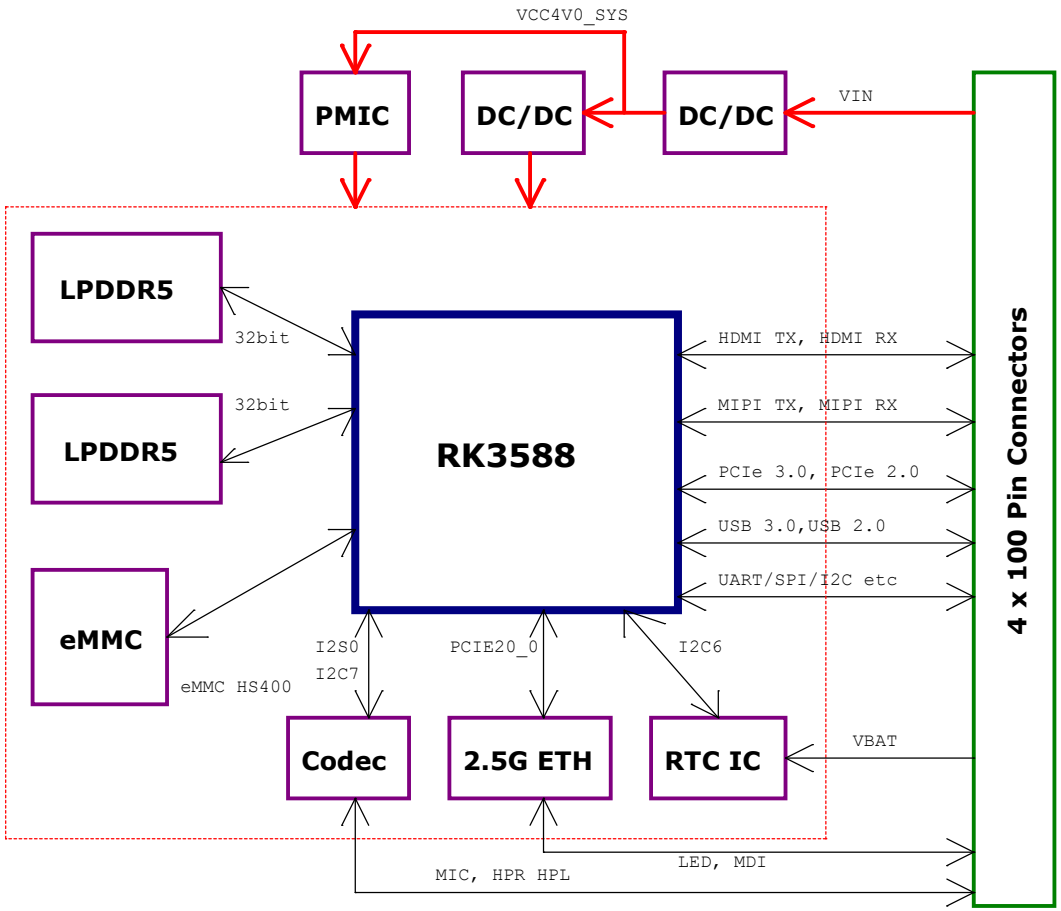
CM3588 Plus



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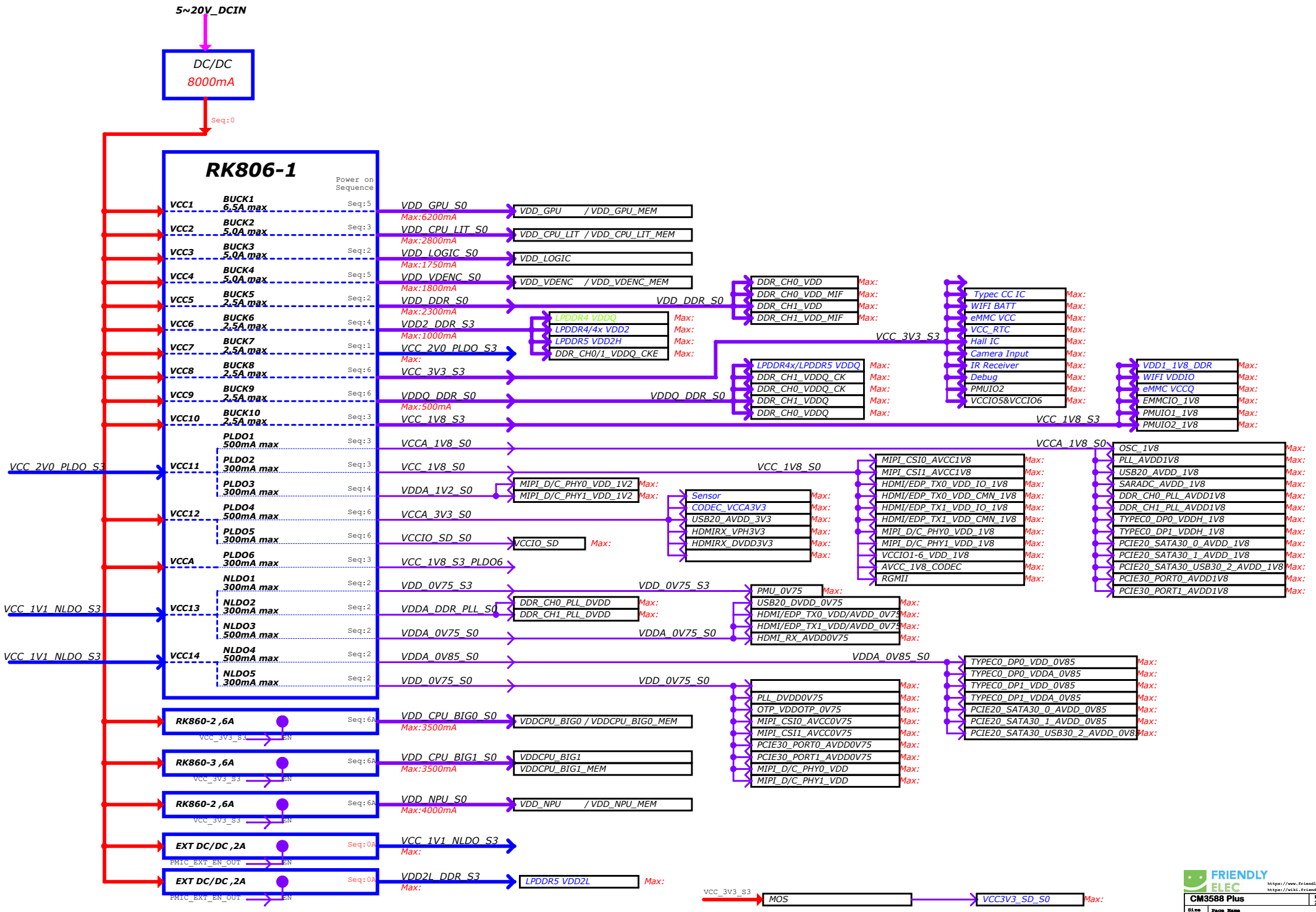
CM3588 Plus		Rev 2404
Size A3	Page Name 01.Block	
Date: Monday, May 20, 2024		Sheet: 1 / 26

Power Tree


5~20V_DCIN
DC/DC
8000mA
Seq:0
RK806-1
Power on Sequence
VCC1 BUCK1 6.5A max Seq:5
VCC2 BUCK2 5.0A max Seq:3
VCC3 BUCK3 5.0A max Seq:2
VCC4 BUCK4 5.0A max Seq:5
VCC5 BUCK5 2.5A max Seq:2
VCC6 BUCK6 2.5A max Seq:4
VCC7 BUCK7 2.5A max Seq:1
VCC8 BUCK8 2.5A max Seq:6
VCC9 BUCK9 2.5A max Seq:6
VCC10 BUCK10 2.5A max Seq:3
PLDO1 500mA max Seq:3
VCC11 PLDO2 300mA max Seq:3
PLDO3 300mA max Seq:4
VCC12 PLDO4 500mA max Seq:6
PLDO5 300mA max Seq:6
VCCA PLDO6 300mA max Seq:3
NLDO1 300mA max Seq:2
VCC13 NLDO2 300mA max Seq:2
NLDO3 500mA max Seq:2
VCC14 NLDO4 500mA max Seq:2
NLDO5 300mA max Seq:2
VCC_2V0_PLDO_S3
VCC_1V1_NLDO_S3
VCC_1V1_NLDO_S3
VDD_GPU_S0 Max:6200mA
VDD_GPU / VDD_GPU_MEM
VDD_CPU_LIT_S0 Max:2800mA
VDD_CPU_LIT / VDD_CPU_LIT_MEM
VDD_LOGIC_S0 Max:1750mA
VDD_LOGIC
VDD_VDENC_S0 Max:1800mA
VDD_VDENC / VDD_VDENC_MEM
VDD_DDR_S0 Max:2300mA
VDD2_DDR_S3 Max:1000mA
VCC_2V0_PLDO_S3 Max:
VCC_3V3_S3
VDDQ_DDR_S0 Max:500mA
VCC_1V8_S3
VCCA_1V8_S0
VCC_1V8_S0
VDDA_1V2_S0
VCCA_3V3_S0
VCCIO_SD_S0
VCCIO_SD Max:
VCC_1V8_S3_PLDO6
VDD_0V75_S3
VDDA_DDR_PLL_S0
VDDA_0V75_S0
VDDA_0V85_S0
VDD_0V75_S0
RK860-2 ,6A Seq:6A
VCC_3V3_S3 EN
VDD_CPU_BIG0_S0 Max:3500mA
VDDCPU_BIG0 / VDDCPU_BIG0_MEM
RK860-3 ,6A Seq:6A
VCC_3V3_S3 EN
VDD_CPU_BIG1_S0 Max:3500mA
VDDCPU_BIG1
VDDCPU_BIG1_MEM
RK860-2 ,6A Seq:6A
VCC_3V3_S3 EN
VDD_NPU_S0 Max:4000mA
VDD_NPU / VDD_NPU_MEM
EXT DC/DC ,2A Seq:0A
PMIC_EXT_EN_OUT EN
VCC_1V1_NLDO_S3 Max:
EXT DC/DC ,2A Seq:0A
PMIC_EXT_EN_OUT EN
VDD2L_DDR_S3 Max:
LPDDR5 VDD2L Max:
VDD_DDR_S0
DDR_CH0_VDD Max:
DDR_CH0_VDD_MIF Max:
DDR_CH1_VDD Max:
DDR_CH1_VDD_MIF Max:
LPDDR4 VDDQ Max:
LPDDR4/4x VDD2 Max:
LPDDR5 VDD2H Max:
DDR_CH0/1_VDDQ_CKE Max:
VDDQ_DDR_S0
LPDDR4x/LPDDR5 VDDQ Max:
DDR_CH1_VDDQ_CK Max:
DDR_CH0_VDDQ_CK Max:
DDR_CH1_VDDQ Max:
DDR_CH0_VDDQ Max:
VCC_3V3_S3
Typec CC IC Max:
WIFI BATT Max:
eMMC VCC Max:
VCC_RTC Max:
Hall IC Max:
Camera Input Max:
IR Receiver Max:
Debug Max:
PMUIO2 Max:
VCCIO5&VCCIO6 Max:
VCC_1V8_S3
VDD1_1V8_DDR Max:
WIFI VDDIO Max:
eMMC VCCQ Max:
EMMCIO_1V8 Max:
PMUIO1_1V8 Max:
PMUIO2_1V8 Max:
VCCA_1V8_S0
OSC_1V8 Max:
PLL_AVDD1V8 Max:
USB20_AVDD_1V8 Max:
SARADC_AVDD_1V8 Max:
DDR_CH0_PLL_AVDD1V8 Max:
DDR_CH1_PLL_AVDD1V8 Max:
TYPEC0_DP0_VDDH_1V8 Max:
TYPEC0_DP1_VDDH_1V8 Max:
PCIE20_SATA30_0_AVDD_1V8 Max:
PCIE20_SATA30_1_AVDD_1V8 Max:
PCIE20_SATA30_USB30_2_AVDD_1V8 Max:
PCIE30_PORT0_AVDD1V8 Max:
PCIE30_PORT1_AVDD1V8 Max:
VCC_1V8_S0
MIPI_D/C_PHY0_VDD_1V2 Max:
MIPI_D/C_PHY1_VDD_1V2 Max:
Sensor Max:
CODEC_VCCA3V3 Max:
USB20_AVDD_3V3 Max:
HDMIRX_VPH3V3 Max:
HDMIRX_DVDD3V3 Max:
MIPI_CSI0_AVCC1V8 Max:
MIPI_CSI1_AVCC1V8 Max:
HDMI/EDP_TX0_VDD_IO_1V8 Max:
HDMI/EDP_TX0_VDD_CMN_1V8 Max:
HDMI/EDP_TX1_VDD_IO_1V8 Max:
HDMI/EDP_TX1_VDD_CMN_1V8 Max:
MIPI_D/C_PHY0_VDD_1V8 Max:
MIPI_D/C_PHY1_VDD_1V8 Max:
VCCIO1-6_VDD_1V8 Max:
AVCC_1V8_CODEC Max:
RGMII Max:
VDD_0V75_S3
DDR_CH0_PLL_DVDD Max:
DDR_CH1_PLL_DVDD Max:
PMU_0V75 Max:
USB20_DVDD_0V75 Max:
HDMI/EDP_TX0_VDD/AVDD_0V75 Max:
HDMI/EDP_TX1_VDD/AVDD_0V75 Max:
HDMI_RX_AVDD0V75 Max:
VDDA_0V75_S0
PLL_DVDD0V75 Max:
OTP_VDDOTP_0V75 Max:
MIPI_CSI0_AVCC0V75 Max:
MIPI_CSI1_AVCC0V75 Max:
PCIE30_PORT0_AVDD0V75 Max:
PCIE30_PORT1_AVDD0V75 Max:
MIPI_D/C_PHY0_VDD Max:
MIPI_D/C_PHY1_VDD Max:
VDDA_0V85_S0
TYPEC0_DP0_VDD_0V85 Max:
TYPEC0_DP0_VDDA_0V85 Max:
TYPEC0_DP1_VDD_0V85 Max:
TYPEC0_DP1_VDDA_0V85 Max:
PCIE20_SATA30_0_AVDD_0V85 Max:
PCIE20_SATA30_1_AVDD_0V85 Max:
PCIE20_SATA30_USB30_2_AVDD_0V8 Max:
VCC_3V3_S3
MOS
VCC3V3_SD_S0 Max:
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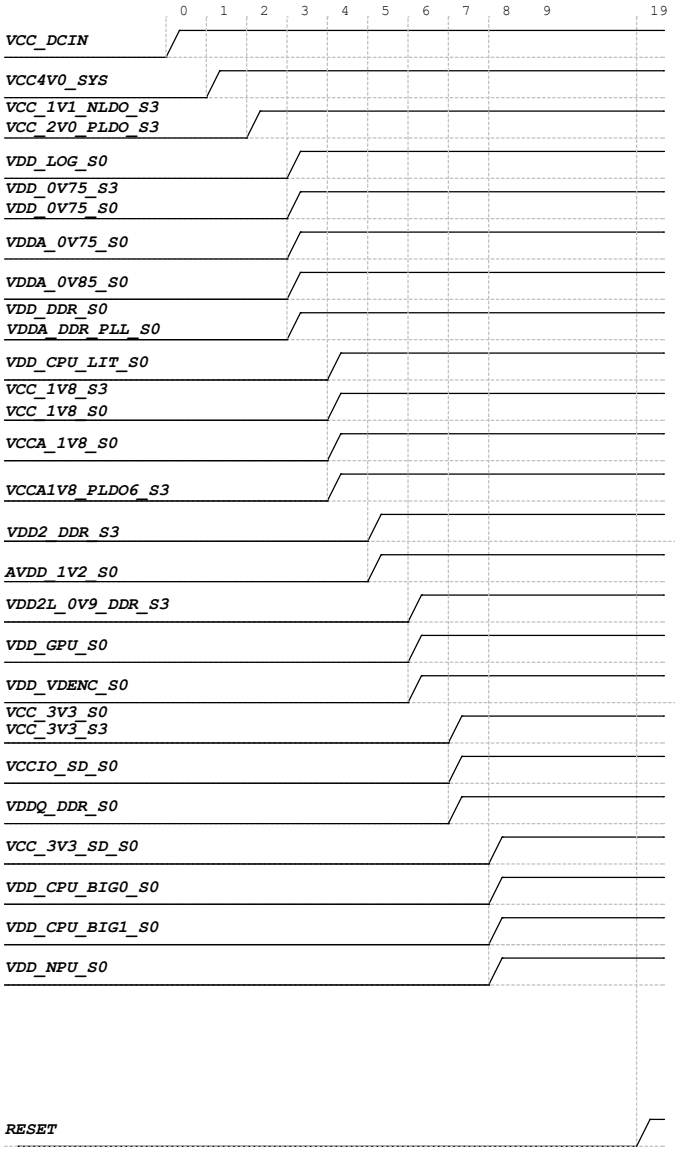
CM3588 Plus
Rev 2404
Size A2
Page Name 02.Power Tree
Date: Monday, May 20, 2024
Sheet: 2 / 26

Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC4V0_SYS	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO	RK806-1_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD

IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	IO Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3 VCC_3V3_S3	3.3V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin G20	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VCCIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_IO_SD	1.8V/3.3V
VCCIO3	Pin Y26	1.8V Only	VCCIO3_1V8	VCC_1V8_S0	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VCCIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_3V3_S3	3.3V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VCCIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_3V3_S0	3.3V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VCCIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	3.3V

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CM3588 Plus		Rev 2404
Size A3	Page Name 03.System Power Sequence	
Date: Monday, May 20, 2024		Sheet: 3 / 26

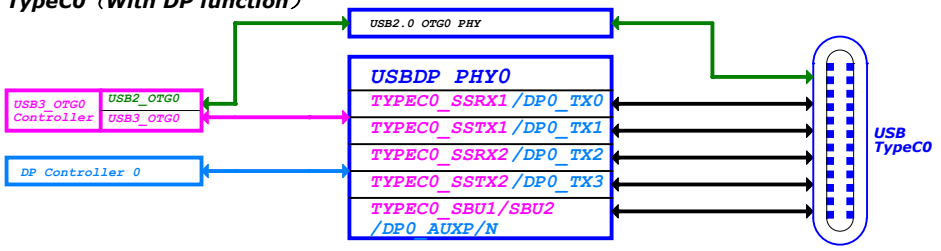
USB Controller Configure Table

Controller Name	Pin Name	Type-C Function	DPx4Lane Function		USB30 OTG+DPx2Lane Function		USB20 OTG+DPx2Lane Function		USB20 OTG+DPx4Lane Function	
			OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2	OPTION1	OPTION2
USB30 OTG0 Device or Host	TYPEC0_SBU1/DP0_AUXP TYPEC0_SBU2/DP0_AUXN	TYPEC0_SBU1 TYPEC0_SBU2	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN	DP0_AUXP DP0_AUXN
	TYPEC0_SSRX1P/DP0_TX0P TYPEC0_SSRX1N/DP0_TX0N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX1P TYPEC0_SSRX1N	DP0_TX0P DP0_TX0N	DP0_TX0P DP0_TX0N		DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N
	TYPEC0_SSTX1P/DP0_TX1P TYPEC0_SSTX1M/DP0_TX1M	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX1P TYPEC0_SSTX1N	DP0_TX1P DP0_TX1N	DP0_TX1P DP0_TX1N		DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N
	TYPEC0_SSRX2P/DP0_TX2P TYPEC0_SSRX2N/DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N	DP0_TX2P DP0_TX2N	TYPEC0_SSRX2P TYPEC0_SSRX2N		DP0_TX2P DP0_TX2N	DP0_TX2P DP0_TX2N	DP0_TX0P DP0_TX0N
	TYPEC0_SSTX2P/DP0_TX3P TYPEC0_SSTX2N/DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N	DP0_TX3P DP0_TX3N	TYPEC0_SSTX2P TYPEC0_SSTX2N		DP0_TX3P DP0_TX3N	DP0_TX3P DP0_TX3N	DP0_TX1P DP0_TX1N
USB20 OTG0 Device or Host	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM			TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM	TYPEC0_USB20_OTG_DP TYPEC0_USB20_OTG_DM
USB30 OTG1 Device or Host	TYPEC1_SBU1/DP1_AUXP TYPEC1_SBU2/DP1_AUXN	TYPEC1_SBU1 TYPEC1_SBU2	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN	DP1_AUXP DP1_AUXN
	TYPEC1_SSRX1P/DP1_TX0P TYPEC1_SSRX1N/DP1_TX0N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX1P TYPEC1_SSRX1N	DP1_TX0P DP1_TX0N	DP1_TX0P DP1_TX0N		DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N
	TYPEC1_SSTX1P/DP1_TX1P TYPEC1_SSTX1M/DP1_TX1M	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX1P TYPEC1_SSTX1N	DP1_TX1P DP1_TX1N	DP1_TX1P DP1_TX1N		DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N
	TYPEC1_SSRX2P/DP1_TX2P TYPEC1_SSRX2N/DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N	DP1_TX2P DP1_TX2N	TYPEC1_SSRX2P TYPEC1_SSRX2N		DP1_TX2P DP1_TX2N	DP1_TX2P DP1_TX2N	DP1_TX0P DP1_TX0N
	TYPEC1_SSTX2P/DP1_TX3P TYPEC1_SSTX2N/DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N	DP1_TX3P DP1_TX3N	TYPEC1_SSTX2P TYPEC1_SSTX2N		DP1_TX3P DP1_TX3N	DP1_TX3P DP1_TX3N	DP1_TX1P DP1_TX1N
USB20 OTG1 Device or Host	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM			TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM	TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM

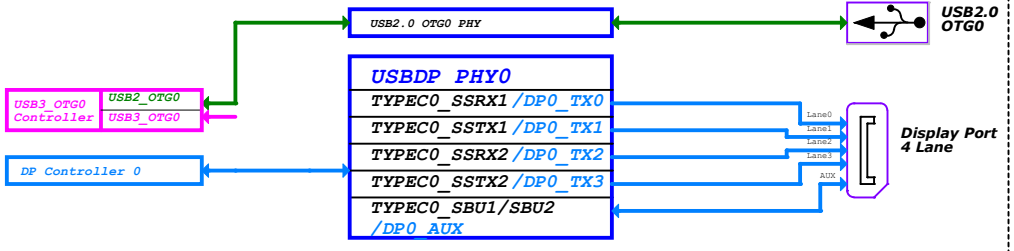
			OPTION1 USB30 HOST	OPTION2 USB30 HOST	OPTION3 USB30 HOST
USB30 HOST2	PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN		USB30_2_SSTXP USB30_2_SSTXN	USB30_2_SSTXP USB30_2_SSTXN	USB30_2_SSTXP USB30_2_SSTXN
	PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN		USB30_2_SSRXP USB30_2_SSRXN	USB30_2_SSRXP USB30_2_SSRXN	USB30_2_SSRXP USB30_2_SSRXN
USB20 HOST0	USB20_HOST0_DP USB20_HOST0_DM		USB20_HOST0_DP USB20_HOST0_DM		
USB20 HOST1	USB20_HOST1_DP USB20_HOST1_DM			USB20_HOST1_DP USB20_HOST1_DM	
					TYPEC1_USB20_OTG_DP TYPEC1_USB20_OTG_DM

Note:
DP Lane swap enable
0:Lane0/1/2/3 TxData mapping to Lane0/1/2/3 TXDP/N
1:Lane0/1/2/3 TxData mapping to Lane2/3/0/1 TXDP/N

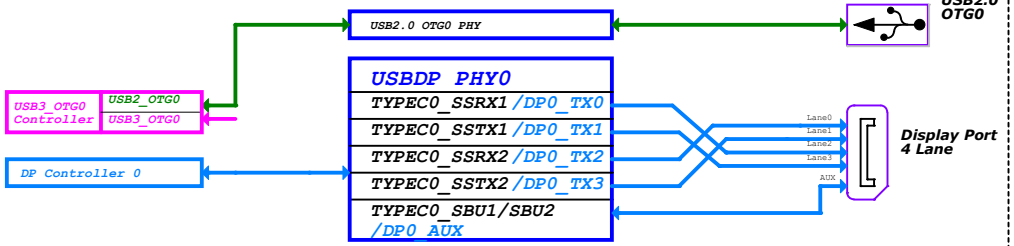
Config0:
TypeC0（With DP function）



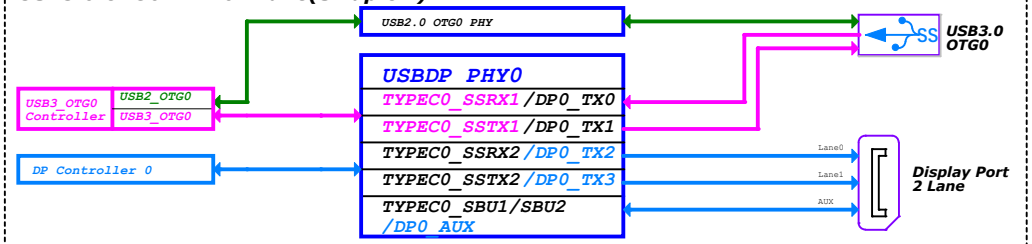
Config1:
USB2.0 OTG0 + DP0 4Lane(Swap OFF)



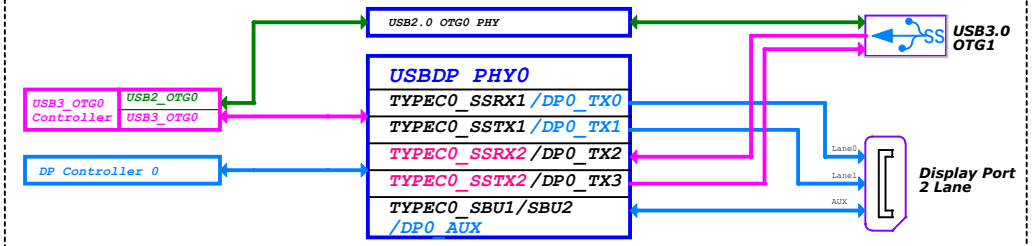
Config2:
USB2.0 OTG0 + DP0 4Lane(Swap ON)



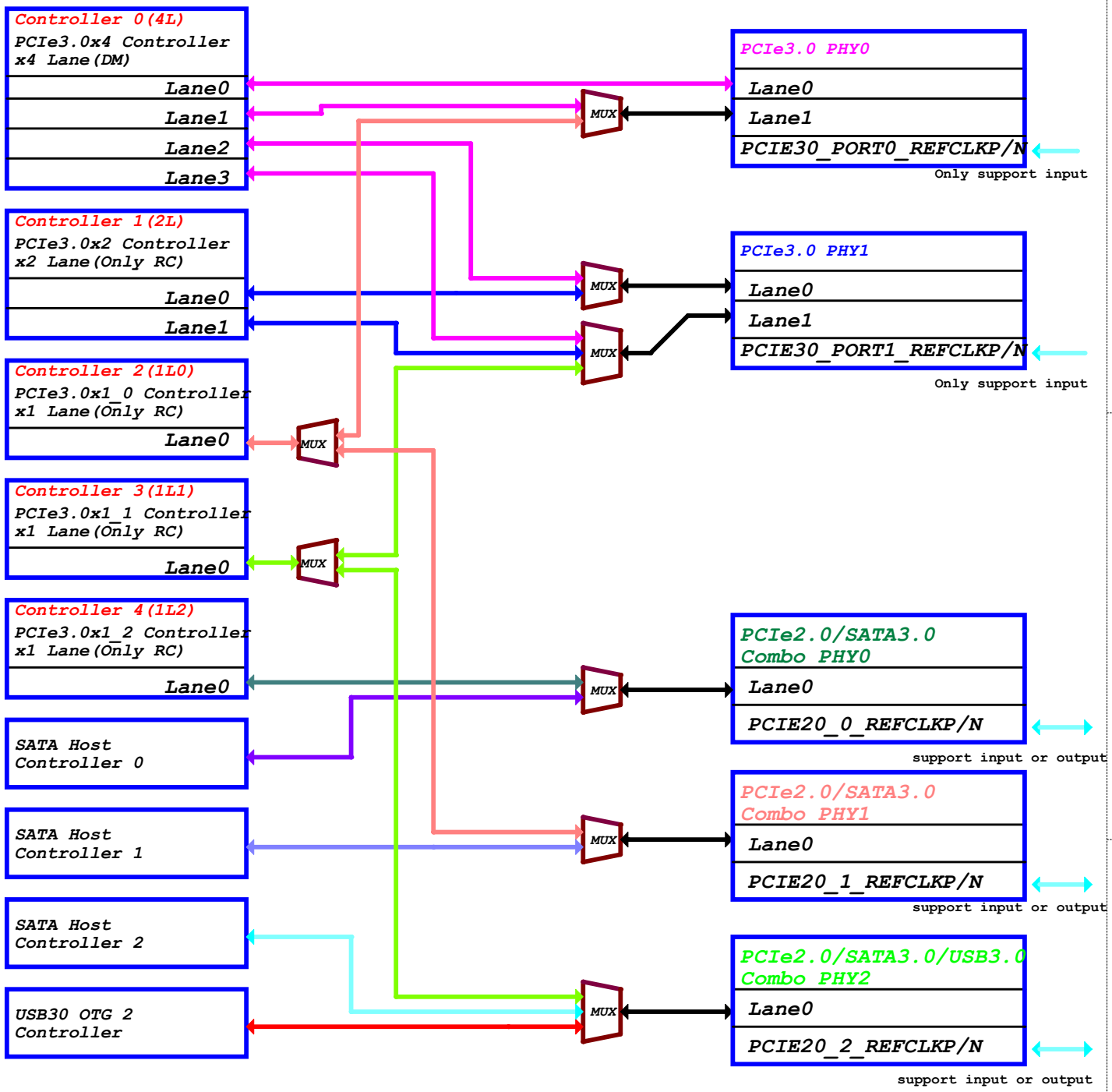
Config3:(Default)
USB3.0 OTG0 + DP0 2Lane(Swap ON)



Config4:
USB3.0 OTG0 + DP0 2Lane(Swap OFF)



PCIe/SATA Connecter Diagram



PCIe Controller Configure Table

Controller Name	Data & Clk Lane Configure			Control GPIO
	OPTION	CLK LANE	DATA LANE	
PCIE30X4 RC & EP	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0	PCIE30X4_CLKREQ_M* PCIE30X4_WAKEN_M* PCIE30X4_PERSTN_M* PCIE30X4_BUTTON_RSTN
	OPTION2	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT0_RX0 PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	
	OPTION3	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT0_TX0 PCIE30_PORT1_TX0 PCIE30_PORT0_RX0 PCIE30_PORT1_RX0 PCIE30_PORT0_TX1 PCIE30_PORT1_TX1 PCIE30_PORT0_RX1 PCIE30_PORT1_RX1	
PCIE30X2 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0	PCIE30X2_CLKREQ_M* PCIE30X2_WAKEN_M* PCIE30X2_PERSTN_M* PCIE30X2_BUTTON_RSTN
	OPTION2	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX0 PCIE30_PORT1_RX0 PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	
PCIE30X1_0 RC	OPTION1	PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN	PCIE30_PORT0_TX1 PCIE30_PORT0_RX1	PCIE30X1_0_CLKREQ_M* PCIE30X1_0_WAKEN_M* PCIE30X1_0_PERSTN_M* PCIE30X1_0_BUTTON_RSTN
	OPTION2	PCIE20_1_REFCLKP PCIE20_1_REFCLKN	PCIE20_1_TXP PCIE20_1_RXP PCIE20_1_TXN PCIE20_1_RXN	
PCIE30X1_1 RC	OPTION1	PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN	PCIE30_PORT1_TX1 PCIE30_PORT1_RX1	PCIE30X1_1_CLKREQ_M* PCIE30X1_1_WAKEN_M* PCIE30X1_1_PERSTN_M* PCIE30X1_1_BUTTON_RSTN
	OPTION2	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TXP PCIE20_2_RXP PCIE20_2_TXN PCIE20_2_RXN	
PCIE20X1_2 RC	OPTION1	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TXP PCIE20_0_RXP PCIE20_0_TXN PCIE20_0_RXN	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

Note:
PCIE30_PORT*_REF_CLKP/N is input gpio

PCIE20_*_REFCLKP/N is output or input gpio

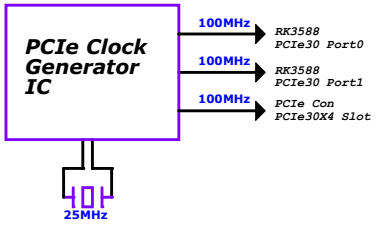
Note:
M*=Mean to M0 or M1,It's the same source,Just multiplex to M0 or M1, So,Only use one at the same time.

PCIe/SATA Function Combination

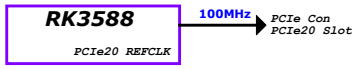
Function Combination

Function Item	PCIEX4	PCIEX2	PCIEX1	SATA
Option1	1(DM)	0	3(RC)	0
Option2	1(DM)	0	2(RC)	1
Option3	1(DM)	0	1(RC)	2
Option4	1(DM)	0	0	3
Option5	0	1(DM)+1(RC)	3(RC)	0
Option6	0	1(DM)+1(RC)	2(RC)	1
Option7	0	1(DM)+1(RC)	1(RC)	2
Option8	0	1(DM)+1(RC)	0	3
Option9	0	1(DM)	4(RC)	1
Option10	0	1(DM)	3(RC)	2
Option11	0	1(DM)	2(RC)	3
Option12	0	0	1(DM)+4(RC)	2
Option13	0	0	1(DM)+3(RC)	3

PCIe3.0 REFCLK



PCIe2.0 REFCLK



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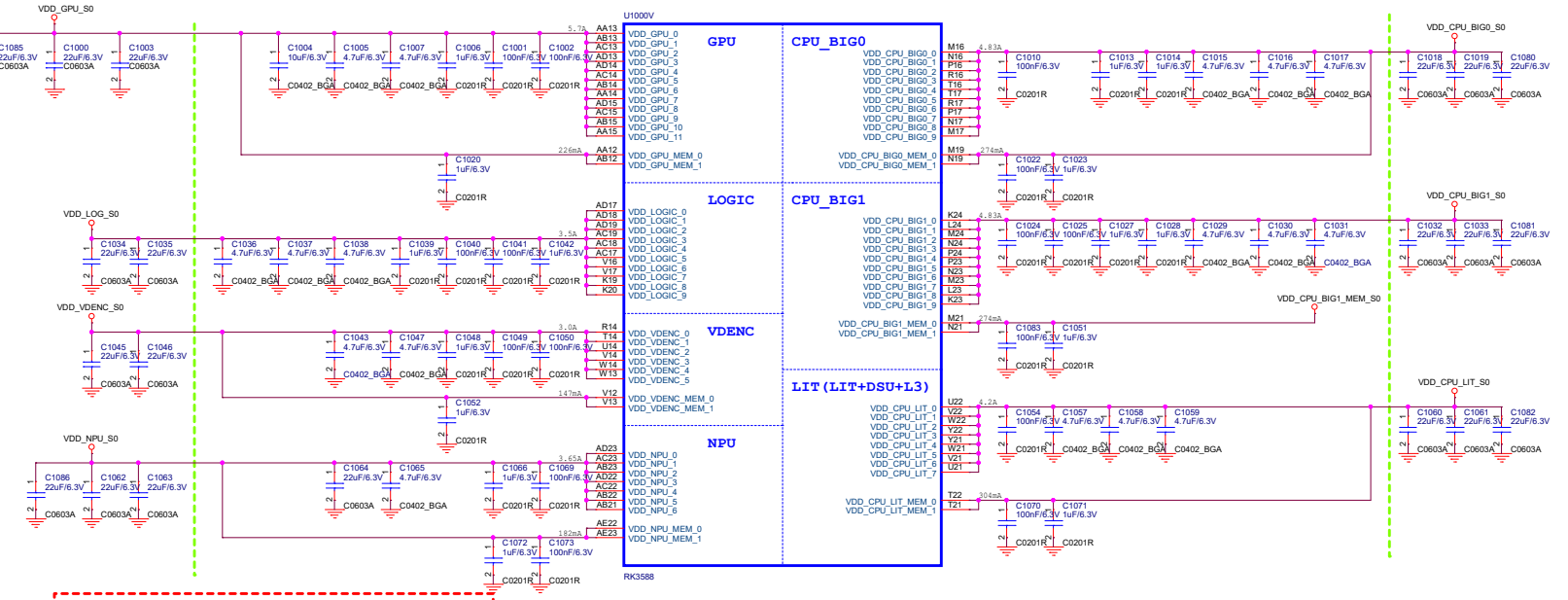
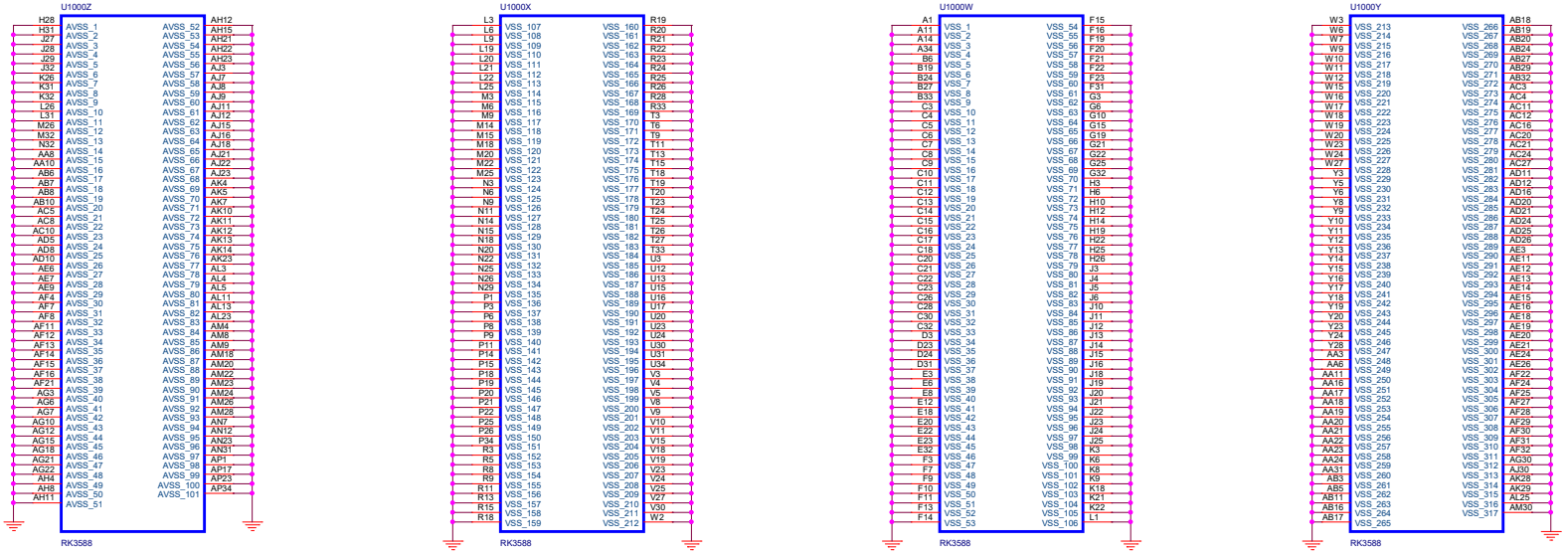
CM3588 Plus		Rev 2404
Size A2	Page Name 05.PCIE Fun Map	
Date: Monday, May 20, 2024		Sheet: 5 / 26

RK3588_V(POWER)



Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package



Size	Page Name	Rev	
A2	06.RK3588_Power/GND	2404	
Date: Monday, May 20, 2024		Sheet: 6 / 26	

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CM3588 Plus

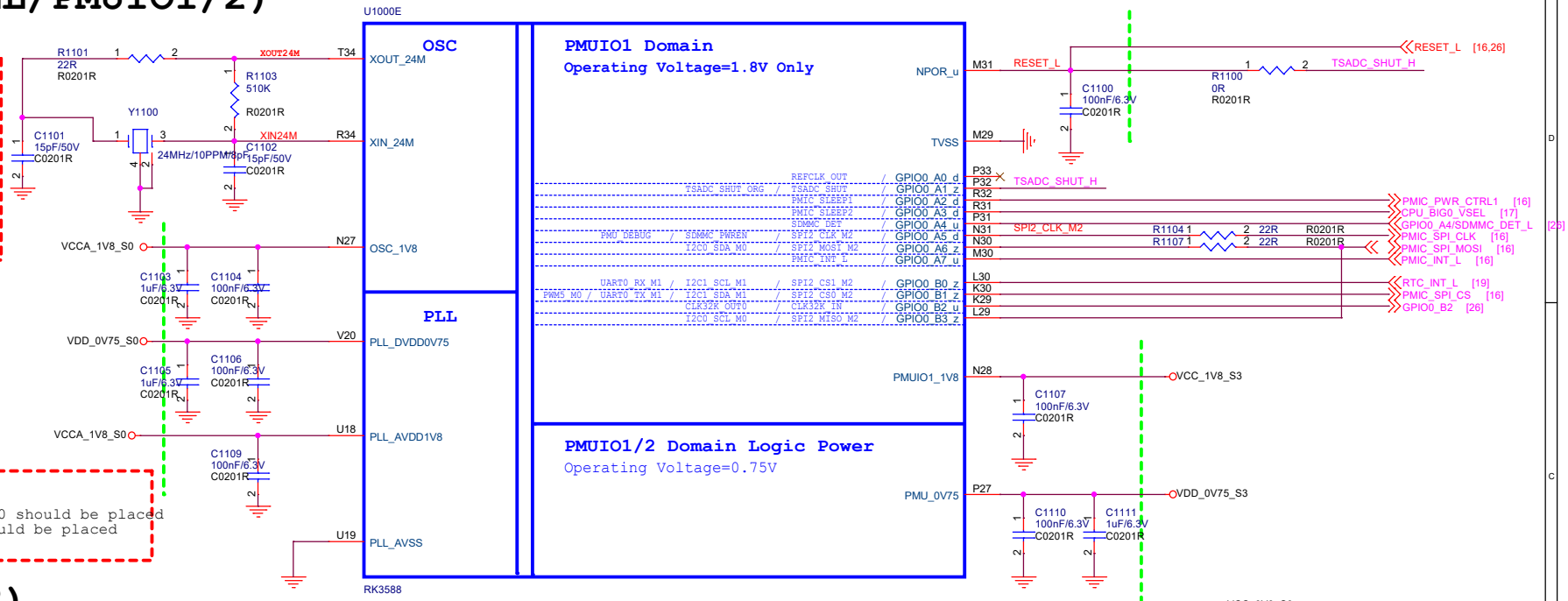
RK3588_E(OSC/PLL/PMUIO1/2)

Note:
Adjusted the load capacitance according to the crystal specification

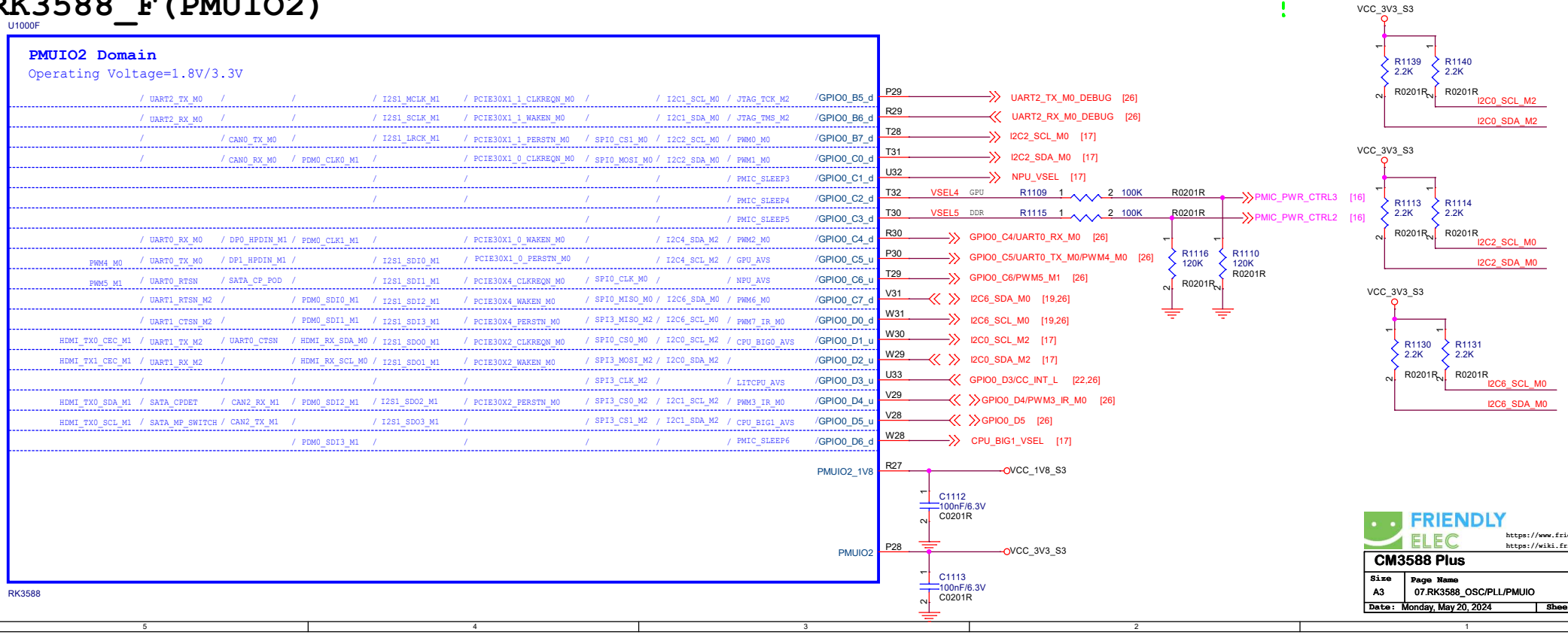
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF

Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package



RK3588_F(PMUIO2)



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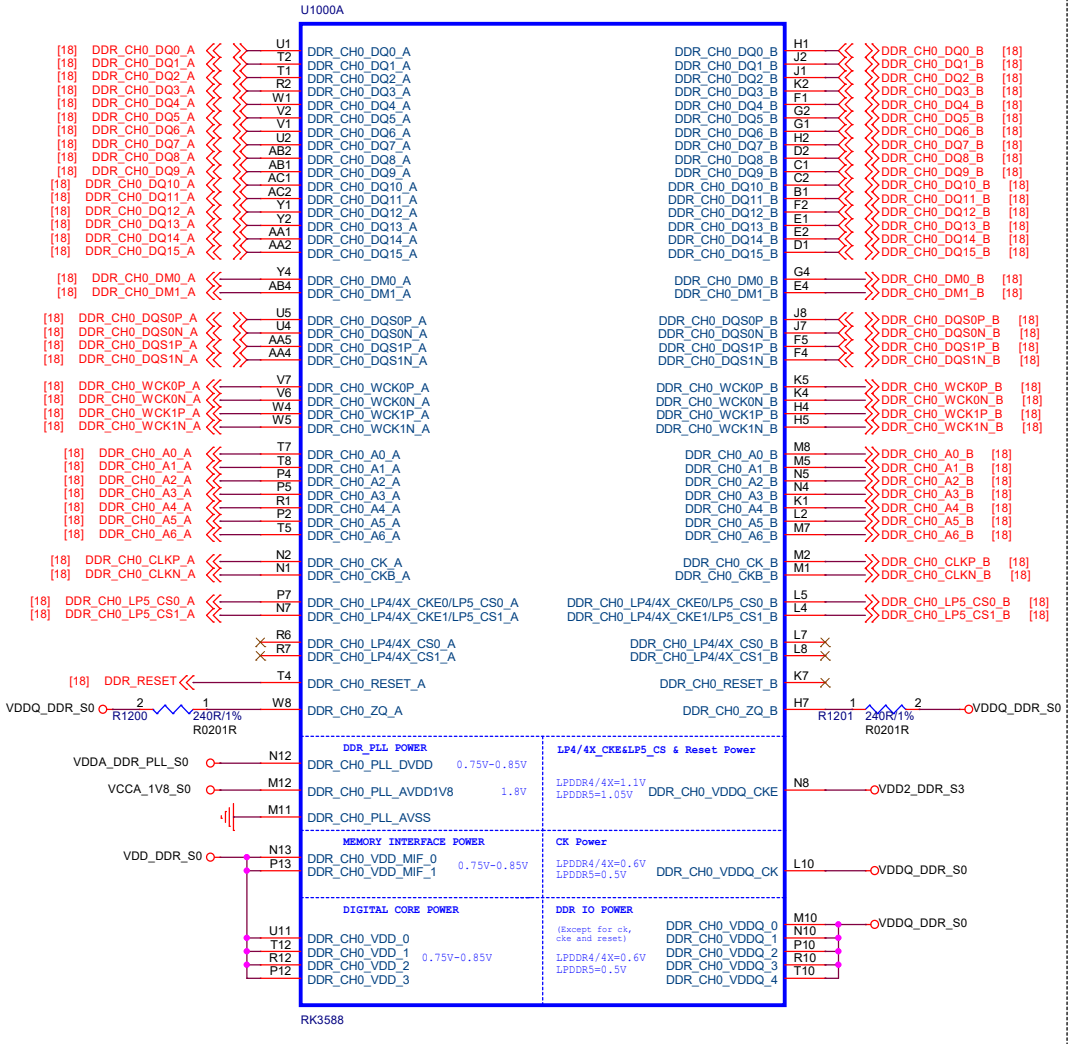
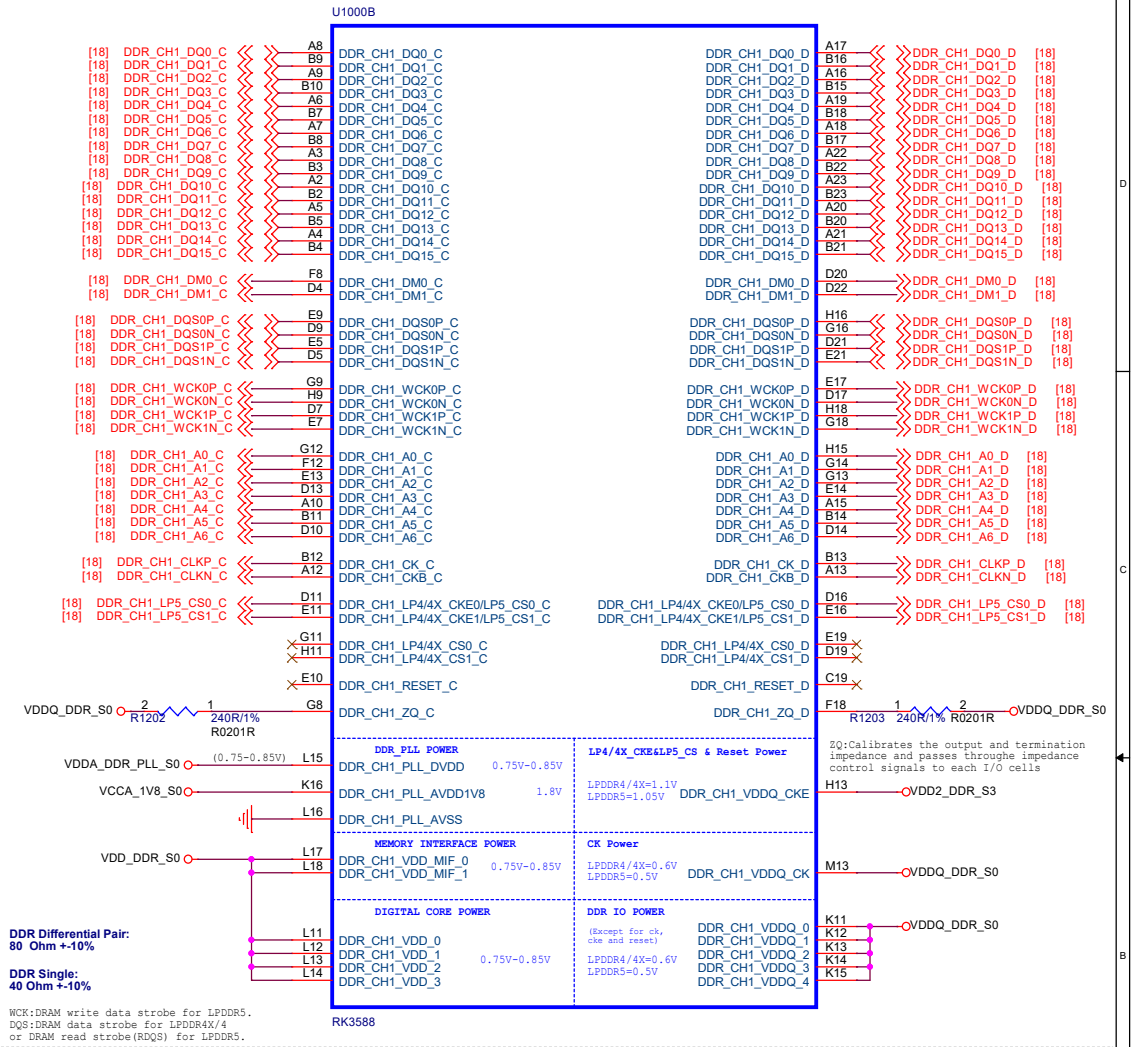
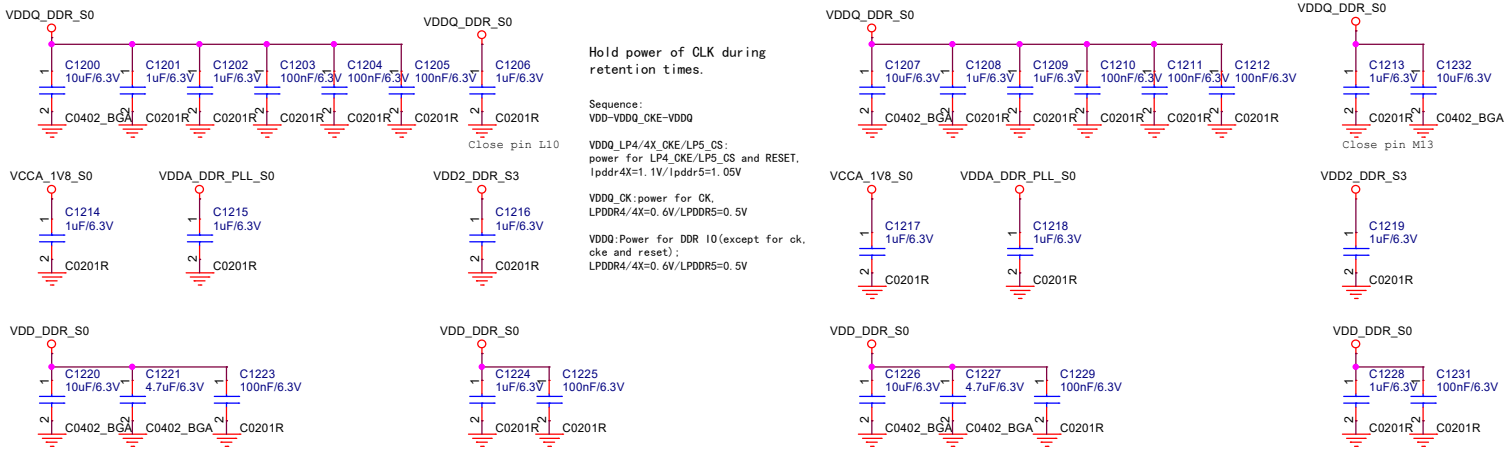
CM3588 Plus	Rev 2404
Size A3	Page Name 07.RK3588_OSC/PLL/PMUIO
Date: Monday, May 20, 2024	Sheet: 7 / 26





DDR FILTER



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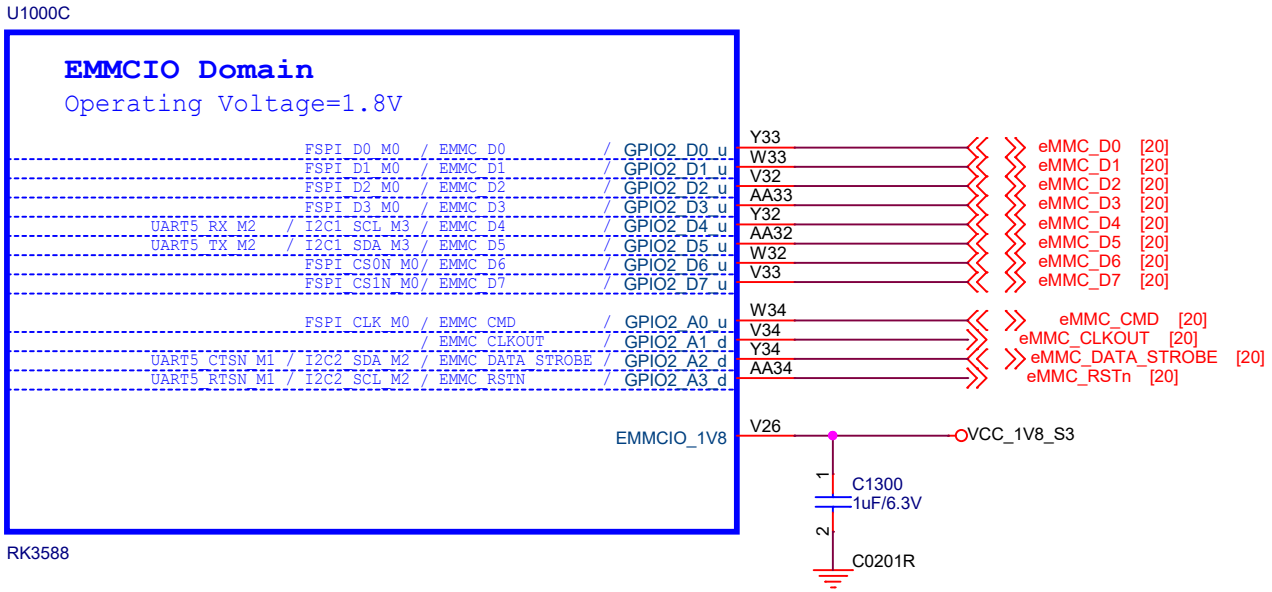
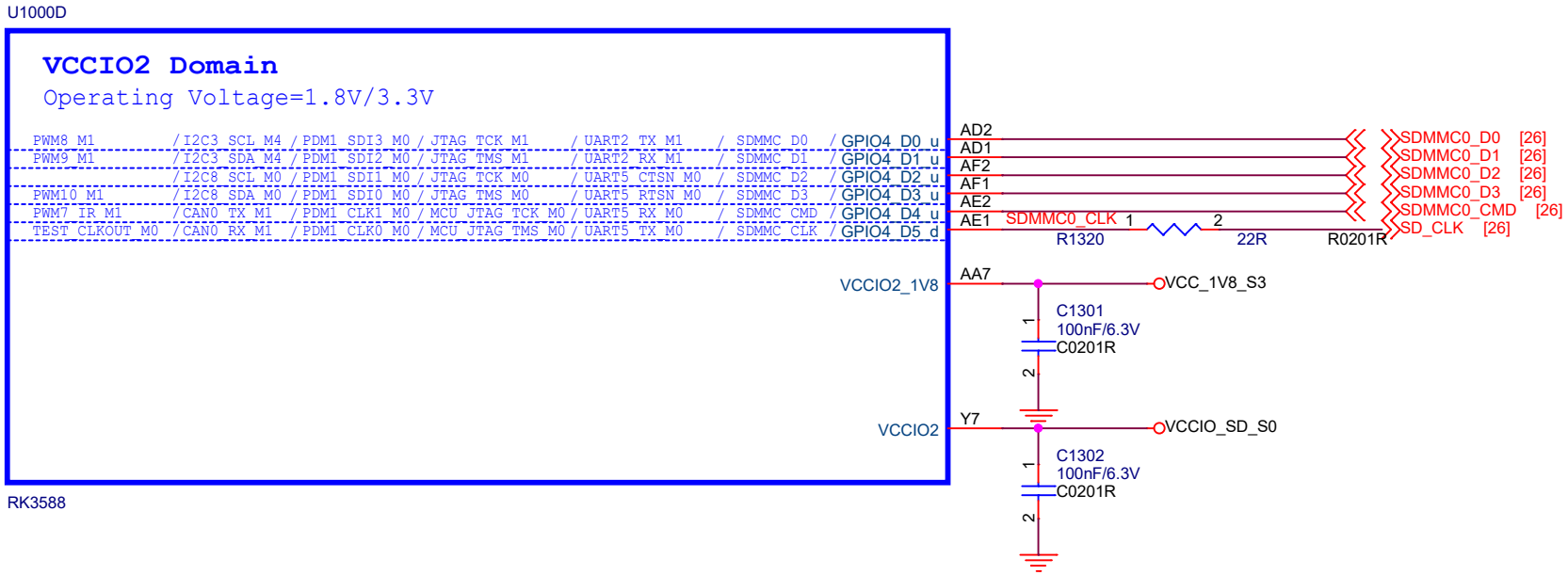
CM3588 Plus		Rev 2404
Size A3	Page Name 08.RK3588 DDR Controler	
Date: Monday, May 20, 2024		Sheet: 8 / 26

RK3588_C(EMMCIO Domain)



RK3588_D(VCCIO2 Domain)



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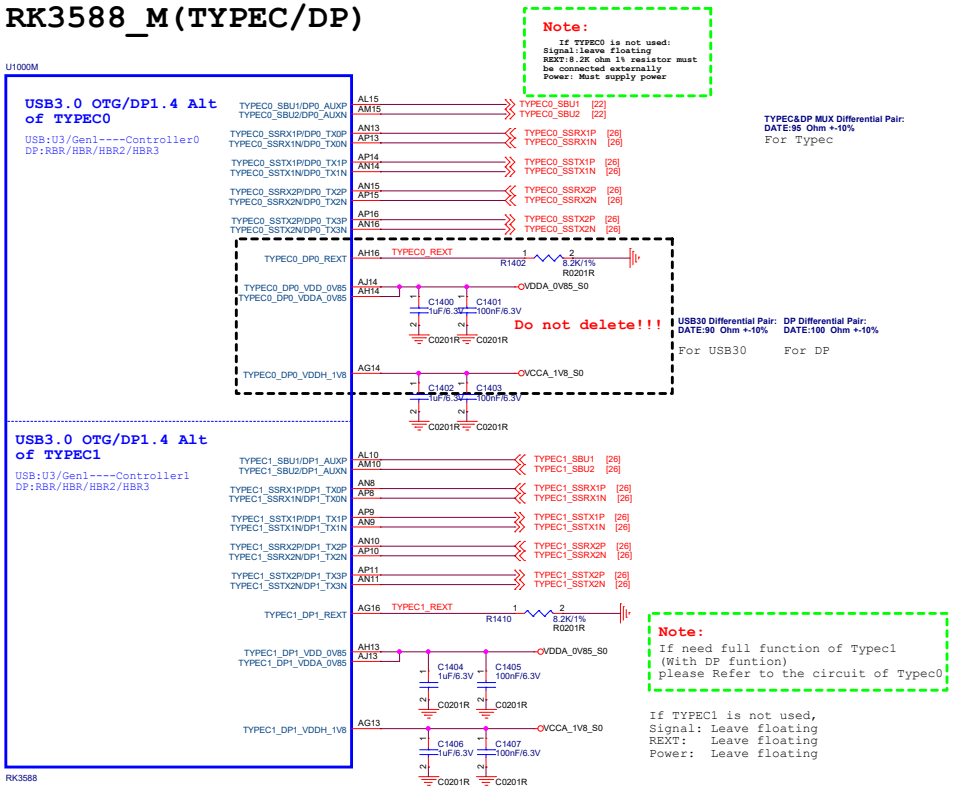
CM3588 Plus		Rev 2404
Size A4	Page Name 09.RK3588_Flash/SD Controller	
Date: Monday, May 20, 2024		Sheet: 9 / 26

RK3588_M(TYPEC/DP)



Note:
If TYPEC0 is not used:
Signal:leave floating
REXT:8.2K ohm 1% resistor must be connected externally
Power: Must supply power

TYPEC&DP MUX Differential Pair: DATE:95 Ohm +-10%
For Typec

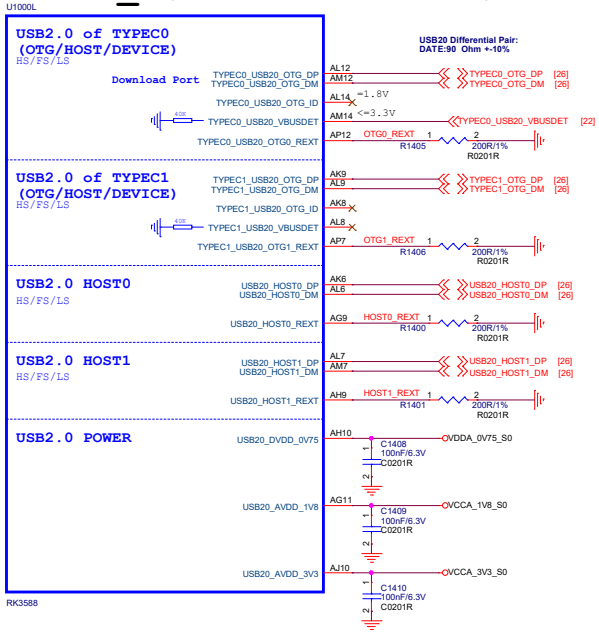
Note:
If need full function of Typec1
(With DP funtion)
please Refer to the circuit of Typec0

If TYPEC1 is not used,
Signal: Leave floating
REXT: Leave floating
Power: Leave floating

USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*DP_TX_Lane0-3*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1* *DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3* *DP:Lane0 Lane1*

RK3588_L(USB2.0 HOST/OTG)



Note:
TYPEC0_USB20_OTG:
DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

TYPEC1_USB20_OTG:
If not used:
DP/DM:Leave floating
ID:Leave floating
VBUSDET:Leave floating
REXT:Leave floating

USB20_HOST0/USB20_HOST1:
If not used:
DP/DM:Leave floating
REXT:Leave floating

Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

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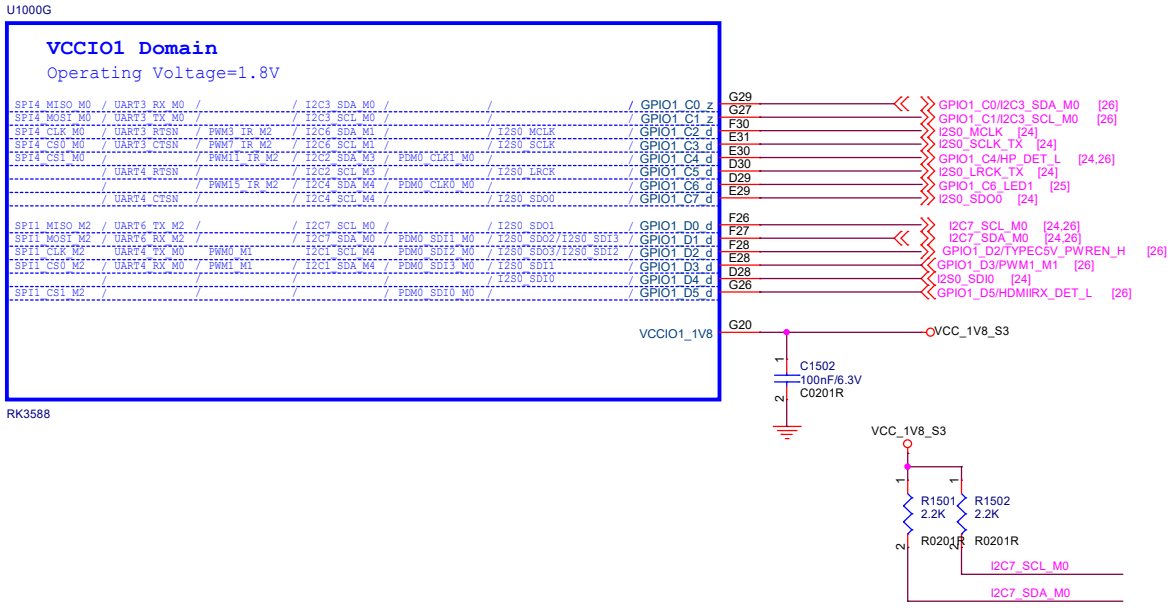
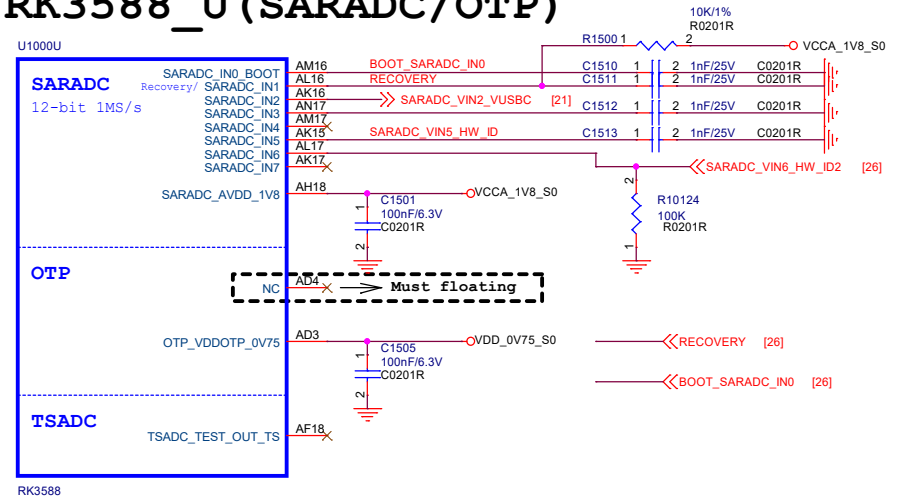
CM3588 Plus		Rev 2404
Size A2	Page Name 10.RK3588_USB30/USB20_Ctrl	
Date: Monday, May 20, 2024	Sheet: 10/ 26	

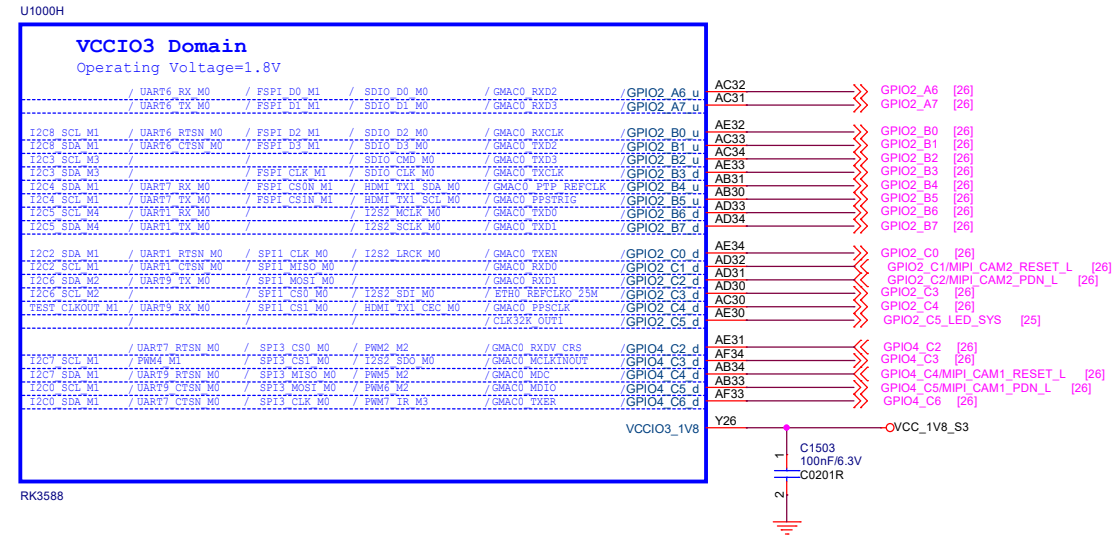
RK3588_G(VCCIO1 Domain)



RK3588_U(SARADC/OTP)



RK3588_H(VCCIO3 Domain)



BOOT MODE CONFIG

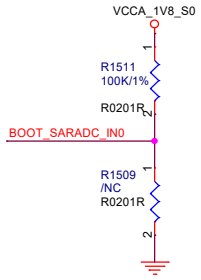
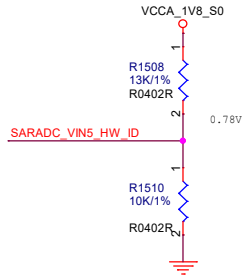


TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	DNP	100K	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

BOARD ID CONFIG



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CM3588 Plus		Rev 2404
Size A3	Page Name 11.RK3588_SARADC/1.8V Only GPIO	
Date: Monday, May 20, 2024	Sheet: 11/ 26	

RK3588_Q/R(MIPI_D/C_PHY0/1)

U1000Q

MIPI DPHY Differential Pair:
100 Ohm +-10%

MIPI CPHY Single:
50 Ohm +-10%

MIPI D/C-PHY DSI_TX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C	AN26	MIPI_DPHY0_TX_CLKP [26]
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B	AP26	MIPI_DPHY0_TX_CLKN [26]
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B	AN24	MIPI_DPHY0_TX_D0P [26]
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A	AP24	MIPI_DPHY0_TX_D0N [26]
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A	AN25	MIPI_DPHY0_TX_D1P [26]
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C	AP25	MIPI_DPHY0_TX_D1N [26]
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B	AN27	MIPI_DPHY0_TX_D2P [26]
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A	AP27	MIPI_DPHY0_TX_D2N [26]
MIPI_DPHY0_TX_D3P/NO_USE	AN28	MIPI_DPHY0_TX_D3P [26]
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C	AP28	MIPI_DPHY0_TX_D3N [26]

MIPI D/C-PHY CSI_RX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C	AN32	MIPI_DPHY0_RX_CLKP [26]
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B	AP31	MIPI_DPHY0_RX_CLKN [26]
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B	AN29	MIPI_DPHY0_RX_D0P [26]
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A	AP29	MIPI_DPHY0_RX_D0N [26]
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A	AN30	MIPI_DPHY0_RX_D1P [26]
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C	AP30	MIPI_DPHY0_RX_D1N [26]
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B	AN33	MIPI_DPHY0_RX_D2P [26]
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A	AP32	MIPI_DPHY0_RX_D2N [26]
MIPI_DPHY0_RX_D3P/NO_USE	AN34	MIPI_DPHY0_RX_D3P [26]
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C	AP33	MIPI_DPHY0_RX_D3N [26]

MIPI D/C-PHY POWER

MIPI_D/C_PHY0_VREG	AF20	C1600 1uF/6.3V	C0201R
MIPI_D/C_PHY0_VDD	AG20	C1602 100nF/6.3V, C1601 1uF/6.3V	VDD_0V75_S0
MIPI_D/C_PHY0_VDD_1V2	AH20	C1603 1uF/6.3V	VDDA_1V2_S0
MIPI_D/C_PHY0_VDD_1V8	AJ20	C1605 1uF/6.3V	VCCA1V8_IMAGE

C0201R

D-PHY 4.5Gbps & C-PHY 2.5Gsps 0.85V
D-PHY 2.5Gbps & C-PHY 1.5Gsps 0.75V

RK3588

U1000R

MIPI D/C-PHY DSI_TX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C	AN20	MIPI_DPHY1_TX_CLKP [26]
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B	AP20	MIPI_DPHY1_TX_CLKN [26]
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B	AN18	MIPI_DPHY1_TX_D0P [26]
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A	AP18	MIPI_DPHY1_TX_D0N [26]
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A	AN19	MIPI_DPHY1_TX_D1P [26]
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C	AP19	MIPI_DPHY1_TX_D1N [26]
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B	AN21	MIPI_DPHY1_TX_D2P [26]
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A	AP21	MIPI_DPHY1_TX_D2N [26]
MIPI_DPHY1_TX_D3P/NO_USE	AN22	MIPI_DPHY1_TX_D3P [26]
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C	AP22	MIPI_DPHY1_TX_D3N [26]

TX and RX port must work in the same mode, DPHY or CPHY

MIPI D/C-PHY CSI_RX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C	AK20	MIPI_DPHY1_RX_CLKP [26]
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B	AL20	MIPI_DPHY1_RX_CLKN [26]
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B	AK18	MIPI_DPHY1_RX_D0P [26]
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A	AL18	MIPI_DPHY1_RX_D0N [26]
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A	AK19	MIPI_DPHY1_RX_D1P [26]
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C	AL19	MIPI_DPHY1_RX_D1N [26]
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B	AK21	MIPI_DPHY1_RX_D2P [26]
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A	AL21	MIPI_DPHY1_RX_D2N [26]
MIPI_DPHY1_RX_D3P/NO_USE	AK22	MIPI_DPHY1_RX_D3P [26]
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C	AL22	MIPI_DPHY1_RX_D3N [26]

MIPI D/C-PHY POWER

MIPI_D/C_PHY1_VREG	AF19	C1608 1uF/6.3V	C0201R
MIPI_D/C_PHY1_VDD	AG19	C1609 1uF/6.3V	VDD_0V75_S0
MIPI_D/C_PHY1_VDD_1V2	AH19	C1611 100nF/6.3V	VDDA_1V2_S0
MIPI_D/C_PHY1_VDD_1V8	AJ19	C1613 1uF/6.3V	VCCA1V8_IMAGE

C0201R

RK3588

Note:
If not used:
Signal:leave floating
Power: Floating

RK3588_P(MIPI_DPHY_CSI_RX_PHY)

U1000P

MIPI CSI Differential Pair:
100 Ohm +-10%

MIPI DPHY CSI_RX Port0

MIPI V1.2/2.5Gbps

MIPI_CSI0_CLK0P/MIPI_CSI0_CLK0N	AJ33/AJ34	MIPI_CSI0_RX_CLK0P/CLK0N [26]
MIPI_CSI0_D0P/MIPI_CSI0_D0N	AG33/AG34	MIPI_CSI0_RX_D0P/D0N [26]
MIPI_CSI0_D1P/MIPI_CSI0_D1N	AH33/AH34	MIPI_CSI0_RX_D1P/D1N [26]
MIPI_CSI0_CLK1P/MIPI_CSI0_CLK1N	AM33/AM34	MIPI_CSI0_RX_CLK1P/CLK1N [26]
MIPI_CSI0_D2P/MIPI_CSI0_D2N	AK33/AK34	MIPI_CSI0_RX_D2P/D2N [26]
MIPI_CSI0_D3P/MIPI_CSI0_D3N	AL33/AL34	MIPI_CSI0_RX_D3P/D3N [26]
MIPI_CSI0_AVCC0V75	AB25	C1616 100nF/6.3V, C1615 1uF/6.3V, VDD_0V75_S0
MIPI_CSI0_AVCC1V8	AB26	C1617 1uF/6.3V, VCCA1V8_IMAGE

C0201R

MIPI DPHY CSI_RX Port1

MIPI V1.2/2.5Gbps

MIPI_CSI1_CLK0P/MIPI_CSI1_CLK0N	AJ31/AJ32	MIPI_CSI1_RX_CLK0P/CLK0N [26]
MIPI_CSI1_D0P/MIPI_CSI1_D0N	AG31/AG32	MIPI_CSI1_RX_D0P/D0N [26]
MIPI_CSI1_D1P/MIPI_CSI1_D1N	AH31/AH32	MIPI_CSI1_RX_D1P/D1N [26]
MIPI_CSI1_CLK1P/MIPI_CSI1_CLK1N	AM31/AM32	MIPI_CSI1_RX_CLK1P/CLK1N [26]
MIPI_CSI1_D2P/MIPI_CSI1_D2N	AK31/AK32	MIPI_CSI1_RX_D2P/D2N [26]
MIPI_CSI1_D3P/MIPI_CSI1_D3N	AL31/AL32	MIPI_CSI1_RX_D3P/D3N [26]
MIPI_CSI1_AVCC0V75	AA25	C1619 1uF/6.3V, VDD_0V75_S0
MIPI_CSI1_AVCC1V8	AA26	C1621 100nF/6.3V, VCCA1V8_IMAGE

C0201R

RK3588

MIPI_CSI_RX Configuration

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0* *MIPI_CSI_RX_D2-3* *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating

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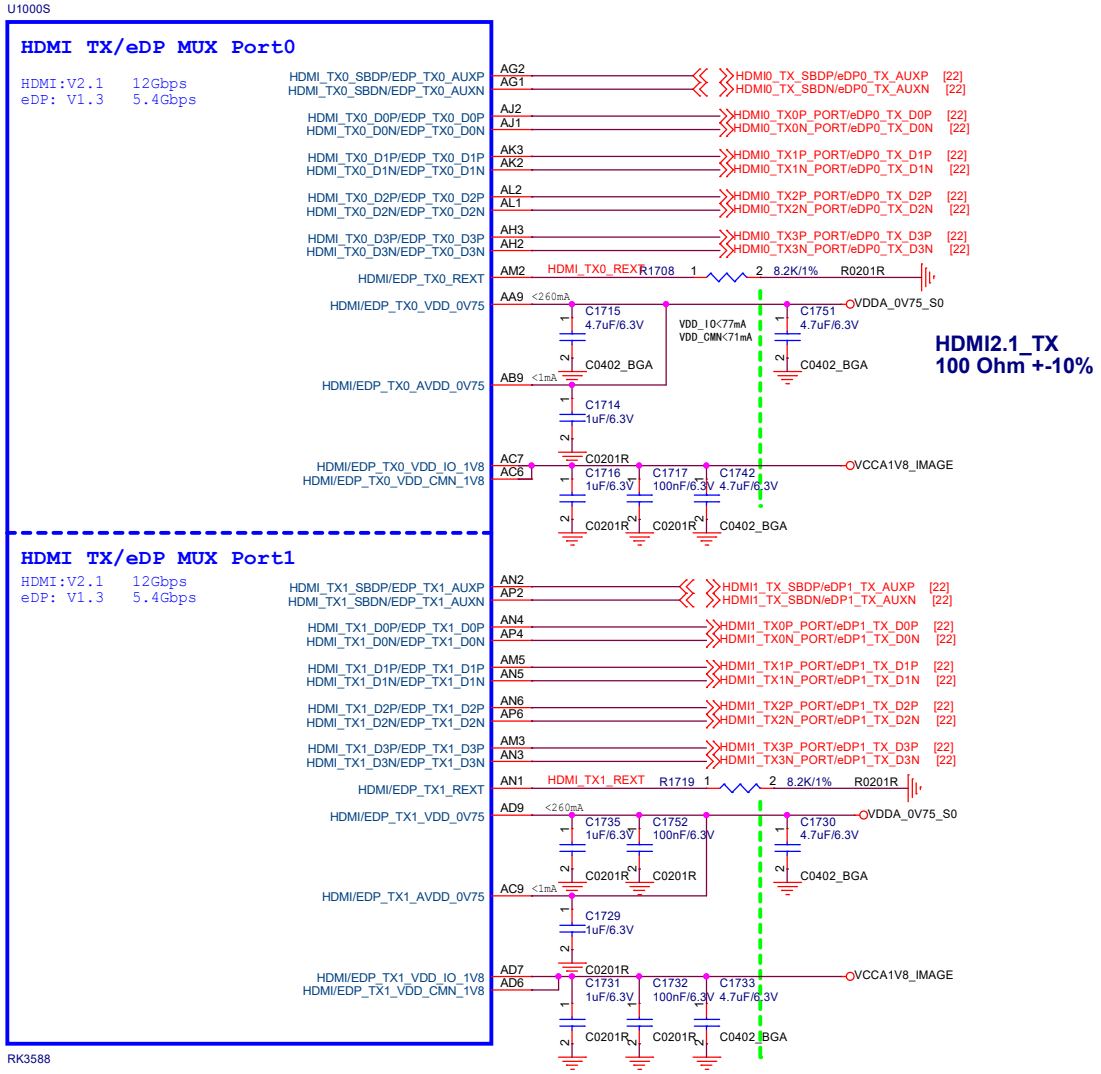
CM3588 Plus		Rev 2404
Size: Custom	Page Name: 12.RK3588_MIPI Interface	
Date: Monday, May 20, 2024		Sheet: 12/ 26

RK3588_S(HDMI2.1 TX)

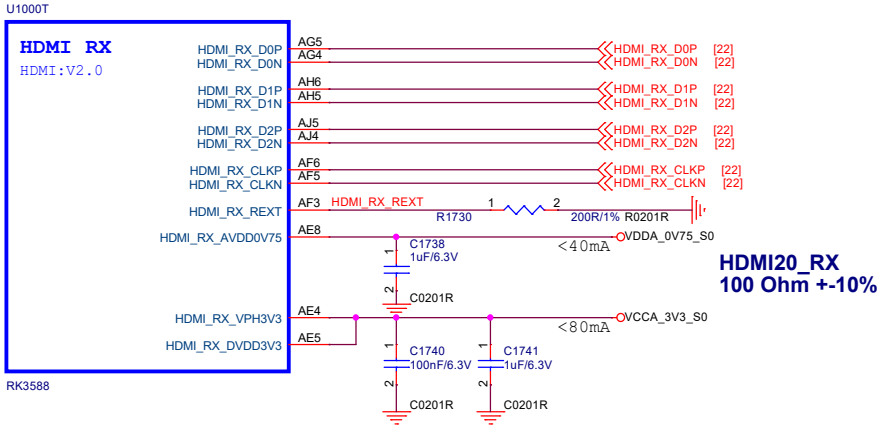
Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.



Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

RK3588_T(HDMI20 RX)



Note:
If not used:
Signal:leave floating
Power: Floating

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CM3588 Plus		Rev 2404
Size A3	Page Name 13.RK3588_HDMI/eDP Interface	
Date: Monday, May 20, 2024	Sheet: 13/ 26	

RK3588_N(PCIE20)

Note:
If not used:
Signal:leave floating
Power: Floating

U1000N

PCIE20/SATA30 Mux0

PCIe20x1_2
1Lane(RC)--4(1L2)

SATA30 HOST
Controller0

MUX

input or output

PCIE20_0_REFCLKP
PCIE20_0_REFCLKN
PCIE20_0_TXP/SATA30_0_TXP
PCIE20_0_TXN/SATA30_0_TXN
PCIE20_0_RXP/SATA30_0_RXP
PCIE20_0_RXN/SATA30_0_RXN

L32 L33 → PCIE20_0_REFCLKP [23] PCIE20_0_REFCLKN [23]
M34 M33 → PCIE20_0_TXP/SATA30_0_TXP [23] PCIE20_0_TXN/SATA30_0_TXN [23]
N33 N34 → PCIE20_0_RXP/SATA30_0_RXP [23] PCIE20_0_RXN/SATA30_0_RXN [23]

PCIE20_SATA30_0_AVDD_0V85 — M28 — C1810 10uF/6.3V — C0402 — VDDA_0V85_S0

PCIE20_SATA30_0_AVDD_1V8 — M27 — C1808 1uF/6.3V — C0201R — VCCA_1V8_S0

CLK Differential Pair:
100 Ohm±10%
DATA Differential Pair:
PCIE20: 85 Ohm ±10%
SATA30: 100 Ohm ±10%
USB30: 90ohm ±10%

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30 Mux1

PCIe30x1_0
1Lane(RC)--2(1L0)

SATA30 HOST
Controller1

MUX

input or output

PCIE20_1_REFCLKP
PCIE20_1_REFCLKN
PCIE20_1_TXP/SATA30_1_TXP
PCIE20_1_TXN/SATA30_1_TXN
PCIE20_1_RXP/SATA30_1_RXP
PCIE20_1_RXN/SATA30_1_RXN

H32 H33 → PCIE20_1_REFCLKP [26] PCIE20_1_REFCLKN [26]
K33 K34 → PCIE20_1_TXP/SATA30_1_TXP [26] PCIE20_1_TXN/SATA30_1_TXN [26]
J33 J34 → PCIE20_1_RXP/SATA30_1_RXP [26] PCIE20_1_RXN/SATA30_1_RXN [26]

PCIE20_SATA30_1_AVDD_0V85 — L28 — C1818 100nF/6.3V — C0201R — VDDA_0V85_S0

PCIE20_SATA30_1_AVDD_1V8 — L27 — C1816 100nF/6.3V — C0201R — VCCA_1V8_S0

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30/USB30 HOST Mux2

PCIe30x1_1
1Lane(RC)--3(1L1)

SATA30 HOST
Controller2

USB30 HOST
Controller2

MUX

input or output

PCIE20_2_REFCLKP
PCIE20_2_REFCLKN
PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP
PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN
PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP
PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN

G31 G30 → PCIE20_2_REFCLKP [26] PCIE20_2_REFCLKN [26]
H30 H29 → PCIE20_2_TXP/SATA30_2_TXP [26] PCIE20_2_TXN/SATA30_2_TXN [26]
J31 J30 → PCIE20_2_RXP/SATA30_2_RXP [26] PCIE20_2_RXN/SATA30_2_RXN [26]

PCIE20_SATA30_USB30_2_AVDD_0V85 — K28 — C1806 1uF/6.3V — C0201R — VDDA_0V85_S0

PCIE20_SATA30_USB30_2_AVDD_1V8 — K27 — C1804 1uF/6.3V — C0201R — VCCA_1V8_S0

PCIE20:Gen1/Gen2
USB 30:Gen1
SATA30:Gen1/Gen2/Gen3

RK3588

Note:
The SATA differential trace impedance is 100 OHM
The SATA trace length is less than 5 inch

RK3588_O(PCIE30)

Note:
Only PCIE3.0 Controller 0 support RC and EP,Other controller only support RC Mode.

U1000O

PCIE30X4

PCIe30X4
4Lane(DM)--0(4L)

PCIe30x1_0
1Lane(RC)--2(1L0)

PCIe30x2
2Lane(RC)--1(2L)

PCIe30x1_1
1Lane(RC)--3(1L1)

PCIE30:
PCIe1.1(2.5Gbps)
PCIe2.1(5Gbps)
PCIe3.0(8Gbps)

PCIE30 PORT0

input PCIE30_PORT0_REF_CLKP PCIE30_PORT0_REF_CLKN

Lane0: PCIE30_PORT0_TX0P/TX0N, PCIE30_PORT0_RX0P/RX0N
Lane1: PCIE30_PORT0_TX1P/TX1N, PCIE30_PORT0_RX1P/RX1N

E33 E34 → PCIE30_PORT0_REFCLKP_IN [26] PCIE30_PORT0_REFCLKN_IN [26]
D32 D33 → PCIE30_PORT0_TX0P [26] PCIE30_PORT0_TX0N [26]
G33 G34 → PCIE30_PORT0_RX0P [26] PCIE30_PORT0_RX0N [26]
C33 C34 → PCIE30_PORT0_TX1P [26] PCIE30_PORT0_TX1N [26]
F32 F33 → PCIE30_PORT0_RX1P [26] PCIE30_PORT0_RX1N [26]

PCIE30_PORT0_RESREF — B34 — PCIE30_0_REF — R1801 1 2 200R/1% R0201R

PCIE30_PORT0_AVDD0V75 — G24 — VDD_0V75_S0
C1802 1uF/6.3V C0201R
C1803 4.7uF/6.3V C0402_BGA

CLK Differential Pair:
100 Ohm ±10%
DATA Differential Pair:
PCIE30: 85 Ohm ±10%

PCIE30_PORT0_AVDD1V8 — G23 — VCCA_1V8_S0
C1800 1uF/6.3V C0201R
C1801 4.7uF/6.3V C0402_BGA

PCIE30 PORT1

input PCIE30_PORT1_REF_CLKP PCIE30_PORT1_REF_CLKN

Lane0: PCIE30_PORT1_TX0P/TX0N, PCIE30_PORT1_RX0P/RX0N
Lane1: PCIE30_PORT1_TX1P/TX1N, PCIE30_PORT1_RX1P/RX1N

A28 B28 → PCIE30_PORT1_REFCLKP_IN [26] PCIE30_PORT1_REFCLKN_IN [26]
B30 A30 → PCIE30_PORT1_TX2P [26] PCIE30_PORT1_TX2N [26]
B32 A32 → PCIE30_PORT1_RX2P [26] PCIE30_PORT1_RX2N [26]
C29 B29 → PCIE30_PORT1_TX3P [26] PCIE30_PORT1_TX3N [26]
C31 B31 → PCIE30_PORT1_RX3P [26] PCIE30_PORT1_RX3N [26]

PCIE30_PORT1_RESREF — A33 — PCIE30_1_REF — R1807 1 2 200R/1% R0201R

PCIE30_PORT1_AVDD0V75 — H24 — VDD_0V75_S0
C1814 1uF/6.3V C0201R
C1815 4.7uF/6.3V C0402_BGA

PCIE30_PORT1_AVDD1V8 — H23 — VCCA_1V8_S0
C1812 100nF/6.3V C0201R
C1813 4.7uF/6.3V C0402_BGA

PCIE20/SATA30 MUX1
PCIE20/SATA30/USB30 MUX2

RK3588

Note:
If Port0 and Port1 are not used,
Port0 and Port1 REF_CLKP/N: Leave floating or tie to VSS
Port0 and Port1 Other Signal: Leave floating
Port0 and Port1 Power: Leave floating or tie to VSS

If Port0 is used ,Port1 is not used,
Port1 REF_CLKP/N: Leave floating or tie to VSS
Port1 Other Signal: Leave floating
Port1 Power: Must supply power

If Port1 is used ,Port0 is not used,
Port0 REF_CLKP/N: Leave floating or tie to VSS
Port0 Other Signal: Leave floating
Port0 Power: Must supply power

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CM3588 Plus		Rev 2404
Size A3	Page Name 14.RK3588_PCIE30/PCIE20/SATA30	
Date: Monday, May 20, 2024	Sheet: 14/ 26	

RK3588_J(VCCIO5 Domain)

U1000J

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	SPI4_MISO_M1		I2C6_SDA_M4	FSPI_D0_M2	I2S3_MCLK	SDIO_D0_M1	GMAC1_TXD2	GPIO3_A0_u	AA29
AUDDSM_LN	SPI4_MOSI_M1	PWM11_IR_M0	I2C6_SCL_M4	FSPI_D1_M2	I2S3_SCLK	SDIO_D1_M1	GMAC1_TXD3	GPIO3_A1_u	AA30
AUDDSM_LP	SPI4_CLK_M1	UART8_TX_M1		FSPI_D2_M2	I2S3_LRCK	SDIO_D2_M1	GMAC1_RXD2	GPIO3_A2_u	AD27
AUDDSM_RN	SPI4_CS0_M1	UART8_RX_M1		FSPI_D3_M2	I2S3_SDO	SDIO_D3_M1	GMAC1_RXD3	GPIO3_A3_u	AE27
AUDDSM_RP	SPI4_CS1_M1	UART8_RTSN_M1			I2S3_SDI	SDIO_CMD_M1	GMAC1_TXCLK	GPIO3_A4_d	AD28
	MIPI_CAMERA0_CLK_M1	UART8_CTSN_M1	I2C4_SDA_M0	FSPI_CLK_M2		SDIO_CLK_M1	GMAC1_RXCLK	GPIO3_A5_d	AH30
	MIPI_CAMERA1_CLK_M1		I2C4_SCL_M0				ETH1_REFCLKO_25M	GPIO3_A6_d	AH27
PWM8_M0	MIPI_CAMERA2_CLK_M1						GMAC1_RXD0	GPIO3_A7_u	AG29
PWM9_M0	MIPI_CAMERA3_CLK_M1						GMAC1_RXD1	GPIO3_B0_u	AG28
PWM2_M1	MIPI_CAMERA4_CLK_M1	UART2_TX_M2					GMAC1_RXDV_CRS	GPIO3_B1_d	AH29
PWM3_IR_M1		UART2_RX_M2			I2S2_SDI_M1		GMAC1_TXER	GPIO3_B2_d	AE28
		UART2_RTSN			I2S2_SDO_M1		GMAC1_TXD0	GPIO3_B3_u	AC28
		UART2_CTSN			I2S2_MCLK_M1		GMAC1_TXD1	GPIO3_B4_u	AC29
PWM12_M0	CAN1_RX_M0	UART3_TX_M1			I2S2_SCLK_M1		GMAC1_TXEN	GPIO3_B5_u	AD29
PWM13_M0	CAN1_TX_M0	UART3_RX_M1			I2S2_LRCK_M1		GMAC1_MCLKINOUT	GPIO3_B6_d	AE29
			I2C3_SCL_M1	SPI1_MOSI_M1	HDMI_TX1_HPD_M1		GMAC1_PTP_REF_CLK	GPIO3_B7_d	AA28
		UART7_TX_M1	I2C3_SDA_M1	SPI1_MISO_M1			GMAC1_PPSTRIG	GPIO3_C0_d	Y29
	PCIE30X2_BUTTON_RSTN	UART7_RX_M1		SPI1_CLK_M1			GMAC1_PPSCLK	GPIO3_C1_d	Y27
PWM14_M0		UART7_RTSN_M1	I2C8_SCL_M4	SPI1_CS0_M1		MIPI_TE0	GMAC1_MDC	GPIO3_C2_d	Y31
PWM15_IR_M0		UART7_CTSN_M1	I2C8_SDA_M4	SPI1_CS1_M1		MIPI_TE1	GMAC1_MDIO	GPIO3_C3_d	Y30
CAN2_RX_M0	PCIE30X4_CLKREQN_M2	UART5_TX_M1	FSPI_CS0N_M2	SPI3_CS0_M3	HDMI_TX1_CEC_M2		CIF_D8	GPIO3_C4_u	AH26
CAN2_TX_M0	PCIE30X4_WAKEN_M2	UART5_RX_M1	FSPI_CS1N_M2	SPI3_CS1_M3	HDMI_TX1_SDA_M1		CIF_D9	GPIO3_C5_u	AH25
	PCIE30X4_PERSTN_M2			SPI3_MISO_M3	HDMI_TX1_SCL_M1		CIF_D10	GPIO3_C6_u	AG26
	PCIE20X1_2_CLKREQN_M0		I2C5_SCL_M0	SPI3_MOSI_M3	HDMI_TX0_SCL_M2		CIF_D11	GPIO3_C7_u	AJ24
PWM8_M2	PCIE20X1_2_WAKEN_M0	UART4_RX_M1	I2C5_SDA_M0	SPI3_CLK_M3	HDMI_TX0_SDA_M2		CIF_D12	GPIO3_D0_u	AH24
PWM9_M2	PCIE20X1_2_PERSTN_M0	UART4_TX_M1		SPI0_MISO_M3	HDMI_RX_CEC_M1		CIF_D13	GPIO3_D1_d	AG23
	PCIE30X2_CLKREQN_M2	UART9_RTSN_M2	I2C7_SCL_M2	SPI0_MOSI_M3	HDMI_RX_SCL_M1		CIF_D14	GPIO3_D2_d	AG25
PWM10_M2	PCIE30X2_WAKEN_M2	UART9_CTSN_M2	I2C7_SDA_M2	SPI0_CLK_M3	HDMI_RX_SDA_M1		CIF_D15	GPIO3_D3_d	AG24
	PCIE30X2_PERSTN_M2	UART9_RX_M2		SPI0_CS0_M3	HDMIRX_HPDOUT_M1	HDMI_TX0_HPD_M1	MCU_JTAG_TCK_M1	GPIO3_D4_d	AA27
PWM11_IR_M3	PCIE30X4_BUTTON_RSTN	UART9_TX_M2		SPI0_CS1_M3	DP1_HPDIN_M0		MCU_JTAG_TMS_M1	GPIO3_D5_d	AB28

VCCIO5_1V8 — W25 — C1903 100nF/6.3V C0201R — OVCC_1V8_S3

VCCIO5 — W26 — C1902 100nF/6.3V C0201R — OVCC_3V3_S3

RK3588

RK3588_K(VCCIO6 Domain)

U1000K

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

	SPI0_MISO_M1	UART9_RTSN_M1			I2S1_MCLK_M0	PCIE30X1_1_CLKREQN_M1	BT1120_D0	CIF_D0	GPIO4_A0_d	AK30
	SPI0_MOSI_M1	UART9_CTSN_M1			I2S1_SCLK_M0	PCIE30X1_1_WAKEN_M1	BT1120_D1	CIF_D1	GPIO4_A1_d	AL30
	SPI0_CLK_M1				I2S1_LRCK_M0	PCIE30X1_1_PERSTN_M1	BT1120_D2	CIF_D2	GPIO4_A2_d	AM29
		UART0_TX_M2				PCIE30X1_0_CLKREQN_M1	BT1120_D3	CIF_D3	GPIO4_A3_d	AL29
	SPI2_MISO_M1	UART0_RX_M2	I2C3_SCL_M2			PCIE30X1_0_WAKEN_M1	BT1120_D4	CIF_D4	GPIO4_A4_d	AL28
	SPI2_MOSI_M1	UART3_TX_M2	I2C3_SDA_M2		I2S1_SDI0_M0	PCIE30X1_0_PERSTN_M1	BT1120_D5	CIF_D5	GPIO4_A5_d	AK27
	SPI2_CLK_M1	UART3_RX_M2	I2C5_SCL_M2		I2S1_SDI1_M0	PCIE30X2_CLKREQN_M1	BT1120_D6	CIF_D6	GPIO4_A6_d	AL27
	SPI2_CS0_M1		I2C5_SDA_M2		I2S1_SDI2_M0	PCIE30X2_WAKEN_M1	BT1120_D7	CIF_D7	GPIO4_A7_d	AM27
	SPI2_CS1_M1	UART8_TX_M0	I2C6_SDA_M3		I2S1_SDI3_M0	PCIE30X2_PERSTN_M1	BT1120_CLKOUT	CIF_CLKIN	GPIO4_B0_d	AK26
SATA2_ACT_LED_M0	SPDIF1_TX_M1	SPI0_CS1_M1	UART8_RX_M0	I2C6_SCL_M3		I2S1_SDO0_M0	PCIE30X1_0_BUTTON_RSTN		MIPI_CAMERA5_CLK_M0	GPIO4_B1_u	AL24
CAN1_RX_M1	PWM14_M1	SPI0_CS0_M1	UART8_RTSN_M0	I2C7_SCL_M3		I2S1_SDO1_M0	PCIE30X1_1_BUTTON_RSTN	BT1120_D8	CIF_HREF	GPIO4_B2_u	AK25
CAN1_TX_M1	PWM15_IR_M1		UART8_CTSN_M0	I2C7_SDA_M3		I2S1_SDO2_M0	PCIE20X1_2_BUTTON_RSTN	BT1120_D9	CIF_VSYNC	GPIO4_B3_u	AM25
SPDIF0_TX_M1	PWM11_IR_M1	DP0_HPDIN_M0	UART9_TX_M1			I2S1_SDO3_M0	PCIE30X4_CLKREQN_M1	BT1120_D10	CIF_CLKOUT	GPIO4_B4_u	AL26
SATA1_ACT_LED_M0	PWM12_M1	SPI3_MISO_M1	UART9_RX_M1			HDMI_RX_CEC_M0	PCIE30X4_WAKEN_M1	BT1120_D11		GPIO4_B5_d	AJ26
SATA0_ACT_LED_M0	PWM13_M1	SPI3_MOSI_M1		I2C5_SCL_M1		HDMI_RX_HPDOUT_M0	PCIE30X4_PERSTN_M1	BT1120_D12		GPIO4_B6_d	AJ27
		SPI3_CLK_M1		I2C5_SDA_M1		HDMI_TX0_SCL_M0	PCIE20X1_2_CLKREQN_M1	BT1120_D13		GPIO4_B7_u	AJ28
		SPI3_CS0_M1		I2C8_SCL_M3		HDMI_TX0_SDA_M0	PCIE20X1_2_WAKEN_M1	BT1120_D14		GPIO4_C0_u	AJ25
SPDIF1_TX_M2	PWM6_M1	SPI3_CS1_M1		I2C8_SDA_M3		HDMI_TX0_CEC_M0	PCIE20X1_2_PERSTN_M1	BT1120_D15		GPIO4_C1_d	AK24

VCCIO6_1V8 — AC25 — C1909 100nF/6.3V C0201R — OVCC_1V8_S3

VCCIO6 — AC26 — C1908 100nF/6.3V C0201R — OVCC_3V3_S3

RK3588

RK3588_I(VCCIO4 Domain)

U1000I

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

		SPI4_MISO_M2	PCIE30X1_1_CLKREQN_M2	DP0_HPDIN_M2		I2C2_SDA_M4	UART6_RX_M1	GPIO1_A0_d	A24
SATA1_ACT_LED_M1		SPI4_MOSI_M2	PCIE30X1_1_WAKEN_M2	DP1_HPDIN_M2		I2C2_SCL_M4	UART6_TX_M1	GPIO1_A1_d	A25
	PWM0_M2	SPI4_CLK_M2		VOP_POST_EMPTY		I2C4_SDA_M3	UART6_RTSN_M1	GPIO1_A2_d	A26
	PWM1_M2	SPI4_CS0_M2		HDMI_TX1_SDA_M2		I2C4_SCL_M3	UART6_CTSN_M1	GPIO1_A3_d	A27
		SPI2_MISO_M0		HDMI_TX1_SCL_M2				GPIO1_A4_d	B25
		SPI2_MOSI_M0		HDMI_TX0_HPD_M0				GPIO1_A5_d	B26
		SPI2_CLK_M0		HDMI_TX1_HPD_M0				GPIO1_A6_d	C24
	PWM3_IR_M3	SPI2_CS0_M0	PCIE30X1_1_PERSTN_M2			PDM1_SDI0_M1		GPIO1_A7_u	C25
		SPI2_CS1_M0	PCIE30X4_CLKREQN_M3			PDM1_SDI1_M1		GPIO1_B0_u	C27
		SPI0_MISO_M2	PCIE30X4_WAKEN_M3			PDM1_SDI2_M1		GPIO1_B1_d	D25
		SPI0_MOSI_M2	PCIE30X4_PERSTN_M3			PDM1_SDI3_M1	UART4_RX_M2	GPIO1_B2_d	D26
SATA0_ACT_LED_M1		SPI0_CLK_M2	PCIE30X1_0_WAKEN_M2			PDM1_CLK1_M1	UART4_TX_M2	GPIO1_B3_d	D27
		SPI0_CS0_M2	PCIE30X1_0_PERSTN_M2			PDM1_CLK0_M1	UART7_RX_M2	GPIO1_B4_u	E24
		SPI0_CS1_M2	PCIE30X1_0_CLKREQN_M2				UART7_TX_M2	GPIO1_B5_u	E25
	HDMI_RX_HPDOUT_M2	SPDIF0_TX_M0	PCIE30X2_WAKEN_M3	MIPI_CAMERA1_CLK_M0		I2C5_SCL_M3	UART1_TX_M1	GPIO1_B6_u	E26
SATA2_ACT_LED_M1	HDMI_RX_CEC_M2	PWM13_M2	SPDIF1_TX_M0	PCIE30X2_PERSTN_M3		MIPI_CAMERA2_CLK_M0	I2C5_SDA_M3	UART1_RX_M1	GPIO1_B7_u	E27
	HDMI_RX_SCL_M2	PWM14_M2		MIPI_CAMERA3_CLK_M0		I2C8_SCL_M2	UART1_RTSN_M1	GPIO1_D6_u	F24
	HDMI_RX_SDA_M2	PWM15_IR_M3	PCIE30X2_CLKREQN_M3	MIPI_CAMERA4_CLK_M0		I2C8_SDA_M2	UART1_CTSN_M1	GPIO1_D7_u	F25

VCCIO4_1V8 — H20 — C1907 100nF/6.3V C0201R — OVCC_1V8_S3

VCCIO4 — H21 — C9951 100nF/6.3V C0201R — OVCC_3V3_S3

RK3588

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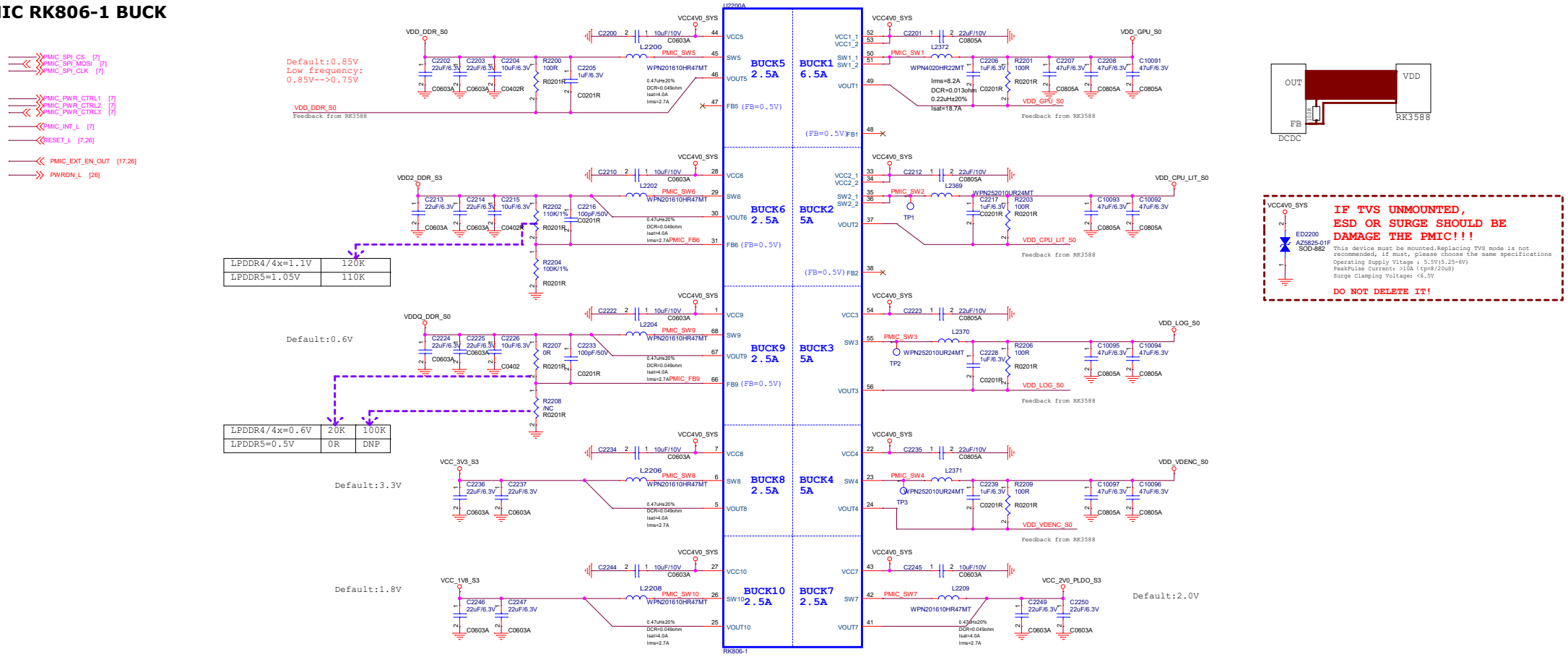
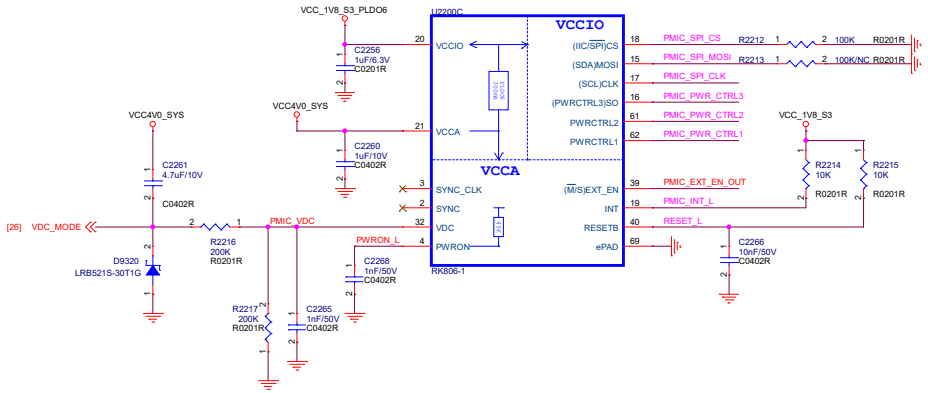
CM3588 Plus		Rev 2404	
Size A2	Page Name 15.RK3588_1.8V/ 3.3V GPIO		
Date: Monday, May 20, 2024		Sheet: 15/ 26	

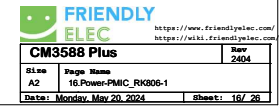
PMIC RK806-1 BUCK



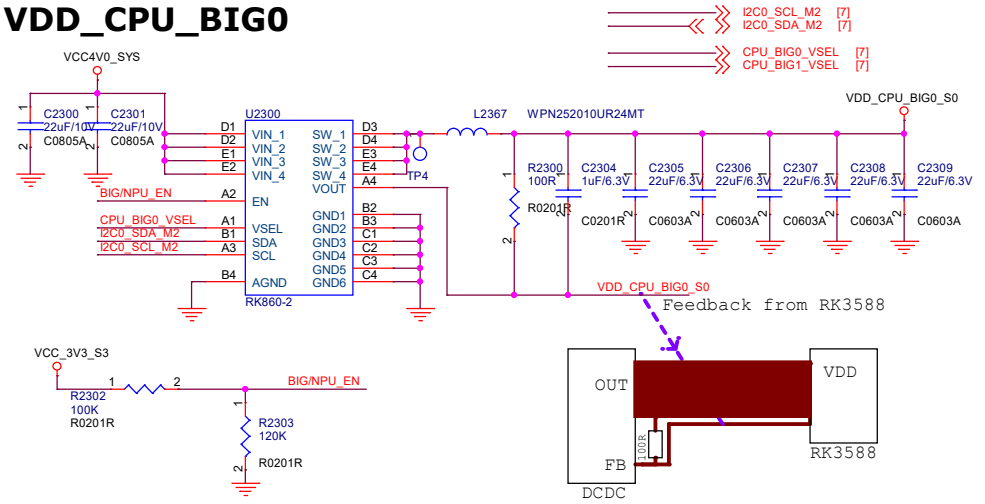
PMIC RK806-1 Managerment



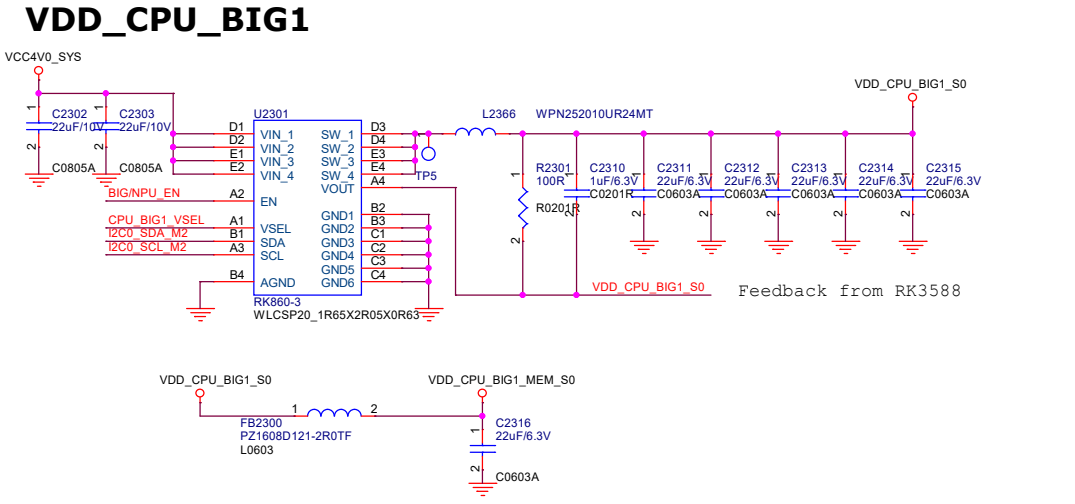
PMIC RK806-1 LDO



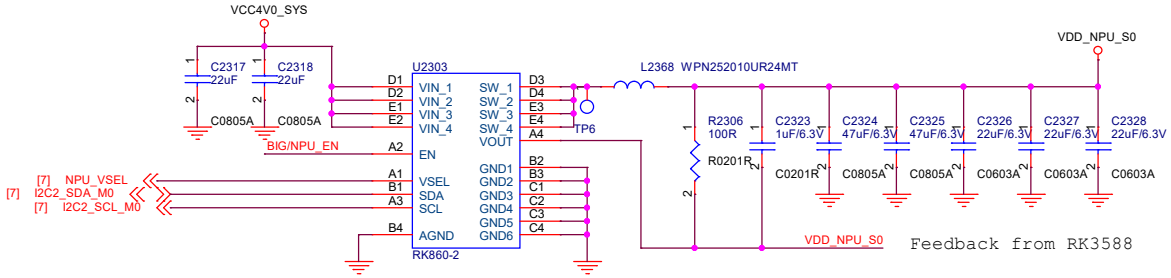
VDD_CPU_BIG0



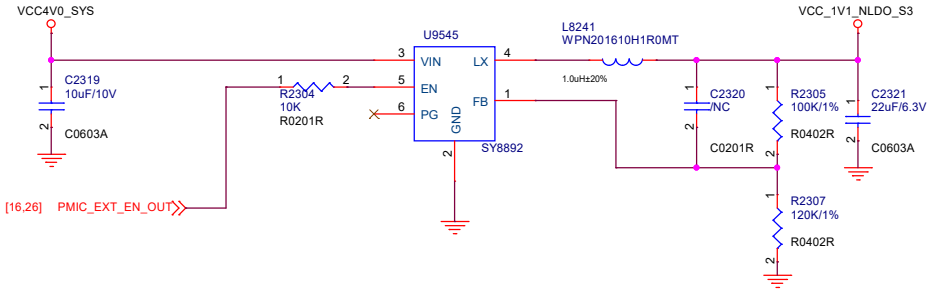
VDD_CPU_BIG1



VDD_NPU



VCC_1V1_NLDO_S3



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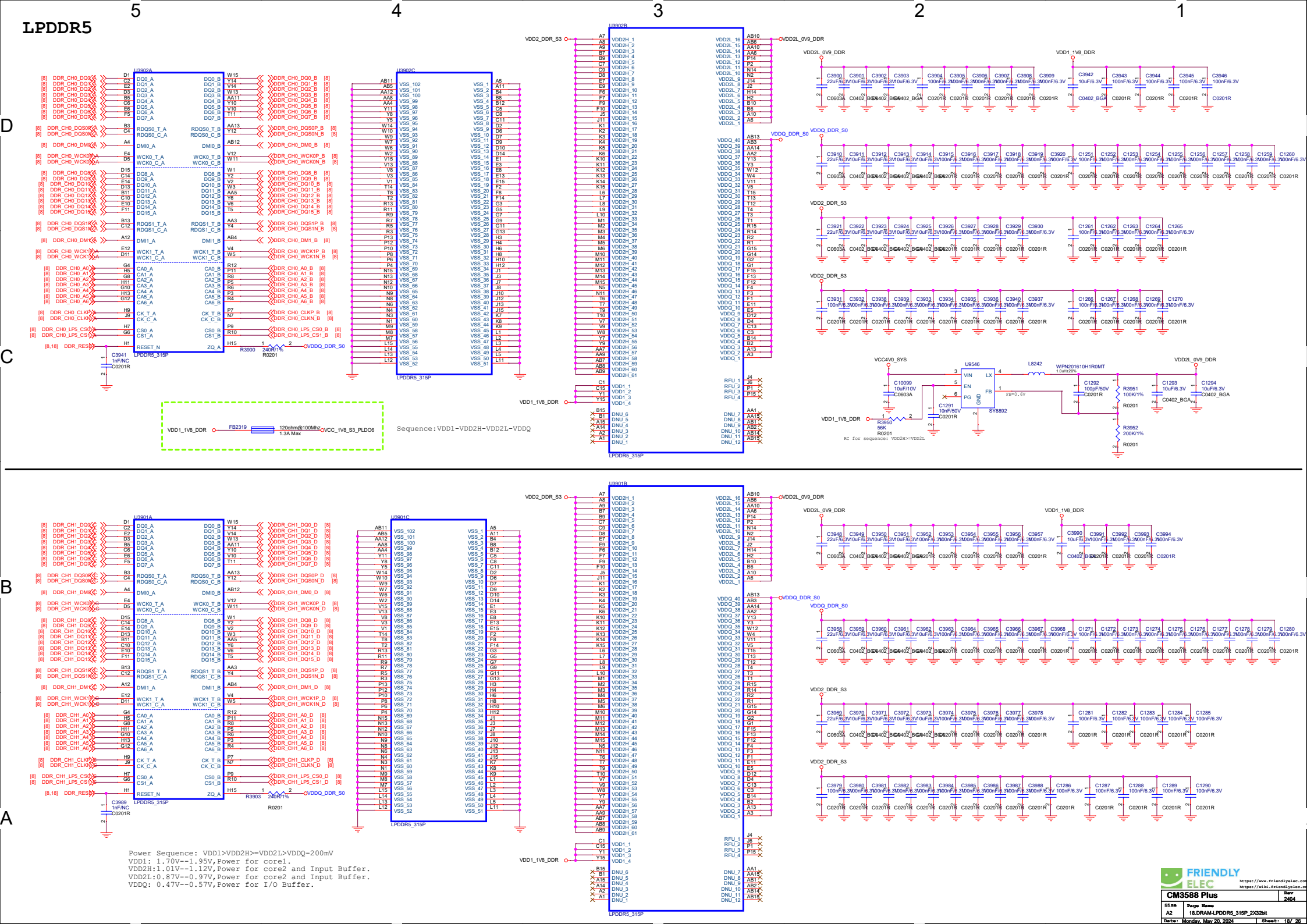
CM3588 Plus	Rev 2404
Size A3	Page Name 17.Power_Ext Discrete
Date: Monday, May 20, 2024	Sheet: 17/ 26

LPDDR5


5
4
3
2
1
D
C
B
A
U3902A
U3902B
U3902C
U3901A
U3901B
U3901C
LPDDR5_315P
VDD2_DDR_S3
VDD2L_0V9_DDR
VDD1_1V8_DDR
VDDQ_DDR_S0
VCC4V0_SYS
VCC_1V8_S3_PLDO6
FB2319
120ohm@100Mhz
1.3A Max
U9546
SY8892
L8242
WPN201610H1R0MT
1.0uHx20%
Sequence:VDD1-VDD2H-VDD2L-VDDQ
Power Sequence: VDD1>VDD2H>=VDD2L>VDDQ-200mV
VDD1: 1.70V--1.95V,Power for corel.
VDD2H:1.01V--1.12V,Power for core2 and Input Buffer.
VDD2L:0.87V--0.97V,Power for core2 and Input Buffer.
VDDQ: 0.47V--0.57V,Power for I/O Buffer.
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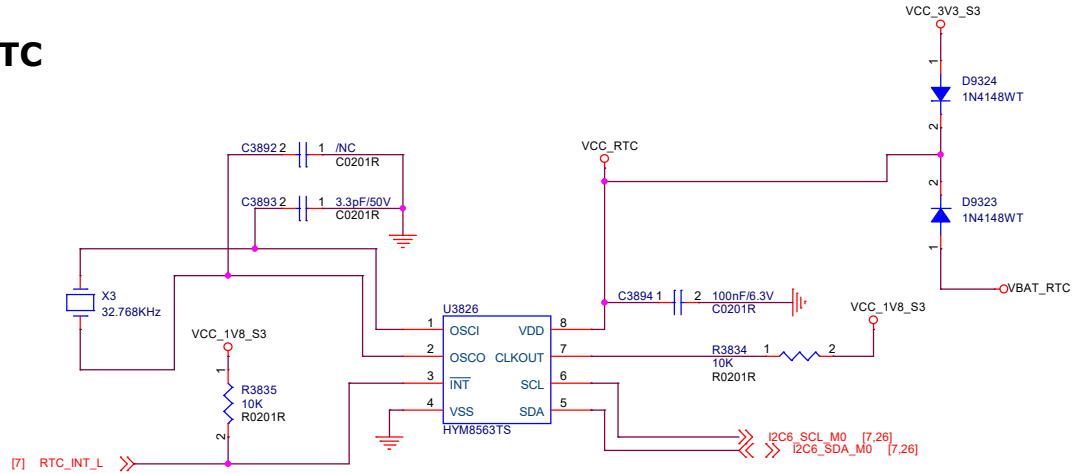
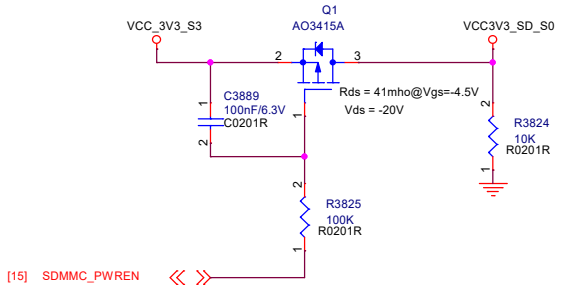
CM3588 Plus
Rev 2404
Size A2
Page Name 18.DRAM-LPDDR5_315P_2X32bit
Date: Monday, May 20, 2024
Sheet: 18/ 26

RTC



Address:Read A3H, Write A2H
7bit address: 0x51

microSD Power



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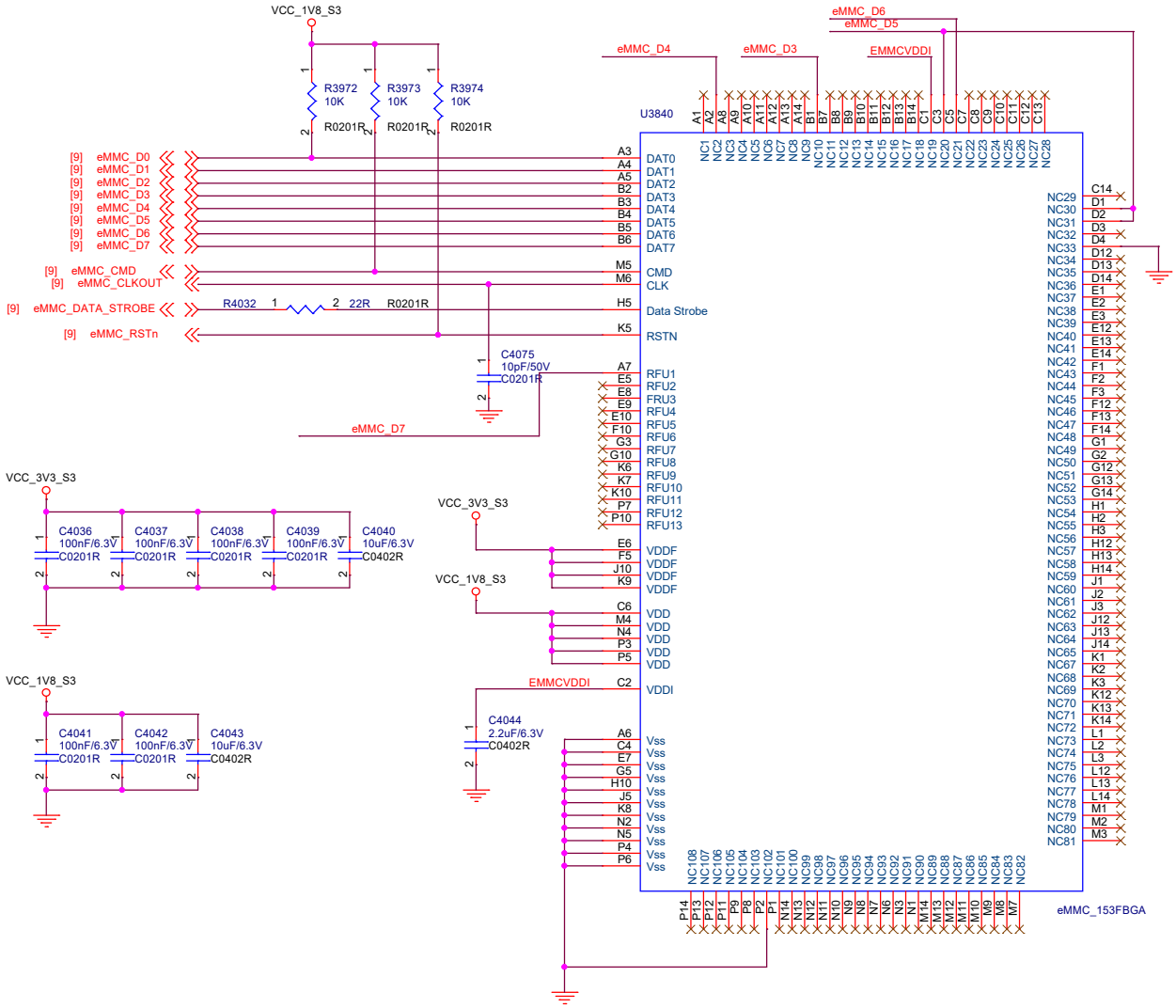
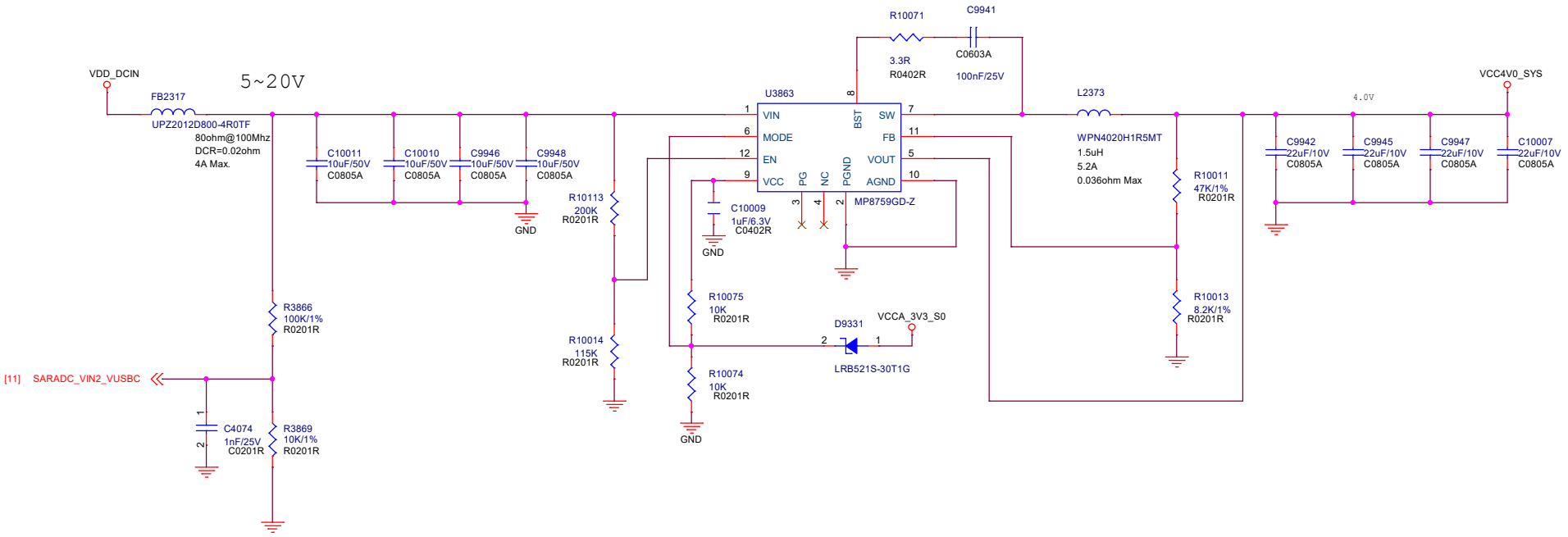
CM3588 Plus	Rev 2404
Size A3	Page Name 19.RTC/microSD Power
Date: Monday, May 20, 2024	Sheet: 19/ 26

eMMC



CM3588 Plus		Rev 2404
Size A3	Page Name 20.eMMC	
Date: Monday, May 20, 2024	Sheet: 20/ 26	

Power IN



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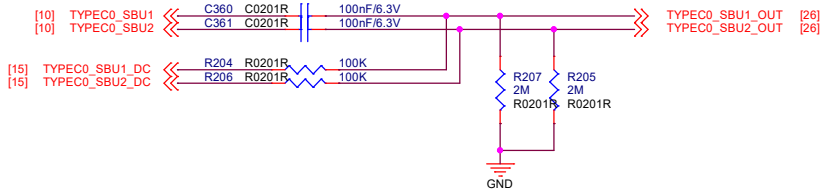
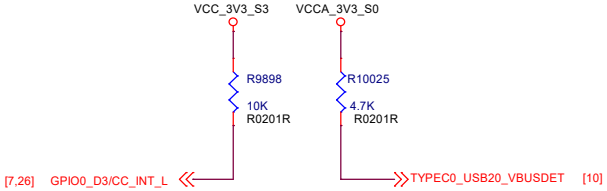
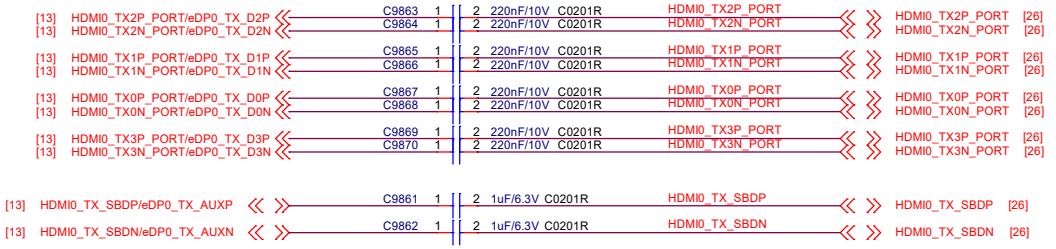
CM3588 Plus	Rev 2404
Size A3	Page Name 21.Power IN
Date: Monday, May 20, 2024	Sheet: 21/ 26

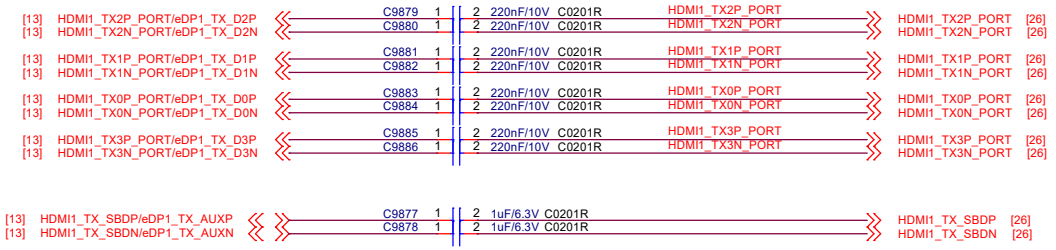
USB3.0 Type-C

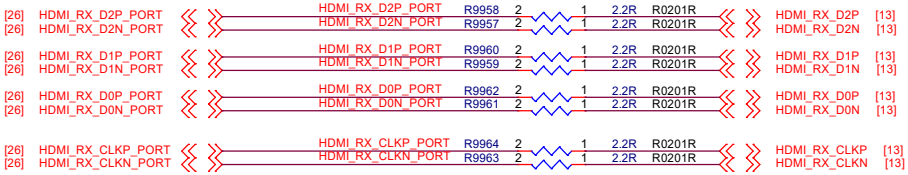




HDMI







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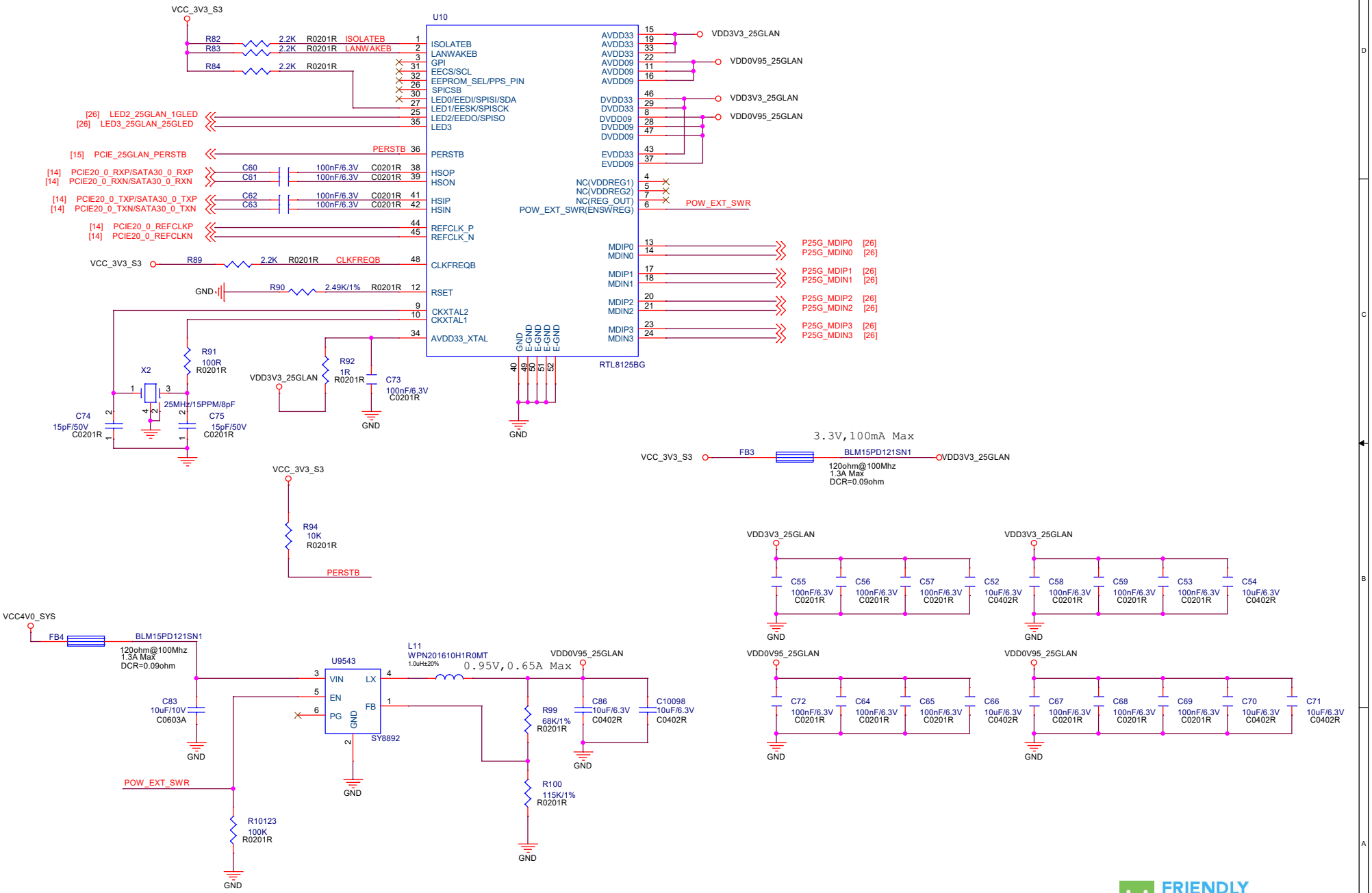
CM3588 Plus		Rev 2404
Size A3	Page Name 22.HDMI	
Date: Monday, May 20, 2024		Sheet: 22/ 26

2.5G Ethernet



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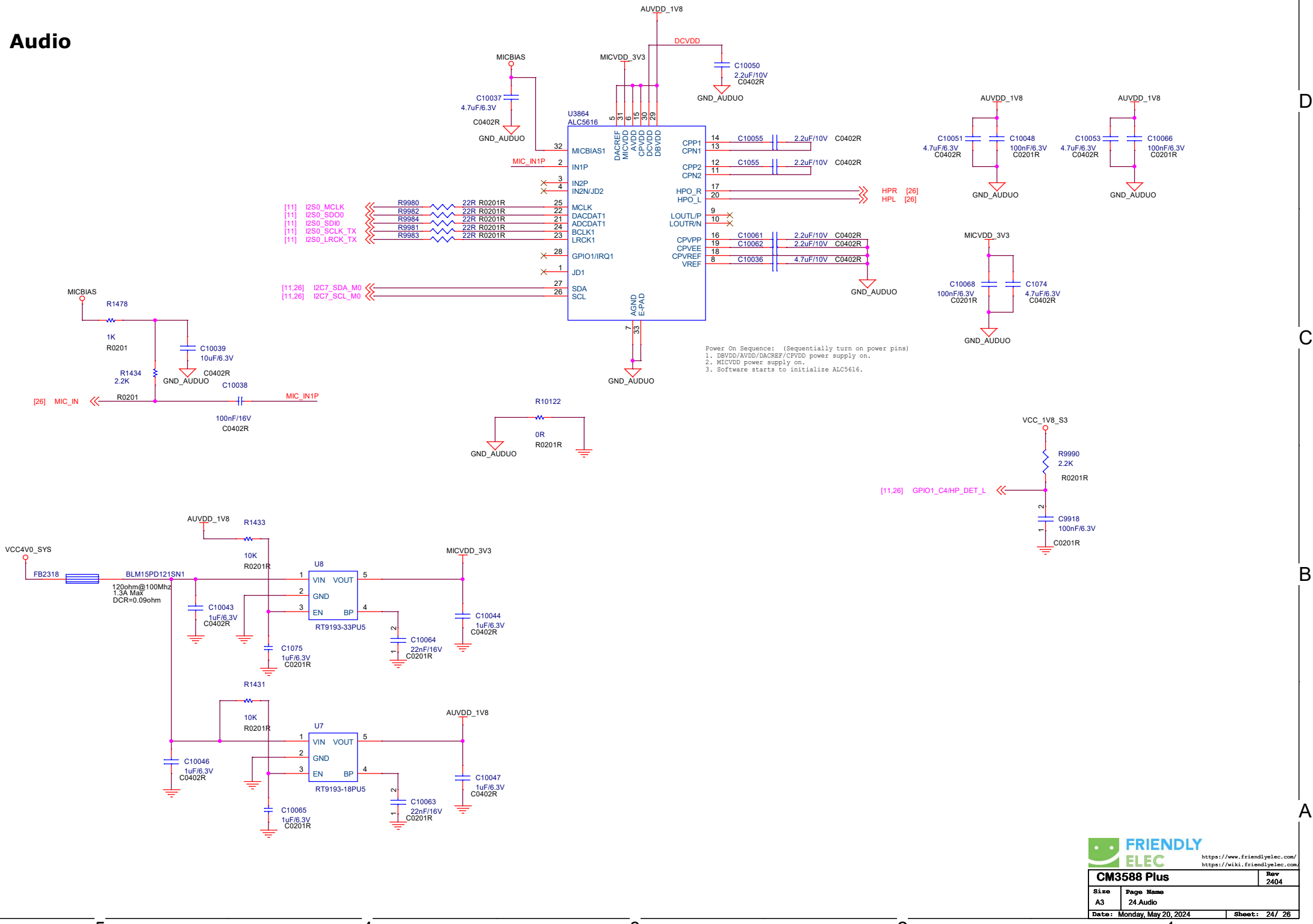
CM3588 Plus		Rev 2404
Size A3	Page Name 23.2.5Gbps	
Date: Monday, May 20, 2024		Sheet: 23/ 26

Audio



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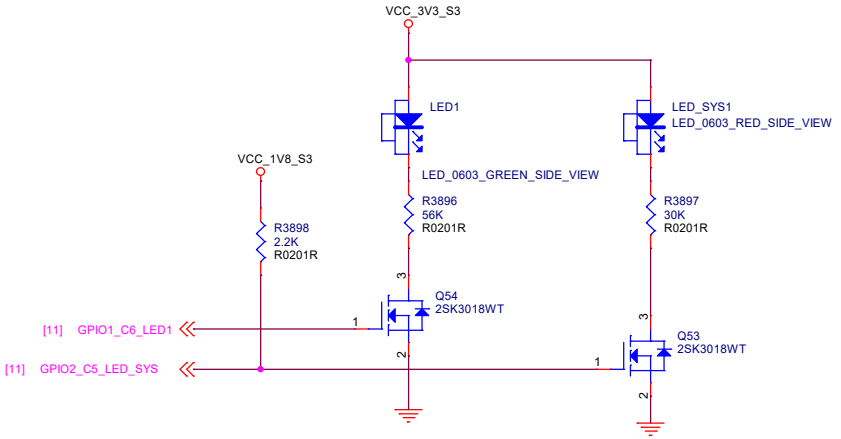
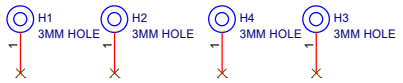
CM3588 Plus	Rev 2404
Size A3	Page Name 24.Audio
Date: Monday, May 20, 2024	Sheet: 24/ 26

LEDs



Holes



UART0	3.3V	M0	UART9	3.3V	M1
UART1	3.3V /1.8V	M0/M1			
UART2	3.3V	Debug Console			
UART3	3.3V /1.8V	M0/M1			
UART4	3.3V	M2			
UART5	/	NC			
UART6	3.3V /1.8V	M0/M1			
UART7	3.3V /1.8V	M0/M1/M2			
UART8	3.3V	M1			

I2C0	3.3V	RK860-3(CPU0), RK860-2(CPU1)
I2C1	3.3V	M2
I2C2	3.3V	RK860-2(NPU)
I2C3	3.3V /1.8V	M0/M1/M3
I2C4	3.3V /1.8V	M0/M1/M2/M3
I2C5	3.3V /1.8V	M0/M3/M4
I2C6	3.3V	24AA025E48T-I/OT, HYM8563TS, FUSB302MPX
I2C7	1.8V	Codec, M0
I2C8	3.3V /1.8V	M1/M2/M4

PWM0	3.3V /1.8V	M1/M2	PWM9	3.3V	M0
PWM1	3.3V /1.8V	M1/M2	PWM10	3.3V	M0
PWM2	3.3V /1.8V	M0/M1/M2	PWM11	3.3V	M0/M1/M3
PWM3	3.3V	M0/M1/M3	PWM12	3.3V	M0/M1
PWM4	3.3V /1.8V	M1/M0	PWM13	3.3V	M0/M1/M2
PWM5	3.3V /1.8V	M1/M2	PWM14	3.3V	M0/M2
PWM6	1.8V	M2	PWM15	3.3V	M0/M1/M3
PWM7	1.8V	M3			
PWM8	3.3V	M0/M2			

SPI0	3.3V	M2
SPI1	3.3V /1.8V	M0/M1
SPI2	/	NC
SPI3	/	NC
SPI4	3.3V	M1/M2

I2S0	1.8V	ALC5616 Codec
I2S1	3.3V	M0
I2S2	3.3V /1.8V	M0/M1
I2S3	3.3V	YES

CAN0	/	NC
CAN1	3.3V	M0
CAN2	3.3V	M1

SPDIF0	3.3V	M0/M1
SPDIF1	3.3V	M0

SDIO	3.3V /1.8V	M0/M1

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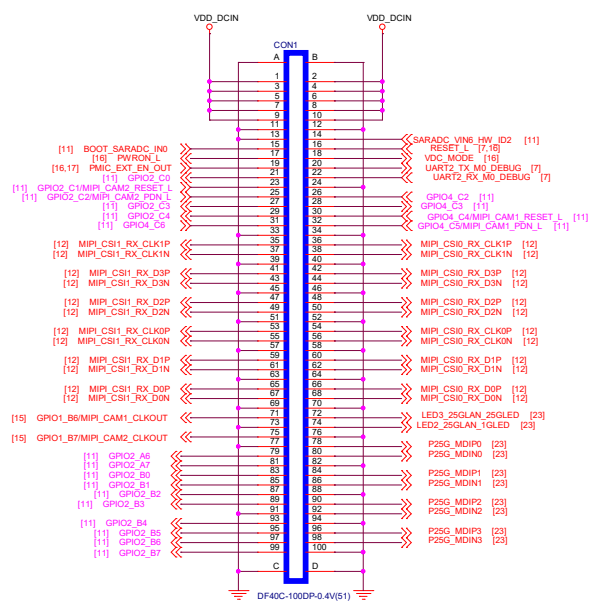
CM3588 Plus		Rev 2404
Size A3	Page Name 25.LEDs/Holes	
Date: Monday, May 20, 2024		Sheet: 25/ 26

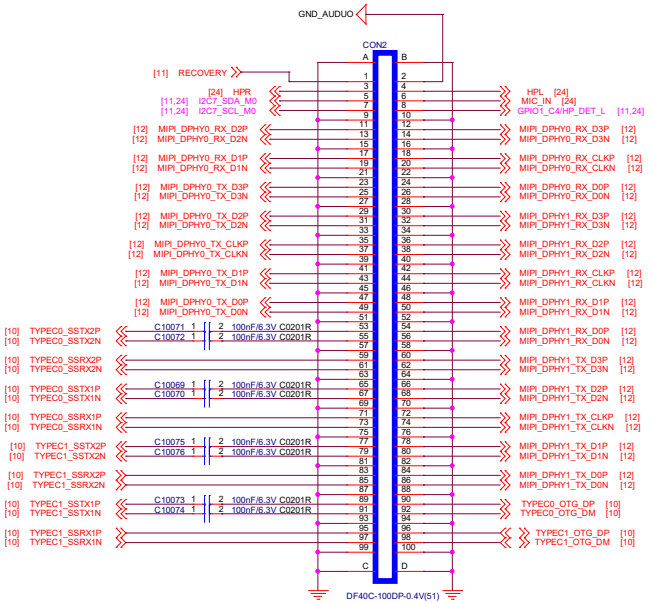
5 4 3 2 1

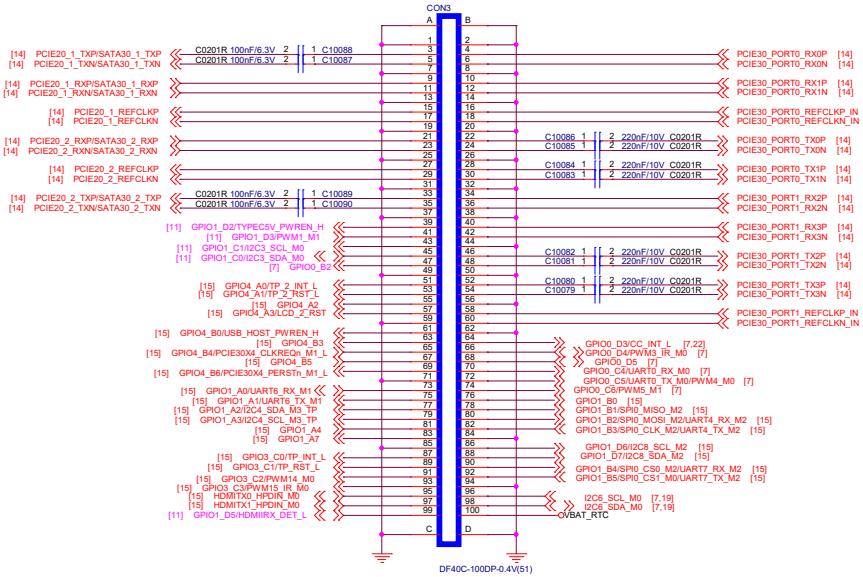
D C B A

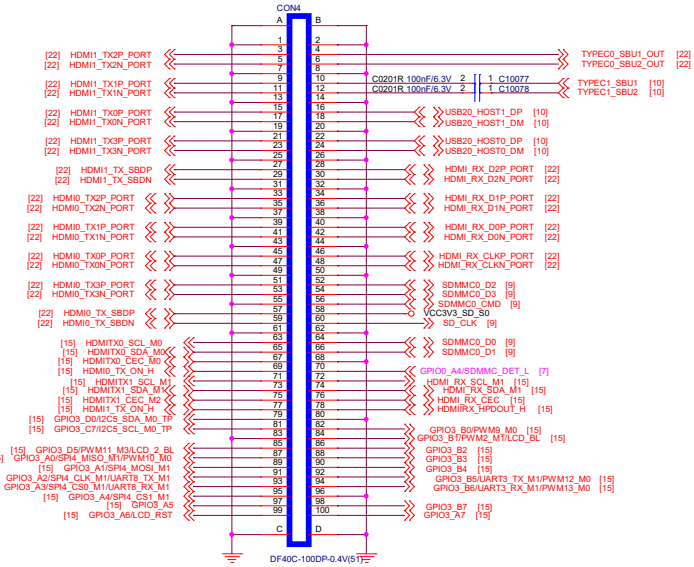
Pinout

VDD_DCIN	5~20VDC Power input, 20W max
BOOT_SARADC_IN0	Pull low to enter USB Maskrom Mode
SARADC_VIN6_HW_ID2	for Carrier Board ID
PWRON_L	Connect to PowerKey
RESET_L	RESET input to RK3588 and PMIC
PMIC_EXT_EN_OUT	Control the power of carrier board
VDC_MODE	Keep float: power up immediately after VDD_DCIN is powered Short to GND: power up afer PowerKey is pressed









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CM3588 Plus	Rev 2404
Size A2	Page Name 26.Connectors
Date: Monday, May 20, 2024	Sheet: 26/ 26