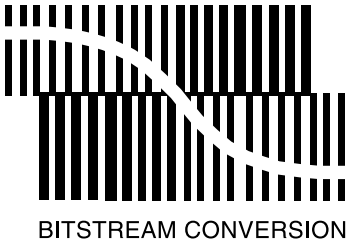
DATA SHEET

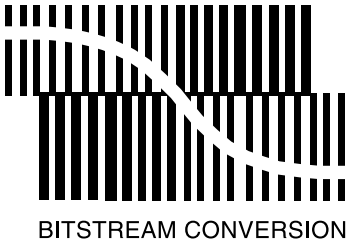


UDA1334ATS
Low power audio DAC with PLL

Product specification
Supersedes data of 2000 Feb 09

2000 Jul 31

集成电路



UDA1334ATS
低功耗音频DAC与PLL

产品规格
取代2000年2月9日的数据

2000年7月31日

CONTENTS

低功耗音频数模转换器与相位锁定环 UDA1334ATS

目录

1 FEATURES

1.1 General

- 2.4 to 3.6 V power supply voltage
- On-board PLL to generate the internal system clock:
  - Operates as an asynchronous DAC, regenerating the internal clock from the WS signal (called audio mode)
  - Generates audio related system clock (output) based on 32, 48 or 96 kHz sampling frequency (called video mode).
- Integrated digital filter plus DAC
- Supports sample frequencies from 16 to 100 kHz in asynchronous DAC mode
- No analog post filtering required for DAC
- Easy application
- SSOP16 package.

1.2 Multiple format data interface

- I^2S-bus and LSB-justified format compatible
- $1f_s$ input data rate.

1.3 DAC digital features

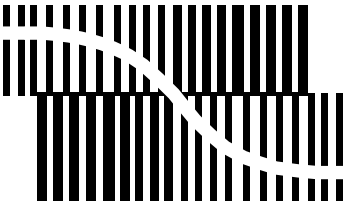
- Digital de-emphasis for 44.1 kHz sampling frequency
- Mute function.

1.4 Advanced audio configuration

- High linearity, wide dynamic range and low distortion.

1.5 PLL system clock generation

- Integrated low jitter PLL for use in applications in which there is digital audio data present but the system cannot provide an audio related system clock. This mode is called audio mode.
- The PLL can generate 256 × 48 kHz and 384 × 48 kHz from a 27 MHz input clock. This mode is called video mode.



2 APPLICATIONS

This audio DAC is excellently suitable for digital audio portable application, specially in applications in which an audio related system clock is not present.

3 GENERAL DESCRIPTION

The UDA1334ATS is a single chip 2 channel digital-to-analog converter employing bitstream conversion techniques, including an on-board PLL. The extremely low power consumption and low voltage requirements make the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates a playback function.

The UDA1334ATS supports the I^2S-bus data format with word lengths of up to 24 bits and the LSB-justified serial data format with word lengths of 16, 20 and 24 bits.

The UDA1334ATS has basic features such as de-emphasis (44.1 kHz sampling frequency, only supported in audio mode) and mute.

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1334ATS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1

低功耗音频数模转换器与相位锁定环 UDA1334ATS

1 特性

1.1 一般信息

- 2.4 到 3.6 V 电源电压
- 板载相位锁定环（PLL）用于生成内部系统时钟：
  – 作为异步数模转换器（DAC）工作，从 WS 信号再生内部时钟（称为音频模式）– 根据 32、48 或 96 kHz 采样频率生成与音频相关的系统时钟（输出）（称为视频模式）。
- 集成数字滤波器与 DAC
- 支持在异步DAC模式下的采样频率范围为16 kHz至100 kHz
- DAC无需模拟后滤波
- 易于应用
- SSOP16封装。

1.2 多种格式数据接口

- 兼容I^2S总线和LSB对齐格式
- $1f_s$ 输入数据速率。

1.3 DAC数字特性

- 44.1 kHz采样频率的数字去强调功能
- 静音功能。

1.4 先进的音频配置

- 高线性度、宽动态范围和低失真。

1.5 PLL系统时钟生成

- 集成低抖动PLL，适用于存在数字音频数据但系统无法提供音频相关系统时钟的应用。此模式称为音频模式。
- PLL可以从27 MHz输入时钟生成256 ×48 kHz和384 ×48 kHz。此模式称为视频模式。

BITSTREAM CONVERSION

2 应用

该音频DAC非常适合数字音频便携式应用，特别是在没有音频相关系统时钟的情况下。

3 一般描述 UDA1334ATS是一

款单芯片2通道数字-模拟转换器，采用比特流转换技术，并集成了一个板载**PLL**。极低的功耗和低电压要求使该设备非常适合用于低电压、低功耗的便携式数字音频设备，且具备播放功能。

UDA1334ATS支持I^2S总线数据格式，字长可达24位，以及LSB对齐的串行数据格式，字长为16、20和24位。

UDA1334ATS具有基本功能，如去强调（44.1 kHz采样频率，仅在音频模式下支持）和静音功能。

4 订购信息

类型编号	封装		
	名称	描述	版本
UDA1334ATS	SSOP16	塑料收缩小外形封装；16个引脚；机身宽度4.4毫米	SOT369-1

5 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	DAC analog supply voltage		2.4	3.0	3.6	V
V_{DDD}	digital supply voltage		2.4	3.0	3.6	V
I_{DDA}	DAC analog supply current	audio mode	–	3.5	–	mA
		video mode	–	3.5	–	mA
I_{DDD}	digital supply current	audio mode	–	2.5	–	mA
		video mode	–	4.5	–	mA
T_{amb}	ambient temperature		−40	–	+85	°C
Digital-to-analog converter (V_{DDA} = V_{DDD} = 3.0 V)						
$V_{o(rms)}$	output voltage (RMS value)	at 0 dB (FS) digital input; note 1	–	900	–	mV
(THD+N)/S	total harmonic distortion-plus-noise to signal ratio	f_s = 44.1 kHz; at 0 dB	–	−90	–	dB
		f_s = 44.1 kHz; at −60 dB; A-weighted	–	−40	–	dB
		f_s = 96 kHz; at 0 dB	–	−85	–	dB
		f_s = 96 kHz; at −60 dB; A-weighted	–	−38	–	dB
S/N	signal-to-noise ratio	f_s = 44.1 kHz; code = 0; A-weighted	–	100	–	dB
		f_s = 96 kHz; code = 0; A-weighted	–	98	–	dB
α_{CS}	channel separation		–	100	–	dB
Power dissipation (at f_s = 44.1 kHz)						
P	power dissipation	audio mode	–	18	–	mW
		video mode	–	24	–	mW

Note

1. The output voltage of the DAC scales proportionally to the power supply voltage.

5 快速参考数据

符号	参数	条件	最小值	典型值	最大值	单位
供应						
V_{DDA}	DAC 模拟供电电压		2.4	3.0	3.6	伏特
V_{DDD}	数字供电电压		2.4	3.0	3.6	伏特
I_{DDA}	DAC 模拟供电电流	音频模式	–	3.5	–	毫安
		视频模式	–	3.5	–	毫安
I_{DDD}	数字供电电流	音频模式	–	2.5	–	毫安
		视频模式	–	4.5	–	毫安
T_{amb}	环境温度		−40	–	+85	°C
数模转换器 (V_{DDA}= V_{DDD}= 3.0 V)						
$V_{o(rms)}$	输出电压 (RMS 值)	在 0 dB (FS) 数字输入下；注 1	–	900	–	毫伏
(THD+N)/S	总谐波失真加噪声与信号比	f_S = 44.1 kHz；在 0 dB	–	−90	–	分贝
		f_S = 44.1 kHz；在 −60 dB; A 加权	–	−40	–	分贝
		f_S = 96 kHz；在 0 dB	–	−85	–	分贝
		f_S = 96 kHz；在 −60 dB; A 加权	–	−38	–	分贝
S/N	信噪比	f_S = 44.1 kHz；代码 = 0；A 加权	–	100	–	分贝
		f_S = 96 kHz；代码 = 0；A 加权	–	98	–	分贝
α_{CS}	通道分离		–	100	–	分贝
功耗（在 f_S= 44.1 kHz 时）						
P	功耗	音频模式	–	18	–	毫瓦
		视频模式	–	24	–	毫瓦

注意

1. DAC的输出电压与电源电压成正比。

6 BLOCK DIAGRAM

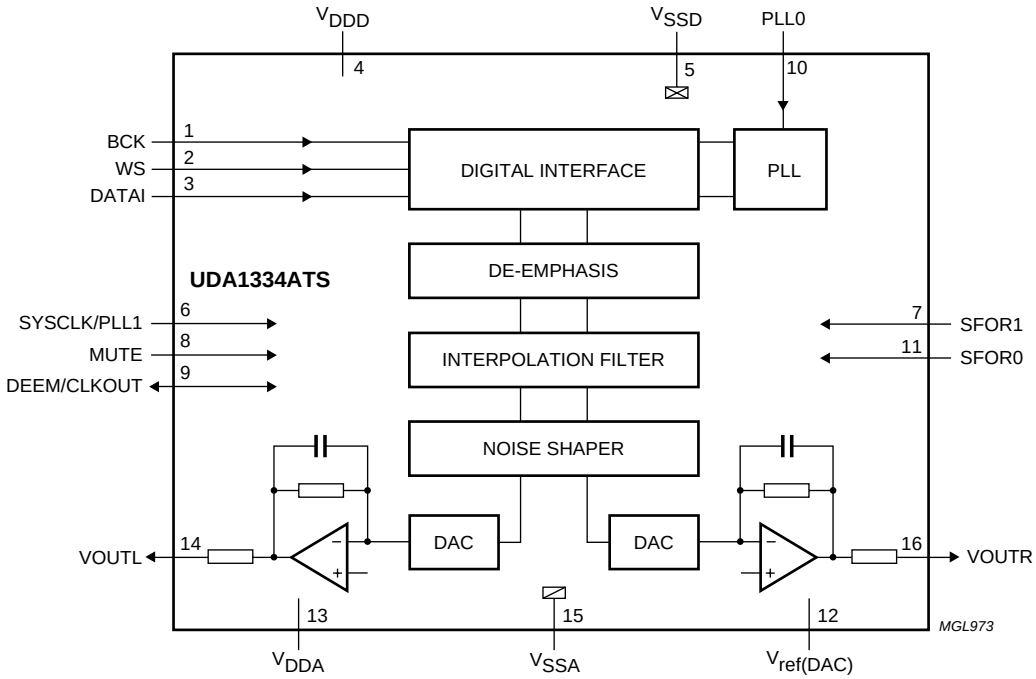


Fig.1 Block diagram.

6 块图

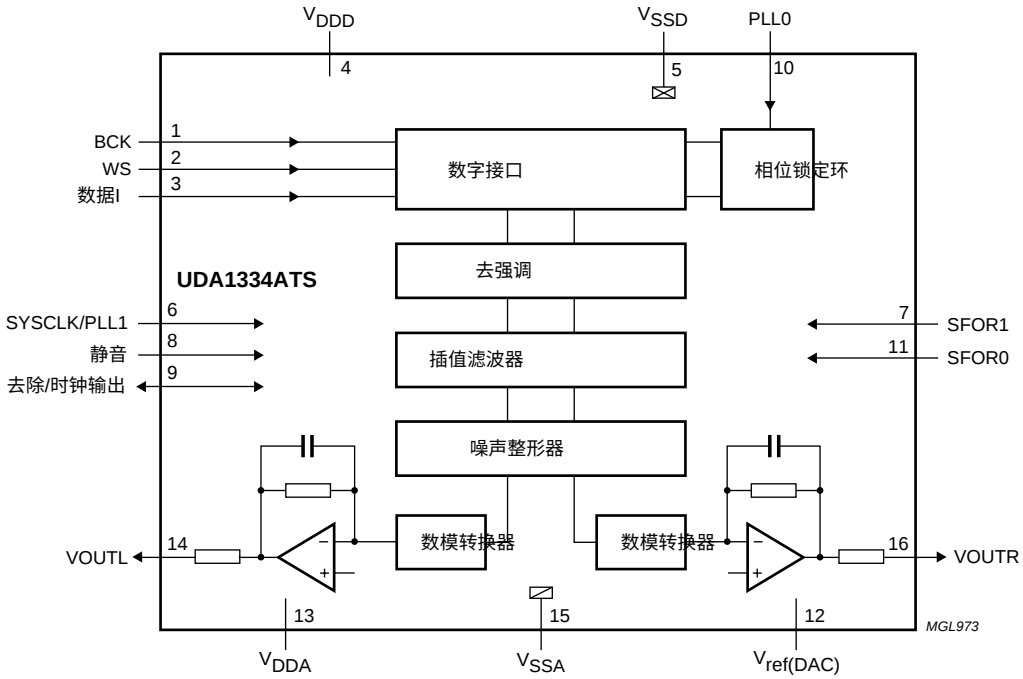

VDDD
VSSD
PLL0
4
5
10
BCK
WS
数据I
1
2
3
数字接口
相位锁定环
去强调
UDA1334ATS
SYSCLK/PLL1
静音
去除/时钟输出
6
8
9
插值滤波器
7
11
SFOR1
SFOR0
噪声整形器
VOUTL
14
数模转换器
数模转换器
16
VOUTR
13
15
12
MGL973
VDDA
VSSA
Vref(DAC)

图1 块图

7 PINNING

SYMBOL	PIN	PAD TYPE	DESCRIPTION
BCK	1	5 V tolerant digital input pad	bit clock input
WS	2	5 V tolerant digital input pad	word select input
DATAI	3	5 V tolerant digital input pad	serial data input
V_{DDD}	4	digital supply pad	digital supply voltage
V_{SSD}	5	digital ground pad	digital ground
SYSCLK/PLL1	6	5 V tolerant digital input pad	system clock input in video mode/PLL mode control 1 input in audio mode
SFOR1	7	5 V tolerant digital input pad	serial format select 1 input
MUTE	8	5 V tolerant digital input pad	mute control input
DEEM/CLKOUT	9	5 V tolerant digital input/output pad	de-emphasis control input in audio mode/clock output in video mode
PLL0	10	3-level input pad; note 1	PLL mode control 0 input
SFOR0	11	digital input pad; note 1	serial format select 0 input
$V_{ref(DAC)}$	12	analog pad	DAC reference voltage
V_{DDA}	13	analog supply pad	DAC analog supply voltage
VOUTL	14	analog output pad	DAC output left
V_{SSA}	15	analog ground pad	DAC analog ground
VOUTR	16	analog output pad	DAC output right

Note

1. Because of test issues these pads are not 5 V tolerant and both pads should be at power supply voltage level or at a maximum of 0.5 V above that level.

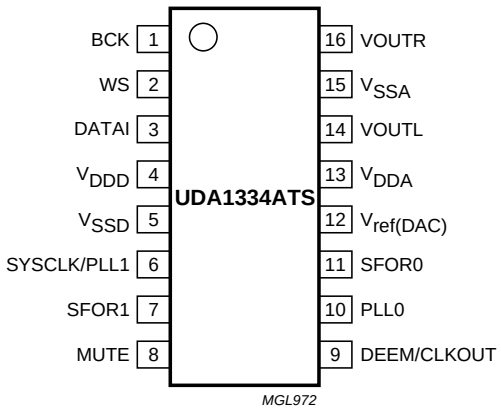


Fig.2 Pin configuration.

7 引脚分配

符号	引脚	焊盘类型	描述
BCK	1	耐受5 V的数字输入焊盘	位时钟输入
WS	2	耐受5 V的数字输入焊盘	字选择输入
数据I	3	耐受5 V的数字输入焊盘	串行数据输入
V_{DDD}	4	数字供电垫	数字供电电压
V_{SSD}	5	数字接地垫	数字接地
SYSCLK/PLL1	6	耐受5 V的数字输入焊盘	视频模式下的系统时钟输入/音频模式下的PLL模式控制1输入
SFOR1	7	耐受5 V的数字输入焊盘	串行格式选择1输入
静音	8	耐受5 V的数字输入焊盘	静音控制输入
去强调/时钟输出	9	5 V耐受数字输入/输出垫	音频模式下的去强调控制输入 视频模式下的时钟输出
PLL0	10	3级输入垫；注意1	PLL模式控制0输入
SFOR0	11	数字输入垫；注意1	串行格式选择0输入
$V_{ref(DAC)}$	12	模拟垫	DAC参考电压
V_{DDA}	13	模拟电源垫	DAC 模拟供电电压
VOUTL	14	模拟输出垫	DAC左输出
V_{SSA}	15	模拟接地垫	DAC模拟接地
VOUTR	16	模拟输出垫	DAC右输出

注意

1. 由于测试问题，这些焊盘不耐受5 V，两个焊盘应处于电源电压水平或最高为该水平的0.5 V。

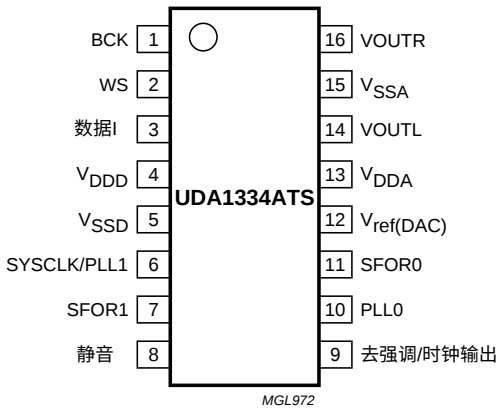


图2 引脚配置

8 FUNCTIONAL DESCRIPTION

8.1 System clock

The UDA1334ATS incorporates a PLL capable of generating the system clock. The UDA1334ATS can operate in 2 modes:

- It operates as an asynchronous DAC, which means the device regenerates the internal clocks using a PLL from the incoming WS signal. This mode is called audio mode.
- It generates the internal clocks from a 27 MHz clock input, based on 32, 48 and 96 kHz sampling frequencies. This mode is called video mode.

In video mode, the digital audio input is slave, which means that the system must generate the BCK and WS signals from the output clock available at pin CLKOUT of the UDA1334ATS. The digital audio signals should be frequency locked to the CLKOUT signal.

Remarks:

1. The WS edge MUST fall on the negative edge of the BCK at all times for proper operation of the digital I/O data interface
2. For LSB-justified formats it is important to have a WS signal with a duty factor of 50%.

8.1.1 AUDIO MODE

Audio mode is enabled by setting pin PLL0 to LOW. De-emphasis can be activated via pin DEEM/CLKOUT according to Table 5.

In audio mode, pin SYSCLK/PLL1 is used to set the sampling frequency range as given in Table 1.

Table 1 Sampling frequency range in audio mode

SYSCLK/PLL1	SELECTION
LOW	f_s = 16 to 50 kHz
HIGH	f_s = 50 to 100 kHz

8.1.2 VIDEO MODE

In video mode, the master clock is a 27 MHz external clock (as is available in video environment). A clock-out signal is generated at pin DEEM/CLKOUT. The output frequency can be selected using pin PLL0. The output frequency is either 12.228 MHz (256 × 48 kHz) with pin PLL0 being at MID level or 18.432 MHz (384 × 48 kHz) with pin PLL0 being HIGH, as given in Table 2.

Table 2 Clock output selection in video mode

PLL0	SELECTION
MID	12.228 MHz clock; note 1
HIGH	18.432 MHz clock; note 2
LOW	audio mode

Notes

1. The supported sampling frequencies are: 96, 48 and 24 kHz or 64, 32 and 16 kHz.
2. The supported sampling frequencies are: 96, 48 and 24 kHz; 72 and 36 kHz or 32 kHz.

8.2 Interpolation filter

The interpolation digital filter interpolates from $1f_s$ to $64f_s$ by cascading FIR filters (see Table 3).

Table 3 Interpolation filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass-band ripple	$0f_s$ to $0.45f_s$	±0.02
Stop band	$>0.55f_s$	−50
Dynamic range	$0f_s$ to $0.45f_s$	>114

8.3 Noise shaper

The 5th-order noise shaper operates at $64f_s$. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a Filter Stream DAC (FSDAC).

8 功能描述

8.1 系统时钟

UDA1334ATS集成了一个能够生成系统时钟的PLL。UDA1334ATS可以在两种模式下工作：

- 它作为异步DAC工作，这意味着设备使用来自输入WS信号的PLL再生内部时钟。此模式称为音频模式。
- 它根据32、48和96 kHz的采样频率，从27 MHz时钟输入生成内部时钟。此模式称为视频模式。

在视频模式下，数字音频输入为从属，这意味着系统必须从UDA1334ATS的CLKOUT引脚可用的输出时钟生成BCK和WS信号。数字音频信号应与CLKOUT信号频率锁定。备注：

1. WS边缘必须始终在BCK的负边缘上下降，以确保数字I/O数据接口的正常操作
2. 对于LSB对齐格式，WS信号的占空比必须为50%，这非常重要。

8.1.1 音频模式

通过将引脚PLL0设置为低电平来启用音频模式。去强调功能可以通过引脚DEEM/CLKOUT激活，具体见表5。

在音频模式下，引脚SYSCLK/PLL1用于设置采样频率范围，如表1所示。

表**1** 音频模式下的采样频率范围

SYSCLK/PLL1	选择
低	f_S = 16 到 50 kHz
高	f_S = 50 到 100 kHz

8.1.2 视频模式

在视频模式下，主时钟为27 MHz的外部时钟（在视频环境中可用）。在引脚DEEM/CLKOUT生成时钟输出信号。输出频率可以通过引脚PLL0进行选择。当引脚PLL0处于中间电平时，输出频率为12.228 MHz（256 ×48 kHz）；当引脚PLL0处于高电平时，输出频率为18.432 MHz（384 ×48 kHz），具体见表2。

表**2** 视频模式下的时钟输出选择

PLL0	选择
中	12.228 MHz 时钟；注 1
高	18.432 MHz 时钟；注 2
低	音频模式

备注

1. 支持的采样频率为：
   96、48和24 kHz，或64、32和16 kHz。
2. 支持的采样频率为：
   96、48和24 kHz；72和36 kHz，或32 kHz。

8.2 插值滤波器

插值数字滤波器通过级联FIR滤波器将1f_S插值到64f_S（见表3）。

表**3** 插值滤波器特性

项目	条件	值 (dB)
通带波动	0f_S 到 0.45f_S	±0.02
阻带	>0.55f_S	−50
动态范围	0f_S 到 0.45f_S	>114

8.3 噪声整形器

5阶噪声整形器在64f_S下工作。它将带内量化噪声移至远高于音频带的频率。这种噪声整形技术使得可以实现高信噪比。噪声整形器的输出通过滤波流DAC（FSDAC）转换为模拟信号。

8.4 Filter stream DAC

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. No post filter is needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportionally to the power supply voltage.

8.5 Power-on reset

The UDA1334ATS has an internal Power-on reset circuit (see Fig.3) which resets the test control block.

The reset time (see Fig.4) is determined by an external capacitor which is connected between pin $V_{ref(DAC)}$ and ground. The reset time should be at least 1 μs for $V_{ref(DAC)} < 1.25$ V. When V_{DDA} is switched off, the device will be reset again for $V_{ref(DAC)} < 0.75$ V.

During the reset time the system clock should be running.

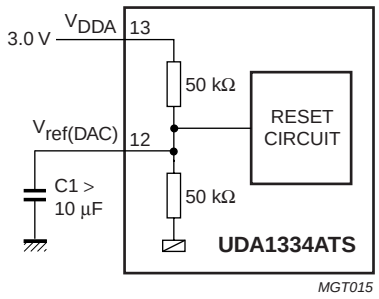


Fig.3 Power-on reset circuit.

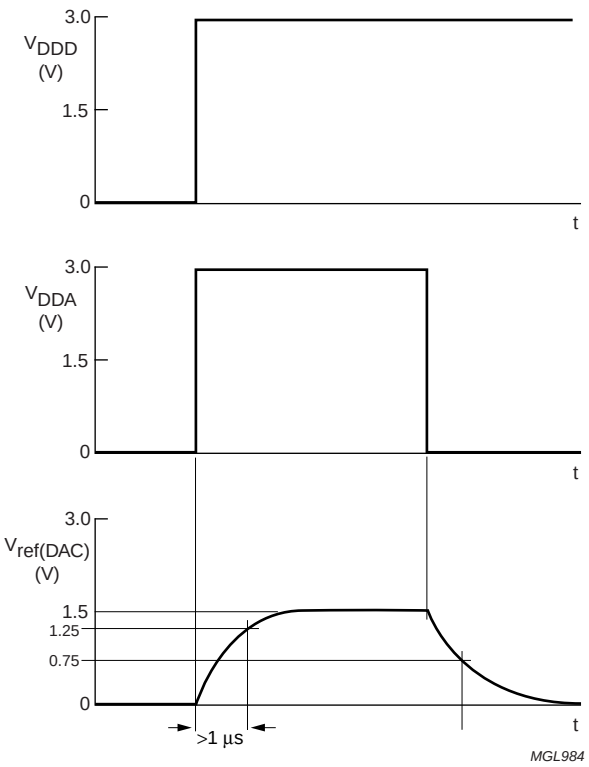


Fig.4 Power-on reset timing.

8.4 滤波流 DAC

FSDAC 是一种半数字重构滤波器，将噪声整形器的 1 位数据流转换为模拟输出电压。滤波器系数作为电流源实现，并在输出运算放大器的虚地处相加。通过这种方式，实现了非常高的信噪比性能和低时钟抖动敏感性。由于 DAC 的固有滤波功能，不需要后置滤波器。板载放大器将 FSDAC 输出电流转换为能够驱动线路输出的电压信号。

8.5 上电复位

UDA1334ATS内部具有上电复位电路（见图3），用于重置测试控制块。

复位时间（见图4）由连接在引脚$V_{ref(DAC)}$和地之间的外部电容决定。对于Vref(DAC)< 1.25 V，复位时间应至少为1μs。当V_{DDA}关闭时，设备将在$V_{ref(DAC)}$< 0.75 V时再次复位。在复位期间，系统时钟应保持运行。

FSDAC的输出电压与电源电压成正比。

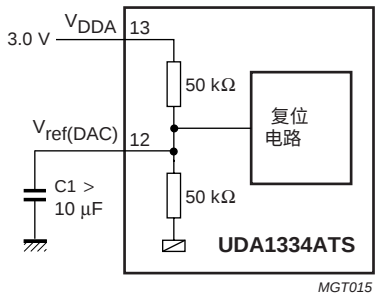


图3 上电复位电路。

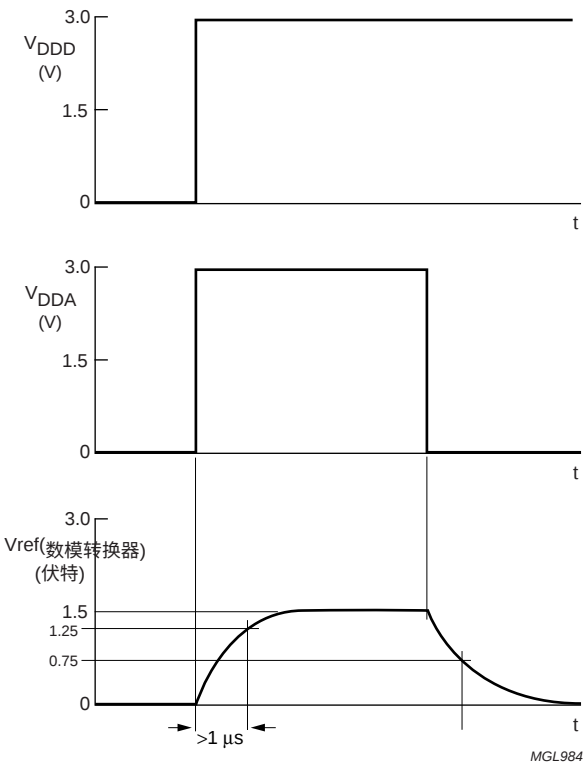


图4 上电复位时序

8.6 Feature settings

8.6.1 Digital interface format select

The digital audio interface formats (see Fig.5) can be selected via pins SFOR1 and SFOR0 as shown in Table 4.

For the digital audio interface holds that the BCK frequency can be maximum 64 times WS frequency.

The WS signal must change at the negative edge of the BCK signal for all digital audio formats.

Table 4 Data format selection

SFOR1	SFOR0	INPUT FORMAT
LOW	LOW	I^2S-bus input
LOW	HIGH	LSB-justified 16 bits input
HIGH	LOW	LSB-justified 20 bits input
HIGH	HIGH	LSB-justified 24 bits input

8.6.2 De-emphasis control

This function is only available in audio mode. In that case, pin DEEM/CLKOUT can be used to activate the digital de-emphasis for 44.1 kHz as given in Table 5.

Table 5 De-emphasis control (audio mode)

DEEM/CLKOUT	FUNCTION
LOW	de-emphasis off
HIGH	de-emphasis on

8.6.3 Mute control

The output signal can be soft muted by setting pin MUTE to HIGH as given in Table 6.

Table 6 Mute control

MUTE	FUNCTION
LOW	mute off
HIGH	mute on

8.6 功能设置

8.6.1 数字接口格式选择

数字音频接口格式（见图5）可以通过引脚SFOR1和SFOR0进行选择，如表4所示。

对于数字音频接口，BCK频率最大可达WS频率的64倍。

WS信号必须在BCK信号的负边缘变化，适用于所有数字音频格式。

表**4** 数据格式选择

SFOR1	SFOR0	输入格式
低	低	I^2S总线输入
低	高	LSB对齐 16位输入
高	低	LSB对齐 20位输入
高	高	LSB对齐 24位输入

8.6.2 去强调控制

此功能仅在音频模式下可用。在这种情况下，引脚DEEM/CLKOUT可用于激活44.1 kHz的数字去强调，如表5所示。

表**5** 去强调控制（音频模式）

去强调/时钟输出	功能
低	去强调关闭
高	去强调开启

8.6.3 静音控制

通过将MUTE引脚设置为高电平，可以软静音输出信号，如表6所示。

表**6** 静音控制

静音	功能
低	静音关闭
高	静音开启

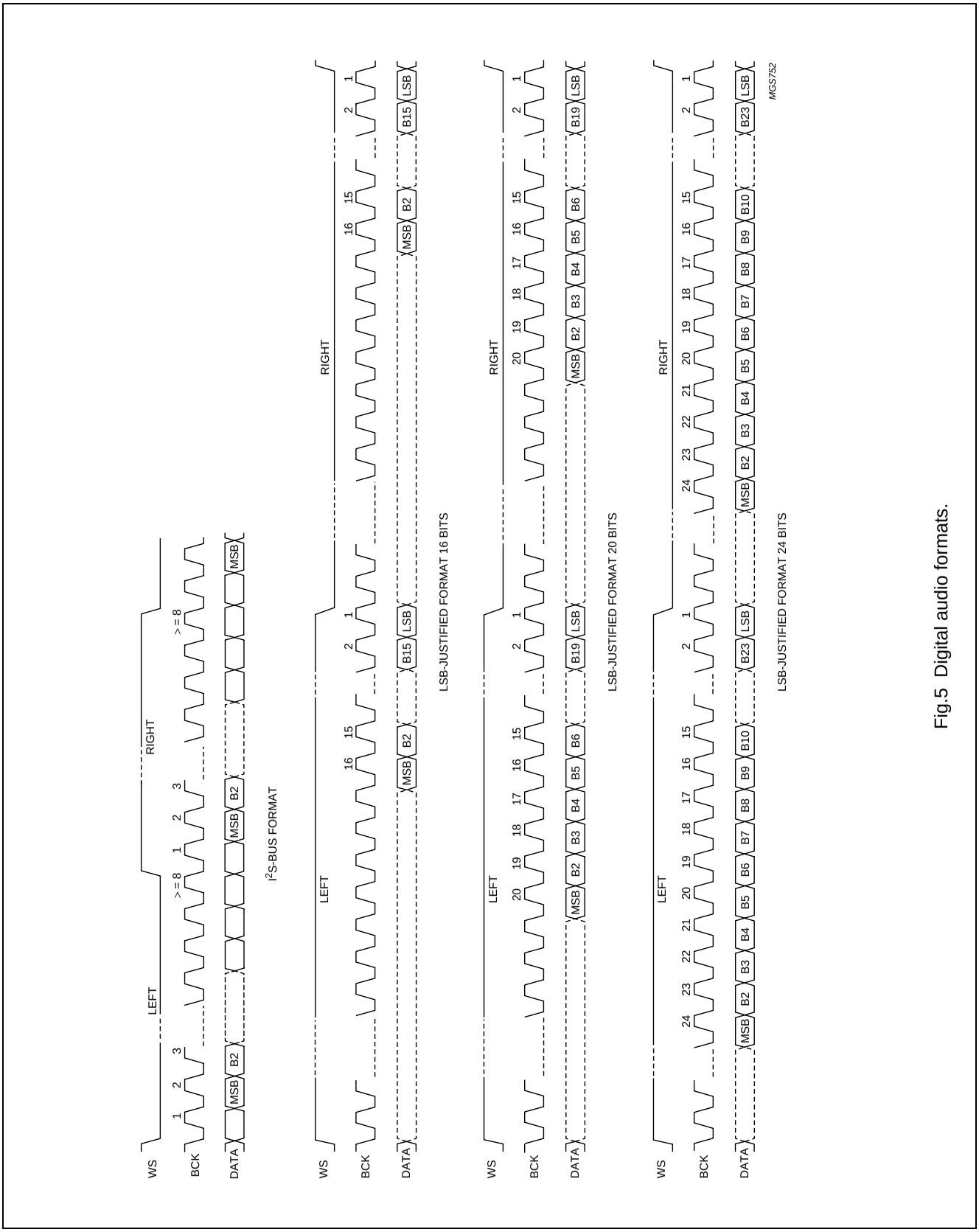


Fig.5 Digital audio formats.

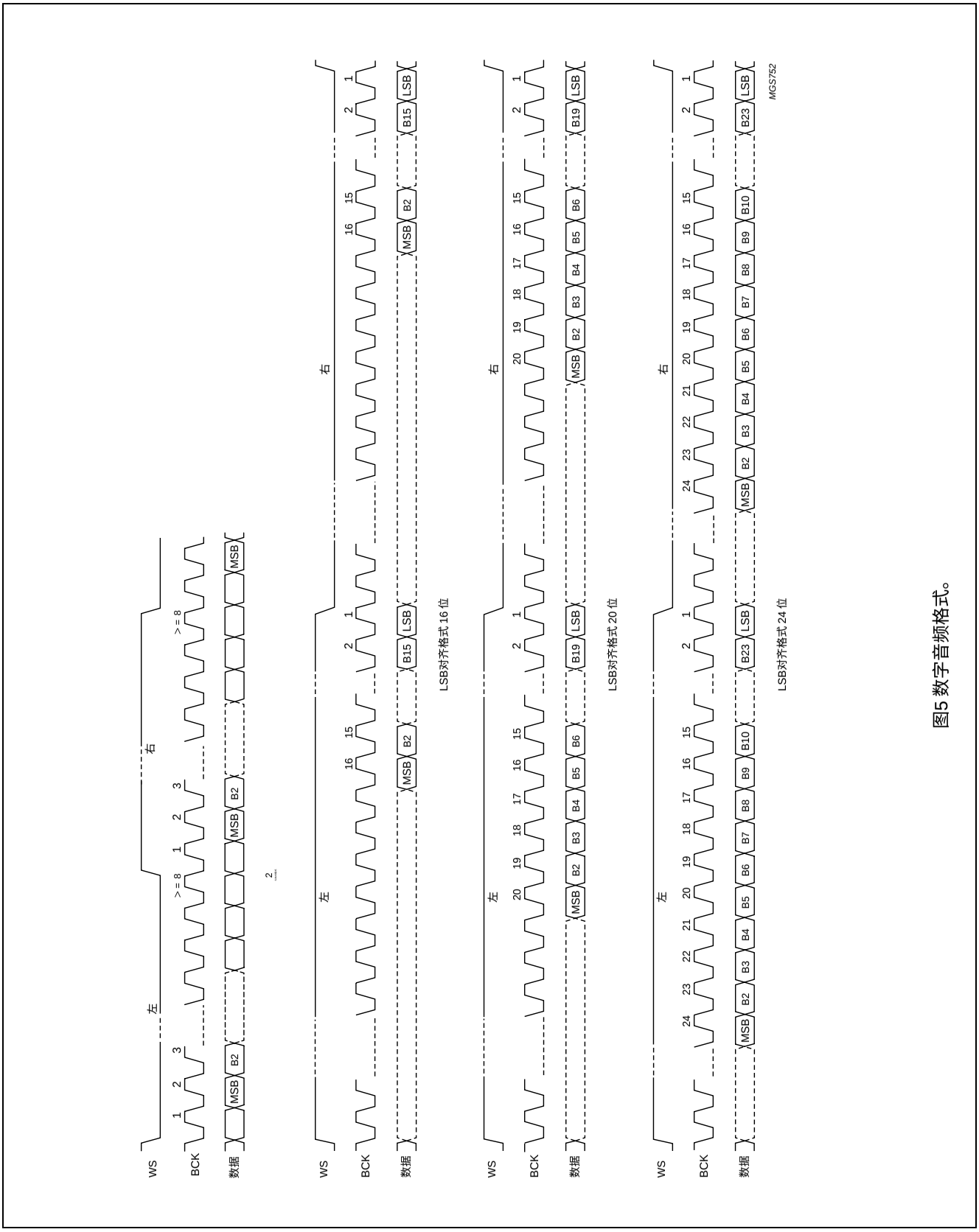

WS
BCK
数据
左
右
MSB
B2
B15
LSB
B19
B23
B3
B4
B5
B6
B7
B8
B9
B10
>= 8
LSB对齐格式 16 位
LSB对齐格式 20 位
LSB对齐格式 24 位
MGS752

图5 数字音频格式。

9 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DD}	supply voltage	note 1	–	4.0	V
$T_{xtal(max)}$	maximum crystal temperature		–	150	°C
T_{stg}	storage temperature		−65	+125	°C
T_{amb}	ambient temperature		−40	+85	°C
V_{es}	electrostatic handling voltage	human body model; note 2	−2000	+2000	V
		machine model; note 2	−250	+250	V
$I_{sc(DAC)}$	short-circuit current of DAC	note 3			
		output short-circuited to V_{SSA}	–	450	mA
		output short-circuited to V_{DDA}	–	300	mA

Notes

1. All supply connections must be made to the same power supply.
2. ESD behaviour is tested according to JEDEC II standard.
3. Short-circuit test at T_{amb} = 0 °C and V_{DDA} = 3 V. DAC operation after short-circuiting cannot be warranted.

10 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

11 THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	145	K/W

12 QUALITY SPECIFICATION

In accordance with *"SNW-FQ-611-E"*.

13 DC CHARACTERISTICS

$V_{DDD} = V_{DDA}$ = 3.0 V; T_{amb} = 25 °C; R_L = 5 kΩ; all voltages with respect to ground (pins V_{SSA} and V_{SSD}); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDA}	DAC analog supply voltage	note 1	2.4	3.0	3.6	V
V_{DDD}	digital supply voltage	note 1	2.4	3.0	3.6	V
I_{DDA}	DAC analog supply current	audio mode	–	3.5	–	mA
		video mode	–	3.5	–	mA
I_{DDD}	digital supply current	audio mode	–	2.5	–	mA
		video mode	–	4.5	–	mA

9 限制值

根据绝对最大额定值系统（IEC 60134）。

符号	参数	条件	最小值	最大值	单位
V_{DD}	供电电压	注 1	–	4.0	伏特
$T_{xtal(max)}$	最大晶体温度		–	150	°C
T_{stg}	储存温度		–65	+125	°C
T_{amb}	环境温度		–40	+85	°C
V_{es}	静电处理电压（人体模型）；注 2		–2000	+2000	伏特
		机器模型；注 2	–250	+250	伏特
$I_{sc(DAC)}$	DAC的短路电流注 3				
		输出短路至 V_{SSA}	–	450	毫安
		输出短路至 V_{DDA}	–	300	毫安

备注

1. 所有供电连接必须连接到同一电源。
2. ESD行为根据JEDEC II标准进行测试。
3. 在T_{amb}= 0 °C和V_{DDA}= 3 V下进行短路测试。短路后DAC的操作无法保证。

10 处理

输入和输出在正常操作中受到静电放电的保护。然而，为了确保安全，建议采取适当的常规预防措施来处理MOS器件。

11 热特性

符号	参数	条件	值	单位
$R_{th(j-a)}$	从结到环境的热阻	在自由空气中	145	K/W

12 质量规格

根据*“SNW-FQ-611-E”*。

13 直流特性

V_{DDD}= V_{DDA}= 3.0 V；T_{amb}= 25 °C；R_L= 5 kΩ；所有电压相对于地（引脚V_{SSA}和V_{SSD}）；除非另有说明。

符号	参数	条件	最小值	典型值	最大值	单位
供应						
V_{DDA}	数模转换器模拟供电电压注释 1		2.4	3.0	3.6	伏特
V_{DDD}	数字供电电压	注 1	2.4	3.0	3.6	伏特
I_{DDA}	数模转换器模拟供电电流音频模式		–	3.5	–	毫安
		视频模式	–	3.5	–	毫安
I_{DDD}	数字供电电流	音频模式	–	2.5	–	毫安
		视频模式	–	4.5	–	毫安

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital input pins: TTL compatible						
V_{IH}	HIGH-level input voltage		2.0	–	5.0	V
V_{IL}	LOW-level input voltage		−0.5	–	+0.8	V
$\lvert I_{LI} \rvert$	input leakage current		–	–	1	μA
C_i	input capacitance		–	–	10	pF
3-level input: pin PLL0						
V_{IH}	HIGH-level input voltage		$0.9V_{DDD}$	–	V_{DDD} + 0.5	V
V_{IM}	MID-level input voltage		$0.4V_{DDD}$	–	$0.6V_{DDD}$	V
V_{IL}	LOW-level input voltage		−0.5	–	+0.5	V
Digital output pins						
V_{OH}	HIGH-level output voltage	I_{OH} = −2 mA	$0.85V_{DDD}$	–	–	V
V_{OL}	LOW-level output voltage	I_{OL} = 2 mA	–	–	0.4	V
DAC						
$V_{ref(DAC)}$	reference voltage	with respect to V_{SSA}	$0.45V_{DD}$	$0.5V_{DD}$	$0.55V_{DD}$	V
$R_{o(ref)}$	output resistance on pin $V_{ref(DAC)}$		–	25	–	kΩ
$I_{o(max)}$	maximum output current	(THD + N)/S < 0.1%; R_L = 5 kΩ	–	1.6	–	mA
R_L	load resistance		3	–	–	kΩ
C_L	load capacitance	note 2	–	–	50	pF

Notes

1. All supply connections must be made to the same external power supply unit.
2. When the DAC drives a capacitive load above 50 pF, a series resistance of 100 Ω must be used to prevent oscillations in the output operational amplifier.

14 AC CHARACTERISTICS

14.1 Analog

$V_{DDD} = V_{DDA}$ = 3.0 V; f_i = 1 kHz; T_{amb} = 25 °C; R_L = 5 kΩ; all voltages with respect to ground (pins V_{SSA} and V_{SSD}); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
DAC				
$V_{o(rms)}$	output voltage (RMS value)	at 0 dB (FS) digital input; note 1	900	mV
ΔV_o	unbalance between channels		0.1	dB
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f_s = 44.1 kHz; at 0 dB	−90	dB
		f_s = 44.1 kHz; at −60 dB; A-weighted	−40	dB
		f_s = 96 kHz; at 0 dB	−85	dB
		f_s = 96 kHz; at −60 dB; A-weighted	−38	dB

符号	参数	条件	最小值	典型值	最大值	单位
数字输入引脚：TTL 兼容						
V_{IH}	高电平输入电压		2.0	–	5.0	伏特
V_{IL}	低电平输入电压		−0.5	–	+0.8	伏特
$\|I_{LI}\|$	输入漏电流		–	–	1	μA
C_i	输入电容		–	–	10	pF
3级输入：引脚 PLL0						
V_{IH}	高电平输入电压		$0.9V_{DDD}$	–	V_{DDD} + 0.5	伏特
V_{IM}	中间输入电压		$0.4V_{DDD}$	–	$0.6V_{DDD}$	伏特
V_{IL}	低电平输入电压		−0.5	–	+0.5	伏特
数字输出引脚						
V_{OH}	高电平输出电压	I_{OH} = −2 毫安	$0.85V_{DDD}$	–	–	伏特
V_{OL}	低电平输出电压	I_{OL} = 2 毫安	–	–	0.4	伏特
数模转换器						
$V_{ref(DAC)}$	参考电压	相对于 V_{SSA}	$0.45V_{DD}$	$0.5V_{DD}$	$0.55V_{DD}$	伏特
$R_{o(ref)}$	输出电阻开启 引脚 $V_{ref(DAC)}$		–	25	–	kΩ
$I_{o(max)}$	最大输出电流	(THD + N)/S < 0.1%; R_L = 5 kΩ	–	1.6	–	毫安
R_L	负载电阻		3	–	–	kΩ
C_L	负载电容	注 2	–	–	50	pF

备注

1. 所有供电连接必须连接到同一个外部电源单元。
2. 当数模转换器驱动超过50 pF的电容负载时，必须使用100 Ω的串联电阻以防止输出运算放大器发生振荡。

14 AC 特性

14.1 模拟

V_{DDD}= V_{DDA}= 3.0 V; f_i= 1 kHz; T_{amb}= 25 °C; R_L= 5 kΩ; 所有电压相对于地（引脚 V_{SSA}和 V_{SSD}）；除非另有说明。

符号	参数	条件	典型值	单位
数模转换器				
$V_{o(rms)}$	输出电压 (RMS 值)	在 0 dB (FS) 数字输入下；注 1	900	毫伏
ΔV_o	通道之间的不平衡		0.1	分贝
(THD + N)/S	总谐波失真加 噪声与信号比	f_S = 44.1 kHz；在 0 dB	−90	分贝
		f_S = 44.1 kHz；在 −60 dB；A加权	−40	分贝
		f_S = 96 kHz；在 0 dB	−85	分贝
		f_S = 96 kHz；在 −60 dB；A加权	−38	分贝

SYMBOL	PARAMETER	CONDITIONS	TYP.	UNIT
S/N	signal-to-noise ratio	f_s = 44.1 kHz; code = 0; A-weighted	100	dB
		f_s = 96 kHz; code = 0; A-weighted	98	dB
α_{CS}	channel separation		100	dB
PSRR	power supply rejection ratio	f_{ripple} = 1 kHz; V_{ripple} = 30 mV (p-p)	60	dB

Note

1. The output voltage of the DAC scales proportionally to the analog power supply voltage.

14.2 Timing

$V_{DDD} = V_{DDA}$ = 2.4 to 3.6 V; T_{amb} = −20 to +85 °C; R_L = 5 kΩ; all voltages with respect to ground (pins V_{SSA} and V_{SSD}); unless otherwise specified; note 1.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output clock timing in video mode (see Fig.6)						
T_{sys}	output clock cycle	f_o = 12.228 MHz	–	81.38	–	ns
		f_o = 18.432 MHz	–	54.25	–	ns
t_{CWL}	output clock LOW time	f_o = 12.228 MHz	$0.3T_{sys}$	–	$0.7T_{sys}$	ns
		f_o = 18.432 MHz	$0.4T_{sys}$	–	$0.6T_{sys}$	ns
t_{CWH}	output clock HIGH time	f_o = 12.228 MHz	$0.3T_{sys}$	–	$0.7T_{sys}$	ns
		f_o = 18.432 MHz	$0.4T_{sys}$	–	$0.6T_{sys}$	ns
Serial input data timing (see Fig.7)						
f_{BCK}	bit clock frequency		–	–	$64f_s$	Hz
t_{BCKH}	bit clock HIGH time		50	–	–	ns
t_{BCKL}	bit clock LOW time		50	–	–	ns
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{su(DATAI)}$	set-up time data input		20	–	–	ns
$t_{h(DATAI)}$	hold time data input		0	–	–	ns
$t_{su(WS)}$	set-up time word select		20	–	–	ns
$t_{h(WS)}$	hold time word select		10	–	–	ns

Note

1. The typical value of the timing is specified for a sampling frequency of 44.1 kHz.

符号	参数	条件	典型值	单位
S/N	信噪比	f_s = 44.1 kHz; 代码 = 0; A 加权	100	分贝
		f_s = 96 kHz; 代码 = 0; A 加权	98	分贝
α_{CS}	通道分离		100	分贝
PSRR	电源抑制比	f_{ripple} = 1 kHz; V_{ripple} = 30 mV (峰峰值)	60	分贝

注意

1. DAC 的输出电压与模拟电源电压成比例缩放。

14.2 定时

V_{DDD}= V_{DDA}= 2.4 到 3.6 V; T_{amb} = −20 到 +85 °C; R_L= 5 kΩ; 所有电压相对于地（引脚 V_{SSA}和 V_{SSD}）；除非另有说明；注 1。

符号	参数	条件	最小值	典型值	最大值	单位
视频模式下的输出时钟定时（见图 6）						
T_{sys}	输出时钟周期	f_o = 12.228 MHz	–	81.38	–	纳秒
		f_o = 18.432 MHz	–	54.25	–	纳秒
t_{CWL}	输出时钟低电平时间	f_o = 12.228 MHz	$0.3T_{sys}$	–	$0.7T_{sys}$	纳秒
		f_o = 18.432 MHz	$0.4T_{sys}$	–	$0.6T_{sys}$	纳秒
t_{CWH}	输出时钟高电平时间	f_o = 12.228 MHz	$0.3T_{sys}$	–	$0.7T_{sys}$	纳秒
		f_o = 18.432 MHz	$0.4T_{sys}$	–	$0.6T_{sys}$	纳秒
串行输入数据时序(见图7)						
f_{BCK}	位时钟频率		–	–	$64f_s$	赫兹
t_{BCKH}	位时钟高电平时间		50	–	–	纳秒
t_{BCKL}	位时钟低电平时间		50	–	–	纳秒
t_r	上升时间		–	–	20	纳秒
t_f	下降时间		–	–	20	纳秒
$t_{su(DATAI)}$	数据输入的设置时间		20	–	–	纳秒
$t_{h(DATAI)}$	数据输入的保持时间		0	–	–	纳秒
$t_{su(WS)}$	字选择的设置时间		20	–	–	纳秒
$t_{h(WS)}$	字选择的保持时间		10	–	–	纳秒

注意

1. 定时的典型值是在采样频率为 44.1 kHz 时指定的。

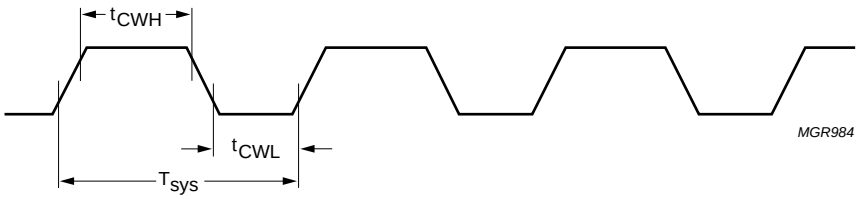


Fig.6 Output clock timing.

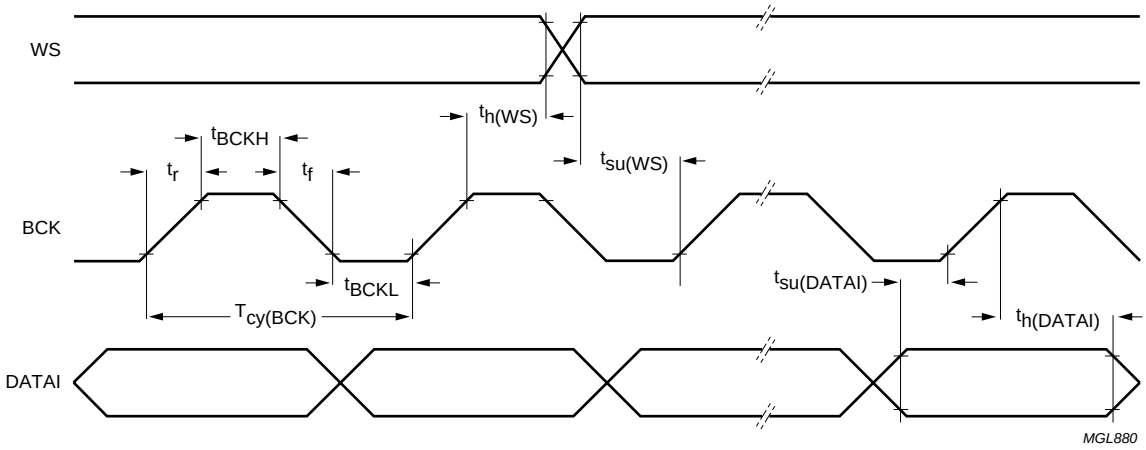


Fig.7 Serial interface timing.

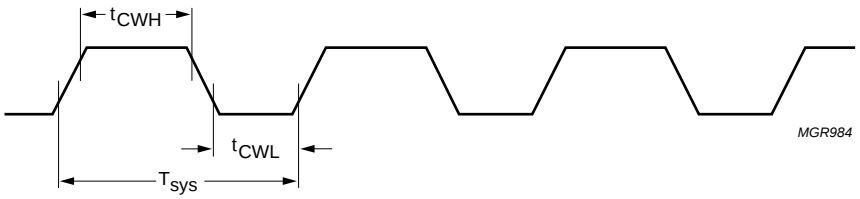


图6 输出时钟时序

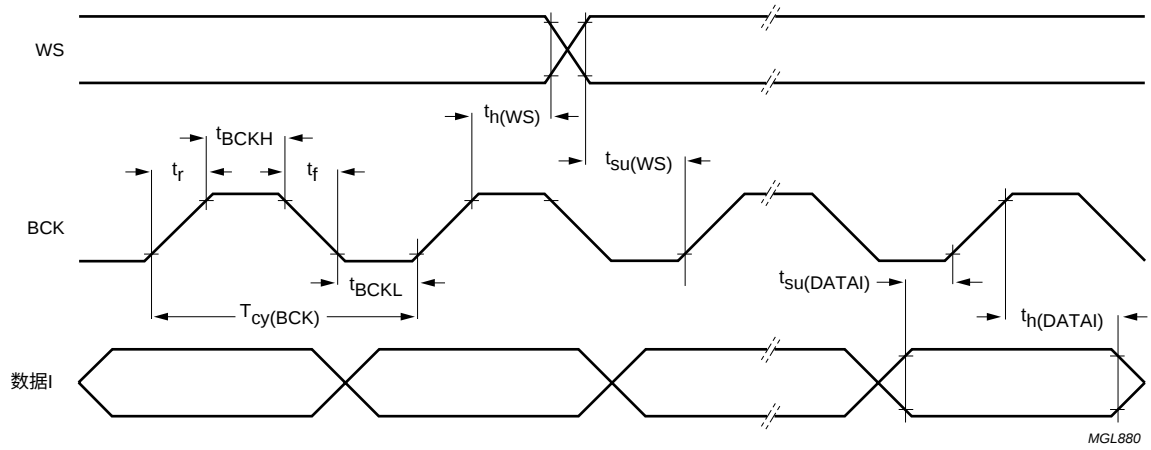
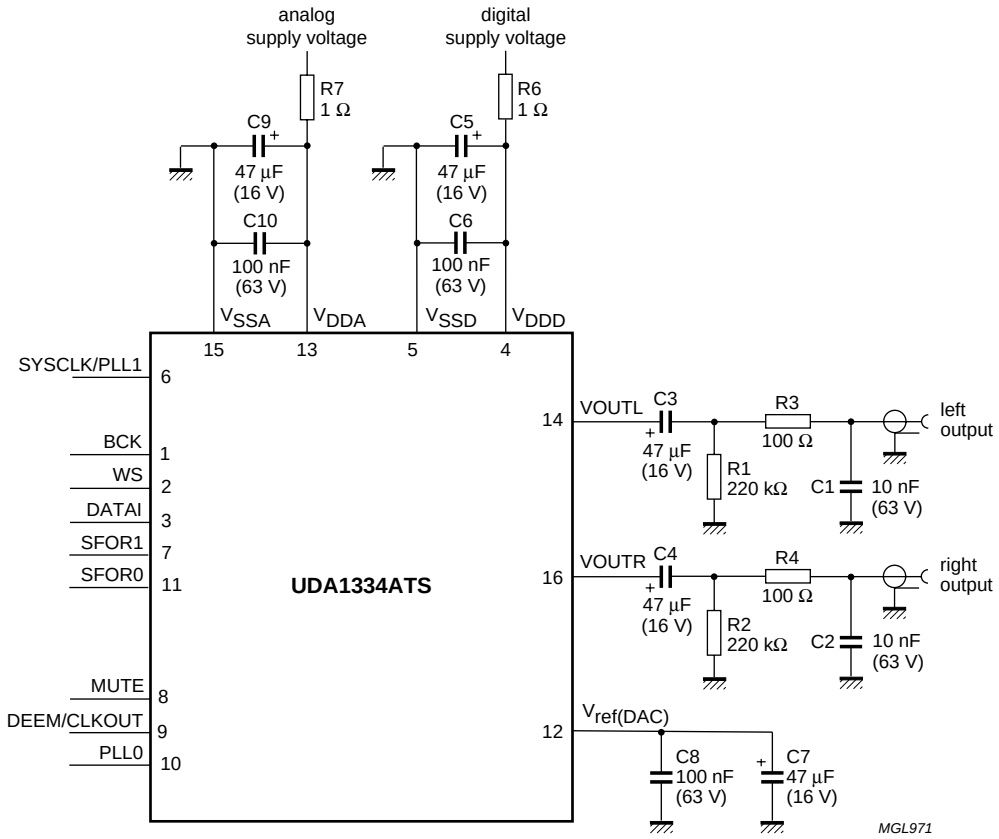


图7 串行接口时序

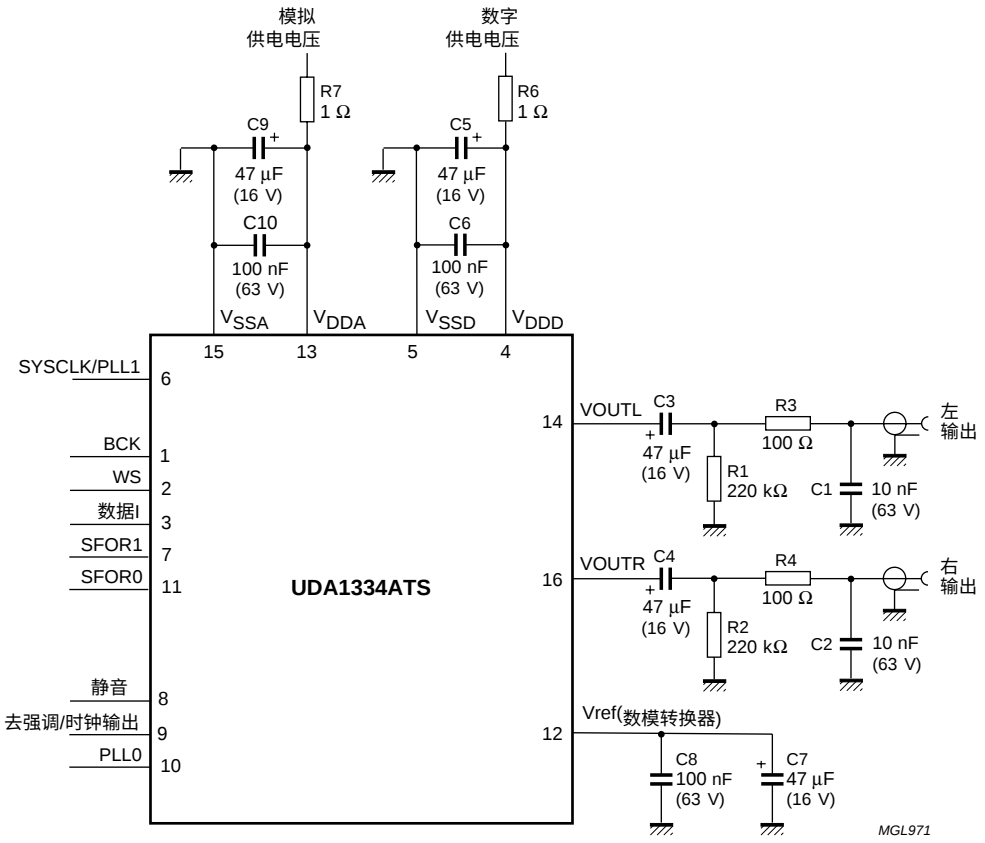
15 APPLICATION INFORMATION



In audio mode, the system does not need to supply a system clock.

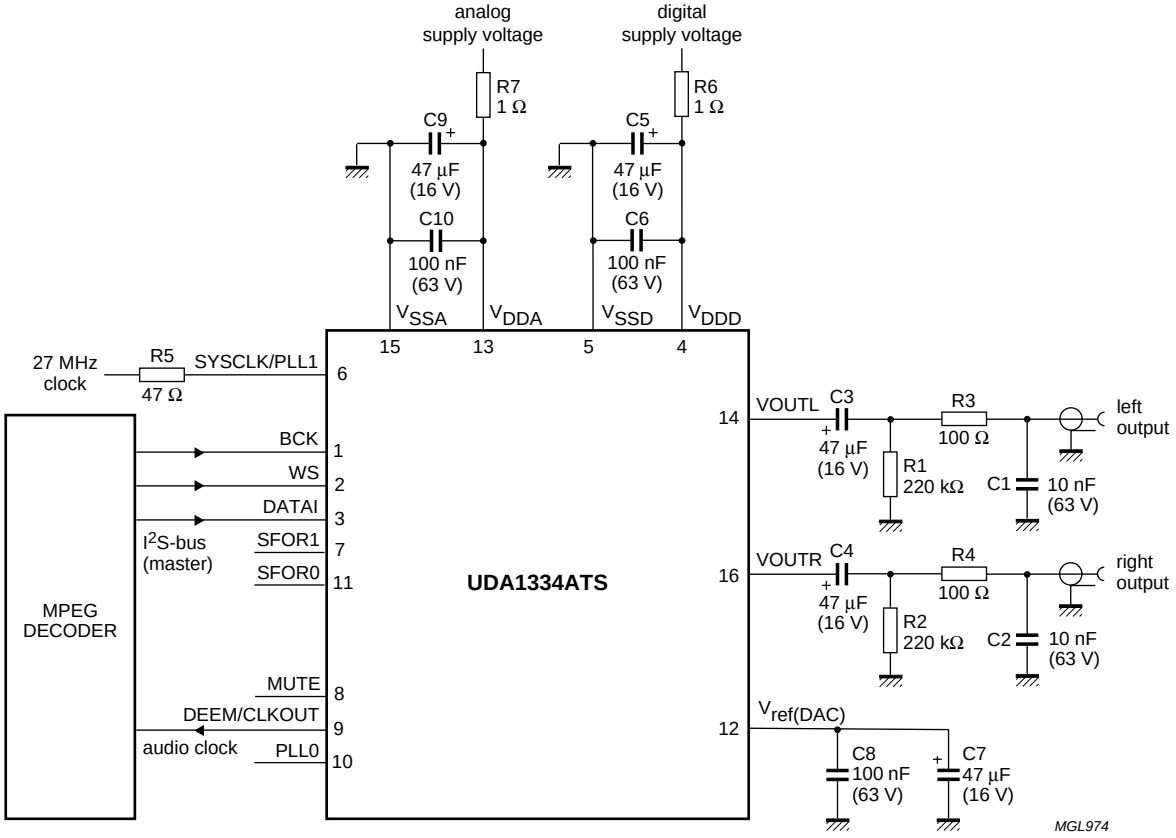
Fig.8 Audio mode application diagram.

15 应用信息



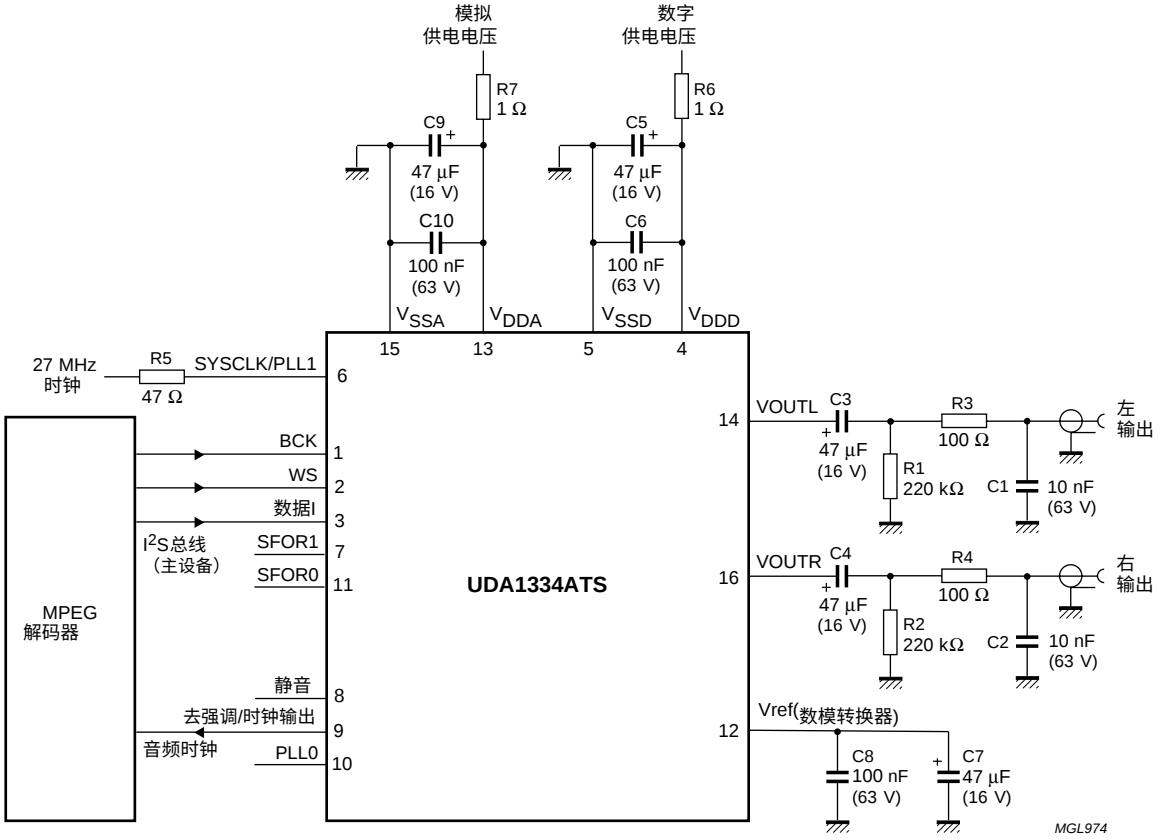
在音频模式下，系统无需提供系统时钟。

图8 音频模式应用图



In video mode, a clock output signal is generated by the UDA1334ATS which is master for the audio signals in the system; the digital audio interface is slave, which means the system must generate the BCK and WS signal from the UDA1334ATS output clock.

Fig.9 Video mode application diagram.

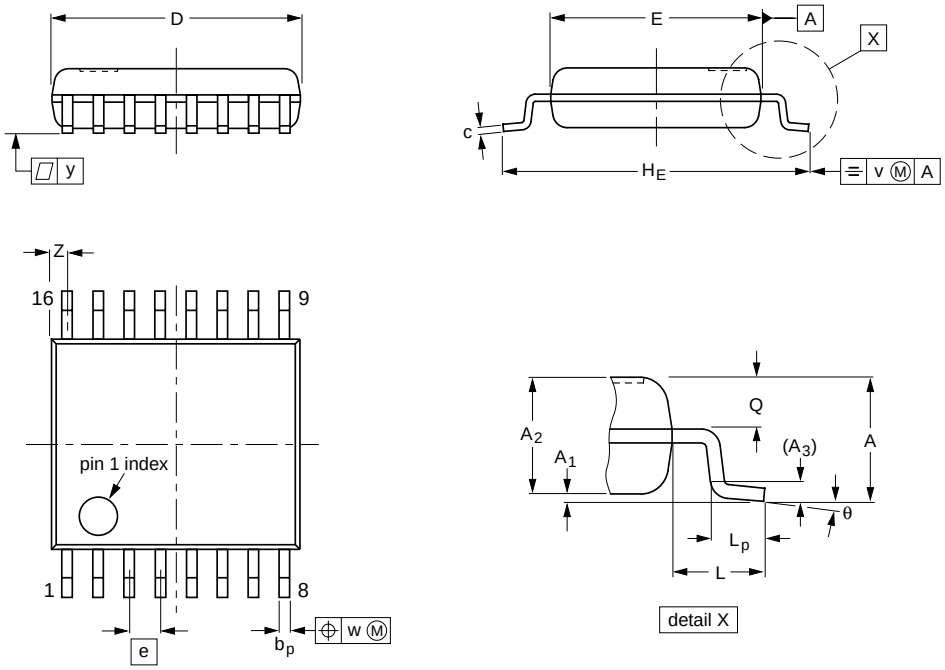


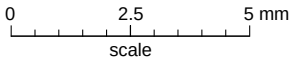
在视频模式下，UDA1334ATS生成一个时钟输出信号，该信号是系统中音频信号的主时钟；数字音频接口为从设备，这意味着系统必须从UDA1334ATS的输出时钟生成BCK和WS信号。

图9 视频模式应用图

16 PACKAGE OUTLINE

SSOP16: plastic shrink small outline package; 16 leads; body width 4.4 mm **SOT369-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.3 5.1	4.5 4.3	0.65	6.6 6.2	1	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

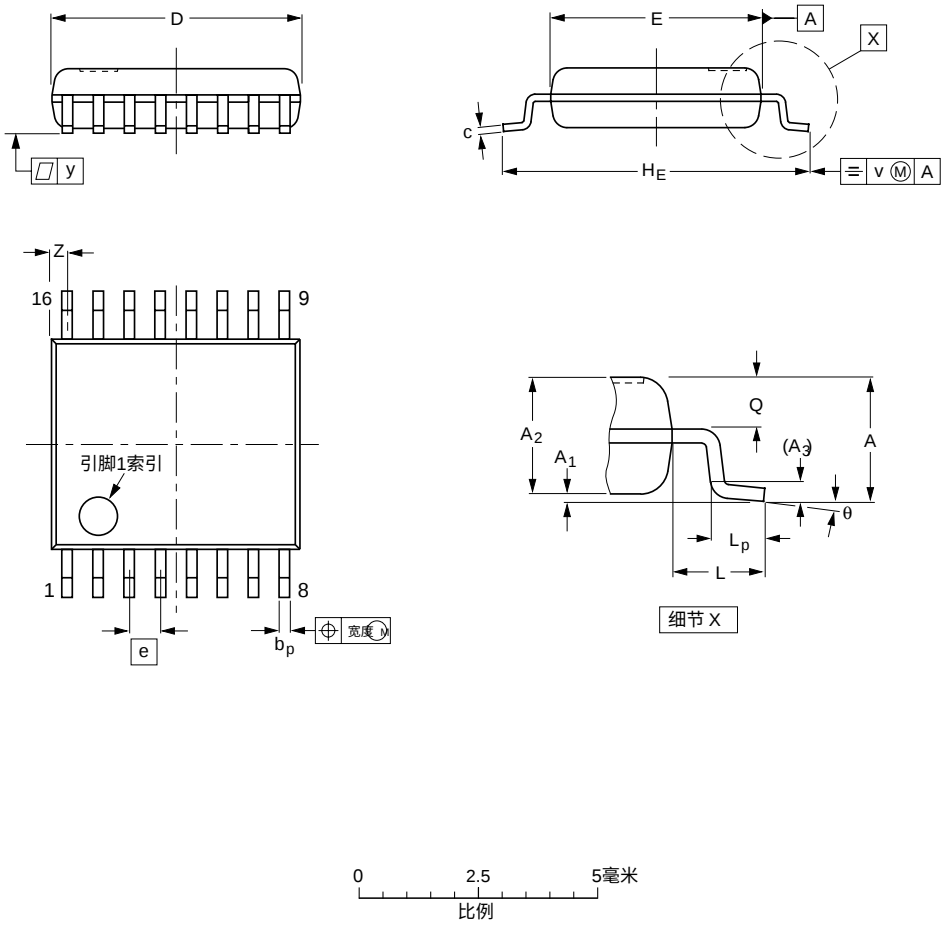
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT369-1		MO-152				~~99-12-27~~ 03-02-19

16 封装轮廓

SSOP16：塑料收缩小外形封装；16个引脚；封装宽度4.4毫米 **SOT369-1**



尺寸（毫米为原始尺寸）

单位	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
毫米	1.5	0.15 0.00	1.4 1.2	0.25	0.32 0.20	0.25 0.13	5.3 5.1	4.5 4.3	0.65	6.6 6.2	1	0.75 0.45	0.65 0.45	0.2	0.13	0.1	0.48 0.18	10^o 0^o

注意

每侧最大0.2毫米的塑料或金属突出物不包括在内。

大纲 版本	参考文献				欧洲 预测	发布日期
	IEC	JEDEC	JEITA			
SOT369-1		MO-152				~~99-12-27~~ 03-02-19

17 SOLDERING

17.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

17.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

17.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

17 焊接

17.1 表面贴装封装焊接简介

本文简要介绍了一项复杂的技术。
有关焊接集成电路的更深入介绍，请参阅我们的《数据手册 IC*26*；集成电路封装》（文档订单号 9398 *652* 9001 1）。

没有一种焊接方法适用于所有表面贴装集成电路封装。
波峰焊并不总是适合表面贴装集成电路或高密度的印刷电路板。在这些情况下，通常使用回流焊接。

17.2 回流焊接

回流焊接需要将焊膏（细焊料颗粒、助焊剂和粘合剂的悬浮液）通过丝网印刷、模板印刷或压力注射施加到印刷电路板上，然后再放置封装。

回流焊接有几种方法；例如，
在传送带式烤箱中使用红外/对流加热。
通过时间（预热、焊接和冷却）根据加热方法的不同而变化，通常在100到200秒之间。

典型的回流峰值温度范围为215到250 °C。封装的顶部表面温度最好保持在230 °C以下。

17.3 波峰焊

传统的单波峰焊不推荐用于表面贴装设备（SMD）或组件密度较高的印刷电路板，因为焊接桥接和不润湿可能会造成重大问题。

为了解决这些问题，专门开发了双波峰焊方法。

如果使用波峰焊，必须遵循以下条件以获得最佳效果：

- 采用双波峰焊方法，包括高向上压力的湍流波，随后是平滑的层流波。
- 对于两侧有引脚且间距（e）为：
  – 大于或等于 1.27 毫米，建议将焊盘的纵向轴线与印刷电路板的运输方向平行；– 小于 1.27 毫米，焊盘的纵向轴线必须与印刷电路板的运输方向平行。

  焊盘的下游端必须设置焊料回流孔。
- 对于四面有引脚的封装，脚印必须以45°角度放置在印刷电路板的运输方向上。脚印必须在下游和侧角处包含焊接盗贼。

在放置和焊接之前，必须用一滴粘合剂固定封装。粘合剂可以通过丝网印刷、针转移或注射器分配施加。粘合剂固化后可以焊接封装。

典型的停留时间为250 °C时4秒。
轻度活化的助焊剂将消除在大多数应用中去除腐蚀性残留物的需要。

17.4 手动焊接 首先通过

焊接两个对角引脚固定元件。使用低电压（2**4** V或更低）的焊接铁施加于引脚的平坦部分。接触时间必须限制在**10**秒以内。

300 °C.

使用专用工具时，所有其他引脚可以在270到320 °C之间的2到5秒内一次性焊接。

17.5 Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW[1]
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable[2]	suitable
PLCC[3], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended[3][4]	suitable
SSOP, TSSOP, VSO	not recommended[5]	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

17.5 表面贴装集成电路封装适用于波峰焊和回流焊接方法的适用性

封装	焊接方法	
	波峰焊	回流[1]
BGA、LFBGA、SQFP、TFBGA	不适用	适用
HBCC、HLQFP、HSQFP、HSOP、HTQFP、HTSSOP、SMS	不适用[2]	适用
PLCC[3]、SO、SOJ	适用	适用
LQFP、QFP、TQFP	不推荐[3][4]	适用
SSOP, TSSOP, VSO	不推荐[5]	适用

备注

1. 所有表面贴装(SMD)封装对湿气敏感。根据湿气含量、最大温度（与时间相关）和封装的体积，可能会由于内部或外部封装的湿气蒸发而导致裂纹（即所谓的爆米花效应）。有关详细信息，请参阅"数据手册 *IC26*；集成电路封装；章节：包装方法"。

2. 这些封装不适合波峰焊接，因为在印刷电路板与散热器（底部版本）之间无法实现焊接接头，并且焊料可能会粘附在散热器上（顶部版本）。
3. 如果考虑波峰焊接，则封装必须以45°角度放置于焊接波的方向上。
   封装的脚印必须在下游和侧角处设置焊料盗贼。
4. 波峰焊仅适用于引脚间距（e）等于或大于0.8毫米的LQFP、TQFP和QFP封装；绝对不适用于引脚间距（e）等于或小于0.65毫米的封装。
5. 波峰焊仅适用于引脚间距（e）等于或大于0.65毫米的SSOP和TSSOP封装；绝对不适用于引脚间距（e）等于或小于0.5毫米的封装。

18 DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

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