UNIVERSITY OF TORONTO
FACULTY OF APPLIED SCIENCE AND ENGINEERING

ECE253F – Digital and Computer Systems
Midterm Examination

October 13, 2022 9:10am - 10:40am
Duration: 90 minutes

Examiners: Profs. N. Enright Jerger and M. Jeffrey

Please enter your name and student number in the spaces provided above as it appears on Quercus. It is important that your name exactly match the Quercus gradebook.

Exam Type D: Examiner specified aids: One single sheet of letter size paper (8.5 x 11 inch), both sides may be used.

Calculator Type 4: No calculators or other electronic devices are allowed.

All questions are to be answered on the examination paper. Your answer **MUST** be fully contained on the same page as the question. **Any material written on the back of each page will be ignored.**

Please state any assumptions you make when answering a question.

The number of marks for each question are indicated. The exam has **15 pages**, including this one.

Q1	Q2	Q3	Q4	Q5	Q6	Q7	Total
5	13	10	5	8	6	8	55

Question 1 [5 Marks]

[3 marks] (a) Assuming that all numbers given below are unsigned integers, fill in the following table with the appropriate number conversions:

9-bit binary	**decimal**	**hexadecimal**
111000001	449	0x1C1
011111101	253	0x0FD
100110000	304	130

[2 marks] (b) What is the minimum number of bits needed to represent decimal 31998?

15 bits

$31998 = 32000 - 2 = 32 \cdot 1000 - 2$

$$32 \cdot 512 < 32 \cdot 1000 - 2 < 32 \cdot 1024$$
$$2^5 \cdot 2^9 < 32 \cdot 1000 - 2 < 2^5 \cdot 2^{10}$$
$$2^{14} < 32 \cdot 1000 - 2 < 2^{15}$$

Question 2 [13 Marks]

[7 marks] (a) Use Boolean algebra to minimize the following function into sum-of-products (SOP) form: $f = \overline{(w+x)(\bar{w}+x+y+\bar{z})}z$. For full marks, show your work and state the theorems used. If you do not know the theorem name, write the simplified form (e.g., $x + x = x$).

$$
\begin{aligned}
f &= \overline{(w+x)} + \overline{(\bar{w}+x+y+\bar{z})} + \bar{z} && \text{DeMorgan's Theorem} && (1)\\
&= \bar{w}\bar{x} + w\bar{x}\bar{y}z + \bar{z} && \text{DeMorgan's Theorem} && (2)\\
&= \bar{w}\bar{x} + w\bar{x}\bar{y} + \bar{z} && \text{Absorption/Redundancy Theorem} && (3)\\
&= \bar{x}(\bar{w} + w\bar{y}) + \bar{z} && \text{Distributive Theorem} && (4)\\
&= \bar{x}(\bar{w} + \bar{y}) + \bar{z} && \text{Absorption/Redundancy Theorem} && (5)\\
&= \bar{x}\bar{w} + \bar{x}\bar{y} + \bar{z} && \text{Distributive Theorem} && (6)
\end{aligned}
$$

[2 marks] (b) Consider again $f = \overline{(w+x)(\bar{w}+x+y+\bar{z})z}$. Report the cost of f in this form, where cost is defined as the number of gates plus the number of gate inputs.

Assuming 3-input NAND and 4-input OR are available:

$$\begin{aligned} cost = & 1+1 \quad \text{Invert w} \\ & +1+1 \quad \text{Invert z} \\ & +2+1 \quad \text{First sum term} \\ & +4+1 \quad \text{Second sum term} \\ & +3+1 \quad \text{3-input NAND} \\ & =16 \end{aligned}$$

Assuming 3-input AND and 4-input OR are available, $cost = 16+1+1 = 18$.
Assuming 2-input AND and 2-input OR are available:

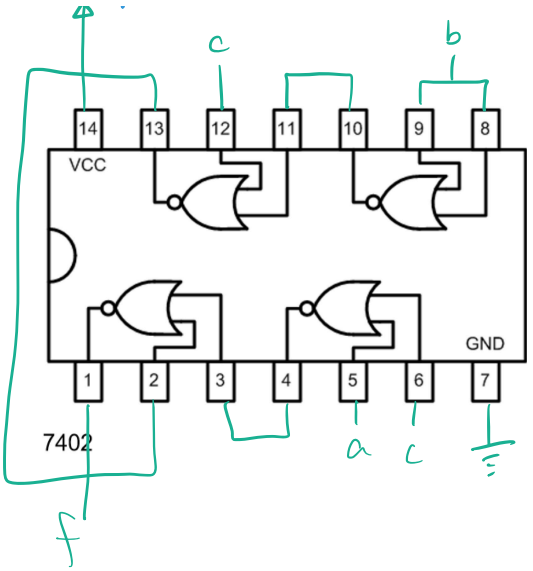
$$\begin{aligned} cost = & 1+1 \quad \text{Invert w} \\ & +1+1 \quad \text{Invert z} \\ & +2+1 \quad \text{First sum term} \\ & +3\cdot(2+1) \quad \text{Second sum term} \\ & +2\cdot(2+1) \quad \text{ANDs} \\ & +1+1 \quad \text{Invert the AND} \\ & =24 \end{aligned}$$

[4 marks] (c) Using Boolean algebra, prove or disprove the following: $xy + \bar{x}z + yz = xy + \bar{x}z$. For full marks, show your work and state the theorems used. If you do not know the theorem name, write the simplified form (e.g., $x + x = x$).

$$
\begin{aligned}
xy + \bar{x}z + yz &= xyz + xy\bar{z} + \bar{x}yz + \bar{x}\bar{y}z + xyz + \bar{x}yz && \text{Combining} && (7)\\
&= xyz + xy\bar{z} + \bar{x}yz + \bar{x}\bar{y}z && \text{Idempotency} && (8)\\
&= xy + \bar{x}z && \text{Combining} && (9)
\end{aligned}
$$

Question 3 [10 Marks]

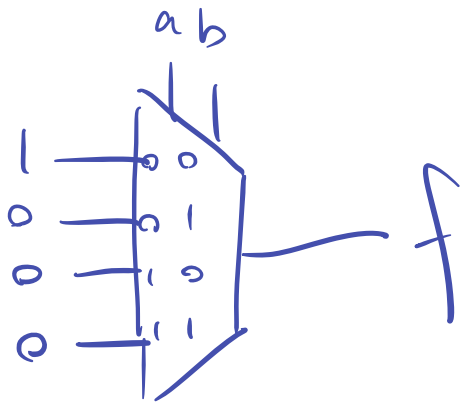
[6 marks] (a) In Lab 1, you used 7400-series chips to build logic circuits. To prepare for your interview at NASA, you are now restricted to only 7402-series chips (quad 2-input NOR shown below). Implement the logic function $f = a\bar{b} + c$, by drawing a schematic of as many connected 7402 chips as you need. 4 chips are given to you; you can use more or fewer as needed. Carefully label the inputs and outputs. You must invert any variable yourself.



One 7402 is sufficient.

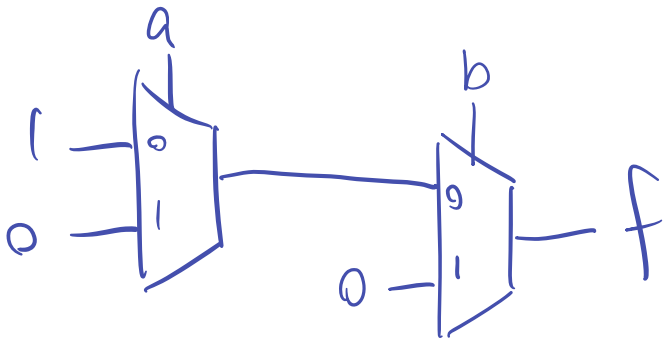
$$
\begin{aligned}
f = a\bar{b} + c &= (a + c)(\bar{b} + c) \quad \text{Distributive Theorem} \\
&= \overline{\overline{(a + c)(\bar{b} + c)}} \\
&= \overline{\overline{(a + c)} + \overline{(\bar{b} + c)}} \\
&= \overline{\overline{(a + c)} + \overline{(\bar{b} + b + c)}}
\end{aligned}
$$

[2 marks] (b) You have run out of 7402 chips! Draw a schematic to implement the NOR function, $f = \overline{(a+b)}$, using only 4-to-1 multiplexers.



[2 marks] (c) The 4-to-1 multiplexers all exploded! Draw a schematic to implement the NOR function, $f = \overline{(a+b)}$, using only 2-to-1 multiplexers.

```
f = b ?  0 :  (a ?  0 :  1)
```



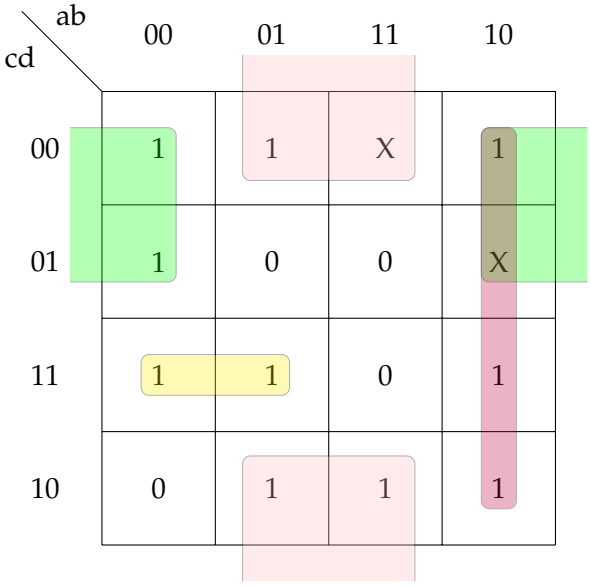
Question 4 [5 Marks]

[2 marks] (a) Fill in the K-map below for the expression $f(x_1, x_2, x_3, x_4) = \prod M(2, 3, 5, 7, 9, 10, 11, 12, 13, 15)$. Note: This is a Product of Sums notation.

x_3x_4 \ x_1x_2	00	01	11	10
00	**1**	**1**	**0**	**1**
01	**1**	**0**	**0**	**0**
11	**0**	**0**	**0**	**0**
10	**0**	**1**	**1**	**0**

[3 marks] (b) For the K-map given below, derive the minimum-cost cover as a sum of products expression. 'X' in the K-map indicates a "don't care".

$$f(a, b, c, d) = a\bar{b} + b\bar{d} + \bar{b}\bar{c} + \bar{a}cd$$



Question 5 [8 Marks]

You are asked to design a multiplier circuit that multiplies 2 2-bit numbers (a[1:0] and b[1:0]). Binary multiplication works the same as decimal multiplication. Your result should be specified as y[3:0].

[2 marks] (a) Complete the truth table for your circuit.

a_1	a_0	b_1	b_0	y_3	y_2	y_1	y_0
0	0	0	0	**0**	**0**	**0**	**0**
0	0	0	1	**0**	**0**	**0**	**0**
0	0	1	0	**0**	**0**	**0**	**0**
0	0	1	1	**0**	**0**	**0**	**0**
0	1	0	0	**0**	**0**	**0**	**0**
0	1	0	1	**0**	**0**	**0**	**1**
0	1	1	0	**0**	**0**	**1**	**0**
0	1	1	1	**0**	**0**	**1**	**1**
1	0	0	0	**0**	**0**	**0**	**0**
1	0	0	1	**0**	**0**	**1**	**0**
1	0	1	0	**0**	**1**	**0**	**0**
1	0	1	1	**0**	**1**	**1**	**0**
1	1	0	0	**0**	**0**	**0**	**0**
1	1	0	1	**0**	**0**	**1**	**1**
1	1	1	0	**0**	**1**	**1**	**0**
1	1	1	1	**1**	**0**	**0**	**1**

(b) You are given the following System Verilog modules:

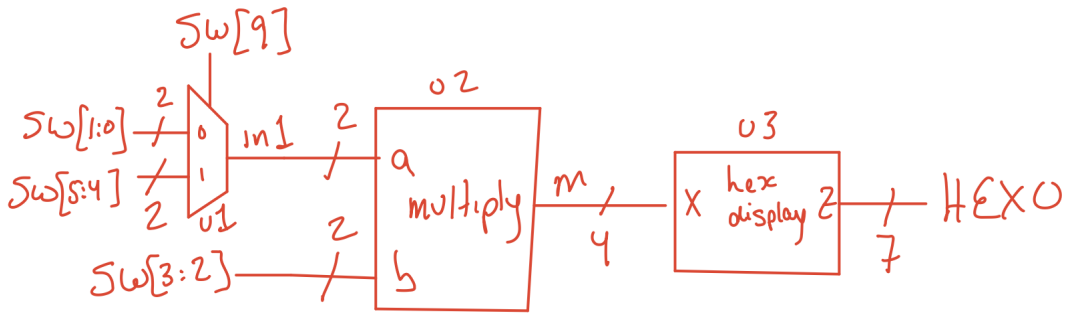
```
module hex_display(input logic [3:0] x, output logic [6:0] z);
module multiply(input logic [1:0] a, b, output logic [3:0] y);
module mux2bit(input logic[1:0] x, y, input logic s, output logic[1:0] f);
```

For the mux, when s is 0, x is selected and when s is 1, y is selected.

You wish to build a circuit that implements the following (SW represents the switches):

- if SW[9] is 0, you want to multiply SW[1:0] by SW[3:2]
- if SW[9] is 1, you want to multiply SW[3:2] by SW[5:4]
- You want to output the result of the multiplication on HEX0

[2 marks] (i) Draw a block-diagram schematic for your circuit. In your schematic, draw each module as a block and clearly specify inputs and outputs along with the width of all signals.



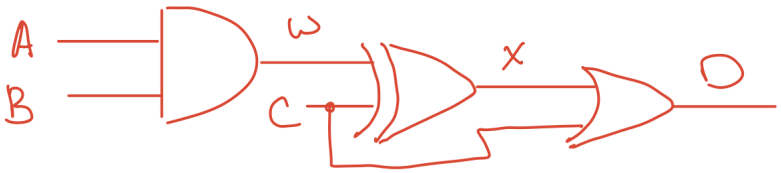
[4 marks] (ii) Using only the modules provided, write only the top-level System Verilog module that implements the circuit described above. You may create any internal signals you require; be sure to name them according to your schematic above.

```
module top_level(input logic [9:0] SW, output logic [6:0] HEX0);

  logic [1:0] in1;
  logic [3:0] m;

  mux2bit u1 (SW[1:0], SW[5:4], SW[9], in1);
  multiply u2 (in1, SW[3:2], m);
  hex_display u3 (m, HEX0);
endmodule
```

Question 6 [6 Marks]

[3 marks] (a) Draw a schematic for the circuit described by the following System Verilog Code. You may use any gates (AND, OR, NOT, XOR, NAND, NOR) in your circuit.

```
module midterm1(input logic A, B, C, output logic D);
  logic w, x;
  assign w=A&B;
  assign x=w^C;
  assign D=x|C;
endmodule
```



[2 marks] (b) Write a simplified sum of products expression for the code in part (a).

$D = AB + C$

[1 mark] (c) Consider the following code:

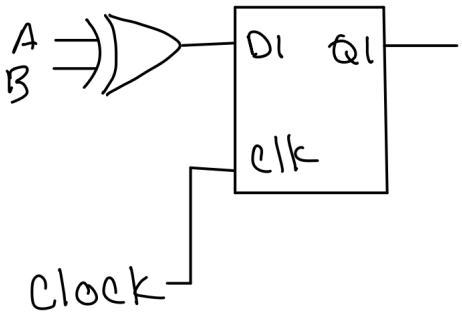
```
module midterm2(input logic A, B, C, output logic D);
  logic w, x;
  assign D=x|C;
  assign x=w^C;
  assign w=A&B;
endmodule
```

True or False: The midterm1 and midterm2 modules generate the exact same hardware.

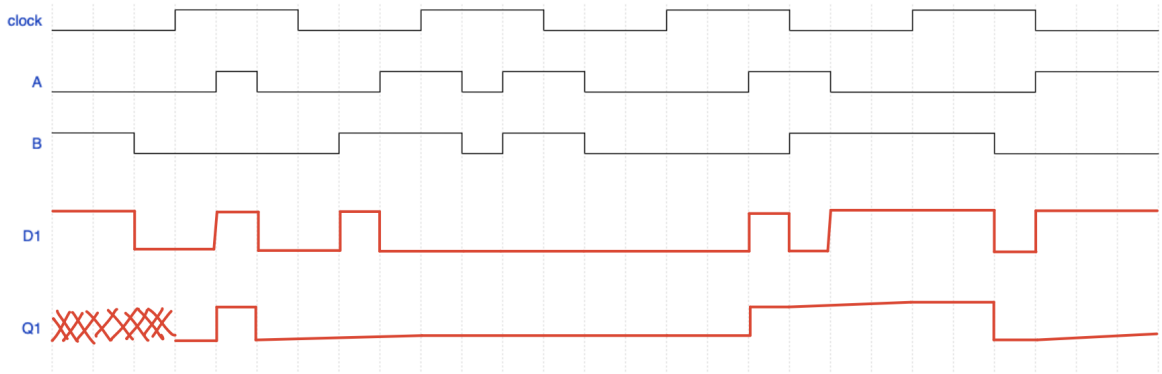
TRUE

Question 7 [8 Marks]

(a) Consider the following circuit

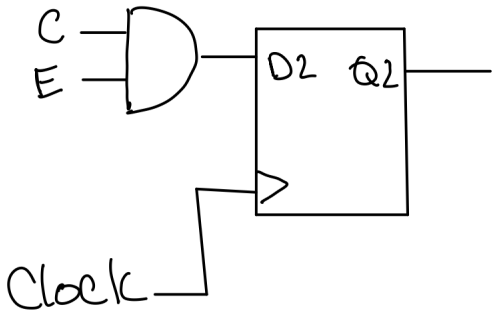


You are given the following waveform for inputs A, B, and clock

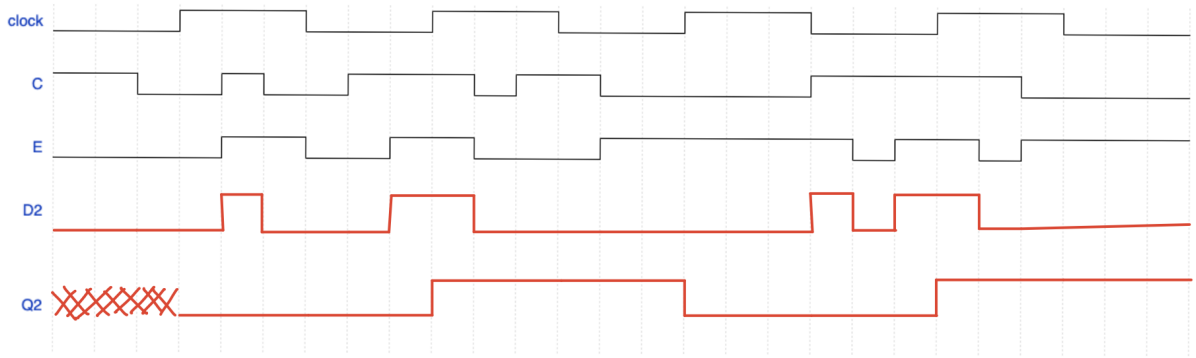


Complete the above waveform for D1, Q1

(b) Consider the following circuit



You are given the following waveform for inputs C, E, and clock



Complete the above waveform for D2, Q2

This page has been left blank intentionally