CSE 120

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Day 11 Notes

Brief Structural Hazard Recap

- Occurs when a read and write try to access the same resource at the same time.
- Memory access: In a vanilla processor design, instructions and data have different physical memory, prevents structural hazards. Common physical memory ie: Von Neumann have this issue.
- Register File: For reading and writing to the same register at the same time, this could be an issue. If you have a fast register file this hazard is resolved.

Beyond the 5 stage pipeline

- Most real pipelines are 10-15 stages
- These deeper pipelines improve throughput and clock frequency, however latency per instruction can inscrease due to hazards.