# ICN2037

## (16 channels double buffer constant current output LED driver chip)



ICN2037 16-channel constant current double buffer output LED driver chip

## Overview

## Package

ICN2037 is a driver IC specially designed for LED display screens.
Use 16 channels of constant current sink current output. ICN2037 integrates "Noise Free
™"technology, has excellent anti-interference characteristics, so that constant current and low dust effect

Not affected by the PCB board. And can choose different external resistance to output sink
The current is adjusted to accurately control the brightness of the LED. Simultaneously
Over-current precise control technology can make the inter-chip error less than ±2.5%, channel
The time error is less than ±3.0%.

ICN2037 integrates double buffer registers, in the display register
At the same time as 16bit data, you can continue to store 16bit serial data,
Compared with general constant current source chips, the refresh rate can be increased by more than 50%.

## characteristic

- ☐ 16 channels constant current sink current output
- ☐ Output current range:
  - 3 ~ 45mA@$V_{DD}$ =5V
  - 3 ~ 30mA@$V_{DD}$ =3.3V
- ☐ Current accuracy
  - Between channels: ±1.8% (typical value) ±3.0% (maximum)
  - Between chips: ±1.5% (typical value) ±2.5% (maximum)
- ☐ Fast output current response *OE* (minimum): 60ns@$V_{DD}$ =5V
- ☐ I/O Schmitt trigger input
- ☐ Maximum data transmission frequency: 30MHz
- ☐ Chip working voltage: $V_{DD}$ =3.3 ~ 6V
- ☐ Working temperature range: -40 ~ 85°C
- ☐ Has the function of improving lamp bead damage
- ☐ With blanking function
- ☐ Has excellent anti-interference ability and low gray level effect
- ☐ Improve the caterpillar phenomenon caused by lamp bead damage
- ☐ Integrated double buffer, refresh rate is more than 50% higher than general constant current chip

Shrink SOP

AP: SSOP24-P-150-0.635

**ICN2037**



## Pin description

SSOP24-P-150-0.635

ICN2037(SSOP24)

| Pin No. | Pin name | Features |
|---|---|---|
| 1 | GND | Ground terminal |
| 2 | SIN | Serial data input |
| 3 | CLK | Clock signal input terminal, sampling data on rising edge |
| 4 | LE | Latch signal input<br>When LE is high, data is transferred to the latch; when LE is low, data is latched |
| 5 ~ 20 | OUT0 ~ OUT15 | Constant current sink current output terminal |
| twenty one | OE | Enable signal input<br>*When OE is* high, turn off OUT0 ~ OUT15<br>*When OE is* low, open OUT0 ~ OUT15 |
| twenty two | SOUT | Serial data output |
| twenty three | R-EXT | External resistance input terminal, adjustable output constant current value |
| twenty four | VDD | Power input |

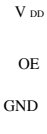


## ICN2037 block diagram

## I/O equivalent circuit

1. CLK, SIN

2. OE




3. LE


4.SOUT


## Timing diagram

Note 1: When the LE pin is set to L, the latch circuit retains data; when the LE pin is set to H, the latch circuit does not retain data, and the data is output directly.

When the OE (GCLK) pin is L, the OUT0 to OUT15 output pins will turn ON and OFF to respond to the data; set the OE (GCLK) pin to H, regardless of the data, all output pins The pin will be OFF. When the OE (GCLK) pin is L, data can be transmitted and latched



## The principle of ICN2037 to improve the refresh rate

General constant current source drive chip data transmission and data display timing diagram


Reasons for low utilization rate of data transmission and data display of general constant current chip:

1. When displaying a high-level data, the data display time may be much longer than the data transmission time, and the data cannot be counted during the extra time of the data display. According to transmission.
2. When displaying a low-level data, the data display time may be much shorter than the data transmission time, and the data cannot be counted during the extra time of data transmission. According to the show.

ICN2037 data transmission and data display timing diagram


ICN2037 data transmission and data display timings are shown in the figure above, data(A) and data(C) are high data, data(B) and data(D) high and low data. Will show
The high and low bits of the display data are combined according to time, so that the excess time of the display high data can be used for data transmission, or use the time of data transmission to
For high-level display, the perfect combination of data transmission and display data can effectively improve the display refresh rate. The basic steps are as follows:

1. When the data(A) transfer is completed, a latch signal is generated on LE to latch data(A)
2. After the data(A) is latched, OE changes from 1 to >0, register data(A) and display data(A)
3. While displaying data(A), transfer data(B)
4. After the data(B) transfer is completed, LE generates a latch signal, latches data(B), and then transfers data(C)
5. After completing the display of data (A), register data (B) and display data (B)
6. Complete the transmission of data (C), complete the display of data (B)
7. Register data(C) and transmit data(D), (same as step 1)



## Truth table

| CLK | LE | OE | SIN | OUT0 … OUT7… OUT15 | SOUT |
|---|---|---|---|---|---|
| | H | L | $D_n$ | $D_n$ … $D_{n-7}$ … $D_{n-15}$ | $D_{n-15}$ |
| | L | L | $D_{n+1}$ | No change | $D_{n-14}$ |
| | H | L | $D_{n+2}$ | $D_{n+2}$ … $D_{n-5}$ … $D_{n-13}$ | $D_{n-13}$ |
| | X | L | $D_{n+3}$ | $D_{n+2}$ … $D_{n-5}$ … $D_{n-13}$ | $D_{n-13}$ |
| | X | H | $D_{n+3}$ | OFF | $D_{n-13}$ |

## Maximum working range (Ta=25°C)

| characteristic | symbol | Rated value | unit |
|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| voltage | | $V_{DD}$ | 0~7.0 | V |
| Output current | | $I_O$ | 45 | mA |
| Input voltage | | $V_{IN}$ | -0.4~$V_{DD}$ +0.4 | V |
| Output withstand voltage | | $V_{OUT}$ | 11V | |
| Clock frequency | | $F_{CLK}$ | 30 | MHz |
| Ground current | | $I_{GND}$ | +1000 | mA |
| Power consumption (Printed circuit board, 25°C) | DN-type | $P_D$ | 3.19 | W |
| Thermal impedance | DN-type | $R_{th(j-a)}$ | 39.15 | °C/W |
| Operating temperature | | $T_{opr}$ | -40 ~ 85 | °C |
| storage temperature | | $T_{stg}$ | -55 ~ 150 | °C |

## DC characteristics ($T_a$=-40°C~85°C, if not otherwise stated)

| characteristic | symbol | Test Conditions | Minimum | Typical value | Max | unit |
|---|---|---|---|---|---|---|
| voltage | $V_{DD}$ | - | 3.3 | 5 | 6.0 | V |
| Output voltage when ON | $V_{O(ON)}$ | OUTn | 0.6 | - | 4 | V |
| High level logic input voltage | $V_{IH}$ | - | 0.7*$V_{DD}$ | - | $V_{DD}$ | V |
| Low level logic input voltage | $V_{IL}$ | - | GND | - | 0.3*$V_{DD}$ | V |
| SOUT high level output current | $I_{OH}$ | $V_{DD}$ =5V | - | - | -1 | mA |
| SOUT low-level output current | $I_{OL}$ | $V_{DD}$ =5V | - | - | 1 | mA |
| Constant current output | $I_O$ | OUTn | 0.5 | - | 45 | mA |





## Dynamic characteristics ($V_{DD}$=4.5~5.5V, $T_a$=-40°C~85°C, if not otherwise specified)

| characteristic | Symbol | test circuit | Test Conditions | Minimum | typical | maximum | unit |
|---|---|---|---|---|---|---|---|
| Serial data transmission frequency | $F_{CLK}$ | 6 | - | - | - | 30 | MHz |
| Clock pulse width | $t_{wCLK}$ | 6 | SCK=H or L | 20 | - | - | ns |
| Latch pulse width | $t_{wLE}$ | 6 | LE=H | 20 | - | - | ns |
| Enable pulse width | $t_{wOE}$ | 6 | OE = H or L, $R_{EXT}$ =890Ω | 60 | - | - | ns |
| Hold time | $t_{HOLD1}$ | 6 | - | 5 | - | - | ns |
| | $t_{HOLD2}$ | 6 | - | 5 | - | - | ns |
| Establishment time | $t_{SETUP1}$ | 6 | - | 5 | - | - | ns |
| | $t_{SETUP2}$ | 6 | - | 5 | - | - | ns |
| Maximum clock rise time | $t_r$ | 6 | | - | - | 500 | ns |
| Maximum clock fall time | $t_f$ | 6 | | - | - | 500 | ns |

## Electrical characteristics ($V_{DD}$=4.5~5.5V, $T_a$=25°C, if not otherwise specified)

| characteristic | symbol | test Circuit | Test Conditions | Minimum | Typical value | maximum | unit |
|---|---|---|---|---|---|---|---|
| High level logic output voltage | $V_{OH}$ | 1 | $I_{OH}$ =-1mA, SOUT | $V_{DD}$ -0.4 | - | $V_{DD}$ | V |
| Low level logic output voltage | $V_{OL}$ | 1 | $I_{OH}$ =+1mA, SOUT | - | - | 0.4 | V |
| High level logic input current | $I_{IH}$ | 2 | $V_{IN}$ =$V_{DD}$ , OE , SIN, CLK | - | - | 1 | μA |
| Low level logic input current | $I_{IL}$ | 3 | $V_{IN}$ =GND, LE, SIN, CLK | - | - | -1 | μA |
| Power supply current | $I_{DD1}$ | 4 | Rext=not connected, OUT off | - | 2.5 | 5.0 | mA |
| | $I_{DD2}$ | 4 | Rext=1.24KΩ, OUT off | - | 4.5 | 7.0 | mA |
| | $I_{DD3}$ | 4 | Rext=620Ω, OUT off | - | 6.0 | 9.0 | mA |
| | $I_{DD4}$ | 4 | Rext=1.24KΩ, OUT on | - | 5.2 | 8.5 | mA |
| | $I_{DD5}$ | 4 | Rext=620Ω, OUT on | - | 6.5 | 9.5 | mA |
| Constant current output | $I_{O1}$ | 5 | $V_{DD}$ =5.0V, $V_O$ =1.0V, $R_{EXT}$ =1.23kΩ | - | 15 | - | mA |
| | $I_{O2}$ | 5 | $V_{DD}$ =5.0V, $V_O$ =1.0V, $R_{EXT}$ =615Ω | - | 30 | - | mA |
| Constant current error | $\Delta I_O$ | 5 | $V_{DD}$ =5.0V, $V_O$ =1.0V, $R_{EXT}$ =1.23kΩ, | - | ±0.27 | ±0.46 | mA |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| Constant current power supply voltage regulation | $\Delta V_{OUT}$ | 5 | OUT0 ~ OUT15<br>$V_{DD}$ =4.5~5.5V, $V_O$ =1.0V,<br>$R_{EXT}$ =1.24kΩ, | - | ±0.2 | - | %/V |
| Constant current output voltage regulation | $\Delta V_{OUT}$ | 5 | OUT0 ~ OUT15<br>$V_{DD}$ =5.0V, $V_O$ =1.0~3.0V,<br>$R_{EXT}$ =1.24kΩ, | - | ±0.1 | | %/V |
| Pull-up resistor | $R_{UP}$ | 3 | OUT0 ~ OUT15<br>OE | 250 | 500 | 800 | kΩ |
| Pull-down resistor | $R_{DOWN}$ | 2 | LE | 250 | 500 | 800 | kΩ |





## Switching characteristics ($T_a$=25°C, $V_{DD}$=5.0V, if not otherwise specified)

| characteristic | | symbol | test Circuit | Test Conditions | most small value | Code type value | most Big value | single Bit |
|---|---|---|---|---|---|---|---|---|
| transmission delay | OE - OUT0 | $t_{pLH3}$ | 6 | LE=H | - | 32 | 36 | ns |
| | OE - OUT1 | $t_{pHL3}$ | 6 | LE=H | - | 45 | 49 | |
| | CLK-SOUT | $t_{pHL}$ | 6 | - | - | 32 | 35 | |
| Output rise time | | $t_{or}$ | 6 | 10~90% of voltage waveform | - | 30 | 35 | ns |
| Fall time of output | | $t_{of}$ | 6 | 90~10% of voltage waveform | - | 45 | 50 | ns |

## Test circuit

Test circuit 1: high-level logic input voltage/low-level logic input voltage

Test circuit 2: High-level logic input current/pull-down resistance

Test circuit 3: low-level logic input current/pull-up resistor

Test circuit 4: power supply current





Test circuit 5: Constant current output/output OFF leakage current/constant current error

Constant current power supply voltage regulation/constant current output voltage regulation

Test circuit 6: switching characteristics





## Timing diagram

1. CLK, SIN, SOUT

$t_{wCLK}$

2. CLK, SIN, LE, OE , OUT0

3. OUT0

## Application information

ICN2037 uses precise current drive control technology, and the current difference between different chips is extremely small between different channels of the same chip.

1) The current difference between channels is <±3.0%, and the current difference between chips is <±2.5%.

2) It has current output characteristics that are not affected by the load terminal voltage, as shown in the figure below. The output current will not change with the change of the LED forward voltage $V_F$.

## Constant current output setting

ICN2037 adjusts the output current (Iout) through an external resistor Rext. The calculation formula is:

$$V_{R\text{-}EXT} = 1.232V;$$

$$Iout = (V_{R\text{-}EXT} / Rext) * 15$$

## Package size

SSOP24-P-150-0.635





# Product order information

| Product number | Encapsulation (lead-free environmental protection) | Weight (g) |
|---|---|---|

## statement:

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