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SHEN ZHEN FINE MADE ELECTRONICS GROUP CO., LTD.

FM6126A/FM6126Q (File No.: S&CIC1618) **16-** channel double buffer constant current output **LED** driver chip

Overview

FM6126A/FM6126Q is a driver IC specially designed for LED modules and displays, with 16 constant current output driving capabilities.

FM6126A/FM6126Q is a driver IC specially designed for LED display, using 16 channels of constant current sink current output. FM6126A/FM6126Q uses

The patented "output clamp" technology can effectively eliminate the dark phenomenon of the first line and prevent damage to the lamp beads. At the same time FM6126A/FM6126Q has excellent

Its anti-interference characteristics, constant current and low ash effects are not affected by the PCB board. Different external resistors can be used to adjust the output stage current for precise control

Control the brightness of the LED. FM6126A/FM6126Q uses precise current control technology to make the inter-chip error less than ±3.0%, and the inter-channel error

Less than ±2.0%

FM6126A/FM6126Q will buffer 16bit display data during the display process (OE=0), so the system can be used during the display of FM6126A/FM6126Q

Then continue to store 16bit serial data, compared with general constant current source chips, the refresh rate can be increased by more than 50%.

FM6126A/FM6126Q integrates 6-bit current gain adjustment on the basis of FM6124, and adds register configuration. Effectively eliminate ghosts and hide, improve low dust

Color cast, pitting, dark first line and other issues.

Features

- ▢ 16 channels constant current sink current output
- ▢ Output current setting range:
  - 0.5 ~ 45mA@VDD=5V
  - 0.5 ~ 25mA@VDD=3.3V
- ▢ Current accuracy
  - Between channels: ±0.9% (typical value) ±2.0% (maximum) Between chips: ±2.5% (typical value) ±3.0% (maximum)
- ▢ Fast output current response OE (minimum): 40ns@VDD=5V
- ▢ 6-bit current gain adjustment: 25% ~ 100%
- ▢ I/O Schmitt trigger trigger input
- ▢ Data transmission frequency: fMAX = 25MHz
- ▢ Chip working voltage: VDD=3.3 ~ 5.5V
- ▢ Operating temperature range: -40 ~ 85°C
- ▢ Eliminate ghosts
- ▢ Integrated double buffer, refresh rate is more than 50% higher than general constant current chip
- ▢ Integrated bidirectional clamp protection circuit in the channel, which can effectively reduce the damage of the lamp beads
- ▢ Effectively solve low gray blocks, color cast, pitting, and dark first line
- ▢ Has excellent anti-interference ability and low grayscale effect
- ▢ Package form: SSOP-24 (e=0.635)/QFN-24-4×4 (0.5mm)

Applications

- ▢ Indoor surface mount module series: P2, P2.5, P3, P3.91, P4, P4.81, P5.
- ▢ Outdoor surface mount module series: P4.81, P5, P6, P8, P10, P10 plug-in lights, P13.33 plug-in lights.

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Pin diagram

SSOP-24 QFN-24

Pin function description

Pin definition	Pin name
GND	Chip ground pin
SIN	Serial data input to the shift register
CLK	Clock signal input terminal
LE	When LE is high with 3 clk widths at the data latch input, the data is transferred to the latch.
	Constant current output terminal
	Output enable signal input terminal, and buffer data at the falling edge When OE is high, turn off OUT0-OUT15 When OE is low, open OUT0-OUT15
SDO	The serial data output terminal can be connected to the SDI terminal of the next driver chip
REXT	The output terminal of the external adjustment resistor can adjust the output current of all channels
VDD	3.3V/5V power input

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Internal block diagram

I/O equivalent circuit

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Instruction definition

The chip contains a simple 16bit shift register, the gray value and configuration value will be latched into the shift register. By counting LE signals
The length is used to parse the control command, and different LE lengths represent different commands. For example, an LE signal with a length of 3 represents the "Data_Latch" command, use
To control the shift register to latch the gray value, and send the 16bit data in the shift register to the output channel. The following table lists all commands and their definitions.

Command name	LE	Instruction description
RESET_OEN	>1	Soft reset signal
DATA_LATCH	3	Latch 16bit data to the output channel
-	4~10	Reserved
WR_REG1	11	Write configuration register 1
WR_REG2	12	Write configuration register 2

Note: The length of LE refers to the number of rising edges of CLK when LE is high. As shown in the figure below, the length of the first LE signal is 3, that is, the command
Let it be the "Data_Latch" command.

Build hold time

The setup and hold time of LE signal and SIN signal are shown in the following table.

Signal name	MIN	Remarks
T_{SU_LE}	7ns	
T_{HD_LE}	7ns	
T_{SW_LE}	10ns	
T_{SU_SIN}	3ns	

T_{HD_SIN}	3ns	

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The principle of FM6126A/FM6126Q to improve the refresh rate

General constant current source drive chip data transmission and data display timing diagram

The data transmission and data display of the general constant current chip are shown in the figure above. The reasons for the low utilization rate of data transmission and data display:

1. When displaying a high-level data, the time of data display may be much longer than the time of data transmission, in the extra time of data display

Data transfer is not possible.

2. When displaying a low-level data, the data display time may be much shorter than the data transmission time, in the extra time of data transmission

Data display cannot be performed.

FM6126A/FM6126Q data transmission and data display timing diagram

FM6126A/FM6126Q data transmission and data display timing is shown in the figure above, data(A) and data(C) are high data, data(B) and data(D) are high

Low-order data. Combine the high and low bits of the display data according to time, so that the excess time of the display high data can be used for data transmission, or

Use the time of data transmission for high-level display, and perfectly match the data transmission and display data, which can effectively improve the display refresh rate.

The basic steps are as follows:

1. When the data(A) transfer is completed, a latch signal is generated on LE to latch data(A)
2. After data(A) is latched, register data(A) from 1~>0 and display data(A)
3. While displaying data(A), transfer data(B)
4. After the data(B) transmission is completed, the latch signal is generated by LE, data(B) is latched, and then data(C) is transmitted
5. After completing the display of data (A), register data (B) and display data (B)
6. Complete the transmission of data (C), complete the display of data (B)
7. Register data(C) and transmit data(D), (same as step 1)

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FM6126A/FM6126Q Elimination circuit timing

The chip blanking time (Tghost) is defined as shown in the figure below. When the OE signal is high, the rising edge of the latch signal (LAT) to the enable signal (OEN) The falling edge interval is the blanking time.

Truth table

CLK	LE	OE	SIN	OUT0 … OUT7 … OUT15	SOUT
	H	L	Dn	Dn… Dn-7… Dn-15	Dn-15
	L	L	Dn+1	No change	Dn-14
	H	L	Dn+2	Dn+2… Dn-5… Dn-13	Dn-13
	×	L	Dn+3	Dn+2… Dn-5… Dn-13	Dn-13
	×	H	Dn+3	OFF	Dn-13

Specifications

Maximum working range (Ta=25°C)

characteristic		symbol	Rated value	unit
voltage		V_{DD}	0~5.5	V
Output current		I_O	45	mA
Input voltage		V_{IN}	-0.4~V_{DD} +0.4	V
Output withstand voltage		V_{OUT}	13V	
Clock frequency		F_{CLK}	30	MHz
Ground current		I_{GND}	+1000	mA
Power consumption (printing On circuit board, 25°C)	DN-type	P_D	3.19	W
Thermal impedance	DN-type	$R_{th(ja)}$	39.15	°C/W
Operating temperature		T_{opr}	-40 ~ 85	°C
storage temperature		T_{stg}	-55 ~ 150	°C

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DC characteristics (Ta=-40°C~85°C, if not otherwise stated)

characteristic	Test Conditions	Minimum	Typical value	Max	unit
voltage	-	3.3	5	5.5	V
Output voltage when ON	OUTn	0.6	-	4	V
High level logic input voltage	-	0.7*V_{DD}	-	V_{DD}	V
Low level logic input voltage	-	GND	-	0.3*V_{DD}	V
SOUT high level output current	V_{DD} =5V	-	-	-1	mA
SOUT low level output current	V_{DD} =5V	-	-	1	mA
Constant current output	OUTn	0.5	-	45	mA

Switching characteristics (Ta=25°C, VDD=5.0V, if not otherwise specified)

characteristic	symbol	Test circuit	Test Conditions	Minimum	Typical value	maximum	unit

Transmission delay time	OE-OUT0 tpLH3	6	LE=H	-	twenty two	26	ns
	OE -OUT1 tpHL3	6	LE=H	-	twenty two	25	
	CLK-SOUT tpHL2	6	-	-	twenty two	30	
Output rise time	tor	6	Voltage waveform 10~90%	-	25	28	ns
Fall time of output	tof	6	90~10% of voltage waveform	-	33	37	ns

Dynamic characteristics (VDD=4.5~5.5V, Ta=-40°C~85°C, if not otherwise specified)

characteristic	symbol	Test circuit	Test Conditions	Minimum	typical value	Max	unit
Serial data transmission frequency	F_{CLK}	6	-	-	-	30	MHz
Clock pulse width	t_{wCLK}	6	SCK=H or L	20	-	-	ns
Latch pulse width	t_{wLE}	6	LE=H	20	-	-	ns
Enable pulse width	t_{wOE}	6	OE = H or L, R_{EXT} =890Ω	40	-	-	ns
Hold time	t_{HOLD1}	6	-	5	-	-	ns
	t_{HOLD2}	6	-	5	-	-	ns
Establishment time	t_{SETUP1}	6	-	5	-	-	ns
	t_{SETUP2}	6	-	5	-	-	ns
Maximum clock rise time	t_r	6		-	-	500	ns
Maximum clock fall time	t_f	6		-	-	500	ns

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Electrical characteristics (VDD=4.5~5.5V, Ta=25°C, if not otherwise stated)

characteristic	Symbol	test circuit	Test Conditions	Minimum	Typical value	Max	unit
High level logic output voltage	V_{OH}	1	I_{OH} =-1mA, SOUT	V_{DD} -0.4	-	V_{DD}	V
Low level logic output voltage	V_{OL}	1	I_{OH} =+1mA, SOUT	-	-	0.4	V
High level logic input current	I_{IH}	2	V_{IN} =V_{DD} , OE , SIN, CLK	-	-	1	μA
Low level logic input current	I_{IL}	3	V_{IN} =GND, LE, SIN, CLK	-	-	-1	μA
Power supply current	I_{DD1}	4	Rext=not connected, OUT off	-	4.8	8	mA
	I_{DD2}	4	Rext=1.24KΩ, OUT off	-	7.2	9	mA
	I_{DD3}	4	Rext=620Ω, OUT off	-	9.2	11	mA
	I_{DD4}	4	Rext=1.24KΩ, OUT on	-	8.7	10	mA
	I_{DD5}	4	Rext=620Ω, OUT on	-	10.7	12	mA
Constant current output	I_{O1}	5	V_{DD} =5.0V, V_O =1.0V, R_{EXT} =1.23kΩ	-	15	-	mA
	I_{O2}	5	V_{DD} =5.0V, V_O =1.0V, R_{EXT} =615Ω	-	30	-	mA
Constant current error	ΔI_O	5	V_{DD} =5.0V, V_O =1.0V, R_{EXT} =1.23 kΩ, OUT0 ~ OUT15	-	±0.15	±0.37	mA
Constant current power supply voltage regulation	%/V	5	V_{DD} =4.5~5.5V, V_O =1.0V, R_{EXT} =1.24 kΩ, OUT0 ~ OUT15	-	±0.2	-	%/V
Constant current output voltage regulation	%/V	5	V_{DD} =5.0V, V_O =1.0~3.0V, R_{EXT} =1.24 kΩ, OUT0 ~ OUT15	-	±0.1		%/V
Pull-up resistor	R_{UP}	3		200	300	500	kΩ
Pull-down resistor	R_{DOWN}	2	LE	200	300	500	kΩ

Test circuit

Test circuit 1: high-level logic input voltage/low-level logic input voltage

Test circuit 2: High-level logic input current/pull-down resistance

Test circuit 3: low-level logic input current/pull-up resistor

Test circuit 4: power supply current

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Test circuit 5: constant current output/output OFF leakage current/constant current error constant current power supply voltage regulation/constant current output voltage regulation

Test circuit 6: switching characteristics

Timing waveform

1. CLK, SIN, SOUT

2.CLK, SIN, LE, OE , OUT0

3. OUT0

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Application information

FM6126A/FM6126Q adopts precise current drive control technology. The current difference between different channels of the same chip is very small.

1) The current difference between channels is <±2%, and the current difference between chips is <±3.0%.

2) It has current output characteristics that are not affected by the load terminal voltage, as shown in the figure below. The output current will not change with the change of the LED forward voltage V_F.

Adjust output current

FM6126A/FM6126Q adjusts the output current (Iout) through an external resistor Rext. The calculation formula is:

$$V_{R\text{-}EXT} = 1.23V;$$

$$Iout = (V_{R\text{-}EXT} / Rext) * 15$$

Package information

▢ SSOP-24 (e=0.635)

symbol	Mm		
	Minimum	Typical value	Max
A	-	1.60	1.65
A1	-	0.15	0.20
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.22	0.25	0.30
c	0.17	0.22	0.25
D	8.55	8.65	8.75
E	5.90	6.00	6.10
E1	3.80	3.90	4.00
e		0.635BSC	
L	0.57	0.60	0.65
L1		1.05BSC	
θ	0°	3°	6°

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▢ QFN-24-4×4 (0.5mm)