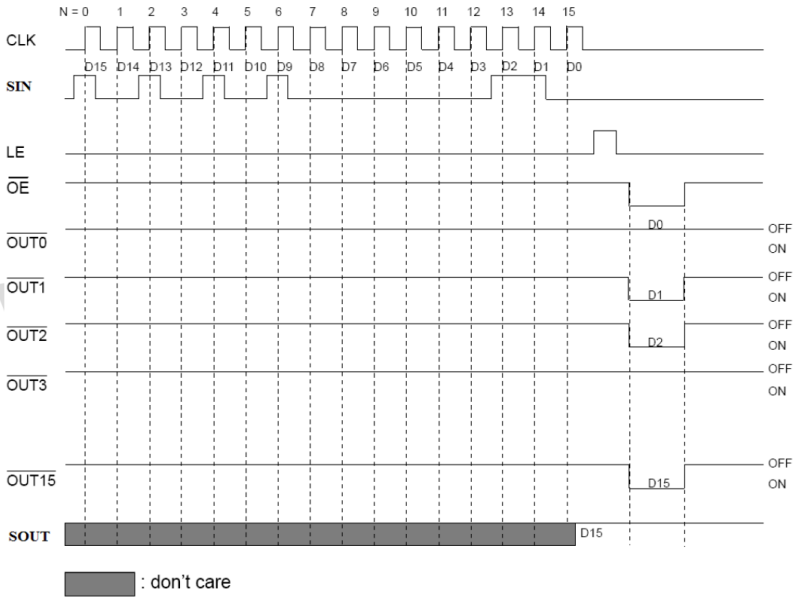
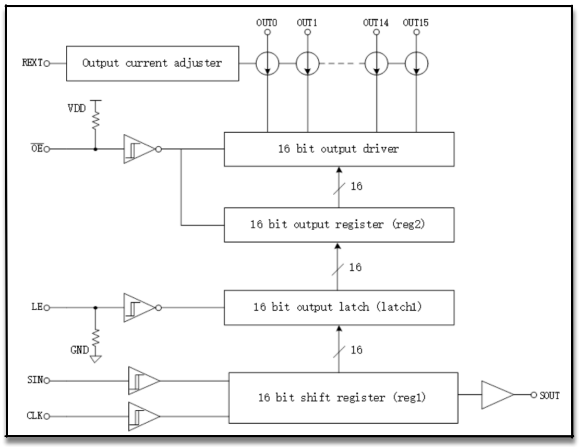
ICN2037 Timing Information



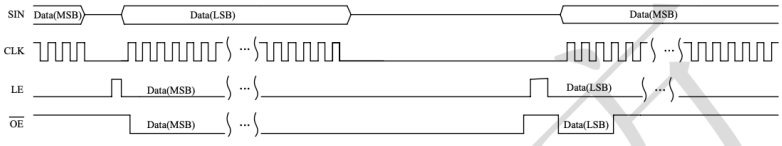


Note 1: When the LE pin is set to L, the latch circuit retains data; when the LE pin is H, the latch circuit does not retain data, and the data is output directly

When the OE (GCLK) pin is L, the OUT0-OUT15 pins will turn ON and OFF to respond to the data; set the OE (GCLK) pin to H, regardless of the data all output pins ..

The pin will be OFF when the OE(GCLK) pin i L, data can be transmitted and latched.

The principle of ICN2037 to improve the refresh rate

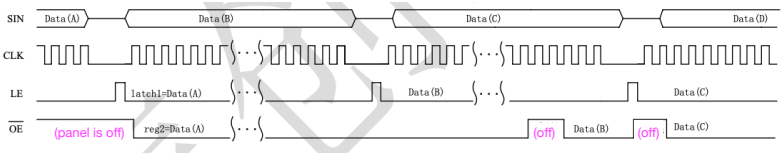


Reasons for low utilization rate of data transmission and data display of general constant current chip:

(1) When display a high-level data, the data display time may be much longer then the data transmission time, and the data cannot be counted during the extra time of the data display. According to transmission.

(2) When displaying low-level data, the data display time may be much shorter than the data transmission time, and the data cannot be counted during the extra time of data transmission. According to the show.

ICN2037 data transmission and data display timing diagram



ICN2037 data transmission and data display timings are shown in the figure above, data(A) and data(C) are high data, data(B) and data(D) high and low data. Will show…

The high and low bits of the display data are combined according to time, so that the excess time of the display high data can be used for data transmission, or use the time of data transmission to …

For hight-level display, the perfect combination of data transmission and display can effectively improve the display refresh rate. The basic steps are as follows:

(1) When the data(A) transfer is completed, a latch signal is generated on LE to latch data(A)

(2) After the data(A) is latched, OE changes from 1 to 0, to register data(A) and display data(A)

(3) While displaying data(A), transfer data(B)

(4) After the data(B) transfer is completed, the latch signal LE is generated, data(B) is latched, and then data(C) is transfered.

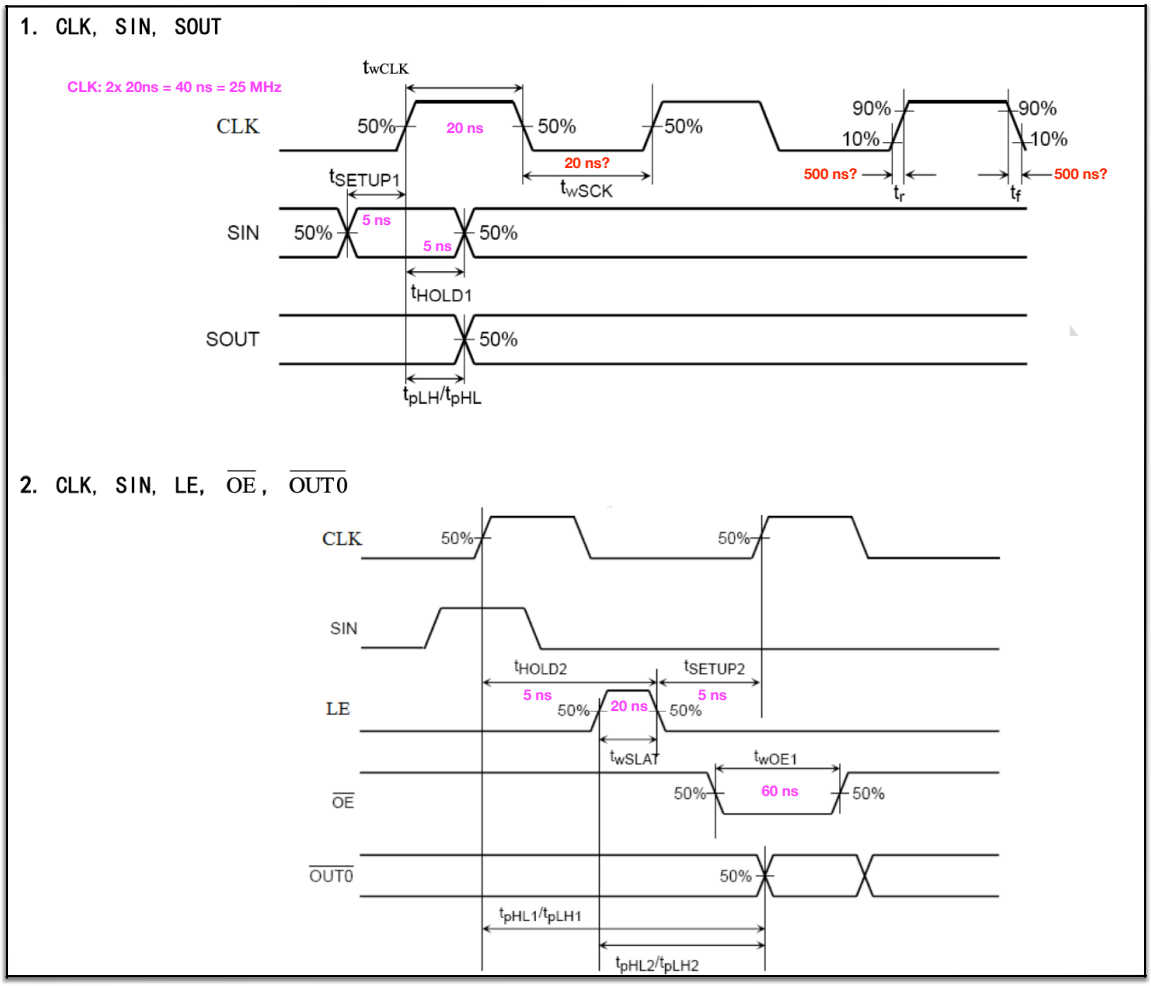
(5) After completing the display of data(A), register data(B) and display data(B)

(6) Complete the transmission of data(C), complete the display of data(B)

(7) register data(C) and transmit data(D), (same as step 1)

ICN2037 - 16 channels double buffer constant current output LED driver chip

ICN2037 Timing Information



Characteristic	Symbol	Test Circuit	Test Conditions	Minimum	Typical	Maximum	Unit
Serial Data Freq.	Fclk	6				30	MHz
Clock pulse width	TwCLK	6	SCK=H or L	20			ns
Latch pulse width	TwLE	6	LE=H	20			ns
Enable pulse width	TwOE	6	OE=H or L, Rext=890 Ohm	60			ns
Hold Time	THld1	6		5			ns
	THld2	6		5			ns
Setup Time	TSup1	6		5			ns
	TSup2	6		5			ns
Max clock rise time	Tr	6				500	ns
Max clock fall time	Tf	6				500	ns