Shenzhen Fuman Electronics Group Co., Ltd.

SHEN ZHEN FINE MADE ELECTRONICS GROUP CO., LTD.

FM6124 (File No.: S&CIC1501) **16-** channel double buffer constant current output **LED** driver chip

Overview

FM6124 is a driver IC specially designed for LED modules and displays, with 16 constant current output driving capabilities. FM6124 adopts

The patented technology of “Out Clamping” can effectively eliminate the dark phenomenon of the first line and prevent damage to the lamp beads. FM6124 adopts an enhanced blanking function design,

Has an excellent blanking effect. At the same time, FM6124 has excellent anti-interference characteristics, constant current and low ash effects are not affected by the PCB board. And can choose differen

The external resistor can adjust the current of the output stage arbitrarily and accurately control the brightness of the LED.

FM6124 will buffer 16bit display data during the display process (the falling edge of OE), so the system can continue to save the data during the display process of FM6124

16bit serial data, compared with general constant current source chip, the refresh rate can be increased by more than 50%.

FM6124 internally adopts current precision control technology, which can make the error between chips less than ±3.5% and the error between channels less than ±2%.

Features

- ▢ 16 equal current output channels
- ▢ Output current setting range:
  - 0.7 ~ 32mA×16@V_{DD} =5V constant current output
  - 0.5 ~ 25mA×16@V_{DD} =3.3V constant current output
- ▢ Current accuracy
  - Current non-uniformity between channels: ±1.25% (typical value)
    ±2% (maximum)
  - Current non-uniformity between chips: ±2% (typical value)
    ±3.5% (maximum)
- ▢ Fast output current response (minimum value): 30ns@V_{DD} =5V
- ▢ I/O Schmitt trigger trigger input
- ▢ Data transmission frequency: f_{MAX} =30MHz (maximum)
- ▢ ESD HBM PASS 4KV
- ▢ Power supply voltage: V_{DD} =3.3 ~ 6V
- ▢ Working temperature range: T_{OPR} =-40 ~ 85°C
- ▢ Has the function of improving lamp bead damage
- ▢ Has excellent blanking effect
- ▢ Effectively eliminate the dark, low gray block, low gray color cast and low gray pitting in the first row
- ▢ Has excellent anti-interference ability and low grayscale effect
- ▢ Improve the caterpillar phenomenon caused by lamp bead damage
- ▢ Integrated double buffer, refresh rate is more than 50% higher than general constant current chip
- ▢ Package form: SSOP-24

Pin definition and description

Pin number	Pin definition	Pin name
1	GND	Chip ground pin
2	SDI	Serial data input to the shift register
3	CLK	Clock signal input terminal
4	LA	When the data latch input terminal LE is high, the data is passed in To the latch.
5-20		Constant current output terminal
twenty one		Output enable signal input terminal, and buffer the number at the falling edge according to When OE is high, turn off OUT0-OUT15 When OE is low, open OUT0-OUT15
twenty two	SDO	The serial data output terminal can be connected to the next driver chip SDI side
twenty three	REXT	The output terminal of the external adjustment resistor can adjust the Output current
twenty four	VDD	3.3V/5V power input

Internal block diagram

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I/O equivalent circuit

Timing diagram

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Truth table

CLK	LE		SIN	... ...	SOUT
	H	L	Dn	DN`···DN-7···DN-15	DN-15
	L	L	Dn+1	No change	DN-14
	H	L	Dn+2	DN+2···DN-5···DN-13	DN-13
	X	L	Dn+3	DN+2···DN-5···DN-13	DN-13
	X	H	Dn+3	OFF	DN-13

Absolute maximum rating (**TA=25** °C)

characteristic	symbol	Rated value	unit
voltage	VDD	0-7.0	V
Output current	IO	32	mA
Input voltage	VIN	-0.4—VDD+0.4	V
Output withstand voltage	VOUT	30	V
Clock frequency	FCLK	30	MHZ
Ground current	IGND	512	mA
Power consumption	PD	3	W
Thermal impedance	RTH(ja)	39.15	°C/W
Operating temperature	TOPR	-40—85	°C
storage temperature	TSTG	-55—150	°C

DC characteristics (If not otherwise specified, **TA=40** °C **—85** °C)

characteristic	symbol	Test Conditions	Minimum	Typical value	Max	unit
voltage	VDD	-	3.3	5	6.0	V
Output voltage when ON	VO(ON)		0.6	-	4	V
High level logic input voltage	VIH	-	0.7*VDD	-	VDD	V
Low level logic input voltage	VIL	-	GND	-	0.3*VDD	V
SOUT high level output current	IOH	VDD=5V	-	-1	-	mA
SOUT low-level output current	IOL	VDD=5V	-	1	-	mA
Constant current output	IO		0.5	-	32	mA

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Dynamic characteristics (if not otherwise specified, **VDD=4.5—5.5V** , **TA=40** °C **—85** °C)

characteristic	symbol	Test circuit	Test Conditions	Minimum	Typical value	Max	unit
Serial data transmission frequency	FCLK	6	-	-	-	30	MHZ
Clock pulse width	TWCLK	6	SCK=H/L	20	-	-	nS
Buffer pulse width	TWLE	6	LE=H	20	-	-	nS
Enable pulse width	TWOE	6	=H/L, REXT=890Ω	30	-	-	nS
Hold time	THOLD1	6	-	5	-	-	nS
	THOLD2	6	-	5	-	-	nS
Establishment time	TSETUP1	6	-	5	-	-	nS
	TSETUP2	6	-	5	-	-	nS
Maximum clock rise time	TR	6		-	-	500	nS
Maximum clock fall time	TR	6		-	-	500	nS

Electrical characteristics

characteristic	symbol	Test circuit	Test Conditions	Minimum	Typical value	Max	unit

High level logic The output voltage	VOH	1	IOH=-1mA, SOUT	VDD-0.4	-	VDD	V
Low level logic The output voltage	VOL	1	IOH=+1mA, SOUT	-	-	0.4	V
High level logic Input Current	IIH	2	VIN=VDD,OE,SIN,CLK	-	-	1	uA
Low level logic Input Current	IIL	3	VIN=GND,LE,SIN,CLK	-	-	-1	uA
Power supply current	IDD1	4	REXT=Not connected, OUT OFF	-	2.0	5.0	mA
	IDD2	4	REXT=1200, OUT OFF	-	5.5	9	mA
	IDD3	4	REXT=600, OUT OFF	-	6.5	10	mA
	IDD4	4	REXT=1200, OUT ON	-	8.2	12	mA
	IDD5	4	REXT=600, OUT ON	-	10	15	mA
Constant current output	IO1	5	VDD=5.0V, VO=2.0V, REXT=1.19KΩ	-	15	-	mA
	IO2	5	VDD=5.0V, VO=2.0V, REXT=595Ω	-	30	-	mA
Constant current error	ΔIO	5	VDD=5.0V, VO=2.0V, REXT=1.19KΩ	-	±0.15	±0.37	mA
Constant current power supply Pressure regulation	%/VD D	5	VDD=4.5-5.5V VO=2.0V, REXT=1.19KΩ	-	±0.2	-	%/V

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Constant current output Pressure regulation	%/VO UT	5	VDD=5.0V VO=1.0-3.0V, REXT=1.19KΩ	-	±0.1		%/V
Pull-up resistor	RUP	3		200	240	350	KΩ
Pull-down resistor	RDO WN	2	LE	250	340	450	KΩ

Switch characteristics

characteristic		symbol	Test circuit	Test Conditions	Minimum	Typical Value	Maximum	Unit
Transmission delay time		TPLH3	6	LE=H	-	25	40	nS
		TPHL3	6	LE=H	-	30	50	
	CLK-SOUT	TPHL	6	-	-	25	30	
Output rise time		TOR	6	10-90% of voltage waveform	-	15	20	nS
Fall time of output		TOR	6	90-10% of voltage waveform	-	26	31	nS

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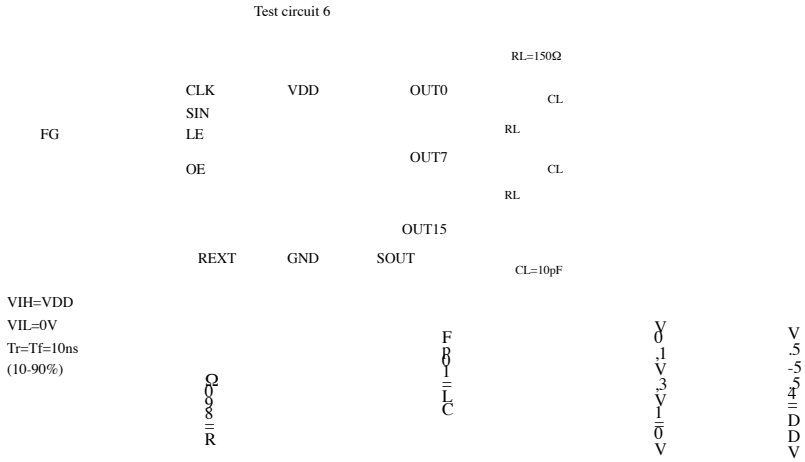
Test circuit



Timing waveform

1. CLK , SIN , SOUT

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2. CLK , **SIN** , **LE** , **OE** , **OUTN**

3.OUTN

Application information

FM6124 uses precise current drive control technology, and the current difference between different channels of the same chip is very small.

1) The current difference between channels is <±2%, and the current difference between chips is <±3.5%.

2) It has current output characteristics that are not affected by the load terminal voltage, as shown in the figure below. The output current will not follow the LED forward voltage V_F The changes change.

Adjust output current

FM6124 adjusts the output current (Iout) through an external resistor Rext. The calculation formula is:

V_{R-EXT} =1.191V;

Iout=(V_{R-EXT} /Rext)*15

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Package information

symbol	Mm		
	Minimum	Typical value	Max
A	-	1.60	1.65
A1	-	0.15	0.20
A2	1.40	1.45	1.50
A3	0.60	0.65	0.70
b	0.22	0.25	0.30
c	0.17	0.22	0.25
D	8.55	8.65	8.75
E	5.90	6.00	6.10
E1	3.80	3.90	4.00
e		0.635BSC	
L	0.57	0.60	0.65
L1		1.05BSC	
θ	0°	3°	6°