

OEM OPERATING INSTRUCTIONS AND SPECIFICATIONS

NI sbRIO-9605/9606 and NI sbRIO-9623/9626/9633/9636

Single-Board RIO OEM Devices

This document provides dimensions, pinouts, connectivity information, and specifications for the National Instruments sbRIO-9605, sbRIO-9606, sbRIO-9623, sbRIO-9626, sbRIO-9633 and sbRIO-9636. The devices are referred to inclusively in this document as the NI sbRIO device.

The NI sbRIO device is available in different configurations. When a feature pertains only to specific models, a list at the beginning of the section shows which models support the feature.

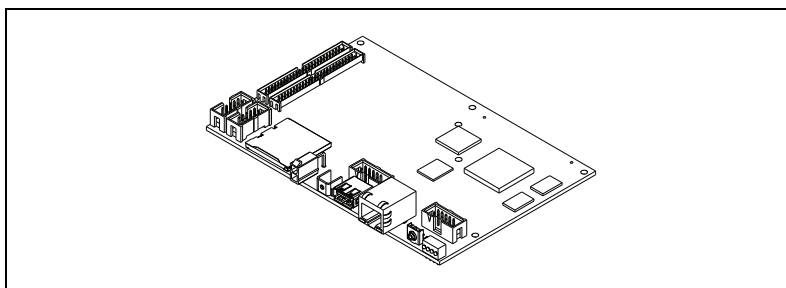


Figure 1. NI sbRIO-9636



Caution The NI sbRIO device must be installed inside a suitable enclosure prior to use. Hazardous voltages may be present.



Caution National Instruments makes no product safety, electromagnetic compatibility (EMC), or CE marking compliance claims for NI sbRIO devices. The end-product supplier is responsible for conformity to any and all compliance requirements.



Caution Exercise caution when placing NI sbRIO devices inside an enclosure. Auxiliary cooling may be necessary to keep the local ambient temperature under the maximum rating for the NI sbRIO device. Refer to the [Specifications](#) section for more information about the maximum local ambient temperature rating.



Caution Do not operate the NI sbRIO device in a manner not specified in these operating instructions. Product misuse can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to National Instruments for repair.

What You Need to Get Started

This section lists the software and hardware you need to start programming the NI sbRIO device.

Software Requirements

You need a development computer with the following software installed on it. Go to ni.com/info and enter the Info Code `rdsoftwareversion` for information about software version compatibility.

- ☐ LabVIEW 2011.1 or later
- ☐ LabVIEW Real-Time Module 2011.1 or later
- ☐ LabVIEW FPGA Module 2011.1 or later
- ☐ NI-RIO 4.1 or later

Hardware Requirements

You need the following hardware to use the NI sbRIO device.

- ☐ NI sbRIO device
- ☐ 9–30 VDC power supply
- ☐ Power plug assembly
- ☐ Ethernet cable

Figure 2 shows the location of features on the NI sbRIO device. The features available vary between device models. Refer to Table 1 or the appropriate section of the manual to see if a feature is available on your model.

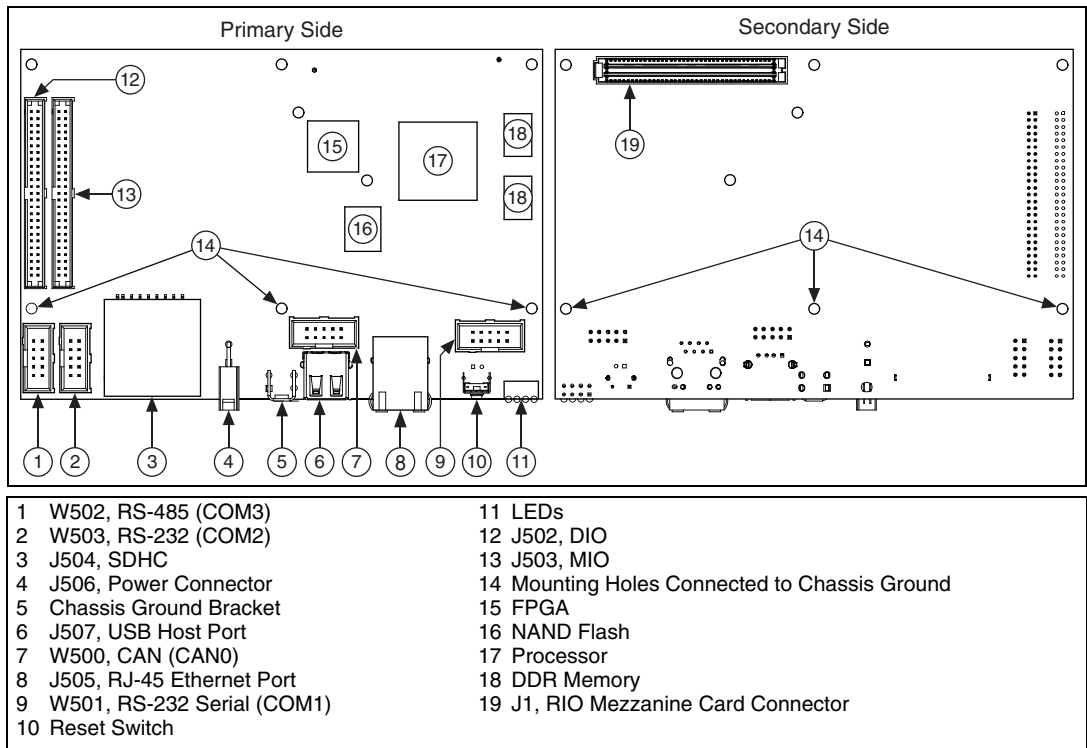


Figure 2. All possible components on the NI sbRIO Device

NI sbRIO Device Features Overview

Table 1 describes the I/O and other components populated on each NI sbRIO device.

Table 1. I/O and other components available on NI sbRIO devices

NI sbRIO device	Memory	RAM	RS-232	RS-485	CAN	USB	SDHC	FPGA	DIO	AI	AO	RMC
sbRIO-9605	256 MB	128 MB	1	—	—	—	—	LX25	—	—	—	1
sbRIO-9606	512 MB	256 MB	1	—	1	1	—	LX45	—	—	—	1
sbRIO-9623	256 MB	128 MB	2	1	—	—	—	LX25	4	16ch-12bit	4ch-12bit	1
sbRIO-9626	512 MB	256 MB	2	1	1	1	1	LX45	4	16ch-16bit	4ch-16bit	1
sbRIO-9633	256 MB	128 MB	2	1	1	1	1	LX25	28	16ch-12bit	4ch-12bit	—
sbRIO-9636	512 MB	256 MB	2	1	1	1	1	LX45	28	16ch-16bit	4ch-16bit	—



Note Devices with an RMC connector have 96 additional FPGA DIO lines available on the connector.

Table 2 lists and describes the connectors on the NI sbRIO device, and the part number and manufacturer of each connector. Refer to the manufacturer for information about using and matching these connectors.

Table 2. NI sbRIO Connector Descriptions

Connector	Description	Manufacturer, Part Number	Recommended Mating Connector	NI Solution
Power	2-position, mini-fit JR, H = 0.411 in.	Molex, 46999-0144	Molex, 50-36-1673 w/ 0457501211	NI, Power Plug Assembly 152834-01
RS-232/485/CAN IDC header	10-pin, 0.100 in. CT, shrouded, H = 0.370 in.	Samtec, TST-105-01-L-D	Tyco, 1658622-1	NI, 10-pin to 9-pin D-SUB, 153158-10
50 Pin IDC Header	50-pin, 2 mm CT, Shrouded, H = 0.155 in.	Samtec, STMM-125-02-L-D	Tyco, 2-111626-3	NI, 50 pos. ribbon cable, 154041-12
RMC Connector	240-pin, 40 x 6 pos., high density open pin field SEARAY	Samtec, SEAF-40-06.5-S-06-2	Samtec, SEAM-40-XX.X-S-06-2	—



Note Samtec SEAM connectors come in multiple heights, indicated in mm by the XX.X portion of the following example part number: SEAM-40-XX.X-S-06-2. The height of the mating connector you select to mate to the RMC connector determines the height of the standoffs you need. Samtec, the connector manufacturer, requires that standoffs be 0.15 mm taller than the combined height of the RMC and mating connectors. Therefore, to determine the required standoff height, you must add the heights of the connectors plus 0.15 mm. For example, if you are using a SEAM-40-03.0-S-06-2 connector to mate to the RMC connector (SEAF-40-06.5-S-06-2), the required standoff height is $3.0\text{ mm} + 6.5\text{ mm} + 0.15\text{ mm} = 9.65\text{ mm}$. Standoffs of this height are available from National Instruments (NI 153166-12) or Samtec (SO-0965-03-02-L-N). Consult Samtec for alternative heights and options. You must observe keepouts and maximum heights with all RMC and mating connector combinations.

Dimensions

This section contains dimensional drawings of the NI sbRIO devices. For three-dimensional models, refer to the **Resources** tab of the NI sbRIO product page at ni.com.

Figure 3 shows the dimensions of the primary side of the NI sbRIO device.

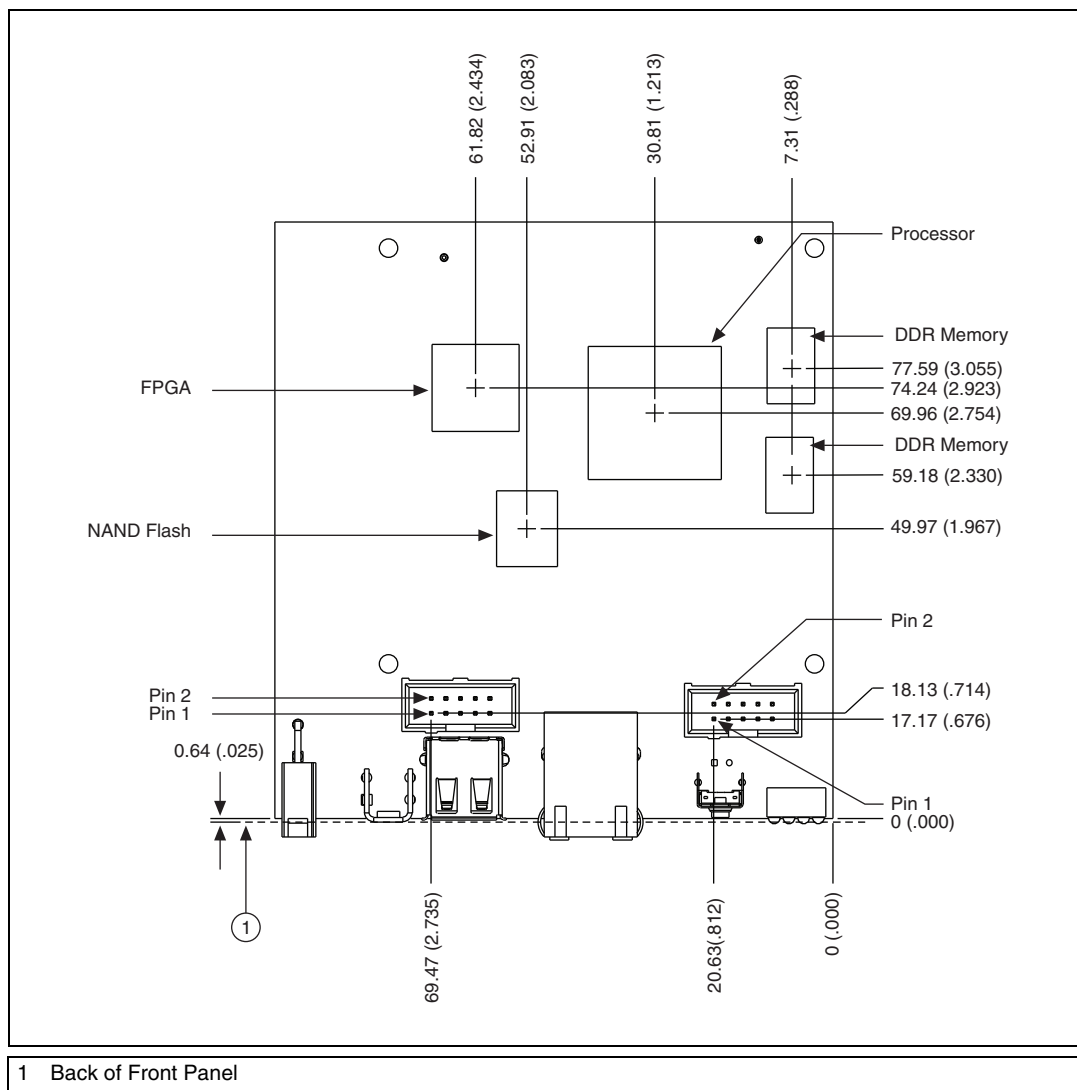


Figure 3. NI sbRIO-9605/9606 Primary-Side Dimensions in mm (in.)

Figure 4 shows the dimensions of the secondary side of the NI sbRIO device.

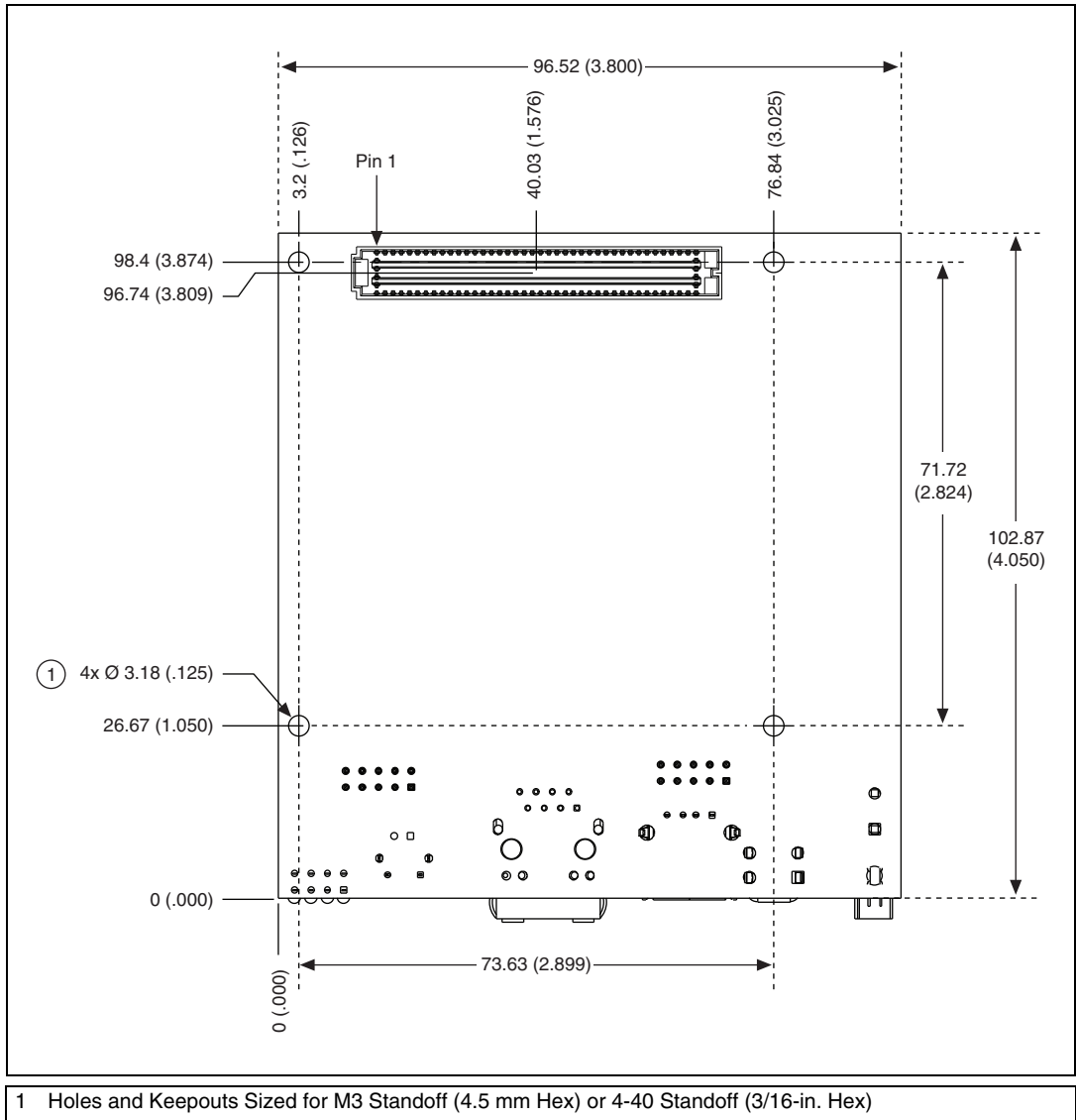


Figure 4. NI sbRIO-9605/9606 Secondary-Side Dimensions in mm (in.)

Figure 5 shows the dimensions of the primary side of the NI sbRIO device.

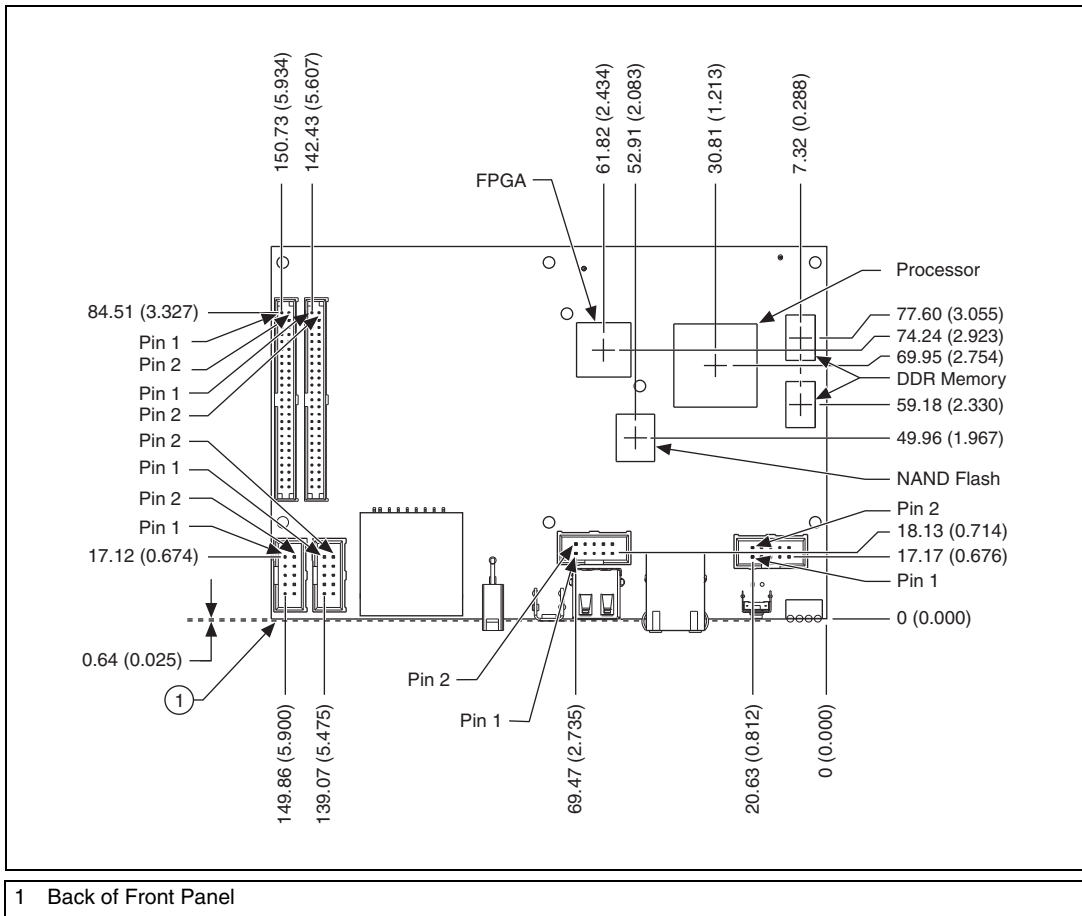


Figure 5. NI sbRIO-9623/9633/9626/9636 Primary-Side Dimensions in mm (in.)

Figure 6 shows the dimensions of the secondary side of the NI sbRIO device.

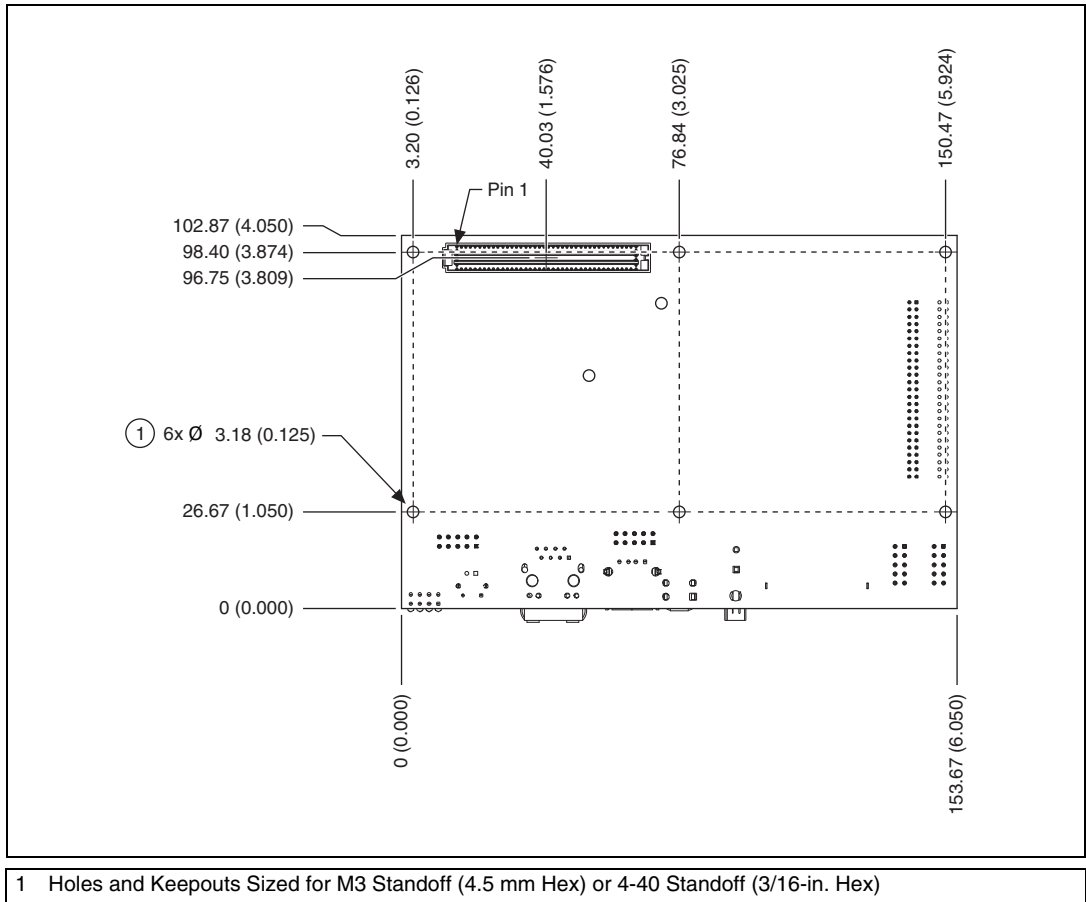


Figure 6. NI sbRIO-9623/9633/9626/9636 Secondary-Side Dimensions in mm (in.)

Figure 7 shows the dimensions of the front of the NI sbRIO device.

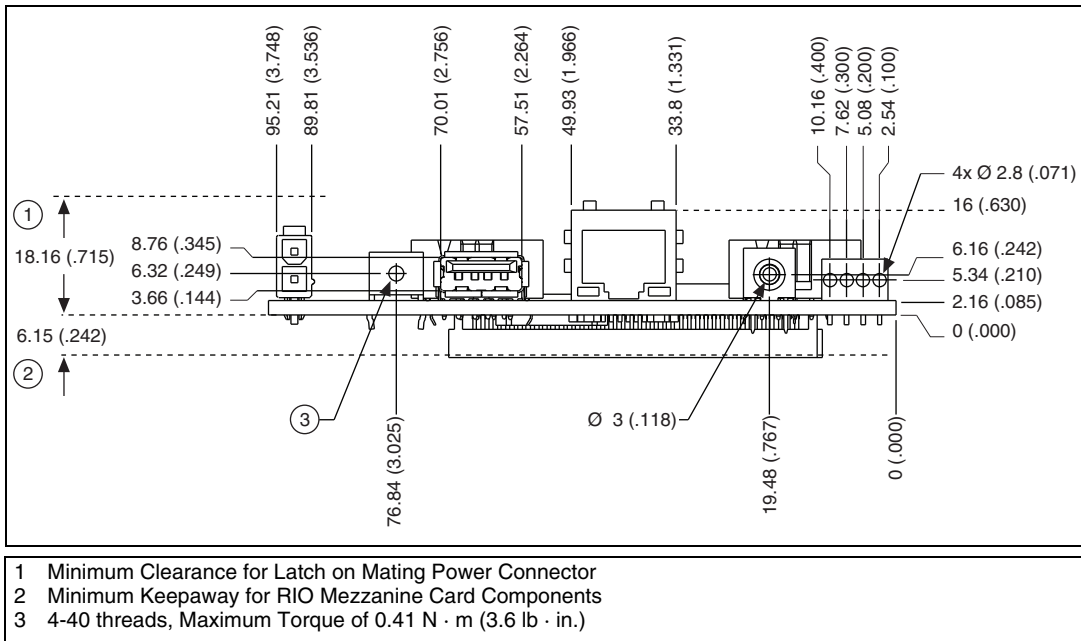


Figure 7. NI sbRIO-9605/9606 Front Dimensions in mm (in.)

Figure 8 shows the dimensions of the front of the NI sbRIO device.

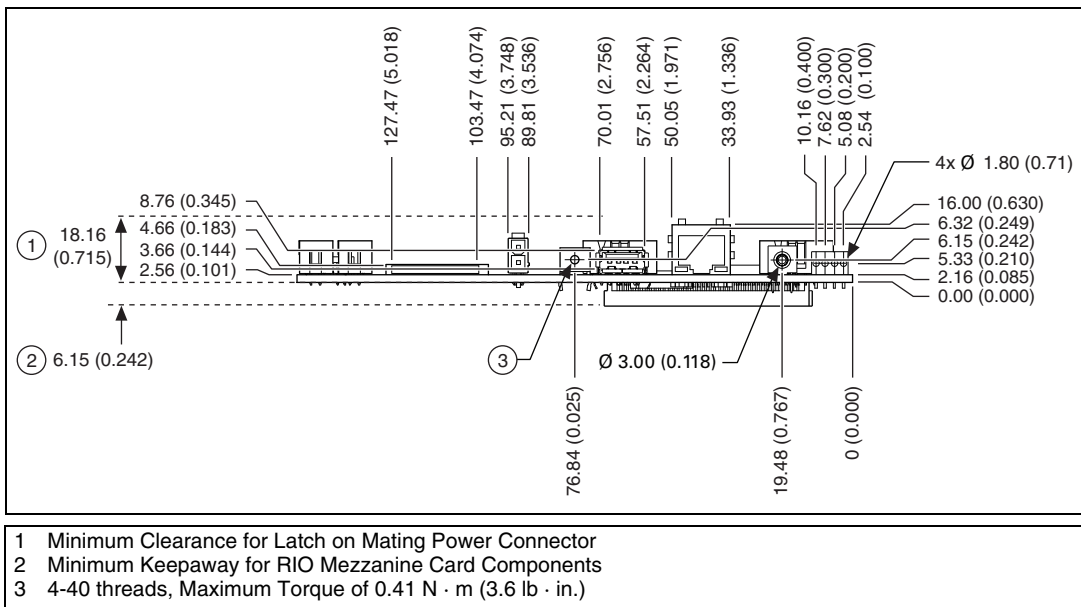


Figure 8. NI sbRIO-9623/9633/9626/9636 Front Dimensions in mm (in.)



Note For more information about the dimensions of the NI sbRIO device, including detailed dimensional drawings, go to ni.com/dimensions.

Maximum Component Heights

The primary side of the NI sbRIO device is the top side of the PCB populated with the power and Ethernet connectors. The secondary side is the bottom. Figures 9 to 12 show the maximum component heights for the different regions of the primary and secondary sides.



Note In addition to the maximum component heights, you must also observe minimum keepaway distances for adjacent PCBs and surfaces. Allow 19.05 mm (0.75 in.) from the surface of the primary side and 7.62 mm (0.300 in.) from the surface of the secondary side.

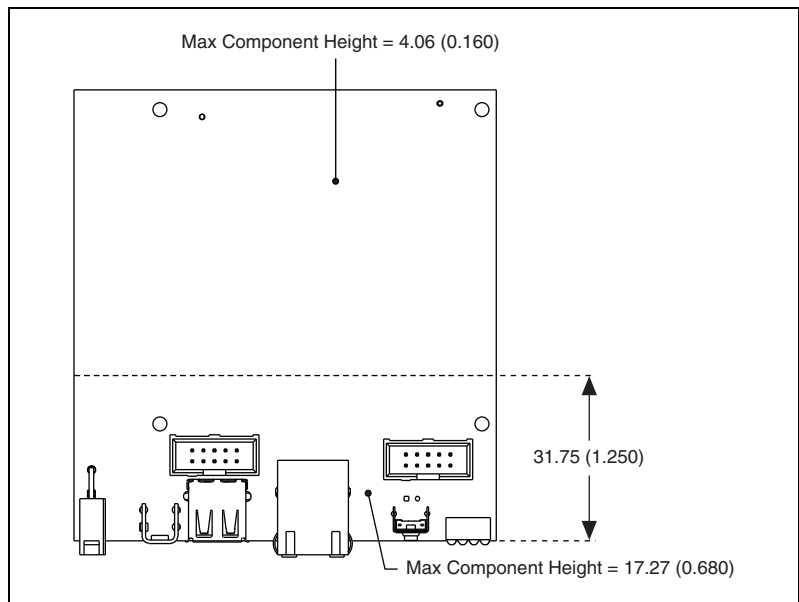


Figure 9. NI sbRIO-9605/9606 Maximum Component Height of Primary Side in mm (in.)

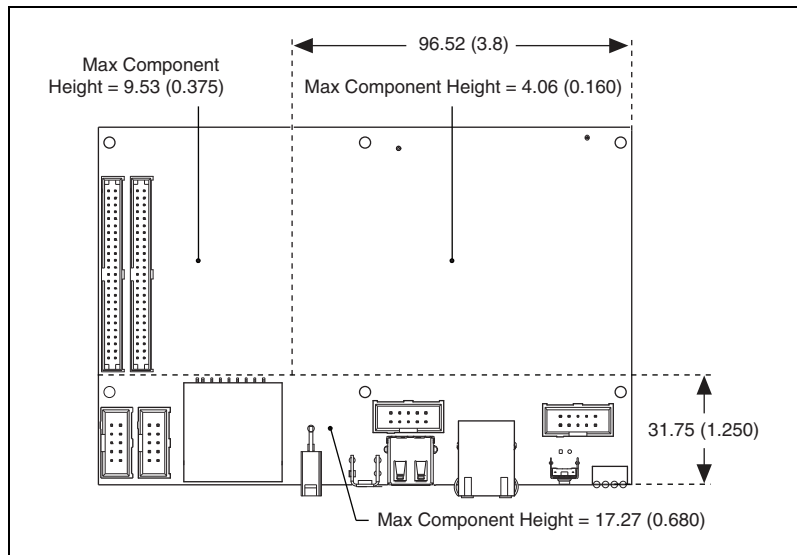


Figure 10. NI sbRIO-9623/9633/9626/9636 Maximum Component Height of Primary Side in mm (in.)

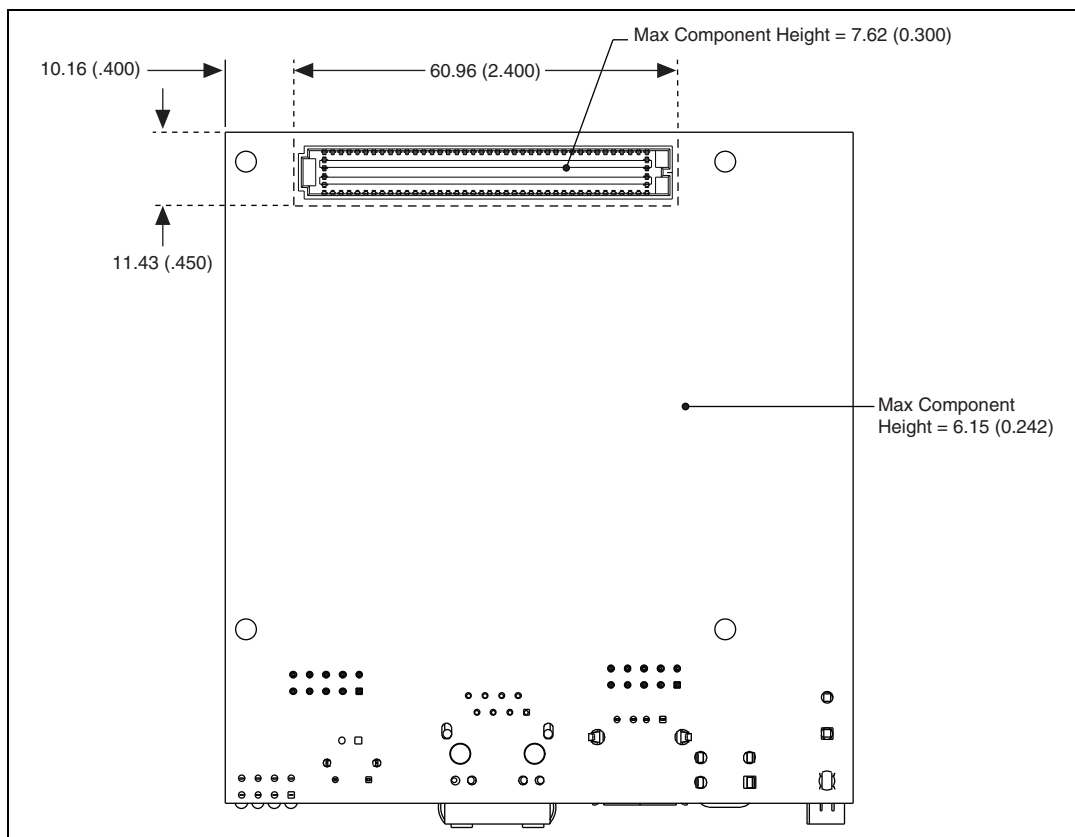


Figure 11. NI sbRIO-9605/9606 Max Component Height of Secondary Side in mm (in.)

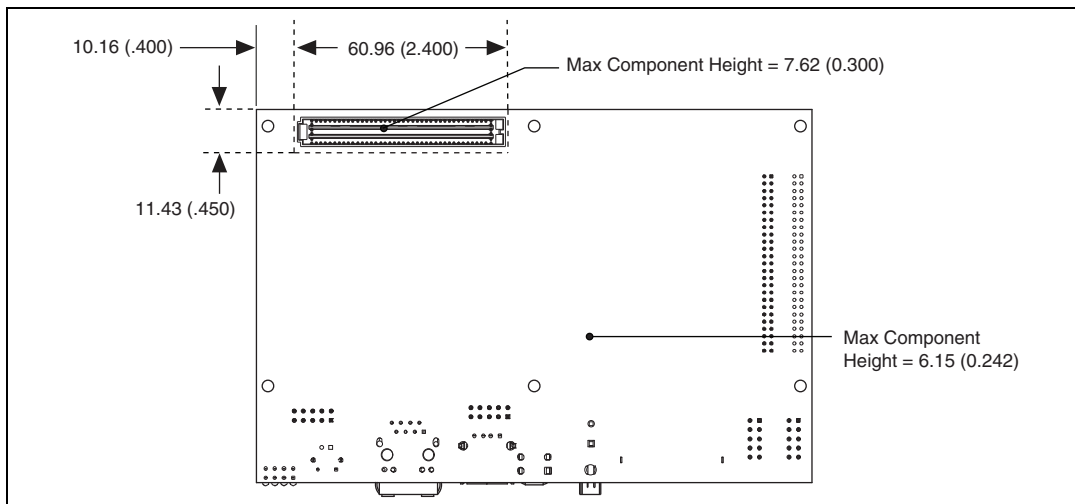


Figure 12. NI sbRIO-9623/9633/9626/9636 Max Component Height of Secondary Side in mm (in.)

Mounting the NI sbRIO Device

The following sections describe how to mount and mate RIO Mezzanine Cards to the NI sbRIO device.

Mounting the NI sbRIO Device

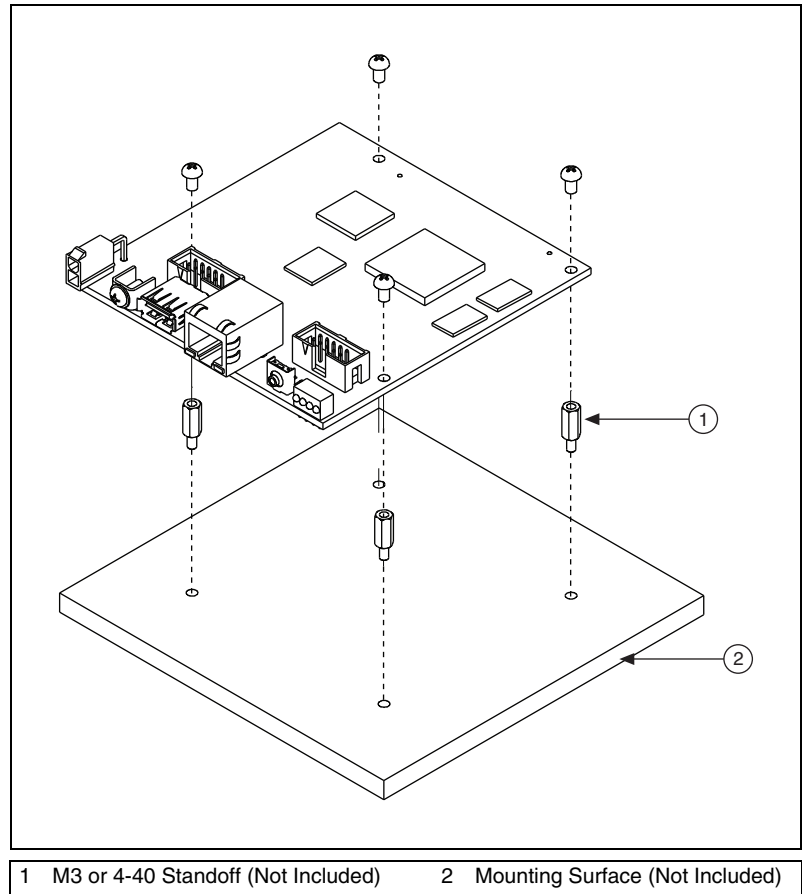


Figure 13. NI sbRIO Device Mounting Procedure



Note Mounting holes on the NI sbRIO device are designed to accommodate M3 or 4-40 fasteners, and standoffs or bosses up to 4.5 mm or 3/16 in. in diameter.



Caution Maintain a minimum keepaway distance of 7.62 mm (0.300 in) when mounting NI sbRIO devices with an RMC connector, and a minimum keepaway distance of 6.15 mm (0.242 in.) when mounting NI sbRIO devices without an RMC connector.

Mating the NI sbRIO Device to a RIO Mezzanine Card

This section applies only to the following NI sbRIO devices:

- NI sbRIO-9605 • NI sbRIO-9623
- NI sbRIO-9606 • NI sbRIO-9626

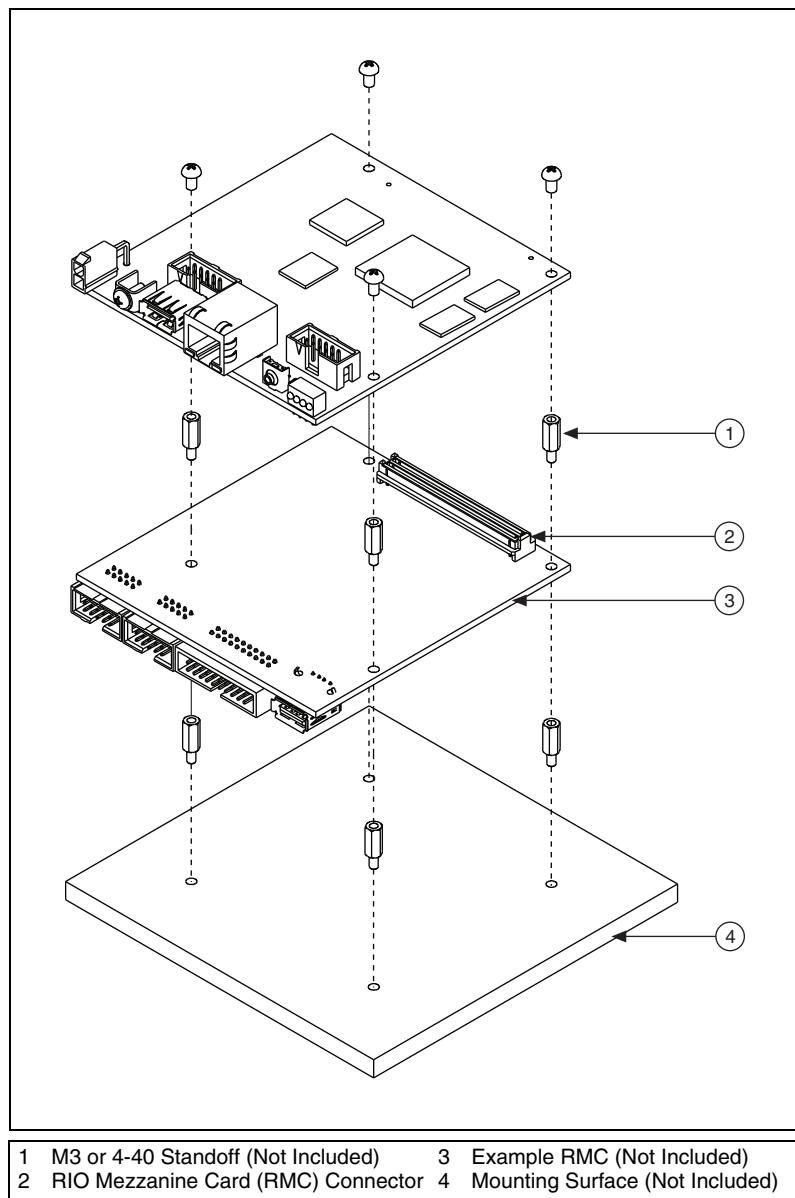


Figure 14. NI sbRIO- Device Mating Procedure

Understanding Ground Connections

The front I/O connector shields, chassis ground bracket, and mounting holes near the front I/O are connected together internally to form chassis ground. Chassis ground is capacitively coupled to digital ground near the power connector. For the best possible ESD protection, connect chassis ground at the mounting holes or the chassis ground bracket to a low inductance earth ground.

When connecting the NI sbRIO device to external devices, ensure that stray ground currents are not using the device as a return path. Significant stray currents traversing through the NI sbRIO device can result in device failure.

To verify correct grounding of the NI sbRIO device, make sure the current flowing into the power connector equals the current flowing out of the power connector. These currents should be measured with a current probe after final assembly of the end system. Investigate and remove any current differences.

Connector Pinouts

The following figures show the pinouts of the I/O connectors on the NI sbRIO device.

Power Connector

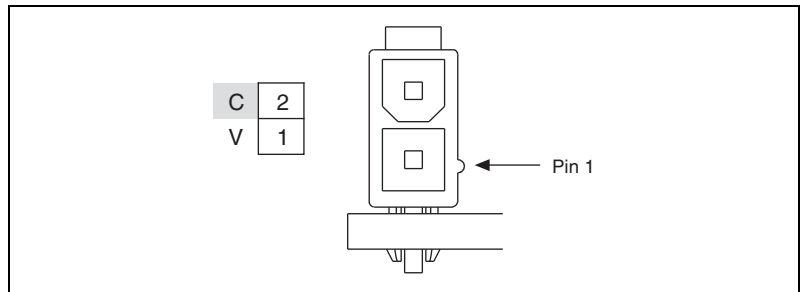


Figure 15. Pinout of the Power Connector

RS-232/CAN Connectors

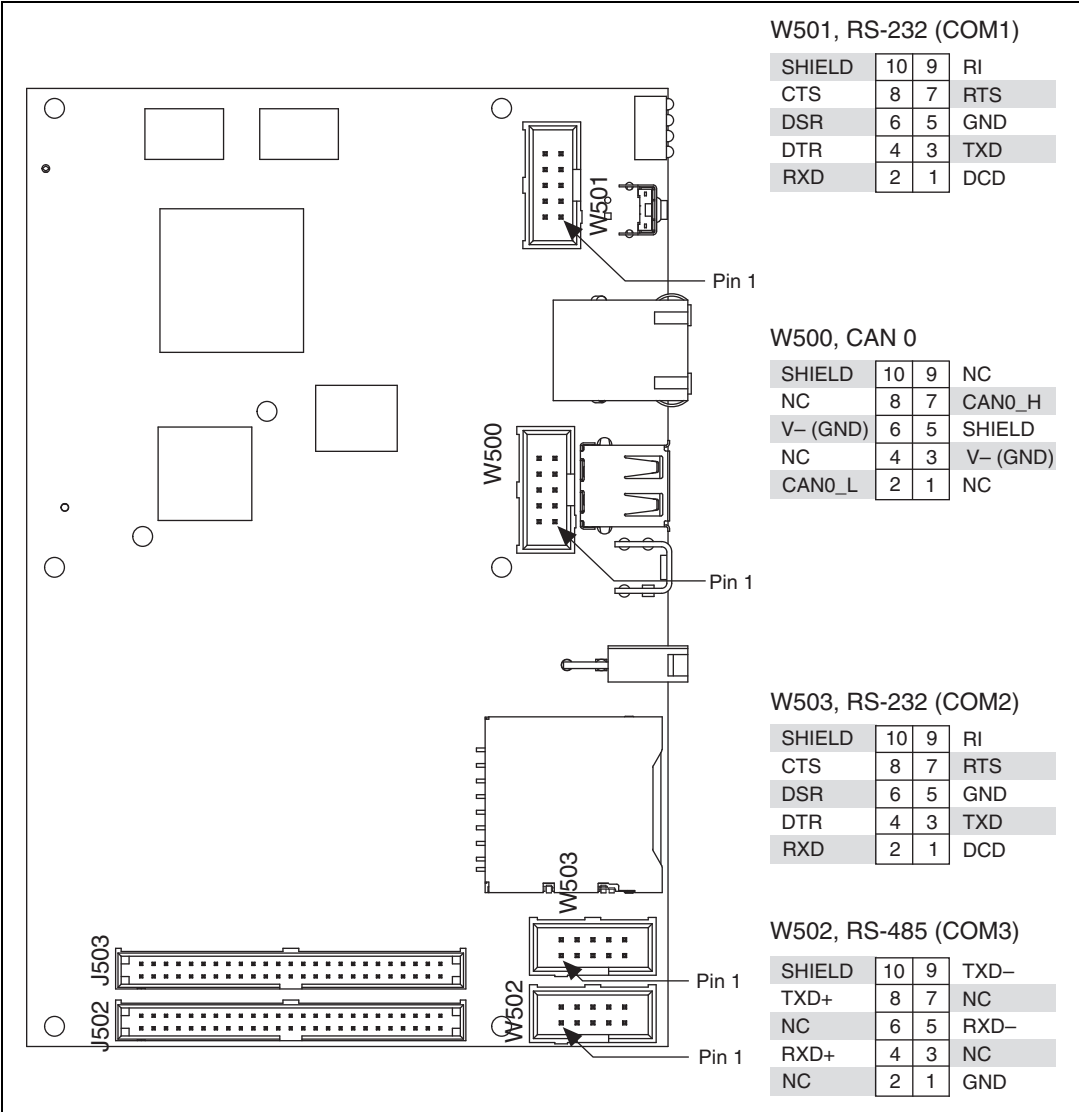


Figure 16. Pinout of the Serial and CAN Connectors

J503/DIO Connectors

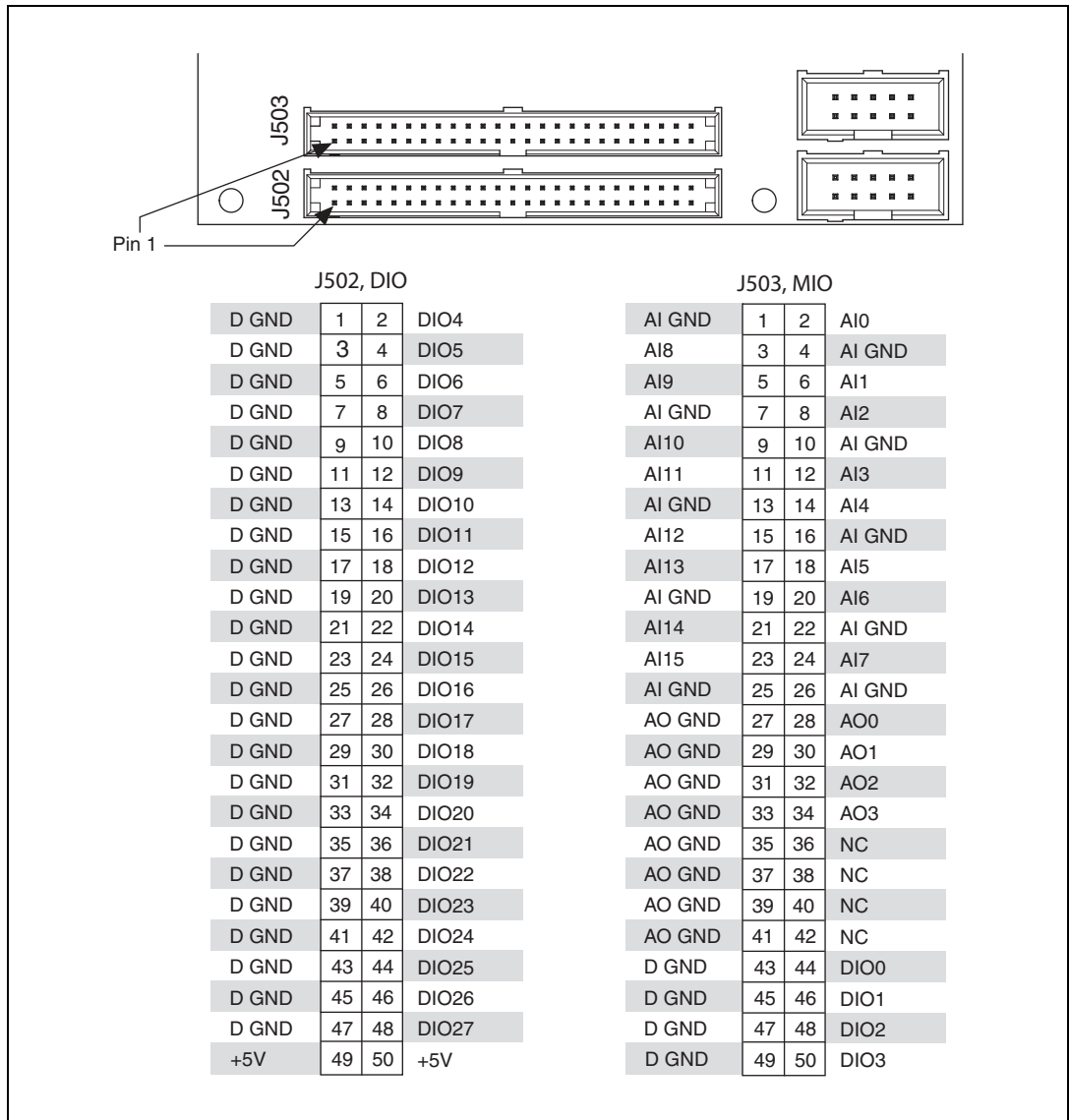


Figure 17. Pinout of DIO and MIO Connectors

RIO Mezzanine Card Connector

This section applies only to the following NI sbRIO devices:

- NI sbRIO-9605
- NI sbRIO-9623
- NI sbRIO-9605
- NI sbRIO-9626

The RIO Mezzanine Card connector provides connections for 96 FPGA I/O channels, as well as pins reserved for future use.

The table on the following page lists the pinout for the RIO Mezzanine Card connector, indicating the pin number and corresponding function.



Note Users interested in additional processor functionality such as serial, CAN, USB, or Ethernet should contact a local National Instruments representative for custom design opportunities. A non-recurring engineering charge (NRE) may apply.



Note Reserved and unused lines should be left disconnected on RIO Mezzanine Cards. Future versions of this manual may update their definition.



Note National Instruments suggests using pins DIO0 through DIO63 first to maintain future compatibility. DIO64 through DIO95 are not guaranteed to be provided on future products.



Caution RMCs are not hot-swappable. Disconnect power before mating or unmating.

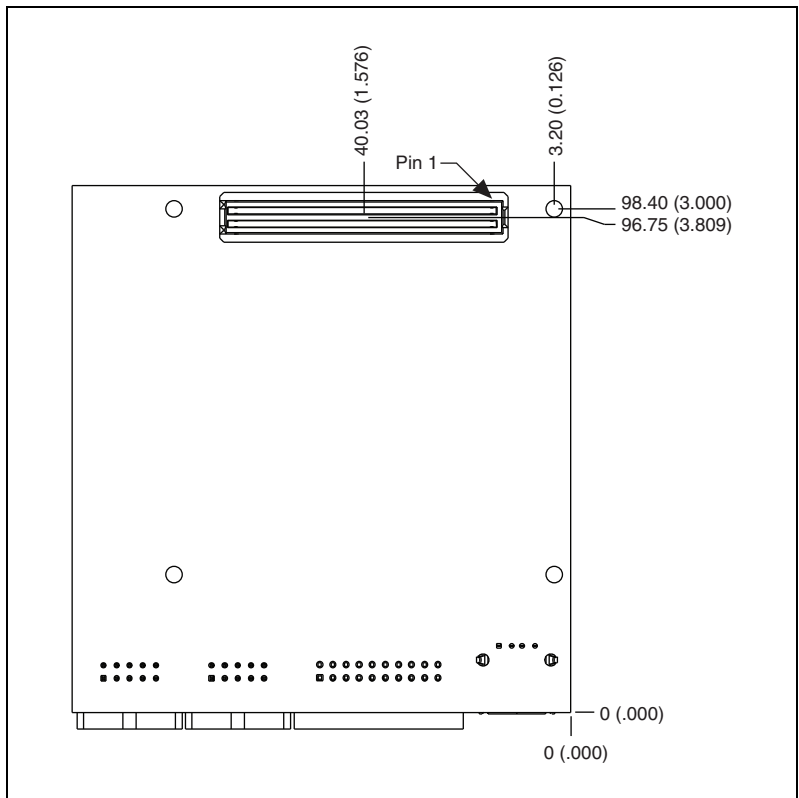


Figure 18. RMC Connector Location and Dimensions on Example RIO Mezzanine Card

Table 3. RIO Mezzanine Card Connector Pinout

1-RESERVED	2-RESERVED	3-RESERVED	4-RESERVED	5-RESERVED	6-RESERVED
7-RESERVED	8-RESERVED	9-RESERVED	10-RESERVED	11-RESERVED	12-RESERVED
13-RESERVED	14-RESERVED	15-RESERVED	16-RESERVED	17-GND	18-RESERVED
19-RESERVED	20-RESERVED	21-RESERVED	22-RESERVED	23-GND	24-RESERVED
25-RESERVED	26-RESERVED	27-RESERVED	28-RESERVED	29-USB_D+	30-GND
31-RESERVED	32-RESERVED	33-RESERVED	34-RESERVED	35-USB_D-	36-GND
37-RESERVED	38-RST#	39-RESERVED	40-RESERVED	41-GND	42-RESERVED
43-RESERVED	44-RESERVED	45-RESERVED	46-RESERVED	47-GND	48-RESERVED
49-RESERVED	50-RESERVED	51-RESERVED	52-RESERVED	53-RESERVED	54-5V
55-RESERVED	56-RESERVED	57-RESERVED	58-RESERVED	59-RESERVED	60-5V
61-RESERVED	62-RESERVED	63-RESERVED	64-RESERVED	65-RESERVED	66-5V
67-RESERVED	68-RESERVED	69-RESERVED	70-RESERVED	71-RESERVED	72-5V
73-RESERVED	74-RESERVED	75-RESERVED	76-RESERVED	77-RESERVED	78-GND
79-RESERVED	80-RESERVED	81-RESERVED	82-RESERVED	83-GND	84-RESERVED
85-RESERVED	86-RESERVED	87-RESERVED	88-GND	89-DIO47	90-DIO15
91-RESERVED	92-DIO63	93-GND	94-DIO79	95-DIO46	96-GND
97-DIO95	98-GND	99-DIO31	100-DIO78	101-GND	102-DIO14
103-GND	104-DIO62	105-DIO30	106-GND	107-DIO45	108-DIO13
109-DIO94	110-DIO61	111-GND	112-DIO77	113-DIO44	114-GND
115-DIO93	116-GND	117-DIO29	118-DIO76	119-GND	120-DIO12
121-GND	122-DIO60	123-DIO28	124-GND	125-DIO43	126-DIO11
127-DIO92	128-DIO59	129-GND	130-DIO75	131-DIO42	132-GND
133-DIO91	134-GND	135-DIO27	136-DIO74	137-GND	138-DIO10
139-GND	140-DIO58	141-DIO26	142-GND	143-DIO41	144-DIO9
145-DIO90	146-DIO57	147-GND	148-DIO73	149-DIO40	150-GND
151-DIO89	152-GND	153-DIO25	154-DIO72	155-GND	156-DIO8
157-GND	158-DIO56	159-DIO24	160-GND	161-DIO39	162-DIO7
163-DIO88	164-DIO55	165-GND	166-DIO71	167-DIO38	168-GND
169-DIO87	170-GND	171-DIO23	172-DIO70	173-GND	174-DIO6
175-GND	176-DIO54	177-DIO22	178-GND	179-DIO37	180-DIO5
181-DIO86	182-DIO53	183-GND	184-DIO69	185-DIO36	186-GND
187-DIO85	188-GND	189-DIO21	190-DIO68	191-GND	192-DIO4
193-GND	194-DIO52	195-DIO20	196-GND	197-DIO35	198-DIO3
199-DIO84	200-DIO51	201-GND	202-DIO67	203-DIO34	204-GND
205-DIO83	206-GND	207-DIO19	208-DIO66	209-GND	210-DIO2
211-GND	212-DIO50	213-DIO18	214-GND	215-DIO33	216-DIO1
217-DIO82	218-DIO49	219-GND	220-DIO65	221-DIO32	222-GND
223-DIO81	224-GND	225-DIO17	226-DIO64	227-GND	228-DIO0
229-GND	230-DIO48	231-DIO16	232-GND	233-RESERVED	234-FPGA_VIO
235-DIO80	236-VBAT	237-GND	238-RESERVED	239-FPGA_CONF	240-FPGA_VIO

RMC Power Requirements

The RIO Mezzanine Card connector provides power on six pins. The 5 V rail consists of pins 54, 60, 66, and 72, and is the main source of power to a RIO Mezzanine Card. The FPGA_VIO rail consists of pins 234 and 240, and is used to supply I/O power and determine I/O levels for the FPGA I/O pins.

Table 4 lists the rail requirements for each of the rails on a RIO Mezzanine Card connector.

Table 4. NI RIO Mezzanine Card Rail Requirements

	Voltage Tolerance	Max Current	Max Ripple and Noise
5 V	+/- 5%	1.5 A	50 mV
FPGA_VIO (3.3 V)	+/- 5%	0.33 A	50 mV

RIO Mezzanine Cards should not source any current onto any of the power pins and should be able to tolerate 5 V and FPGA_VIO coming up in any order.

RMC VBAT

The NI sbRIO device implements an onboard real-time clock (RTC) to keep track of absolute time. The RMC connector provides a VBAT line to power the RTC. Without a battery, absolute time will be reset during a power cycle. Batteries connected to VBAT must have a nominal output between 3.0 V and 3.6 V, and a maximum output of 3.7 V. If VBAT is not being used, leave it disconnected.

USB on RMC Connector

The USB pair on the RMC Connector has a 90 Ω differential trace impedance. To ensure the best possible signal integrity, route the USB pair with a similar trace impedance. If USB is not being used, leave it disconnected.

RMC RST#

The RST# signal indicates that power provided through the RMC Connector is valid. RST# is guaranteed to be asserted (active low) for at least 1 ms when the controller is powered up or reset. There should be no more than 30 pF on the RST# line of a RIO Mezzanine Card. This includes the RMC Connector, traces, vias, and device pins. Refer to [3.3 V Digital I/O on RIO Mezzanine Card Connector](#) in the *Specifications* section for output logic levels.

FPGA_CONF

The FPGA_CONF signal asserts high when the FPGA has been programmed. When the FPGA is unconfigured the signal is floating. A pulldown resistor is required when using this signal to ensure it returns to ground.

3.3 V Digital I/O

The NI sbRIO device provides 3.3 V digital I/O via the RIO Mezzanine Card connector and the 50-pin IDC headers. The following sections provide figures and specifications for a single DIO channel on each connector.

3.3 V DIO on RMC Connector

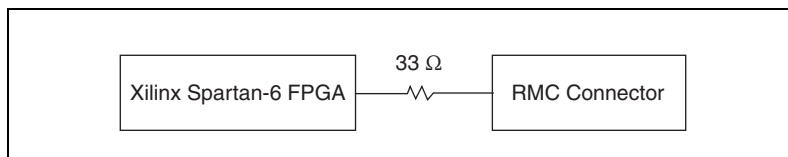


Figure 19. Circuitry of One 3.3 V DIO Channel on the RIO Mezzanine Card Connector

The NI sbRIO device is tested with all DIO channels driving ± 3 mA DC loads. DIO lines are floating before and during FPGA configuration. To ensure startup values, place pull-up or pull-down resistors on a RIO Mezzanine Card. The DIO channels on the NI sbRIO device are routed with a $55\ \Omega$ characteristic trace impedance. Route all RIO Mezzanine Cards with a similar impedance to ensure the best signal quality. Refer to [3.3 V Digital I/O on RIO Mezzanine Card Connector](#) in the *Specifications* section for the logic levels.

3.3 V DIO on IDC Header

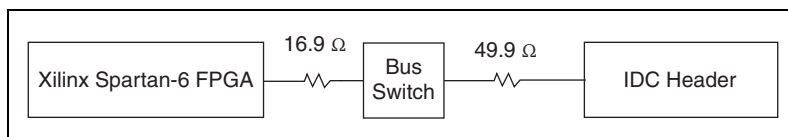


Figure 20. Circuitry of One 3.3 V DIO Channel on the IDC Header

The NI sbRIO device is tested with all DIO channels driving ± 3 mA DC loads. DIO lines are floating before and during FPGA configuration. To ensure startup values, place pull-up or pull-down resistors on a RIO Mezzanine Card. The DIO channels on the NI sbRIO device are routed with

a 55 Ω characteristic trace impedance. Route all RIO Mezzanine Cards with a similar impedance to ensure the best signal quality. Refer to [3.3 V Digital I/O on 50-Pin IDC Connector](#) in the *Specifications* section for the logic levels.

Integrated Analog Input

This section applies only to the following NI sbRIO devices:

- NI sbRIO-9623 • NI sbRIO-9633
- NI sbRIO-9626 • NI sbRIO-9636

Each NI sbRIO-9623/9633 devices has 16 multiplexed, 0–5 V, single-ended, 12-bit analog input (AI) channels. Each NI sbRIO-9626/9636 device has 16 multiplexed, ± 10 V, single-ended or eight differential, 16-bit AI channels. Connector J503, the MIO connector, provides connections for analog inputs, outputs, and grounds. Refer to Figure 17 for a pinout of connector J503.

The following figure shows the circuitry for one AI channel on the NI sbRIO-9623/9633.

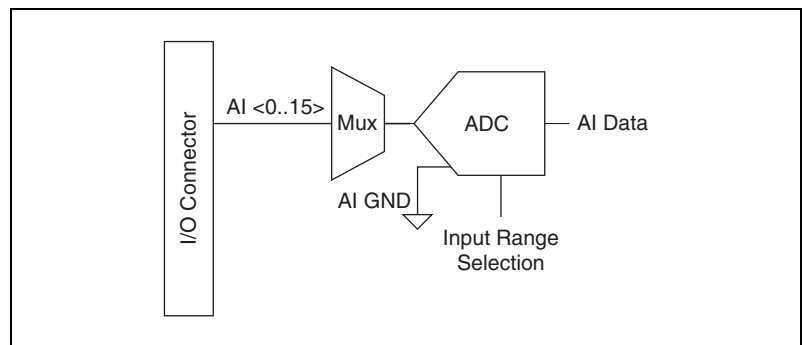


Figure 21. Single-Ended Analog Input on the NI sbRIO-9623/9633

The following figure shows the circuitry for one AI channel on the NI sbRIO-9626/9636.

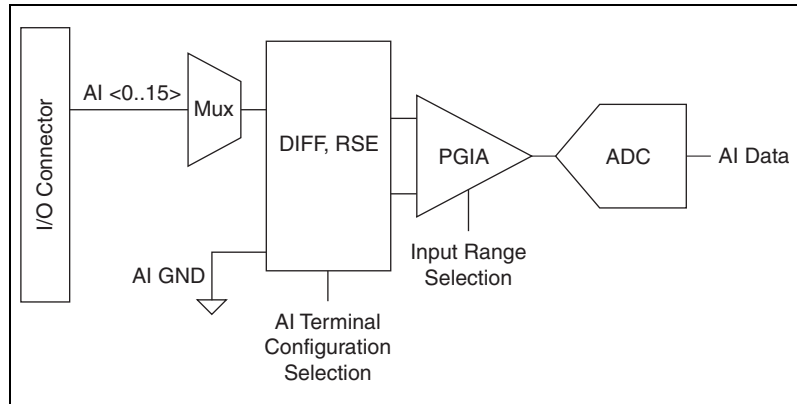


Figure 22. Single-Ended Analog Input on the NI sbRIO-9626/9636

Analog Input Range

An input range is a set of input voltages that an analog input channel can digitize with the specified accuracy. NI sbRIO devices with selectable input ranges have a programmable gain instrumentation amplifier (PGIA), which amplifies or attenuates the AI signal depending on the input range. You can program the input range for each AI channel independently on the NI sbRIO 9626/9636.

The ADC converts analog inputs into discrete digital values. For a 12-bit ADC there are 2^{12} (4,096) possible values, and for a 16-bit ADC there are 2^{16} (65,536) possible values. These values are spread evenly across the input range, and the voltage difference between values is proportional to the input range selected for the channel. The voltage difference between values is the *size of the least significant bit* (LSB size) for the channel. The following equation shows how to calculate the LSB size for a channel set to the –10 V to 10 V input range, with a 16-bit ADC.

$$\frac{10 \text{ V} - (-10 \text{ V})}{65,536} = 305 \text{ } \mu\text{V} \quad (1)$$

The NI sbRIO-9626/9636 uses a scaling method that requires some codes (typically about 5% of the codes) to lie outside the specified range. This method improves absolute accuracy, but it increases the LSB size by about 5% over the calculated value.

Choose an input range that matches the expected range of your input signal. A large input range accommodates large variations in signals but

results in a larger LSB and, therefore, lower resolution. A smaller input range improves the resolution, but large input signals may go out of range.

For more information about selecting ranges, refer to the *LabVIEW Help*.

Table 5 shows the input ranges and resulting LSB sizes for AI channels on each NI sbRIO device.

Table 5. NI sbRIO Device Input Range and Resolutions

Device	Input Range	Bit Resolution	LSB Size
NI sbRIO 9623/9633	0 V to 5 V	12-bit	1.22 mV
NI sbRIO 9626/9636	–10 V to 10 V	16-bit	320 μV*
	–5 V to 5 V		160 μV*
	–2 V to 2 V		64 μV*
	–1 V to 1 V		32 μV*
* Includes 5% overranging.			

Working Voltage Range

The PGIA on NI sbRIO devices operates normally by amplifying signals of interest while rejecting common-mode signals under the following three conditions:

- The common-mode voltage (V_{cm}), which is equivalent to subtracting AIGND from AI–, must be less than ± 10 V. V_{cm} is a constant for all range selections.
- The signal voltage (V_s), which is equivalent to subtracting AI+ from AI–, must be less than or equal to the range selection of the given channel. If V_s is greater than the range selected, the signal clips and information is lost.
- The total working voltage of the positive input, which is equivalent to ($V_{cm} + V_s$), or subtracting AIGND from AI+, must be less than the maximum working voltage specified for that range. Refer to the [NI sbRIO-9626/9636](#) section for the maximum working voltage for each range.

If any of these conditions are exceeded, the input voltage is clamped until the fault condition is removed.

Best Practices for Scanning Multiple Channels

NI sbRIO devices can scan multiple channels at high rates and digitize the signals accurately. If your application scans multiple channels, settling error can affect the accuracy of your measurements. Settling error is a difference between the input value and the value that the ADC digitizes, and is the result of switching between multiplexed input channels. National Instruments defines settling error as the difference between a single-channel measurement of a signal and a multiple-channel measurement of the same signal. Settling errors are directly proportional to channel-to-channel voltage step size and the time between acquisitions. NI sbRIO devices scan at a fixed rate equal to the maximum aggregate rate.

To ensure the lowest possible settling errors, design your application according to the following best practices:

1. **Use Low-Impedance Sources**—Ensure that the impedance of signal sources is less than 1 k Ω . High-impedance sources increase settling errors and decrease accuracy at fast scanning rates. You can reduce impedance by connecting a voltage-follower circuit between the signal source and the AI pin of the channel. For more information about reducing impedance, go to ni.com/info and entering the Info Code rdbbis.
2. **Use Short, High-Quality Cabling**—Using short, high-quality cables can minimize several effects that degrade accuracy, including crosstalk, transmission line effects, and noise. The capacitance of the cable can also increase the settling error. National Instruments recommends using individually shielded twisted-pair wires shorter than 2 m to connect AI signals to the device. Refer to the [Connecting Analog Input Signals](#) section for more information.
3. **Minimize Voltage Step between Adjacent Channels**—Settling error increases with the voltage step between channels. If you know the expected input ranges of your signals, you can group signals with similar expected ranges together on adjacent channels.



Note When you program your I/O node with a scan list, the NI sbRIO device scans channels in numerical order at a fixed rate. Calling a second I/O node adds an extra delay before the first channel but does not reduce settling error.

Differential Measurement Configurations

To attain more accurate measurements and less noise on NI sbRIO-9626/9636 devices, use a differential measurement configuration. A differential measurement configuration requires two inputs for each measurement, reducing the number of available channels from 16 to eight. Table 6 shows the signal pairs that are valid for differential connection configurations.

Table 6. Differential Analog Input Signals on the NI sbRIO-9626/9636

Channel	Signal +	Signal -
0	AI0	AI8
1	AI1	AI9
2	AI2	AI10
3	AI3	AI11
4	AI4	AI12
5	AI5	AI13
6	AI6	AI14
7	AI7	AI15

The following figure shows how to make a differential connection for a floating signal and for a ground-referenced signal.

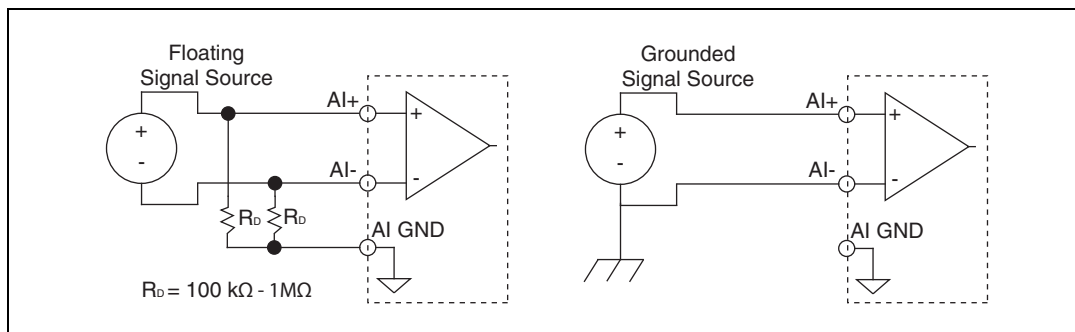
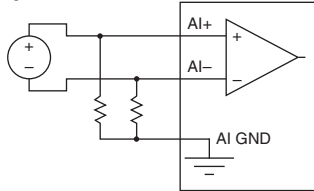
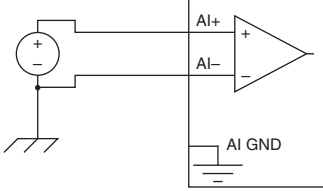
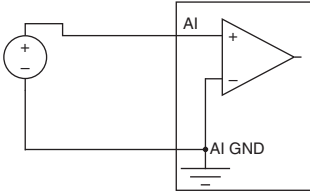
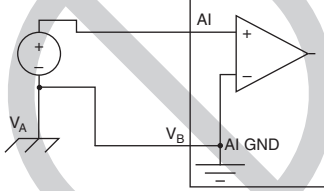


Figure 23. Differential Connections with Floating and Grounded Signal Sources

Connecting Analog Input Signals

Table 7 summarizes the recommended input configuration for both types of signal sources.

Table 7. NI sbRIO Analog Input Configuration

AI Ground-Reference Setting	Floating Signal Sources (Not Connected to Building Ground)	Ground-Referenced Signal Sources
	<p>Examples:</p> <ul style="list-style-type: none"> • Ungrounded thermocouples • Signal conditioning with isolated outputs • Battery devices 	<p>Example:</p> <ul style="list-style-type: none"> • Plug-in instruments with non-isolated outputs
Differential	<p>Signal Source</p> 	<p>Signal Source</p> 
Referenced Single-Ended (RSE)	<p>Signal Source</p> 	<p>NOT RECOMMENDED</p> <p>Signal Source</p>  <p>Ground-loop potential ($V_A - V_B$) are added to measured signal.</p>

Connecting Floating Signal Sources

What Are Floating Signal Sources?

A floating signal source is not connected to the building ground system, but has an isolated ground-reference point. Some examples of floating signal sources are outputs of transformers, thermocouples, battery-powered devices, optical isolators, and isolation amplifiers. An instrument or device that has an isolated output is a floating signal source.

When to Use Differential Connections with Floating Signal Sources

Use DIFF input connections for any channel that meets any of the following conditions:

- The input signal is low level (less than 1 V).
- The leads connecting the signal to the device are greater than 3 m (10 ft).
- The input signal requires a separate ground-reference point or return signal.
- The signal leads travel through noisy environments.
- Two analog input channels, AI+ and AI–, are available for the signal.

DIFF signal connections reduce noise pickup and increase common-mode noise rejection. DIFF signal connections also allow input signals to float within the common-mode limits of the PGIA.

Refer to the [*Using Differential Connections for Floating Signal Sources*](#) section for more information about differential connections.

When to Use Referenced Single-Ended (RSE) Connections with Floating Signal Sources

Only use RSE input connections if the input signal meets the following conditions:

- The input signal can share a common reference point, AI GND, with other signals that use RSE.
- The input signal is high-level (greater than 1 V).
- The leads connecting the signal to the device are less than 3 m (10 ft).

DIFF input connections are recommended for greater signal integrity for any input signal that does not meet the preceding conditions.

In the single-ended modes, more electrostatic and magnetic noise couples into the signal connections than in DIFF configurations. The coupling is the

result of differences in the signal path. Magnetic coupling is proportional to the area between the two signal conductors. Electrical coupling is a function of how much the electric field differs between the two conductors.

With this type of connection, the NI sbRIO device rejects both the common-mode noise in the signal and the ground potential difference between the signal source and the device ground.

Using Differential Connections for Floating Signal Sources

It is important to connect the negative lead of a floating source to AI GND (either directly or through a bias resistor). Otherwise, the source may float out of the maximum working voltage range of the PGIA device and the return erroneous data.

The easiest way to reference the source to AI GND is to connect the positive side of the signal to AI+ and connect the negative side of the signal to AI GND as well as to AI– without using resistors. This connection works well for DC-coupled sources with low source impedance (less than 100 Ω).

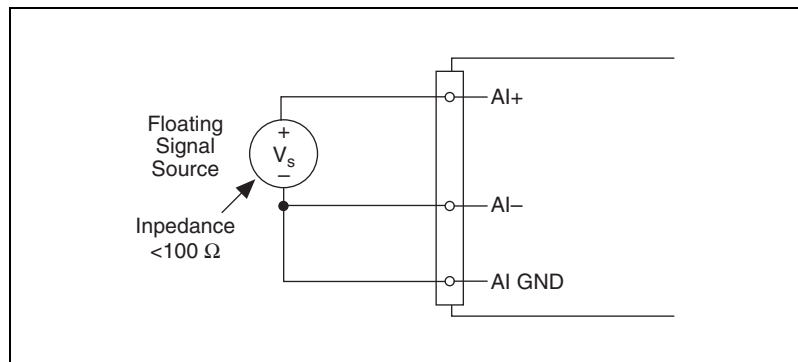


Figure 24. Differential Connections for Floating Signal Sources without Bias Resistors

However, for larger source impedances, this connection leaves the DIFF signal path significantly off balance. Noise that couples electrostatically onto the positive line does not couple onto the negative line because it is connected to ground. This noise appears as a differential mode signal instead of a common-mode signal, and thus appears in your data. In this case, instead of directly connecting the negative line to AI GND, connect the negative line to AI GND through a resistor that is about 100 times the equivalent source impedance. The resistor puts the signal path nearly in balance, so that about the same amount of noise couples onto both connections, yielding better rejection of electrostatically coupled noise. This configuration does not load down the source (other than the very high input impedance of the PGIA).

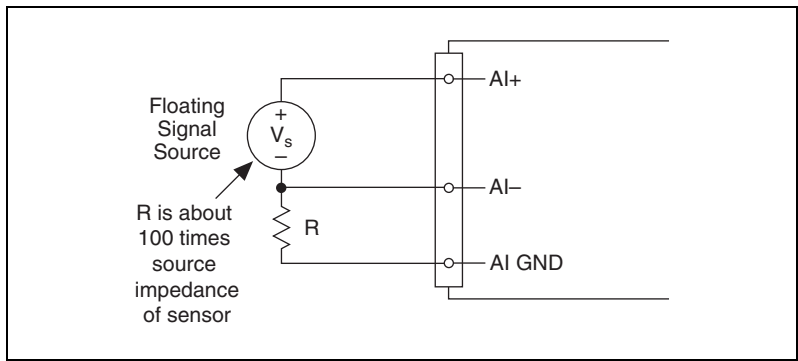


Figure 25. Differential Connections for Floating Signal Sources with Single Bias Resistor

You can fully balance the signal path by connecting another resistor of the same value between the positive input and $AI\ GND$, as shown in Figure 26. This fully balanced configuration offers slightly better noise rejection, but has the disadvantage of loading the source down with the series combination (sum) of the two resistors. If, for example, the source impedance is $2\ k\Omega$ and each of the two resistors is $100\ k\Omega$, the resistors load down the source with $200\ k\Omega$ and produce a -1% gain error.

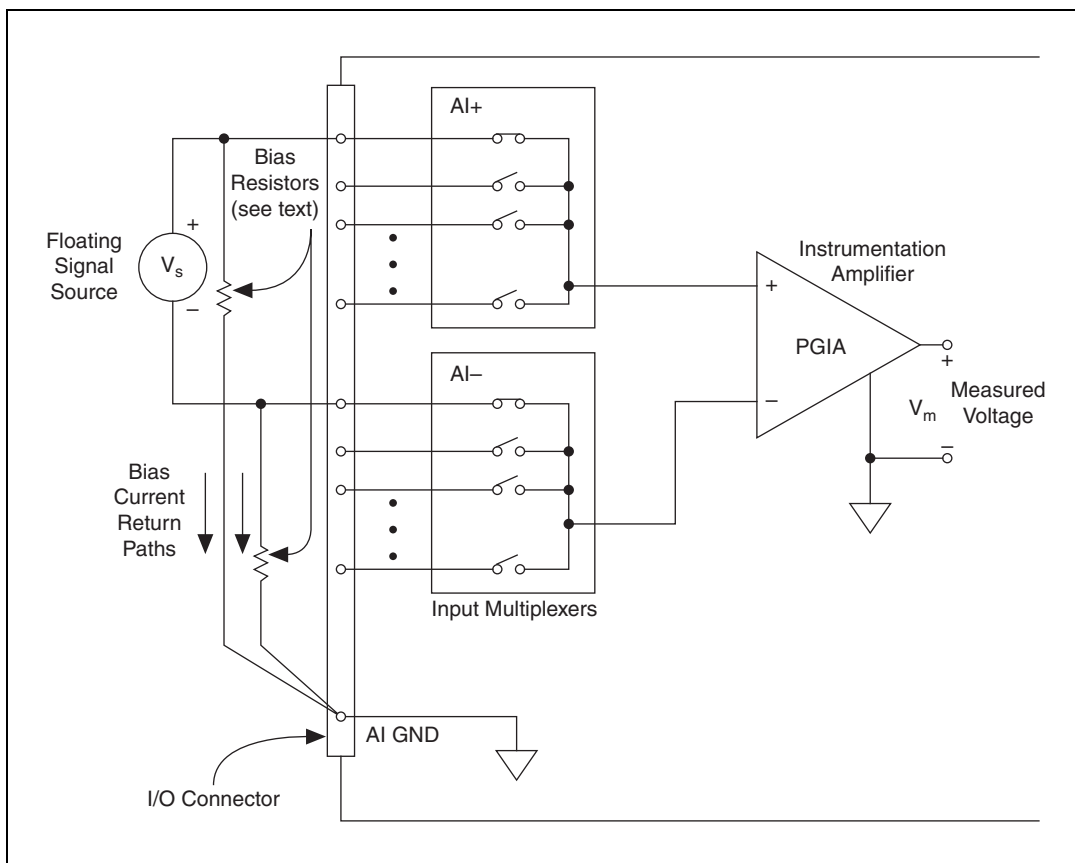


Figure 26. Differential Connections for Floating Signal Sources with Balanced Bias Resistors

Both inputs of the PGIA require a DC path to ground in order for the PGIA to work. If the source is AC coupled (capacitively coupled), the PGIA needs a resistor between the positive input and AI GND. If the source has low-impedance, choose a resistor that is large enough not to significantly load the source but small enough not to produce significant input offset voltage as a result of input bias current (typically 100 k Ω to 1 M Ω). In this case, connect the negative input directly to AI GND. If the source has high output impedance, balance the signal path as previously described using the same value resistor on both the positive and negative inputs; be aware that there is some gain error from loading down the source, as shown in Figure 27.

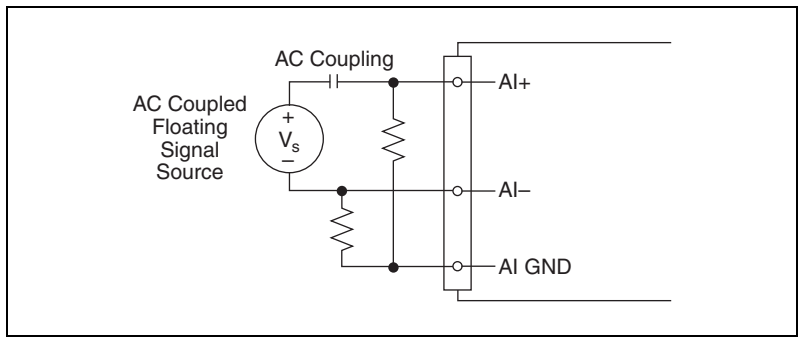


Figure 27. Differential Connections for AC Coupled Floating Sources with Balanced Bias Resistors

Integrated Analog Output

This section applies only to the following NI sbRIO devices:

- NI sbRIO-9623 • NI sbRIO-9633
- NI sbRIO-9626 • NI sbRIO-9636

The NI sbRIO-9623/9633 each have four 12-bit analog output (AO) channels capable of driving 0 V to 5 V. The NI sbRIO-9626-9636 each have four 16-bit AO channels capable of driving ± 10 V. All AO channels are ground-referenced. Connector J503 provides connections for analog inputs, outputs, and grounds. Refer to Figure 17 for a pinout of connector J503.

Figure 28 shows an AO channel on the NI sbRIO-9623/9633.

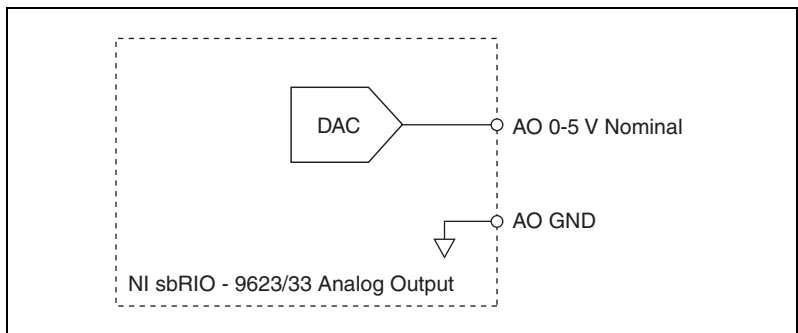


Figure 28. Analog Output Channel on NI sbRIO-9623/9633

Figure 29 shows an AO channel on the NI sbRIO-9626/9636.

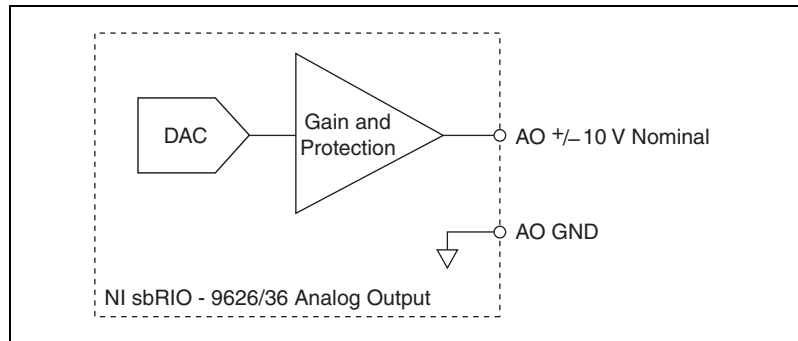


Figure 29. Analog Output Channel on NI sbRIO-9626/9636

Analog Output Startup and Initialization

The analog output on the NI sbRIO device does not get powered until the first time the FPGA is loaded after applying board power. The analog output is initialized (made active and set to 0 V) the first time the FPGA is loaded with a bitfile in which either AI or AO functionality of the board is used. The AO is re-initialized to 0 V every time the FPGA is loaded with a bitfile containing AI or AO functionality.

Powering the NI sbRIO Device

The NI sbRIO device requires an external power supply that meets the specifications in the [Power Requirements](#) section. The NI sbRIO device filters and regulates the supplied power and provides power for RIO Mezzanine Cards. Complete the following steps to connect a power supply to the device.



Caution Do not mate or unmate the power supply connectors while power is applied.

1. Ensure the power supply is off.
2. Connect the V lead of the power supply to position 1 of the power connector plug. Figure 30 shows the positions on the power connector.

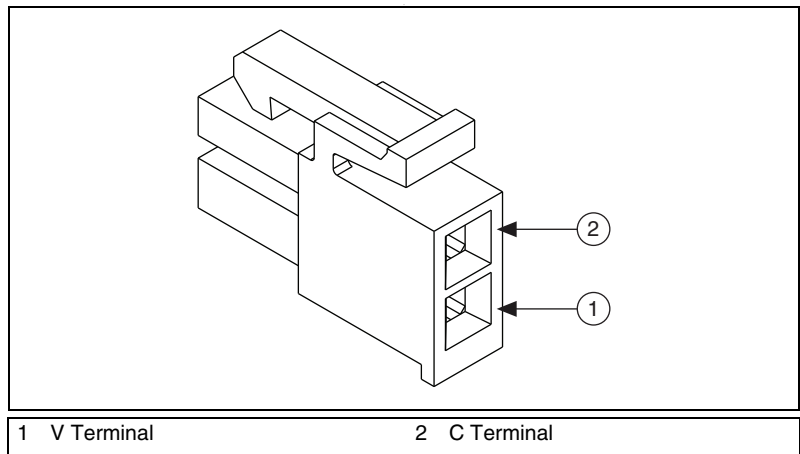


Figure 30. NI sbRIO Device Power Connector

3. Connect the C lead of the power supply to position 2 of the 2-position power connector plug.
4. Insert the power connector plug into the power connector receptacle of the NI sbRIO device until the connector latches into place.
5. Turn on the power supply.

Powering On the NI sbRIO Device

The NI sbRIO device runs a power-on self test (POST) when you apply power to the device. During the POST, the Power and Status LEDs turn on. When the Status LED turns off, the POST is complete. If the LEDs do not behave in this way when the system powers on, refer to the [Understanding LED Indications](#) section.

Device Startup Options

You can configure the following device startup options in NI Measurement & Automation Explorer (MAX):

- Safe Mode
- Console Out
- IP Reset
- No App
- No FPGA App

To turn these startup options on or off, select the controller under **Remote Systems** in the MAX configuration tree, then select the **Controller Settings** tab. Refer to the MAX Help for information about the startup options and how to configure the controller.

You can configure the device to launch an embedded stand-alone LabVIEW RT application each time it resets. Refer to the *Running a Stand-Alone Real-Time Application (RT Module)* topic of the *LabVIEW Help* for more information.

Device Reset Options

You can configure the device to launch a LabVIEW FPGA application each time it is reset. Table 8 lists the reset options available on the NI sbRIO device. These options determine how the FPGA behaves when the device is reset in various conditions. Use the RIO Device Setup utility to select reset options. Access the RIO Device Setup utility by selecting **Start» All Programs»National Instruments»NI-RIO»RIO Device Setup**.

Table 8. NI sbRIO Reset Options

Reset Option	Behavior
Do not autoload VI	Does not load the FPGA bit stream from flash memory.
Autoload VI on device powerup	Loads the FPGA bit stream from flash memory to the FPGA when the device powers on.
Autoload VI on device reboot	Loads the FPGA bit stream from flash memory to the FPGA when you reboot the device either with or without cycling power.



Note If you want a VI to run when loaded to the FPGA, complete the following steps.

1. Right-click the FPGA Target item in the **Project Explorer** window in LabVIEW.
2. Select **Properties**.
3. In the **General** category of the **FPGA Target Properties** dialog box, place a check in the **Run when loaded to FPGA** checkbox.
4. Compile the FPGA VI.

Connecting the NI sbRIO Device to a Network

Connect the device to an Ethernet network using the RJ-45 Ethernet port on the controller front panel. Use a standard Category 5 (CAT-5) or better shielded, twisted-pair Ethernet cable to connect the device to an Ethernet hub, or use an Ethernet crossover cable to connect the device directly to a computer.



Caution To prevent data loss and to maintain the integrity of your Ethernet installation, do *not* use a cable longer than 100 m.

The first time you power up the device, it attempts to initiate a DHCP network connection. If the device is unable to initiate a DHCP connection, it connects to the network with a link-local IP address with the form `169.254.x.x`. After powerup, you must install software on the device and configure the network settings in Measurement & Automation Explorer (MAX).



Note Installing software may change the network behavior of the device. For information about network behavior by installed software version, go to ni.com/info and enter the Info Code [ipconfigrio](#).

Connecting Serial Devices

NI sbRIO devices populated with RS-232 and RS-485 serial ports can connect to devices such as displays or input devices. Use the Serial VIs to read from and write to the serial port from a LabVIEW RT application. For more information about using the Serial VIs, refer to the *Serial VIs and Functions* topic of the *LabVIEW Help*.

Connecting CAN Networks

NI sbRIO devices populated with one IDC header provide connections to a CAN bus. CAN-enabled NI sbRIO devices have pins for CAN_H and CAN_L, which can connect to the CAN bus signals. The CAN port uses an NXP PCA82C251T high-speed CAN transceiver that is fully compatible with the ISO 11898 standard and supports baud rates up to 1 Mbps.

The port has two common pins (GND) that serve as the reference ground for CAN_H and CAN_L. You can connect the CAN bus reference ground (sometimes referred to as CAN_V-) to one or both COM pins. The port also has an optional shield pin (SHLD) that can connect to a shielded CAN cable. Connecting SHLD may improve signal integrity and EMC performance.

CAN Bus Topology and Termination

A CAN bus consists of two or more CAN nodes cabled together. The CAN_H and CAN_L pins of each node are connected to the main CAN bus cable through a short connection called a *stub*. The pair of signal wires, CAN_H and CAN_L, constitutes a transmission line. If the transmission line is not terminated, signal changes on the bus cause reflections that can cause communication errors. The CAN bus is bidirectional, and both ends of the cable must be terminated. This requirement does not mean that every node on the bus should have a termination resistor; only the two nodes at the far end of the cable should have termination resistors.

Figure 31 shows a simplified diagram of a CAN bus with multiple CAN nodes and proper termination resistor (R_t) locations.

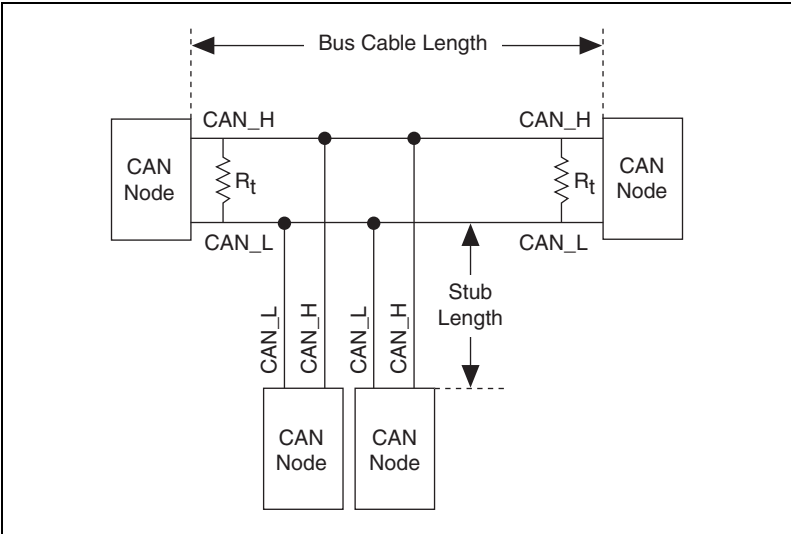


Figure 31. CAN Bus Topology and Termination Resistor Locations

Cable Specifications

Cables should meet the physical medium requirements specified in ISO 11898, shown in Table 9. Belden cable (3084A) meets all these requirements and is suitable for most applications.

Table 9. ISO 11898 Specifications for Characteristics of a CAN_H and CAN_L Pair of Wires

Characteristic	Value
Impedance	95 Ω minimum, 120 Ω nominal, 140 Ω maximum
Length-related resistance	70 m Ω /m nominal
Specific line delay	5 ns/m nominal

Termination Resistors

The termination resistors (R_t) should match the nominal impedance of the CAN cable and therefore comply with the values in Table 10.

Table 10. Termination Resistor Specification

Characteristic	Value	Condition
Termination resistor, R_t	100 Ω min, 120 Ω nominal, 130 Ω max	Minimum power dissipation: 220 mW

Cable Lengths

The cabling characteristics and desired bit transmission rates affect the allowable cable length. You can find detailed cable length recommendations in the ISO 11898, CiA DS 102, and DeviceNet specifications.

ISO 11898 specifies 40 m total cable length with a maximum stub length of 0.3 m for a bit rate of 1 Mb/s. The ISO 11898 specification allows for significantly longer cable lengths at lower bit rates, but each node should be analyzed for signal integrity problems.

Number of CAN Nodes

The maximum number of nodes depends on the electrical characteristics of the nodes on the network. If all nodes meet the ISO 11898 requirements, you can connect at least 30 nodes to the bus. You can connect higher numbers of nodes if the electrical characteristics of the node do not degrade signal quality below ISO 11898 signal level specifications.

USB Port

This section applies only to the following NI sbRIO devices:

- NI sbRIO-9606 • NI sbRIO-9633
- NI sbRIO-9626 • NI sbRIO-9636

The NI sbRIO devices populated with USB ports support common USB mass-storage devices such as USB Flash drives and USB-to-IDE adapters formatted with FAT16 and FAT32 file systems. LabVIEW usually maps USB devices to the U:, V:, W:, or X: drive, starting with the U: drive if it is available. Refer to Figure 32 and Table 11 for USB pin locations and signal descriptions.

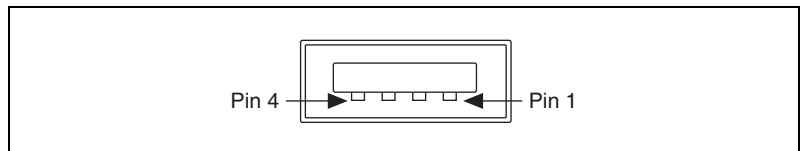


Figure 32. USB Port Pin Locations

Table 11. USB Port Signal Descriptions

Pin	Signal Name	Signal Description
1	VCC	Cable power (+5 V)
2	D–	USB data–
3	D+	USB data+
4	GND	Ground

Using the System Clock to Provide Data Timestamps

At startup, the system clock of the NI sbRIO-9605/9606 resets to January 1, 1970, 12:00 a.m. (midnight), unless VBAT is implemented on the RMC. For information about synchronizing the system clock with an SNTP time server on the network at startup, go to ni.com/info and enter the Info Code `criosntp`.

Using the Reset Button

Pressing the Reset button reboots the processor. The FPGA continues to run unless you select the **Autoload VI on device reboot** boot option. Refer to the [Device Reset Options](#) section for more information.



Note To force the device into safe mode, hold the reset button down for 5 seconds, then release. The device will be in safe mode with output from the COM1 serial port enabled.

Understanding LED Indications

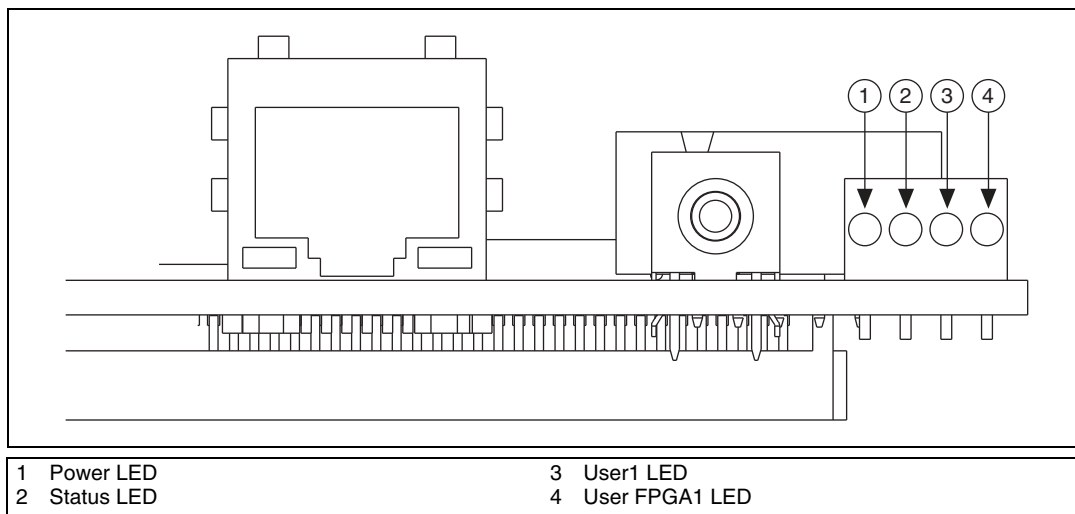


Figure 33. NI sbRIO Device LEDs

Power LED

The Power LED is lit while the NI sbRIO device is powered on. This LED indicates that the power supply connected to the device is adequate.

Status LED

The STATUS LED is off during normal operation. The NI sbRIO device runs a power-on self test (POST) when you apply power to the device. During the POST, the Power and Status LEDs turn on. When the Status LED turns off, the POST is complete. The NI sbRIO Device indicates specific error conditions by flashing the Status LED a certain number of times every few seconds, as shown in Table 12.

Table 12. Status LED Indications

Number of Flashes Every Few Seconds	Indication
2	The device has detected an error in its software. This usually occurs when an attempt to upgrade the software is interrupted. Reinstall software on the device. Refer to the <i>Measurement & Automation Explorer Help</i> for information about installing software on the device.
3	The device is in safe mode. Refer to the <i>Measurement & Automation Explorer Help</i> for information about safe mode.
4	The software has crashed twice without rebooting or cycling power between crashes. This usually occurs when the device runs out of memory. Review your RT VI and check the memory usage. Modify the VI as necessary to solve the memory usage issue.
Continuously flashing or solid	The device has detected an unrecoverable error. Contact National Instruments.

User1 LED

You can define the User1 LED to meet the needs of your application. To define the LED, use the RT LEDs VI in LabVIEW. For more information about the RT LEDs VI, refer to the *LabVIEW Help* section at **Real-Time Module»Real-Time VIs»RT Utilities VIs»RT LEDs**.

User FPGA1 LED

You can use the User FPGA1 LED to help debug your application or easily retrieve application status. Use the LabVIEW FPGA Module and NI-RIO software to define the User FPGA1 LED to meet the needs of your application. Refer to the *LabVIEW Help* section at **Real-Time Module»Real-Time VIs»RT Utilities VIs»RT LEDs** for information about programming this LED.

Troubleshooting Network Communication

If the NI sbRIO device cannot communicate with the network, you can perform the following troubleshooting steps.

1. Hold the Reset button down for 5 seconds, then release it. The Status LED turns on, then starts blinking three times every few seconds. The device is now in Safe Mode with output from the COM1 serial port enabled. You can use a serial port terminal to read the IP address of the controller. If you want the controller to attempt a new DHCP connection, proceed to step 2.
2. Hold the Reset button down for 5 s, then release it. The Status LED repeats the same behavior. The NI sbRIO device attempts to establish a new DHCP connection. If it fails, it assigns itself a link-local IP address. If the DHCP connection is successful and appropriate for your application, skip to step 4.
3. Configure the IP and other network settings in MAX.
4. Press and release the Reset button to reboot the device.



Note If the device is restored to the factory network settings, the LabVIEW run-time engine does not load. You must reconfigure the network settings and reboot the device for the LabVIEW run-time engine to load.

Specifications

Unless otherwise noted, the following specifications are typical for the range -40 to 85 °C for the NI sbRIO device.

Processor Speed

NI sbRIO-9605/9606/9623/9626
9633/9636..... 400 MHz

Memory

NI sbRIO-9605/9623/9633
Nonvolatile memory 256 MB
System memory 128 MB

NI sbRIO-9606/9626/9636
Nonvolatile memory 512 MB
System memory 256 MB



Note For information about the life span of the nonvolatile memory and about best practices for using nonvolatile memory, go to ni.com/info and enter the Info Code SSDBP.

FPGA

NI sbRIO-9605/9623/9633

FPGA type	Xilinx Spartan-6 LX25
Number of flip-flops.....	30,064
Number of 6-input LUTs.....	15,032
Number of DSP48s.....	38
Available block RAM.....	936 kbits
Number of DMA channels	5

NI sbRIO-9606/9626/9636

FPGA type	Xilinx Spartan-6 LX45
Number of flip-flops.....	54,576
Number of 6-input LUTs.....	27,288
Number of DSP48s.....	58
Available block RAM.....	2,088 kbits
Number of DMA channels	5

Network

Network interface	10BaseT and 100BaseTX Ethernet
Compatibility	IEEE 802.3
Communication rates	10 Mbps, 100 Mbps, auto-negotiated
Maximum cabling distance.....	100 m/segment

RS-232 DTE Serial Port

Baud rate support.....	Arbitrary
Maximum baud rate.....	230,400 bps
Data bits	5, 6, 7, 8
Stop bits	1, 2

Parity Odd, Even, Mark, Space, None

Flow control RTS/CTS, XON/XOFF,
DTR/DSR, None

RS-485 Serial Port

Maximum baud rate 460,800 bps

Data bits 5, 6, 7, 8

Stop bits..... 1, 1.5, 2

Parity Odd, Even, Mark, Space, None

Flow control XON/XOFF

Wire Mode 4-wire, 2-wire, 2-wire auto

Isolation Voltage,
port to earth ground..... None

Embedded CAN

Transceiver NXP PCA82C251T

Maximum baud rate 1 Mbps

Minimum baud rate 10 kbps

USB Port

Compatibility USB 2.0 High Speed

Maximum data rate 480 Mb/s

Maximum current..... 500 mA

Internal RTC

Accuracy 200 ppm; 35 ppm @ 25 °C

VBAT input range..... 3.0 to 3.6 V (Nominal);
3.7 V Max

SD Port

SD card support..... SD and SDHC standards

3.3 V Digital I/O on RIO Mezzanine Card Connector

Number of DIO channels.....	96
Max tested current per channel.....	±3 mA
Max total current, all lines	288 mA



Note The performance of the RMC DIO lines is bounded by the FPGA, signal integrity, the application timing requirements, and the RMC design. A general SPI application will typically be able to meet these requirements and achieve frequencies of up to 10 MHz. For more information on using DIO to connect to RMCs, go to ni.com/info and enter the Info Code RMC_{DIO}.

Input logic levels	
Input low voltage, V_{IL}	0 V min; 0.8 V max
Input high voltage, V_{IH}	2.0 V min; 3.465 V max
Output logic levels	
Output high voltage, V_{OH} sourcing 3 mA	2.4 V min; 3.465 V max
Output low voltage, V_{OL} sinking 3 mA	0.0 V min; 0.4 V max

3.3 V Digital I/O on 50-Pin IDC Connector

Number of DIO channels	
NI sbRIO-9623/9626	4
NI sbRIO-9633/9636	28
Max tested current per channel.....	±3 mA
Max total current, all lines	
NI sbRIO-9623/9626	12 mA
NI sbRIO-9633/9636	84 mA
Input logic levels	
Input low voltage, V_{IL}	0 V min; 0.8 V max
Input high voltage, V_{IH}	2.0 V min; 5.25 V max
Output logic levels	
Output high voltage, V_{OH} sourcing 3 mA	2.4 V min; 3.465 V max
Output low voltage, V_{OL} sinking 3 mA	0.0 V min; 0.4 V max

Analog Input Characteristics

NI sbRIO-9623/9633

Number of channels 16 single-ended

ADC Resolution 12 bits

Maximum aggregate sampling rate 500 kS/s

Input range 0–5 V nominal

Input impedance

Powered on, idle 250 M Ω

Acquiring 500 kS/s 325 k Ω

Powered off/overload 1 k Ω

Overvoltage protection None

AI accuracy

Measurement Conditions	Percent of Reading (Gain Error)	Percent of Range* (Offset Error)
Typical (25 °C, ± 5 °C)	0.11%	0.03%
Max (–40 to 85 °C)	0.55%	0.16%
* Range = 5 V		



Note For information about measuring the local ambient temperature, refer to the [Environmental](#) section.

INL $\pm 0.024\%$ of range

DNL $\pm 0.024\%$ of range

Input bandwidth (–3 dB) 6 MHz

NI sbRIO-9626/9636

Number of channels 16 single-ended or 8 differential

ADC Resolution 16 bits

Maximum aggregate sampling rate 200 kS/s

Input range ± 10 V, ± 5 V, ± 2 V, ± 1 V

Maximum working voltage (signal + common mode)

Range	Working voltage
10 V	±11 V
5 V	± 10.5 V
2 V	± 9 V
1 V	± 8.5 V

Input impedance

Powered on> 1 G Ω in parallel with 100 pF

Powered off/overload2.3 k Ω min

Overvoltage protection

Powered on ±25 V, for up to 2 AI pins

Powered off ±15V

AI accuracy

Measurement Conditions	Range	Percent of Reading (Gain Error)	Percent of Range (Offset Error)
Typical (25 °C, ±5 °C)	1 V	0.042%	0.007%
	2 V		0.007%
	5 V		0.007%
	10 V		0.008%
Max (–40 to 85 °C)	1 V	0.380%	0.179%
	2 V	0.360%	0.138%
	5 V	0.348%	0.113%
	10 V	0.344%	0.105%

Gain drift.....12 ppm of reading/°C

Offset drift4 ppm of range/°C

AI Noise

Range	Working voltage
10 V	200 μ V _{RMS}
5 V	105 μ V _{RMS}
2 V	45 μ V _{RMS}
1 V	30 μ V _{RMS}

INL..... ±64 ppm of range, max

DNLNo missing codes guaranteed

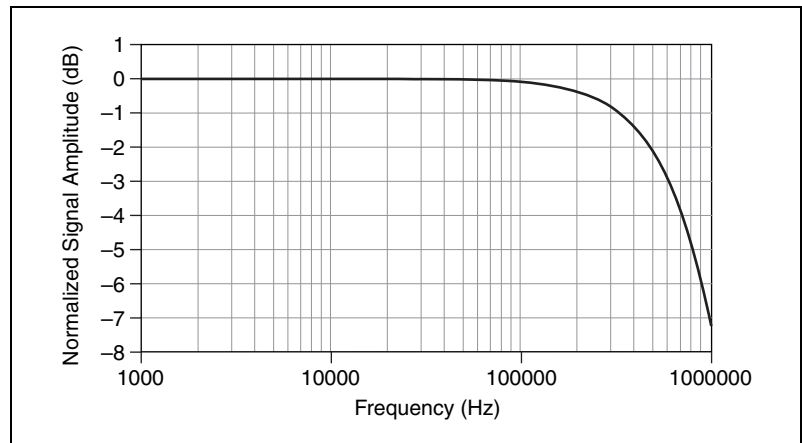
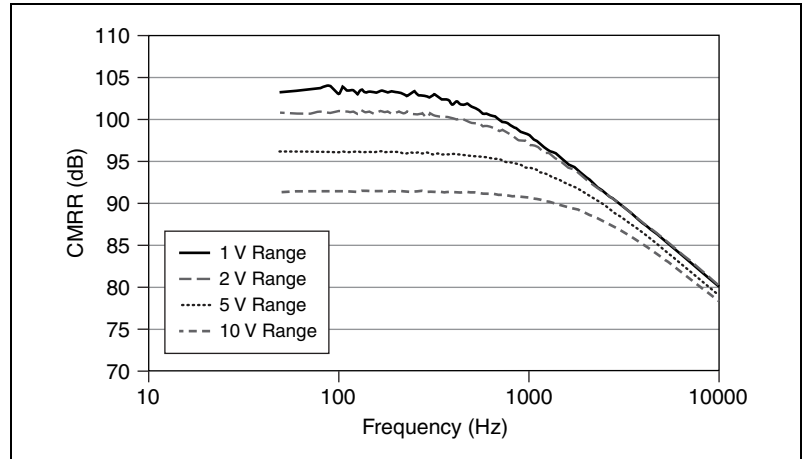
CMRR, DC to 60 Hz..... -80 dB

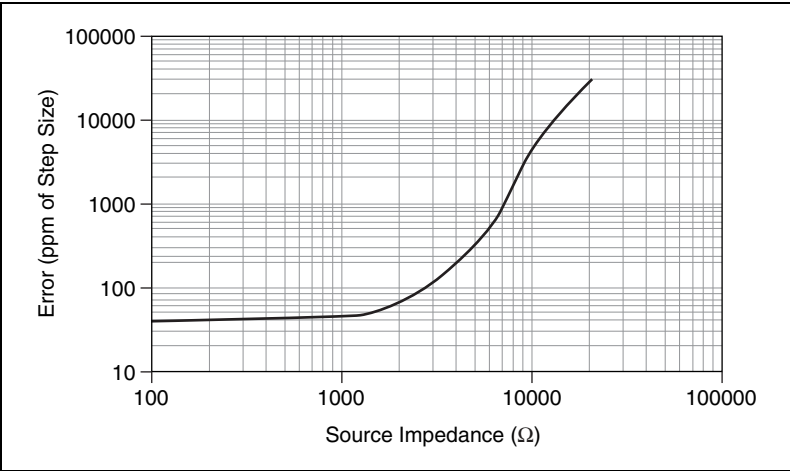
Input bandwidth (-3 dB)..... 600 kHz, typical

Settling error (multichannel scanning)... ± 60 ppm step size, typical

Crosstalk (10 kHz) -70 dB

Typical performance graphs





Analog Output Characteristics

NI sbRIO-9623/9633

Number of channels.....	4
DAC resolution.....	12 bits
Max update rate ¹	336 kS/s
Range	0–5 V
Output impedance	13 Ω typical, 27 Ω max
Current drive.....	±1 mA / channel max.
Protection.....	Short-circuit to ground
Power-on state ²	0 V

¹ This is the maximum update rate when running one AO channel in a loop with the FPGA top-level clock set to 40 MHz.

² When power is applied, the analog outputs remain high impedance until the FPGA loads for the first time. When the FPGA loads, the analog outputs become low-impedance sources driving 0 V. During the transition from high to low impedance, the outputs typically glitch for about 60 μs. The magnitude of the glitch is inversely proportional to the load capacitance. With a 300 pF load, the peak is typically 0.25 V.

AO accuracy

Measurement Conditions	Percent of Reading (Gain Error)	Percent of Range* (Offset Error)
Typical (25 °C, ± 5 °C)	0.12%	0.02%
Max (–40 to 85 °C)	0.80%	0.12%
* Range is 5 V.		



Note For information about measuring the local ambient temperature, refer to the [Environmental](#) section.

INL $\pm 0.018\%$ of range, max

Capacitive drive 1 nF, typical

Slew rate 0.75 V / μ sec, typical

NI sbRIO-9626/9636

Number of channels 4

DAC resolution 16 bits

Max update rate¹ 336 kS/s

Range ± 10 V

Overrange operating voltage

Minimum 10.3 V

Typical 10.6 V

Max 10.9 V

Output impedance 0.4 Ω typical

Current drive ± 3 mA / channel max.

Protection Short-circuit to ground

Power-on state² 0 V

¹ This is the maximum update rate when running one AO channel in a loop with the FPGA top-level clock set to 40 MHz.

² When the analog output initializes, a glitch occurs for about 20 μ s, peaking at 1.3 V, typical.

AO accuracy

Measurement Conditions	Percent of Reading (Gain Error)	Percent of Range* (Offset Error)
Typical (25 °C, ±5 °C)	0.09%	0.02%
Max (–40 to 85 °C)	0.50%	0.20%
* Range is 10 V.		

Gain drift.....	23 ppm of reading/°C
Offset drift	5.4 ppm of range/°C
INL.....	±194 ppm of range, max
DNL	±16 ppm of range, max
Capacitive drive.....	1.5 nF, typical
Slew rate	3.7 V / μsec, typical
Settling time (100 pF load to 320 μV)	
FS step	50 μs
2 V step.....	12 μs
0.2 V step.....	9 μs

Power Requirements

The NI sbRIO device requires a power supply connected to the power connector. Refer to Figure 2 for the location of the power connector. Refer to the [Powering the NI sbRIO Device](#) section for information about connecting the power supply.



Caution Exceeding the power limits may cause unpredictable behavior by the device.

Recommended power supply.....	55 W, 30 VDC max
Power supply voltage range.....	9–30 VDC ¹

¹ The NI sbRIO device is 1–2% more efficient with a 9 V power supply than with a 30 V power supply.

The total power required by the NI sbRIO device from its power supply depends heavily on how it is being used, and can be approximated by the following calculations:

$$\text{Total power requirement} = P_{int} + P_{DIO} + P_{5V} + P_{USB}$$

where P_{int} is the power consumption by the NI sbRIO device internal operation, including integrated I/O functions

P_{DIO} is the power consumption by the 3.3 V DIO lines across the RMC, MIO, or DIO connectors

P_{5V} is the power consumption by the 5 V voltage output across the RMC or MIO connectors

$P_{3.3V}$ is the power consumption by the 3.3 V voltage output across the RMC Connector

P_{USB} is the power consumption of a device plugged into the USB port

P_{SD} is the power consumption of an SD card plugged into the SD slot

P_{AO} is the power consumption of the Analog output across the MIO connector

When calculating each component of the maximum power consumption the following efficiency factors must be used:

$$\eta_{3.3\text{ V}}, \eta_{DIO} \text{ and } \eta_{SD} = 80\%$$

$$\eta_{5\text{ V}} \text{ and } \eta_{USB} = 90\%$$

$$\eta_{AO} = 50\%$$

P_{AO} is the power consumption of the Analog output across the MIO connector



Note You must add 10% to the calculated or measured total power requirement to account for transient and startup conditions.

Maximum P_{int} Refer to Table 13.

Maximum P_{DIO} Total DIO current \times 3.3 V / 0.8

Maximum P_{5V} Total 5 V current \times 5 V / 0.9

Maximum $P_{3.3V}$ Total 3.3 V current \times 3.3 V / 0.8

Maximum P_{USB} Total USB current \times 5 V / 0.9

Maximum P_{SD} ¹ Total SD current \times 3.3 V / 0.8

Maximum P_{AO}

NI sbRIO-9623/9633Total AO current $\times 5 \text{ V} / 0.5$

NI sbRIO-9626/9636Total AO current $\times 15 \text{ V} / 0.5$

Table 13. NI sbRIO Device Maximum Power Levels

Model	P_{int}	P_{DIO}	P_{5V}	$P_{3.3V}$	P_{USB}	P_{SD}	P_{AO}		
NI sbRIO-9605	5.66 W	1.79 W	8.33 W	1.36 W	N/A	N/A	N/A		
NI sbRIO-9606	8.10 W				2.78 W				
NI sbRIO-9623	7.50 W				N/A			0.04 W	
NI sbRIO-9626	11.86 W			N/A	2.78 W	0.83 W	0.3 W		
NI sbRIO-9633	9.04 W	0.41 W	0.04 W						
NI sbRIO-9636	11.86 W		0.3 W						

Example power requirement calculations:

For an NI sbRIO-9606 with an RMC board drawing 1 A of current from the 5 V output, 100 mA of current from the 3.3 V output, 30 mA total current through the 3.3 V DIO pins, and a USB device pulling 200 mA, calculate the total power requirement as follows:

$$P_{int} = 8.10 \text{ W}$$

$$P_{3.3V} = 0.41 \text{ W}$$

$$P_{DIO} = 0.12 \text{ W}$$

$$P_{5V} = 5.56 \text{ W}$$

$$P_{USB} = 1.11 \text{ W}$$

$$\text{Adding 10\% for transient conditions, } 15.55 \text{ W} \times 1.1 = 17.11 \text{ W}$$

$$\text{Total power requirement} = 17.11 \text{ W}$$



Note These calculations are intended to approximate the maximum power requirements for an NI sbRIO device system. For a more accurate estimate of a specific application's power consumption it is recommended to directly measure a board running the application in an environment representative of the intended use case.

¹ The SD specification allows 200 mA maximum current draw for an SD card. If your SD card does not specify maximum current draw, assume 200 mA.

NI sbRIO-9605

Power consumption while
sourcing RMC 19.1 W Max

NI sbRIO-9606

Power consumption while
sourcing RMC 25.4 W Max

NI sbRIO-9623

Power consumption while
sourcing RMC 21.7 W Max

NI sbRIO-9626

Power consumption while
sourcing RMC 29.9 W Max

NI sbRIO-9633

Power consumption..... 21.9 W Max

NI sbRIO-9636

Power consumption..... 24.7 W Max

Environmental

The NI sbRIO device is intended for indoor use only.

Local ambient temperature near device
(IEC 60068-2-1, IEC 60068-2-2)

NI sbRIO-960x –40 to 85 °C

NI sbRIO-962x –40 to 85 °C

NI sbRIO-963x –40 to 85 °C



Note Measure the local ambient temperature by placing thermocouples on both sides of the PCB, 0.2 in. (5 mm) from the board surface. Avoid placing thermocouples next to hot components such as the FPGA, processor, or near board edges, which can cause inaccurate temperature measurements. In addition to the local ambient temperature, the case temperature of the components should not exceed the recommended maximum case temperature.

Component Maximum Case Temperature

Table 14. Component Maximum Case Temperature

Component*	Manufacturer	Max Case Temp.
FPGA	Xilinx	93 °C
Processor	Freescall	107 °C
DDR memory	Micron	97 °C
NAND flash	Micron	90 °C
* Refer to Figure 2 for component locations		



Note Some systems may require a heat sink or air flow to remain within the maximum allowed temperature ranges. A heat spreader is available from National Instruments that you can mount on the NI sbRIO device. The heat spreader is NI 9695, part number 153901-01.



Note For information about and examples of environmental and design factors that can affect the thermal performance of NI sbRIO systems, so to ni.com/info and enter the Info Code `sbriocooling`.

Storage temperature

(IEC 60068-2-1, IEC 60068-2-2)–40 to 85 °C

Operating humidity

(IEC 60068-2-56)10 to 90% RH, noncondensing

Storage humidity

(IEC 60068-2-56)5 to 95% RH, noncondensing

Maximum altitude.....5,000 m

Pollution Degree (IEC 60664).....2

Physical Characteristics

Weight

NI sbRIO-960585 g (2.998 oz)

NI sbRIO-960689 g (3.139 oz)

NI sbRIO-9623123 g (4.24 oz)

NI sbRIO-9626133 g (4.69 oz)

NI sbRIO-9633131 g (4.62 oz)

NI sbRIO-9636132 g (4.66 oz)

Safety Voltages

Connect only voltages that are within this limit.

V terminal to C terminal 30 VDC max,
Measurement Category I

Measurement Category I is for measurements performed on circuits not directly connected to the electrical distribution system referred to as MAINS voltage. MAINS is a hazardous live electrical supply system that powers equipment. This category is for measurements of voltages from specially protected secondary circuits. Such voltage measurements include signal levels, special equipment, limited-energy parts of equipment, circuits powered by regulated low-voltage sources, and electronics.



Caution Do not connect the system to signals or use for measurements within Measurement Categories II, III, or IV.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *NI and the Environment* Web page at ni.com/environment. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)



EU Customers At the end of the product life cycle, all products *must* be sent to a WEEE recycling center. For more information about WEEE recycling centers, National Instruments WEEE initiatives, and compliance with WEEE Directive 2002/96/EC on Waste and Electronic Equipment, visit ni.com/environment/weee.

电子信息产品污染控制管理办法（中国 RoHS）



中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令 (RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 ni.com/environment/rohs_china。(For information about China RoHS compliance, go to ni.com/environment/rohs_china.)

Where to Go for Support

The National Instruments Web site is your complete resource for technical support. At ni.com/support you have access to everything from troubleshooting and application development self-help resources to email and phone assistance from NI Application Engineers.

National Instruments corporate headquarters is located at 11500 North Mopac Expressway, Austin, Texas, 78759-3504. National Instruments also has offices located around the world to help address your support needs. For telephone support in the United States, create your service request at ni.com/support and follow the calling instructions or dial 512 795 8248. For telephone support outside the United States, visit the Worldwide Offices section of ni.com/niglobal to access the branch office Web sites, which provide up-to-date contact information, support phone numbers, email addresses, and current events.

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