DSD Final Project Scores (RISC-V)

(1) Baseline Area: (um2) 截圖:

```
Library(s) Used:

    typical (File: /home/raid7_2/course/cvsd/CBDK_IC_Contest/CIC/SynopsysDC/db/typical.db)

Number of ports:                         1525
Number of nets:                         22109
Number of cells:                        21129
Number of combinational cells:          16892
Number of sequential cells:              4234
Number of macros/black boxes:               0
Number of buf/inv:                       3829
Number of references:                     144

Combinational area:             165221.519847
Buf/Inv area:                    26223.132713
Noncombinational area:          114187.491386
Macro/Black Box area:                0.000000
Net Interconnect area:         2487626.109314

Total cell area:                279409.011233
Total area:                    2767035.120547
1
```

(2) Total Simulation Time of given hasHazard testbench: (ns) 截圖:

```
-------------------------- Simulation FINISH !!--------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 29446250 PS + 0
```

(3) Area*Total Simulation Time: (um2 * ns):

8.22755E+12

(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)

2.5

2. BrPred

(1) Total execution cycles of given I_mem_BrPred: 截圖:

```
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 601500 PS + 0
./Final_tb.v:158              #(`CYCLE) $finish;
ncsim> exit
[b05027@cad29 BrPred]$
```

(2) Total execution cycles of given I_mem_hasHazard: 截圖:

```
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 517500 PS + 0
./Final_tb.v:158              #(`CYCLE) $finish;
ncsim> exit
[b05027@cad29 BrPred]$
```

(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): (um2)

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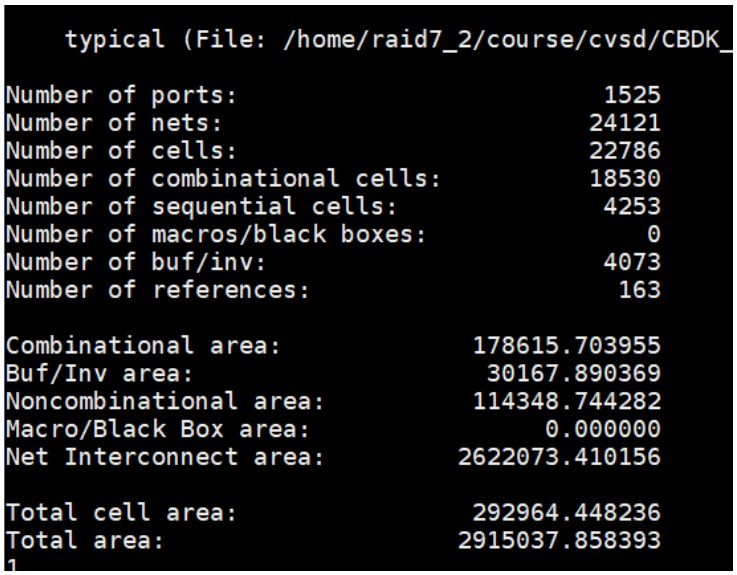
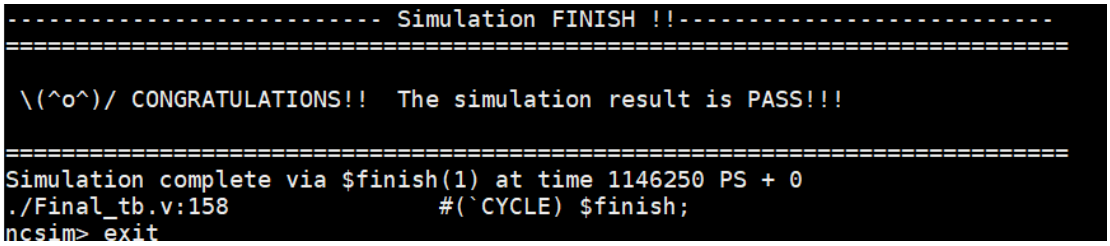
3. Compressed instructions

(1) Area (Total area of compressed design minus baseline design, two design clock cycle need to be same): (um2) 截圖:



= 13558

(2) Total Simulation Time of given I_mem_compression: (ns) 截圖:



(3) Area*Total Simulation Time: (um2 * ns)

3.3581E+11

(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)

2.5