Final Exam

Please complete each problem. Show all of your work, even if you cannot obtain the correct answer. You may use only two sheets of letter sized paper for assistance. (80 points total)

1. (4 pt) Perform the following number system conversions.

   (a) $00101011_2 = ?_{16}$
   (b) $00010011_2 = ?_8$
   (c) $163_{16} = ?_8$
   (d) $\text{AFDB} = ?_2$

2. (2 pt) Find the eight bit two's complement representation of each of the following numbers.

   (a) -10
   (b) -36

3. (3 pt) Perform the following binary arithmetic using the four bit two's complement representation, showing all carries. For each case, determine if overflow occurs. If it does, state why it occurs.

   $5 + -1$

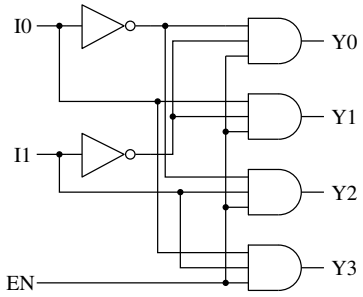
4. (4 pt) Write the function table and draw the circuit diagram for a two input CMOS OR gate. Note that this gate should use six transistors.

5. (3 pt) Use Karnaugh maps to find a minimal sum of products represention of the following logic function.

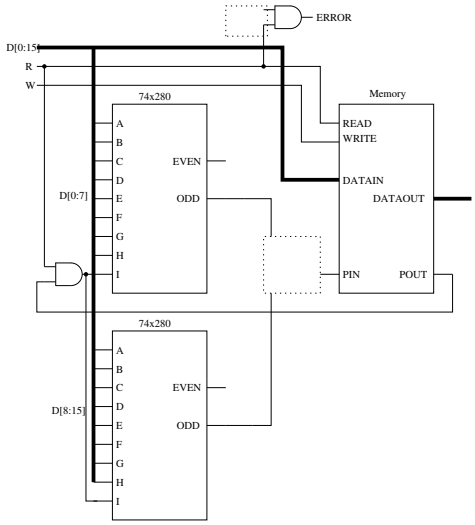
   $F = \prod_{W,X,Y,Z}(6, 7, 8, 9, 10, 11, 12, 13, 14)$

6. (2 pt) Briefly describe the role of the sensitivity list in the VHDL process statement.

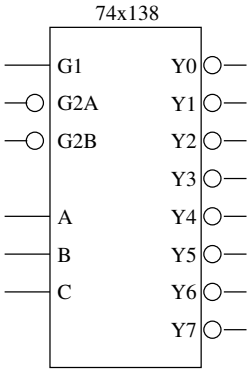
7. (10 pt) Using the following logic circuit (a) write a logic function for each output (Y0, Y1, Y2, and Y3) and (b) determine which common component this logic circuit represents.



8. (8 pt) You have been asked to extend the memory parity circuit to work with a 16 bit data bus. Given the following schematic diagram, correctly connect the two areas in the dotted lines - the ERROR signal circuit and the PIN input to the memory. You may need to use some additional logic gates.

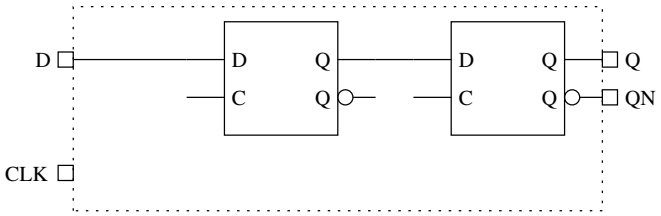


9. (4 pt) Using input signals SRC_L, SEL0, SEL1, and SEL2, configure the inputs of the 74x128 decoder below to cause it to behave as a 1-bit demultiplexer.

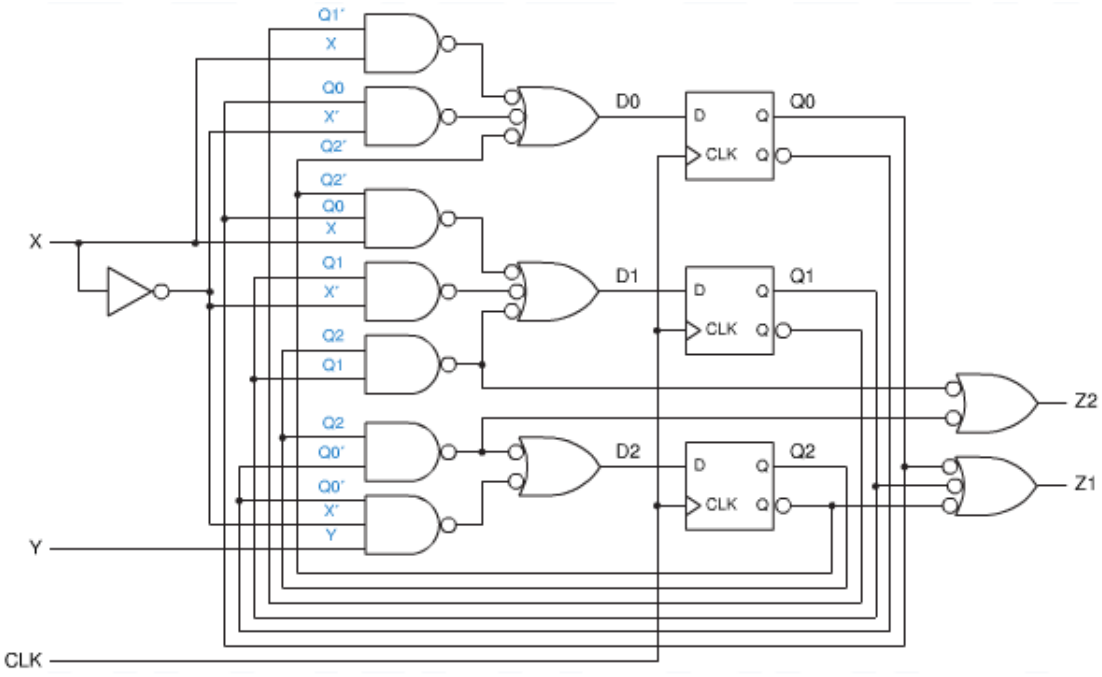


10. (2 pt) Briefly explain the key difference between a latch and a flip-flop.

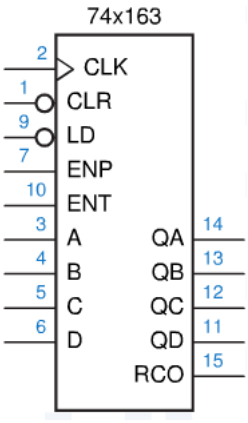
11. (4 pt) The following figure is a partial implementation of a D flip-flop using two D latches. Correctly connect the clock input (CLK) within the circuit. Note that you may need to use one or more logic gates to complete this problem.



12. (6 pt) Write the excitation equations for the following state machine.

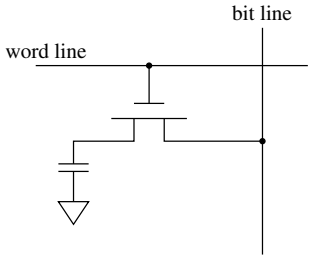


13. (6 pt) Configure the 74x163 counter below to be a free running counter.



14. (2 pt) How many bits of data can a RAM with 4 address bits and 16 data bits store?

15. (4 pt) Given the following one bit DRAM cell, what voltage levels would you place on the word line and the bit line to write a value of zero to the bit stored?



16. (2 pt) To implement a single bit using SRAM, would you use a D latch or a D flip-flop?

17. (4 pt) Briefly decribe the difference between EEPROM and flash EEPROM.

18. (10 pt) The following diagram of a ROM with 6 address inputs and 1 data output is missing two standard combinational logic components. Correctly complete the diagram by drawing and connecting the two components.