Final Exam

Please complete each problem. Show all of your work, even if you cannot obtain the correct answer. You may use only two sheets of letter sized paper for assistance. (80 points total)

1. (4 pt) Perform the following number system conversions.

   (a) $00101011_2 = ?_{16}$
   (b) $00010011_2 = ?_8$
   (c) $163_{16} = ?_8$
   (d) $\text{AFDB} = ?_2$

   Solution:

   (a) $00101011_2 = 0010_2 1011_2 = 2\text{B}_{16}$
   (b) $00010011_2 = 010_2 011_2 = 23_8$
   (c) $163_{16} = 0001_2 0110_2 0011_2 = 000_2 101_2 100_2 011_2 = 543_8$
   (d) $\text{AFDB} = 1010_2 1111_2 1101_2 1100_2 = 1010111111011100_2$

2. (2 pt) Find the eight bit two's complement representation of each of the following numbers.

   (a) -10
   (b) -36
   Solution:

   (a)
   $$\begin{aligned} 10 = \quad & 00001010_2 \\ & \Downarrow \text{complement} \\ & 11110101_2 \\ + \quad & 00000001_2 \\ & 11110110_2 \\ & = 1 \cdot -128 + 1 \cdot 64 + 1 \cdot 32 + 1 \cdot 16 + 1 \cdot 4 + 1 \cdot 2 = -10 \end{aligned}$$

   (b)
   $$\begin{aligned} 36 = \quad & 00100100_2 \\ & \Downarrow \text{complement} \\ & 11011011_2 \\ + \quad & 00000001_2 \\ & 11011100_2 \\ & = 1 \cdot -128 + 1 \cdot 64 + 1 \cdot 16 + 1 \cdot 8 + 1 \cdot 4 = -36 \end{aligned}$$

3. (3 pt) Perform the following binary arithmetic using the four bit two's complement representation, showing all carries. For each case, determine if overflow occurs. If it does, state why it occurs.

   $5 + -1$

   Solution:

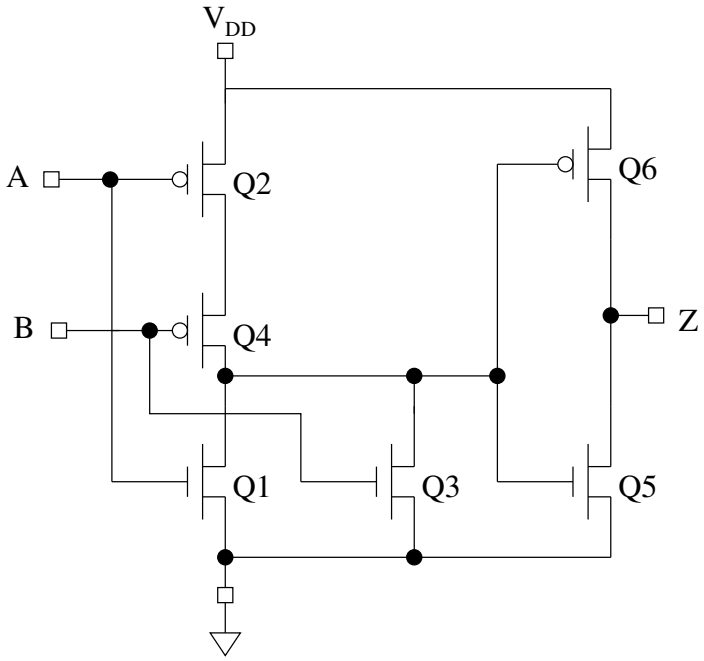
   $5 = 0101_2$
   $-1 = 1111_2$

C	1	1	1	1	0
		0	1	0	1
	+	1	1	1	1
		0	1	0	0

   Overflow does not occur.

4. (4 pt) Write the function table and draw the circuit diagram for a two input CMOS OR gate. Note that this gate should use six transistors.

   Solution:



A	**B**	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Z**
L	L	off	on	off	on	on	off	L
L	H	off	on	on	off	off	on	H
H	L	on	off	off	on	off	on	H
H	H	on	off	on	off	off	on	H

5. (3 pt) Use Karnaugh maps to find a minimal sum of products represention of the following logic function.

$F = \prod_{W,X,Y,Z}(6, 7, 8, 9, 10, 11, 12, 13, 14)$

Solution:

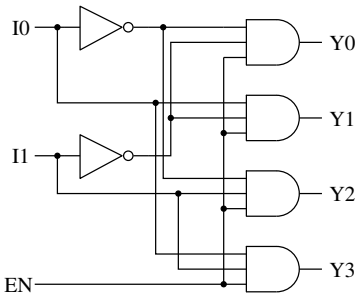
$F = \prod_{W,X,Y,Z}(6, 7, 8, 9, 10, 11, 12, 13, 14) = \sum_{W,X,Y,Z}(0, 1, 2, 3, 4, 5, 15) = W' \cdot X' + W' \cdot Y' + W \cdot X \cdot Y \cdot Z$

YZ \ WX	00	01	11	10
00	0 1	4 1	12	8
01	1 1	5 1	13	9
11	3 1	7	15 1	11
10	2 1	6	14	10

6. (2 pt) Briefly describe the role of the sensitivity list in the VHDL process statement.
Solution:

The sensitivity list informs the simulator which signals should trigger the process to run when they change.

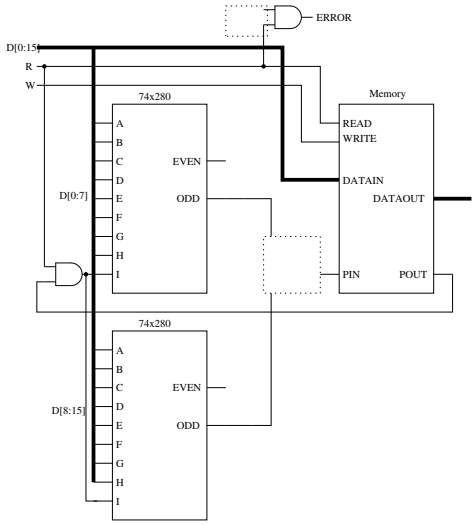
7. (10 pt) Using the following logic circuit (a) write a logic function for each output (Y0, Y1, Y2, and Y3) and (b) determine which common component this logic circuit represents.



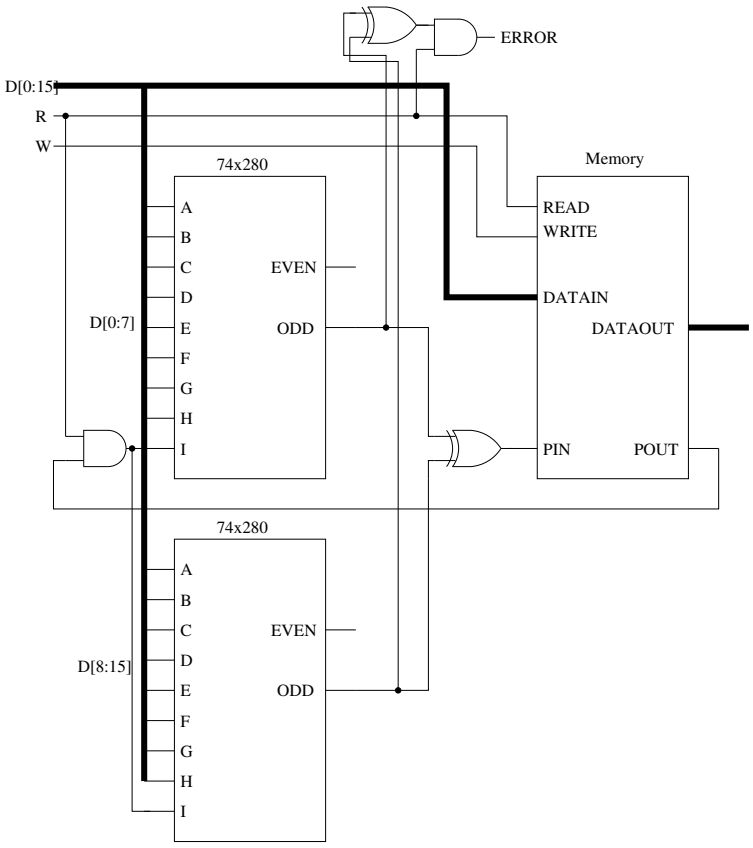
Solution:

(a)
$Y0 = I0' \cdot I1' \cdot EN$
$Y1 = I0 \cdot I1' \cdot EN$
$Y2 = I0' \cdot I1 \cdot EN$
$Y3 = I0 \cdot I1 \cdot EN$
(b) This is a 2-to-4 binary decoder with enable.

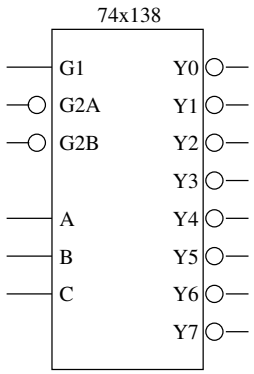
8. (8 pt) You have been asked to extend the memory parity circuit to work with a 16 bit data bus. Given the following schematic diagram, correctly connect the two areas in the dotted lines - the ERROR signal circuit and the PIN input to the memory. You may need to use some additional logic gates.



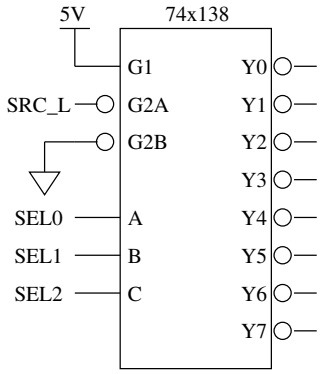
Solution:



9. (4 pt) Using input signals SRC_L, SEL0, SEL1, and SEL2, configure the inputs of the 74x128 decoder below to cause it to behave as a 1-bit demultiplexer.



Solution:

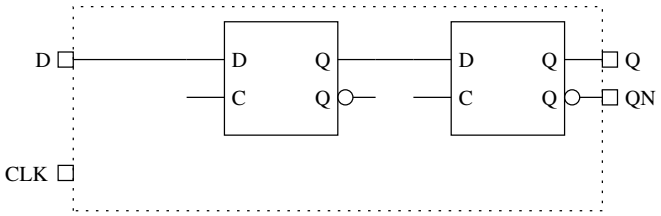


10. (2 pt) Briefly explain the key difference between a latch and a flip-flop.

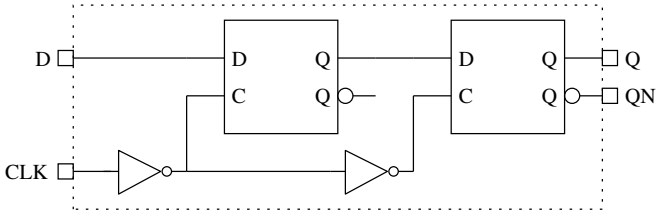
Solution:

A flip-flop operates using a clock signal, a latch does not.

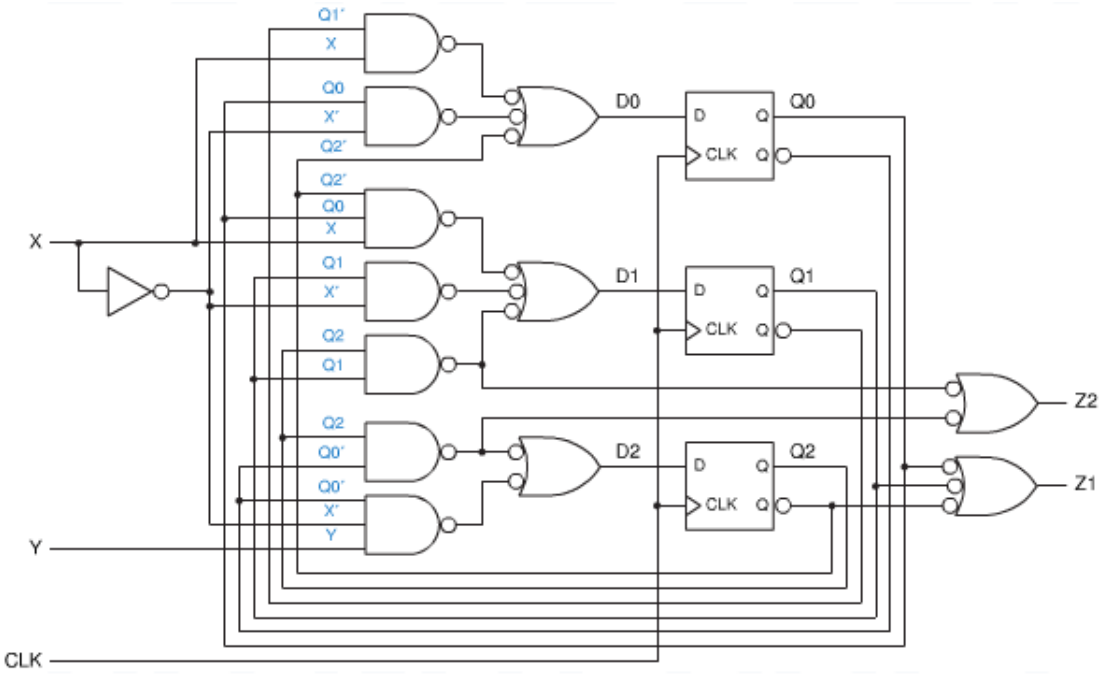
11. (4 pt) The following figure is a partial implementation of a D flip-flop using two D latches. Correctly connect the clock input (CLK) within the circuit. Note that you may need to use one or more logic gates to complete this problem.



Solution:



12. (6 pt) Write the excitation equations for the following state machine.



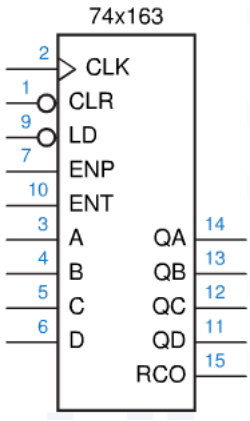
Solution:

$$D0 = Q1' \cdot X + Q0 \cdot X' + Q2$$

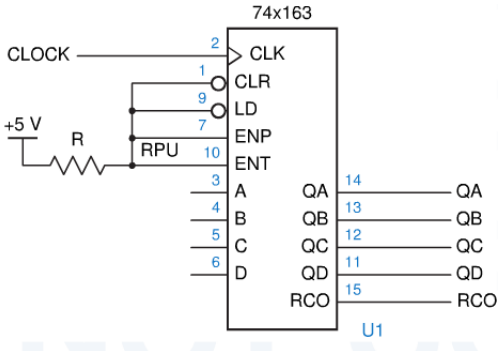
$$D1 = Q2' \cdot Q0 \cdot X + Q1 \cdot X' + Q2 \cdot Q1$$

$$D2 = Q2 \cdot Q0' \cdot Q0] \cdot X' \cdot Y$$

13. (6 pt) Configure the 74x163 counter below to be a free running counter.



Solution:

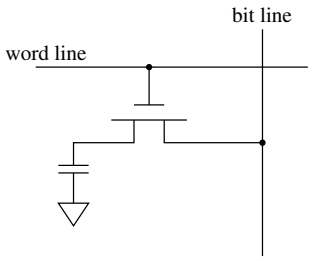


14. (2 pt) How many bits of data can a RAM with 4 address bits and 16 data bits store?

Solution:

$2^4 * 16 = 256$ bits

15. (4 pt) Given the following one bit DRAM cell, what voltage levels would you place on the word line and the bit line to write a value of zero to the bit stored?



Solution:

The word line should be high, the bit line should be low.

16. (2 pt) To implement a single bit using SRAM, would you use a D latch or a D flip-flop?

    Solution:

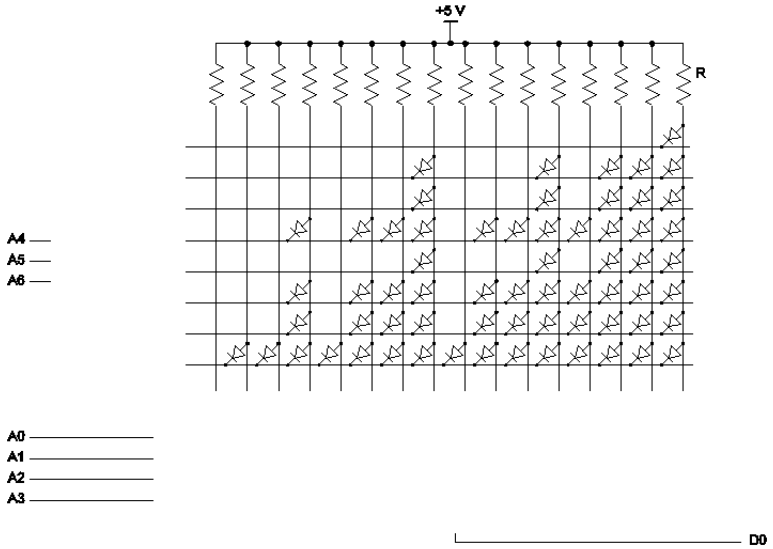
    A D latch would be used, since an SRAM is not a synchronous circuit.

17. (4 pt) Briefly decribe the difference between EEPROM and flash EEPROM.

    Solution:

    Flash EEPROM can be erased in large chunks, EEPROM can be erased at the bit level.

18. (10 pt) The following diagram of a ROM with 6 address inputs and 1 data output is missing two standard combinational logic components. Correctly complete the diagram by drawing and connecting the two components.



Solution: