	Marwadi University **Faculty of Engineering and Technology** **Department of Information and Communication Technology**
Subject: Capstone Project (01CT1718)	**Innovation and Originality**
	Name: Kirtan A. Makwana | **Enrolment No: 92200133031**

Innovation and Originality

Introduction:

In this project we used existing technologies in new way or configuring the FPGA board such way not addressed anywhere. This project focuses on implementing reliable communication protocols (UART, SPI, I2C) on FPGA boards. While many examples of these protocols exist for microcontrollers, very few focus on FPGA-based implementation with Verilog HDL in a modular and educational format. This makes our project stand out as both technically original and practically useful for students, educators, and developers.

Novel Approach:

The innovative part of our project is the use of FPGA hardware to implement standard communication protocols in a modular and reusable way. Instead of relying on software-driven microcontroller solutions, we designed dedicated hardware modules (UART, SPI, I2C) using Verilog HDL. Each protocol is built as an independent module with a clean top-level integration, making it easy to test, reuse, and expand.

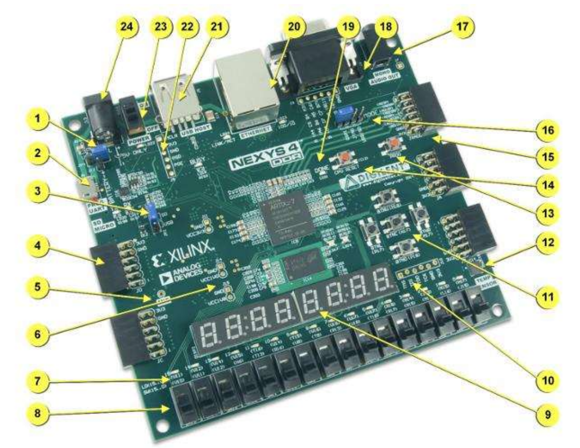


Figure 1. Nexys4 DDR board features.

Callout	Component Description	Callout	Component Description
1	Power select jumper and battery header	13	FPGA configuration reset button
2	Shared UART/ JTAG USB port	14	CPU reset button (for soft cores)
3	External configuration jumper (SD / USB)	15	Analog signal Pmod connector (XADC)
4	Pmod connector(s)	16	Programming mode jumper
5	Microphone	17	Audio connector
6	Power supply test point(s)	18	VGA connector
7	LEDs (16)	19	FPGA programming done LED
8	Slide switches	20	Ethernet connector
9	Eight digit 7-seg display	21	USB host connector
10	JTAG port for (optional) external cable	22	PIC24 programming port (factory use)
11	Five pushbuttons	23	Power switch
12	Temperature sensor	24	Power jack

We also took advantage of the inbuilt sensors on the Nexys 4 DDR FPGA board (such as the ADXL362 accelerometer and ADT7420 temperature sensor) to directly test real-world communication. This eliminates the need for extra hardware and creates a direct bridge between theory and practice.

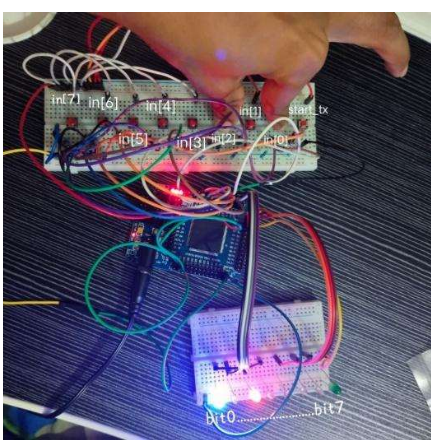
Another novel point is the educational orientation. We are not just building protocols—we are creating a framework that students and researchers can use as a learning platform for FPGA-based communication. This helps fill the gap between theoretical classroom teaching and industry-ready FPGA prototyping.

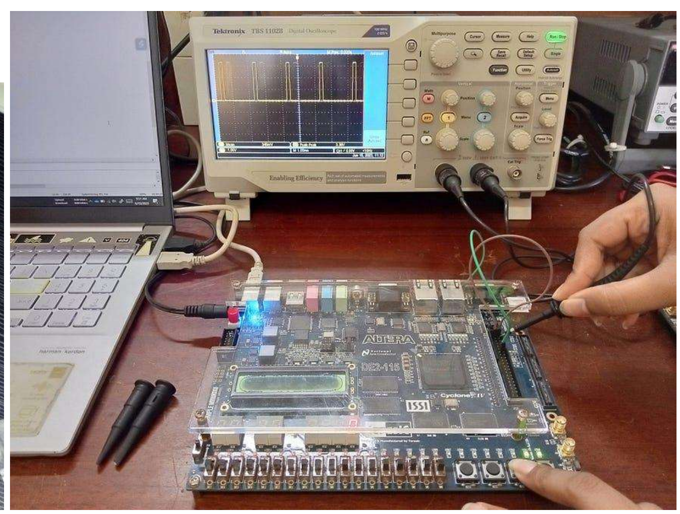
Comparison with Existing Solutions:

Most existing UART, SPI, and I2C designs are implemented in microcontrollers (Arduino, STM32, etc.). These are easier to use but are software-driven and limited in speed and flexibility. Our FPGA approach provides parallelism, reconfigurability, and higher.

Many online resources provide HDL code snippets with proper modular design, documentation, or testing with real sensors. Our project can give a structured, modular, and tested design flow along with hardware demonstrations.

Commercial IP cores exist for UART/SPI/I2C, but they are often costly or proprietary. This project provides an open, educational alternative that is low-cost and easily adaptable for student projects and research





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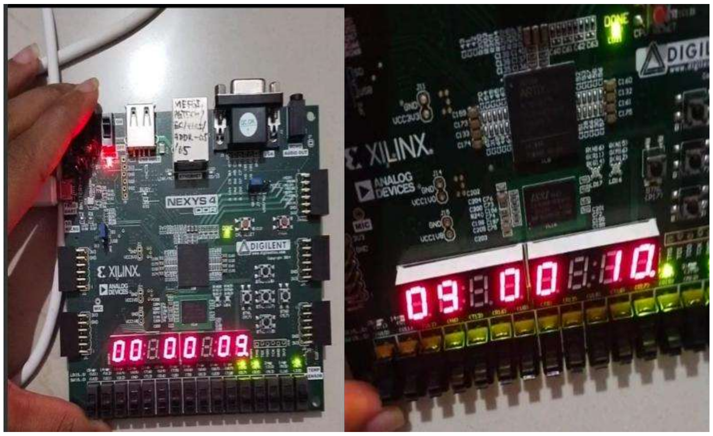

ICT Relevance:

This project fits directly into ICT areas like Digital Logic Design, VLSI, and Embedded Systems. It also supports modern ICT trends:

- IoT: Most IoT devices rely on UART, SPI, and I2C for sensor communication.
- VLSI/Chip Prototyping: FPGAs are used as the first step before chip manufacturing.
- Industry Readiness: Students trained in FPGA communication protocols are better prepared for careers in hardware design and system integration.

In this project we design the basic requirement of decided topic with digital design flow and then according to flow of the definition we decide to use which kind of method to use in Verilog code to design the architecture of the definition then make the code such that it can be synthesizable and implementable on FPGA board. By following this process with different trials, we can accomplish the final definition requirements.

By solving this problem, the project not only helps students and educators but also strengthens the link between academic training and industry requirements in ICT.

References:

This are some references which shows existing resources for implementation of project
https://medium.com/@namiwije/implementation-of-uart-protocol-using-fpga-a04d0b3b5bcb
https://iopscience.iop.org/article/10.1088/1742-6596/1449/1/012027/pdf
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