Marwadi University	Marwadi University Faculty of Engineering and Technology Department of Information and Communication Technology
Subject: Capstone Project (01CT1718)	Deployment and Operations Section
	Name: Kirtan A. Makwana / Enrolment No: 92200133031

Deployment and Operations Section

Introduction:

The objective of the Capstone project is to build reliable communication protocols like UART/SPI/I2C over FPGA board on Altera Cyclone II or Nexys4 DDR to easily interface sensors and different module to interface the Input and Output via FPGA boards using the unique features of the FPGA board. It will help the people to understand the FPGA and communication protocol structure and use of it while testing.

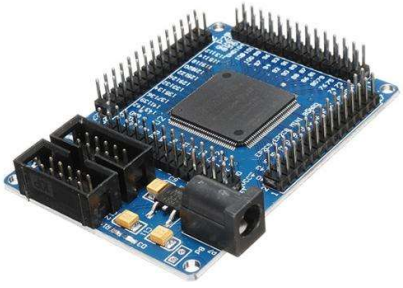
Project Proposal:

A Field-Programmable Gate Array (FPGA) is a semiconductor device based on a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. FPGAs are reconfigurable, meaning that the logic functions within the FPGA can be reprogrammed to implement different designs or algorithms after manufacturing. This reconfigurability contrasts with fixed-function Application-Specific Integrated Circuits (ASICs), making FPGAs highly versatile for prototyping and deployment in a wide range of applications.

The FPGA boards are quite faster than usual microcontroller because of its capability to adapt the advantage of different parameter like high speed parallel processing, custom GPIO interfaces, frequency trading, While FPGAs offer superior hardware-level performance and flexibility, microcontrollers are generally better for cost-sensitive or low-power applications with sequential tasks, thanks to their easier development process and lower unit cost.

Here we can use FPGA board of Altera Cyclone II or Xilinx Nexys 4 DDR, which are very well known FPGA Board for implementing Prototype of HDL design on it and test its compatibility for moving forward the Chip manufacturing or for making a design for an system in less time to build application with low cost.

Altera Cyclone II with EP2C5T144 chip



- EPROM chip configuration using EPCS4, the size of 4Mbit
- Onboard 50M active patch crystal (Crystal Slaughter halfback)
- Power supply with a largemouth outlet, single 5V power supply
- Board has power indicator and resets switch
- Onboard 3 SMD LED, the LED test can be done an experiment, more experiments using lead to complete

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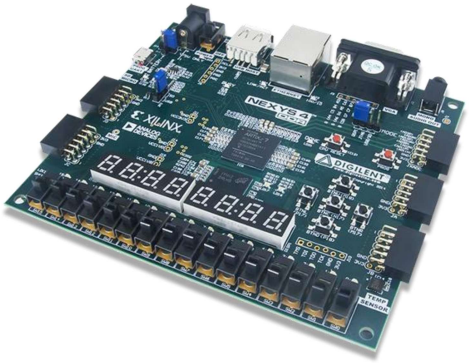
Nexys 4 DDR with XC7A100TCS0324A



Nexys 4 DDR

Artix-7 FPGA

Features	
• Programmable over JTAG and Quad-SPI Flash • On-chip analog-to-digital converter	
Key Specifications	
FPGA Part #	XC7A100T-1CSG324C
Logic Slices	15,850 (4 6-input LUTs & 8 flip-flops each)
Block RAM	4,860 Kbits
Clock Tiles	6 (each with PLL)
DSP Slices	240
Internal clock	450 MHz+
DDR2	128 MiB
Cellular RAM	16MB
Ethernet	10/100 PHY
Connectivity and Onboard I/O	
SD	microSD card connector
Pmod Connectors	4 Pmod ports
VGA	12-bit VGA port
Audio	PWM audio output
Microphone	PDM mic
Temp sensor	One temperature sensor
Display	2 4-digit seven segment displays
Switches	16
Buttons	4
LEDs	16
Tri-color LEDs	2

Deployment Process:

- **Hardware Platform:**
  - Altera Cyclone II was chosen initially and Xilinx Nexys 4 DDR were chosen for deployment due to their popularity in academic FPGA projects and built-in peripherals for UART, SPI, and I2C testing.
- **Software Tools:**
  - Quartus II for synthesis and programming Cyclone II.
  - Vivado for Nexys 4 DDR.
  - ModelSim for pre-deployment simulation.
- **Peripheral Devices:**
  - UART: loopback test using USB-to-UART interface.
  - SPI: accelerometer (ADXL362) connected via SPI bus.
  - I2C: temperature sensor (ADT7420) interfaced on Nexys 4 DDR board.

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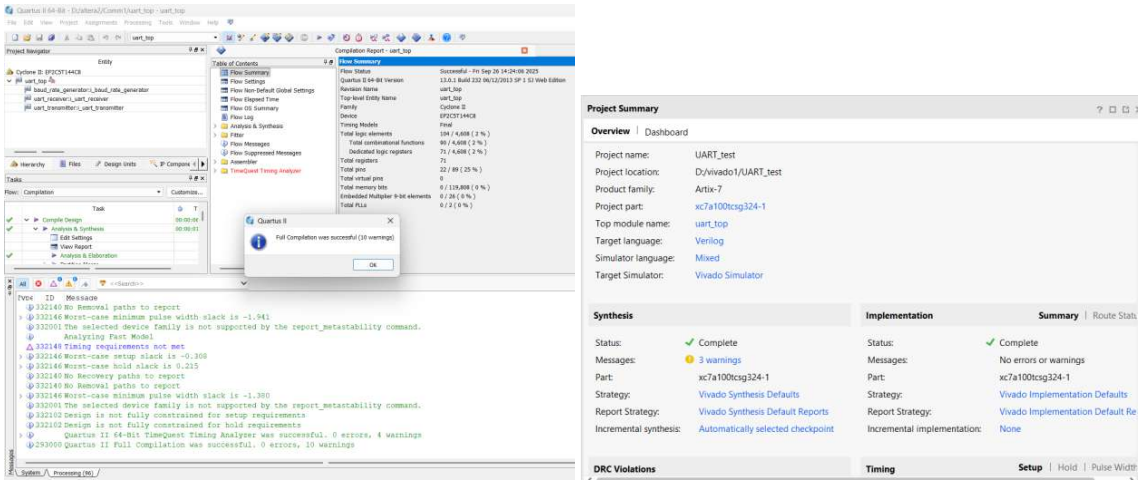
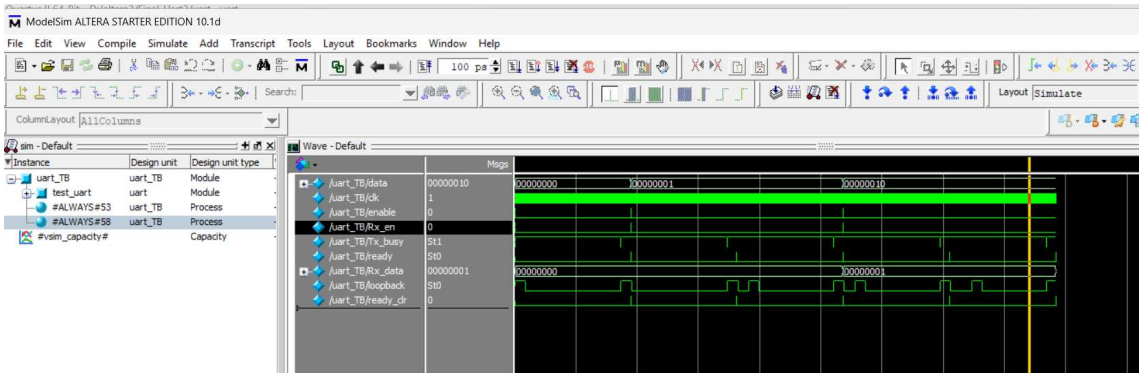


After doing basic test of functionality, we test it on simulation, via testbench we can verify is easily what will happen at any instance.

Testbench are usually not considered under Synthesisable code for the regular code but it shows the waveform, here we used ModeSim software to simulate the testbenches.

UART simulation testing :



SPI simulation testing :

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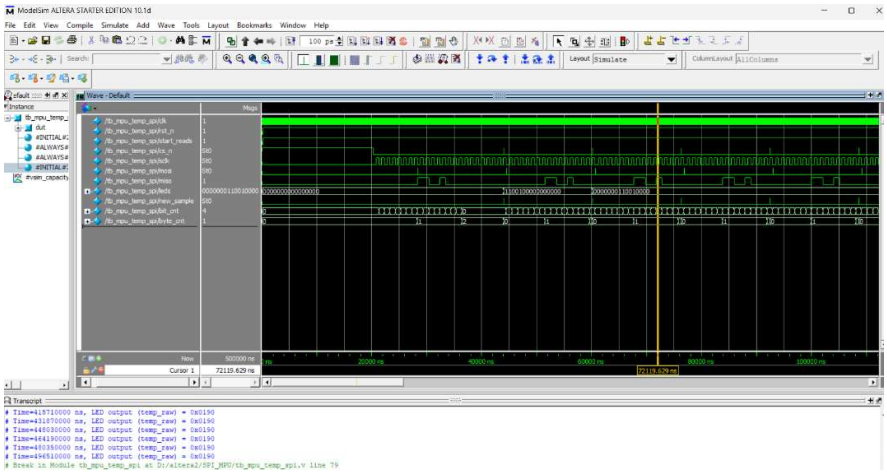
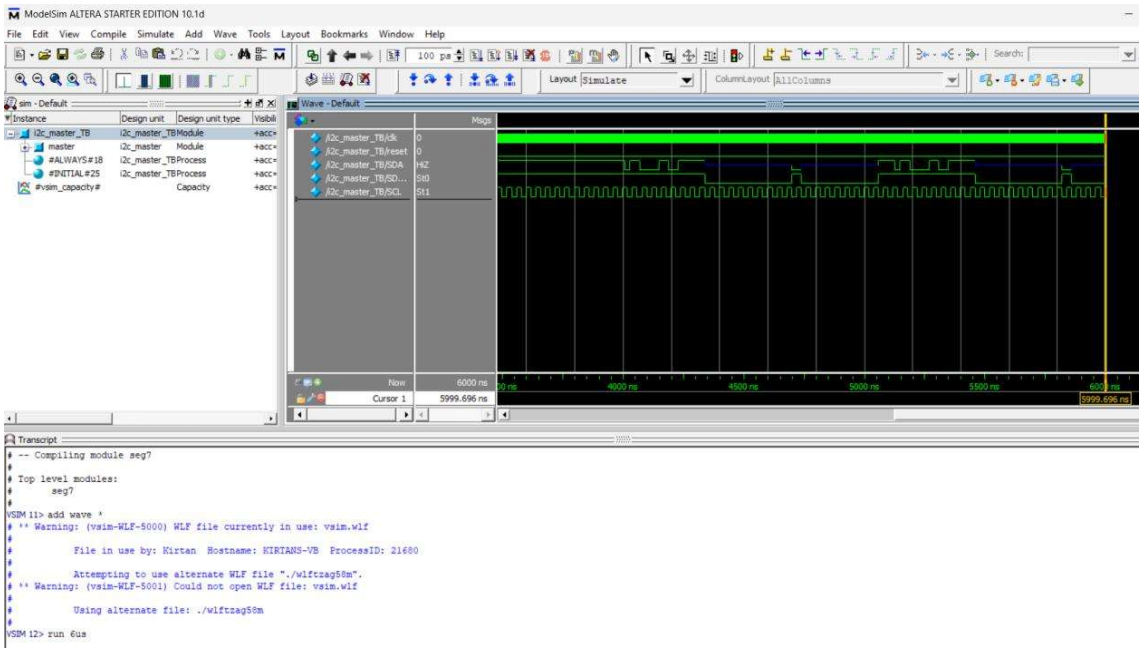


I2C simulation testing :



Deployment Steps

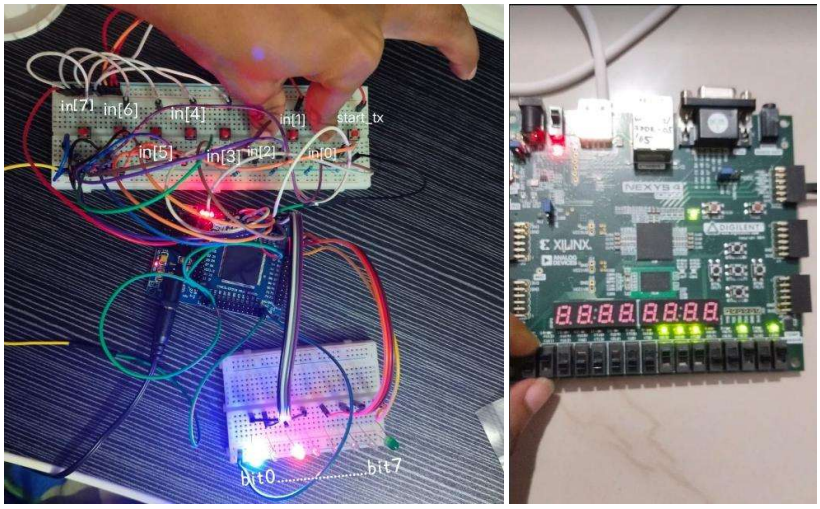
1. **Design Compilation:**
   - Verilog HDL modules compiled in Quartus/Vivado.
   - Errors checked and synthesized into FPGA bitstream (.sof / .bit files).
2. **Programming FPGA:**

- FPGA configured using USB Blaster (Altera) or Digilent Programmer (Xilinx).
- Onboard LEDs and seven-segment display used for initial validation.

3. **Peripheral Integration:**
   - External sensors connected via GPIO headers.
   - Pin constraints defined in Quartus .qsf or Vivado .xdc file.
4. **Live Deployment:**
   - FPGA connected to PC via USB-UART bridge.
   - Sensor data sent over UART for monitoring in a serial terminal (e.g., PuTTY, Tera Term).
   - FPGA operational beyond simulation → working in **real hardware environment**.

Monitoring Strategy:

After implementing the UART we were able to see the same IO result on Nexys 4 DDR board. Then we tried to integrate SPI protocol on 3 axis accelerometer sensor ADXL362. Which went very well as documented before. Following that we also tried to implement I2C protocol with ADT7420. Here we designed the respective SPI/I2C Master module inside of FPGA board with Verilog and got almost accurate result from the sensor by structure we followed from the before document.



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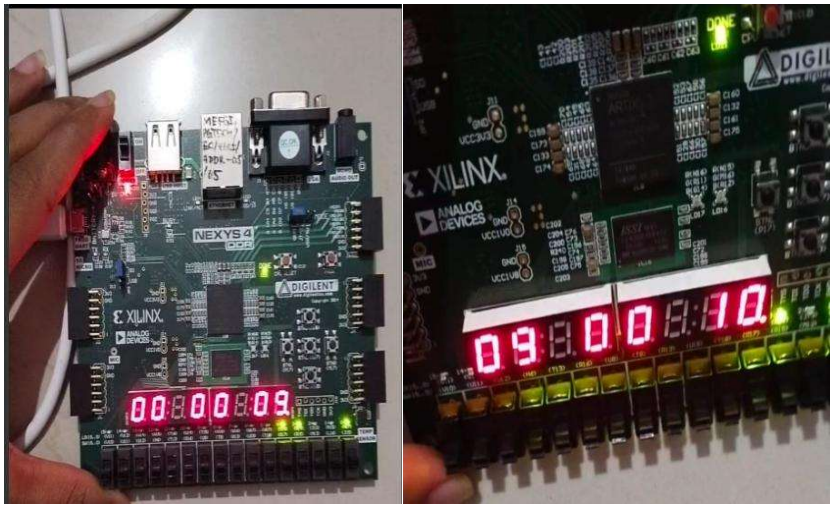

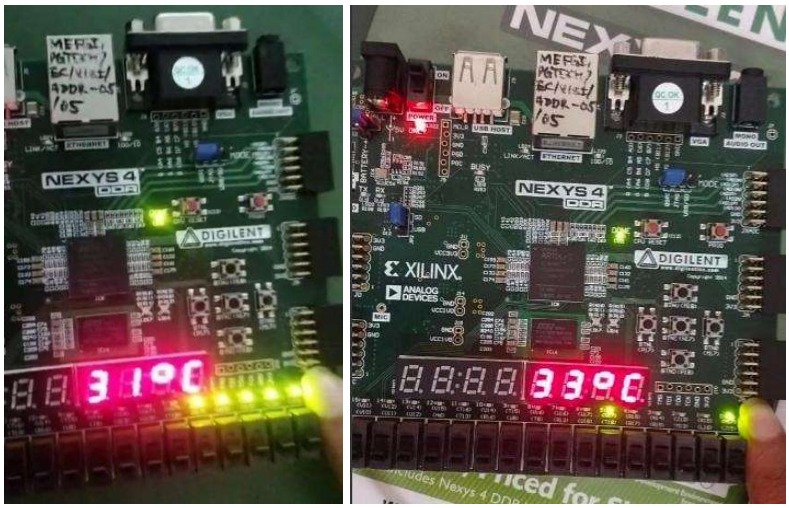

Maintenance Plan:

To keep the system reliable, we created a simple maintenance plan:

- **Weekly tasks:** Back up HDL files and rerun testbenches to confirm no errors were introduced.
- **Monthly tasks:** Inspect FPGA board, cables, and sensors; apply any software or tool updates.
- **Quarterly tasks:** Perform deeper checks, like timing verification, and update documentation.

We also considered possible issues:

- Limited GPIO pins → solved by using one protocol at a time or bus expanders.
- Clock mismatches at higher speeds → solved by refining clock dividers.
- Sensor connection issues → solved by carefully checking datasheet timing diagrams.

Using version control (e.g., GitHub) ensures all changes are tracked, and backups protect against accidental data loss.

Challenges:

During deployment, a few challenges were faced:

- **GPIO limits** on Cyclone II made it tricky to connect multiple sensors at once.
- **Timing mismatches** in UART at very high baud rates caused some errors.
- **SPI integration** with the ADXL362 accelerometer was unstable until CPOL/CPHA were corrected.
- **No built-in dashboards** for FPGA meant we had to log data through UART instead.

Each of these was solved step by step, and the final system ran smoothly.

Conclusion:

The deployment and operations stage proved that the communication protocols (UART, SPI, and I2C) designed in Verilog worked in real hardware, not just in simulation. Live testing on FPGA with sensors confirmed correct data transfer, while monitoring logs and reports showed stable performance. The maintenance plan ensures the system can be kept reliable for long-term use. Despite some hardware and timing challenges, the project successfully met its objectives and is ready to be used as a learning platform or extended for more advanced designs.

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