Marwadi University	Marwadi University Faculty of Engineering and Technology Department of Information and Communication Technology
Subject: Capstone Project (01CT1718)	Testing and Validation
	Name: Kirtan A. Makwana / Enrolment No: 92200133031

Testing and Validation

Introduction:

The objective of the Capstone project is to build reliable communication protocols like UART/SPI/I2C over FPGA board on Altera Cyclone II or Nexys4 DDR to easily interface sensors and different module to interface the Input and Output via FPGA boards using the unique features of the FPGA board. It will help the people to understand the FPGA and communication protocol structure and use of it while testing.

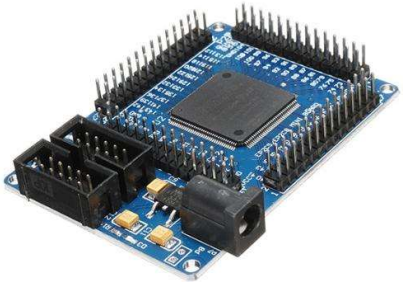
Project Proposal:

A Field-Programmable Gate Array (FPGA) is a semiconductor device based on a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. FPGAs are reconfigurable, meaning that the logic functions within the FPGA can be reprogrammed to implement different designs or algorithms after manufacturing. This reconfigurability contrasts with fixed-function Application-Specific Integrated Circuits (ASICs), making FPGAs highly versatile for prototyping and deployment in a wide range of applications.

The FPGA boards are quite faster than usual microcontroller because of its capability to adapt the advantage of different parameter like high speed parallel processing, custom GPIO interfaces, frequency trading, While FPGAs offer superior hardware-level performance and flexibility, microcontrollers are generally better for cost-sensitive or low-power applications with sequential tasks, thanks to their easier development process and lower unit cost.

Here we can use FPGA board of Altera Cyclone II or Xilinx Nexys 4 DDR, which are very well known FPGA Board for implementing Prototype of HDL design on it and test its compatibility for moving forward the Chip manufacturing or for making a design for an system in less time to build application with low cost.

Altera Cyclone II with EP2C5T144 chip



- EPROM chip configuration using EPCS4, the size of 4Mbit
- Onboard 50M active patch crystal (Crystal Slaughter halfback)
- Power supply with a largemouth outlet, single 5V power supply
- Board has power indicator and resets switch
- Onboard 3 SMD LED, the LED test can be done an experiment, more experiments using lead to complete

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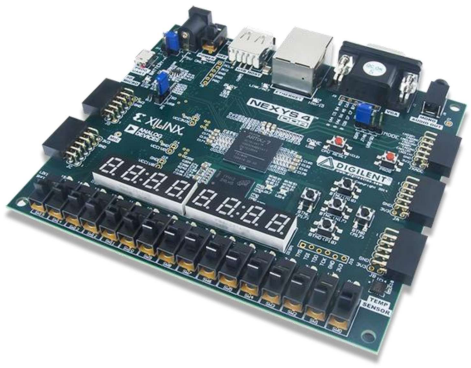
Nexys 4 DDR with XC7A100TCS0324A



Nexys 4 DDR

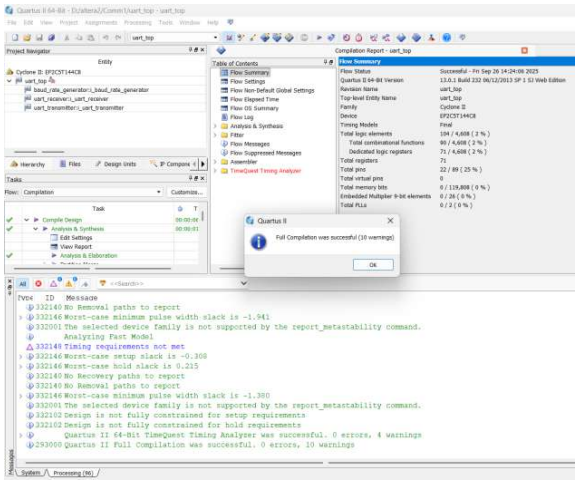
Artix-7 FPGA

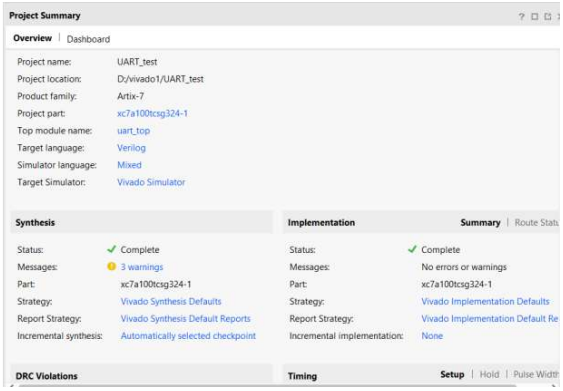
Features	
• Programmable over JTAG and Quad-SPI Flash • On-chip analog-to-digital converter	
Key Specifications	
FPGA Part #	XC7A100T-1CSG324C
Logic Slices	15,850 (4 6-input LUTs & 8 flip-flops each)
Block RAM	4,860 Kbits
Clock Tiles	6 (each with PLL)
DSP Slices	240
Internal clock	450 MHz+
DDR2	128 MiB
Cellular RAM	16MB
Ethernet	10/100 PHY
Connectivity and Onboard I/O	
SD	microSD card connector
Pmod Connectors	4 Pmod ports
VGA	12-bit VGA port
Audio	PWM audio output
Microphone	PDM mic
Temp sensor	One temperature sensor
Display	2 4-digit seven segment displays
Switches	16
Buttons	4
LEDs	16
Tri-color LEDs	2

Testing Methodology:

The Testing methodology starts from the basic programming on the FPGA board like GPIO pins clock generation. First of all we have taken the FPGA board which are used for regular education purpose which is Altera Cyclone II which can be programmed by open source Quartus II software which it we create Verilog code such that it should pass Synthesis test and should compile which the software.

The same process is applied on Xilinx Vivado software. Wee test each GPIO and Clock generation by performing different experiments.





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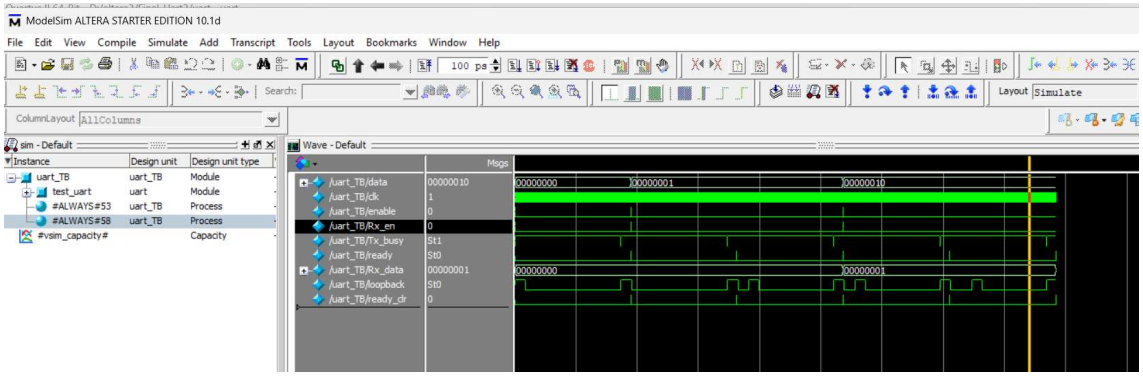
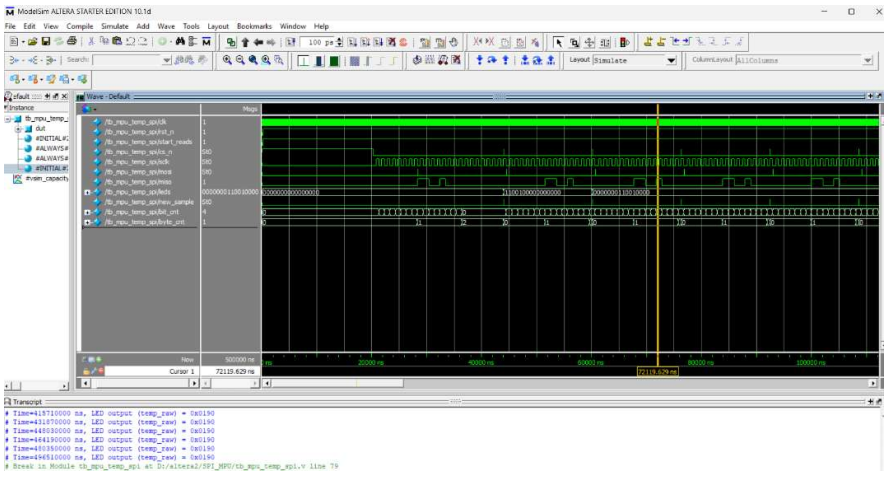
After doing basic test of functionality, we test it on simulation, via testbench we can verify is easily what will happen at any instance.

Testbench are usually not considered under Synthesisable code for the regular code but it shows the waveform, here we used ModeSim software to simulate the testbenches.

UART simulation testing :



SPI simulation testing :



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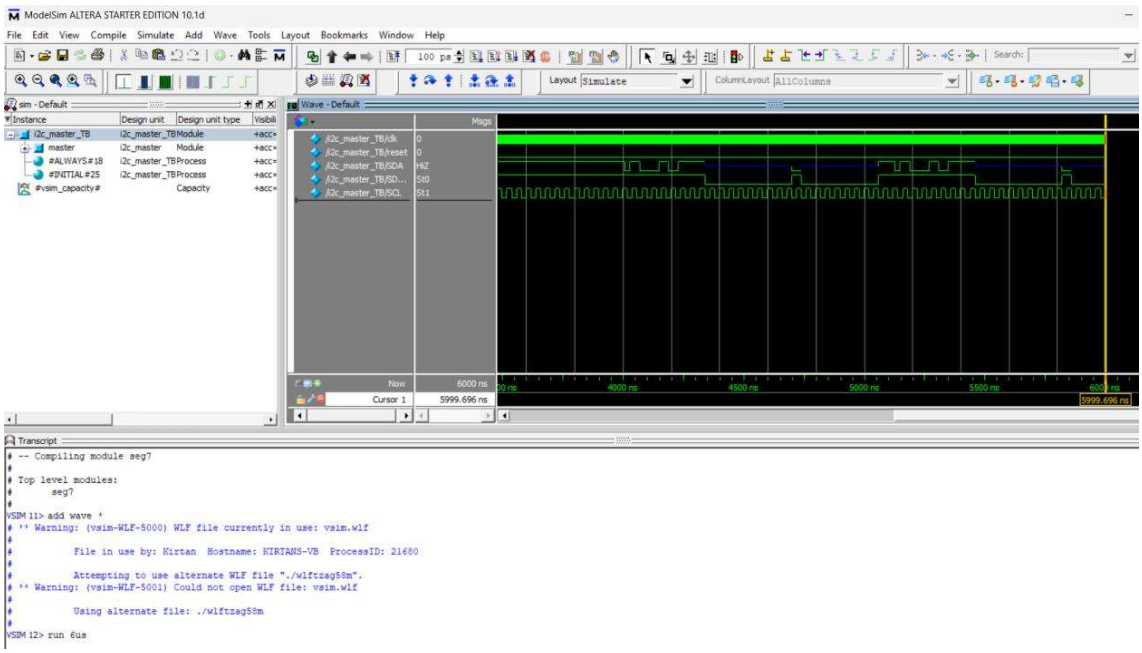
I2C simulation testing :



On the above simulation you can see that UART is showing the data which are being transmitted and received at particular baud rate of 9600.

Whenever the data is transmitted then the receiver side starts the counter the receives same number of bits and same data on receiver side.

Same on the SPI we have set such condition in the testbench to simulate it as the slave device. We have designed the master device such that when CS line goes low it sends the data on MOSI line one by one following the state machine and sending the 7bit data with read bit (i.e.), total 8 bit data when the sensor gets the data on the bus it will respond the data from the MISO line with the data which it want to send the data can be format of any 1byte or 2 byte according to sensor datasheet here we are getting 2 bytes from the Slave device we designed into the testbench.

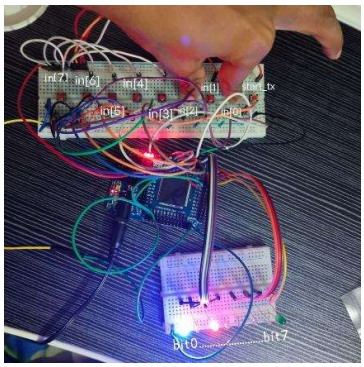
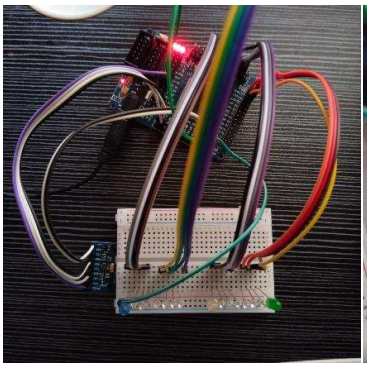
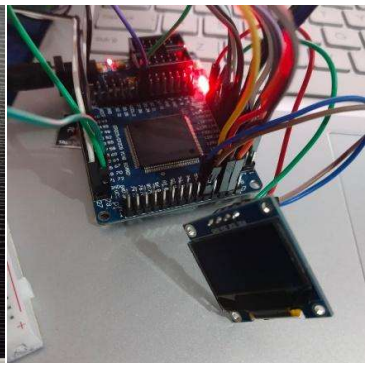
Next, we can see the Wave form for I2C simulation where we are having some of the same functionality as SPI but different in bus management, the I2C will contain only 2 wires (SCL,SDA) where we use SDA line to communicate between sensor and module one to one. In wave form we ca nsee when SDA direction is set to 1 then master slave can send address and data here we are sending only address with read bit, after receiving acknowledgement the SDA line goes low and then it goes high impedence z where it is allowing slave device to set values on the SDA line while master read the value on it.

Unit Tests:

The below first photo is test of UART on FPGA board of Altera Cyclone 2 whre while pressing start TX button we ca send desired data and see the same on LED by connecting RX and TX together.

The second set was tried to perform SPI over MPU9250/6500 which has SPI interface in it, which was quite not able to get success.

In the third photo we tried to implantation of the I2C by waking up the whole I2C display and practice it to perform I2C communication with it, which also turned out to be failure to implement. The MPU9250/6500 was also having the I2C interface but we weren't able to perform it well on with multiple number of wires, buttons, registers and LED sorting on the breadboard

From above trails we understood that we might lack some wiring on the board of misconfiguration with the sensor and connection. So, we decided to try the FPGA board of Xilinx Nexys 4 DDR which is having inbuilt peripharels/sensor with protocol interface like SPI and I2C.

Integration Tests:

After implementing the UART we were able to see the same IO result on Nexys 4 DDR board. Then we tried to integrate SPI protocol on 3 axis accelerometer sensor ADXL362. Which went very well as documented before. Following that we also tried to implement I2C protocol with ADT7420. Here we designed the respective SPI/I2C Master module inside of FPGA board with Verilog and got almost accurate result from the sensor by structure we followed from the before document.

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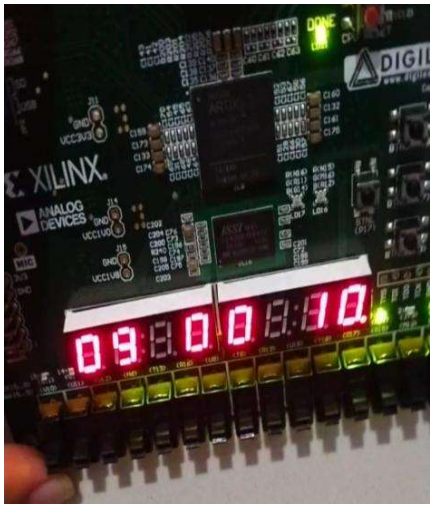

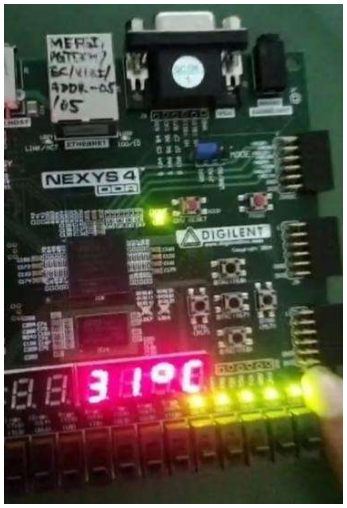

Validation Against Objectives:

The project successfully met its objectives by implementing UART, SPI, and I2C protocols on FPGA and validating them with real sensors. Testing showed accurate baud rate generation, reliable SPI data transfer with the ADXL362 accelerometer, and successful temperature readouts from the ADT7420 via I2C. Minor deviations were observed at very high baud rates, which can be improved by clock optimization. Overall, the validation confirms that the system fulfills stakeholder needs for educational and prototyping purposes.

References:

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