Marwadi University	Marwadi University Faculty of Engineering and Technology Department of Information and Communication Technology	
Subject: Capstone Project (01CT1718)	Project Definition and Scope	
	Date: 19/09/2025	Enrolment No: 92200133031

Project Definition and Scope

Description:

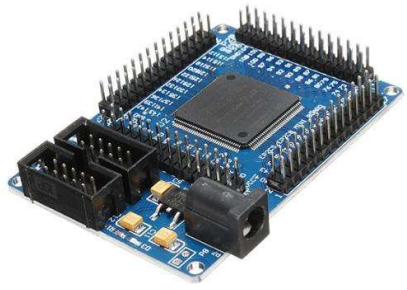
The objective of the Capstone project is to build reliable communication protocols like UART/SPI/I2C over FPGA board to easily interface sensors and different module to interface the Input and Output via FPGA boards using the unique features of the FPGA board. It will help the people to understand the FPGA and communication protocol structure and use of it while testing.

Project Proposal:

A Field-Programmable Gate Array (FPGA) is a semiconductor device based on a matrix of configurable logic blocks (CLBs) connected via programmable interconnects. FPGAs are reconfigurable, meaning that the logic functions within the FPGA can be reprogrammed to implement different designs or algorithms after manufacturing. This reconfigurability contrasts with fixed-function Application-Specific Integrated Circuits (ASICs), making FPGAs highly versatile for prototyping and deployment in a wide range of applications.

The FPGA boards are quite faster than usual microcontroller because of its capability to adapt the advantage of different parameter like high speed parallel processing, custom GPIO interfaces, frequency trading, While FPGAs offer superior hardware-level performance and flexibility, microcontrollers are generally better for cost-sensitive or low-power applications with sequential tasks, thanks to their easier development process and lower unit cost.

Here we can use FPGA board of Altera Cyclone II or Xilinx Nexys 4 DDR, which are very well known FPGA Board for implementing Prototype of HDL design on it and test its compatibility for moving forward the Chip manufacturing or for making a design for an system in less time to build application with low cost.



Altera Cyclone 2 with EP2C5T144 chip

- EPROM chip configuration using EPCS4, the size of 4Mbit
- Onboard 50M active patch crystal (Crystal Slaughter halfback)
- Power supply with a largemouth outlet, single 5V power supply
- Board has power indicator and resets switch
- Onboard 3 SMD LED, the LED test can be done an experiment, more experiments using lead to complete

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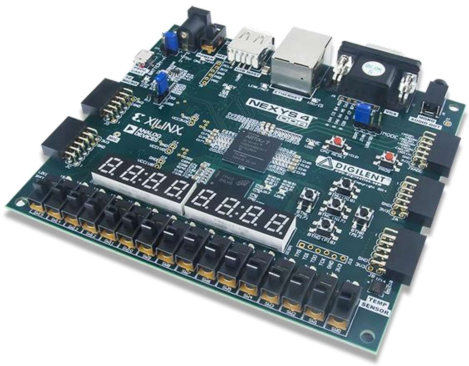

Nexys 4 DDR

Artix-7 FPGA

Features	
• Programmable over JTAG and Quad-SPI Flash • On-chip analog-to-digital converter	
Key Specifications	
FPGA Part #	XC7A100T-1CSG324C
Logic Slices	15,850 (4 6-input LUTs & 8 flip-flops each)
Block RAM	4,860 Kbits
Clock Tiles	6 (each with PLL)
DSP Slices	240
Internal clock	450 MHz+
DDR2	128 MiB
Cellular RAM	16MB
Ethernet	10/100 PHY
Connectivity and Onboard I/O	
SD	microSD card connector
Pmod Connectors	4 Pmod ports
VGA	12-bit VGA port
Audio	PWM audio output
Microphone	PDM mic
Temp sensor	One temperature sensor
Display	2 4-digit seven segment displays
Switches	16
Buttons	4
LEDs	16
Tri-color LEDs	2

Nexys4 DDR with XC7A100TCS0324A

The Objective:

The objectives of this project are mentioned below,

- To understand real-time application off FPGA board
- To gain practical experience in designing testing and prototyping the FPGA boards
- To discover different FPGA boards which can accelerate ASIC development

This project aligns with ICT domain like Digital Logic Design, Digital design using Verilog, System Design with FPGA, VLSI design etc. In this project we design the basic requirement of decided topic with digital design flow and then according to flow of the definition we decide to use which kind of Method to use in Verilog code to design the architecture of the definition then make the code such that it can be synthesizable and implementable on FPGA board. By following this process with different trials we can accomplish the final definition requirements.

Feasibility Analysis:

- ***Technical Feasibility:***

This project can be done using Verilog HDL on FPGA boards like Altera Cyclone II or Xilinx Nexys 4 DDR. Free software tools such as Quartus II (for Altera) or Vivado (for Xilinx) will be used for design and synthesis. ModelSim will help in simulation. Sensors with I2C and

SPI can be easily connected to their GPIO. These tools are widely used, free for students, and suitable for testing communication protocols.

- ***Economical Feasibility:***

The FPGA boards mentioned above are highly pricing in market around 4k to 30k in rupees but it can be provided by the college from departments student resources. This can help us to avoid the high cost.

- ***Ethical Considerations:***

Since the project may use sensors connected to them, there is data privacy kind of thing. There is also test or dummy data can be used where possible with buttons and switches. Open-source free tools should be properly. The project mainly supports learning and research, so ethical risks are minimal.

Market/User Needs Analysis:

The Market/User are student and developers who are trying to understand the FPGA board and give it a fresh start by implementing such basic protocols and topics which can he understand properly and he can be ready for industry level implementation by learning from this. By this project they can understand use of FPGA board and ASIC flow prototyping structure.

Novelty Review:

The are many published article and resources are there which shows theory of communication protocols but there are rarely resources which explain these protocols for implementation on FPGA board with Hardware Description Language like Verilog HDL. To show implementation of UART/SPI/I2C protocol.

- https://www.analog.com/en/resources/analog-dialogue/articles/uart-a-hardware-communication-protocol.html
- https://wiki.analog.com/resources/fpga/peripherals/spi_engine/spi_bus_interface
- https://learn.sparkfun.com/tutorials/i2c/all
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