Loïc Pottier

PhD in Computer Science

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Driving license

Education

2015 – 2018 **PhD in Computer Science**, *LIP laboratory – École Normale Supérieure de Lyon.* "Co-scheduling for large-scale applications: memory and resilience", under the supervision of Anne Benoit and Yves Robert in the ROMA team, defended on September 18, 2018

2013 – 2015 **Master of Science**, *University of Versailles, with High Honors («Bien»)* . Major in Computer Science, specialized in High Performance Computing

2010 – 2013 **Bachelor of Science**, *University of Caen, with Honors («Assez Bien»)* . Major in Computer Science

2010 **High school diploma**, Caen, *with Honors («Assez Bien »).* Major in Science, minor in Mathematics

Publications

– authors are listed in alphabetical order

Thesis

[T1] Loïc Pottier. "Co-scheduling for large-scale applications : memory and resilience". PhD thesis. Université de Lyon, Sept. 2018.

Book Chapters

[B1] G. Aupy, A. Benoit, L. Pottier, P. Raghavan, Y. Robert, and M. Shantharam. "Co-scheduling high-performance computing applications". In: *Big Data Management and Processing*. Ed. by K.-C. Li, H. Jiang, and A. Zomaya. Chapman and Hall/CRC Press, 2017. Chap. 5. ISBN: 9781351650045.

Articles in International Refereed Journals

[J1] G. Aupy, A. Benoit, S. Dai, L. Pottier, P. Raghavan, Y. Robert, and M. Shantharam. "Co-scheduling Amdahl applications on cache-partitioned systems". In: *International Journal of High Performance Computing and Applications* (2017). DOI: 10.1177/1094342017710806.

[J2] A. Benoit, L. Pottier, and Y. Robert. "Resilient co-scheduling of malleable applications". In: *International Journal of High Performance Computing and Applications* (2017). DOI: 10.1177/1094342017704979.

Articles in International Refereed Conferences

[C1] G. Aupy, A. Benoit, B. Goglin, L. Pottier, and Y. Robert. "Co-scheduling HPC workloads on cache-partitioned CMP platforms". In: *IEEE International Conference on Cluster Computing, CLUSTER 2018, Belfast, UK, September 10-13*. IEEE. Sept. 2018. DOI: 10.1109/CLUSTER.2018.00052.

[C2] A. Benoit, S. Perarnau, L. Pottier, and Y. Robert. "A performance model to execute workflows on high-bandwidth-memory architectures". In: *47th International Conference on Parallel Processing, ICPP 2018, Eugene, USA, August 13-16*. Aug. 2018. DOI: 10.1145/3225058.3225110.

[C3] A. Benoit, L. Pottier, and Y. Robert. "Resilient application co-scheduling with processor redistribution". In: *45th International Conference on Parallel Processing, ICPP 2016, Philadelphia, USA, August 16-19*. Aug. 2016. DOI: 10.1109/ICPP.2016.21.

Articles in International Refereed Workshops

[W1] G. Aupy, A. Benoit, L. Pottier, P. Raghavan, Y. Robert, and M. Shantharam. "Co-scheduling algorithms for cache-partitioned systems". In: *19th Workshop on Advances in Parallel and Distributed Computational Models APDCM 2017*. IEEE Computer Society Press, 2017. DOI: 10.1109/IPDPSW.2017.60.

Research Reports

[R1] G. Aupy, A. Benoit, B. Goglin, L. Pottier, and Y. Robert. *Co-scheduling HPC workloads on cache-partitioned CMP platforms*. Research Report RR-9154. Inria, Feb. 2018.

[R2] A. Benoit, S. Perarnau, L. Pottier, and Y. Robert. *A performance model to execute workflows on high-bandwidth memory architectures*. Research Report RR-9165. ENS Lyon ; Inria Grenoble Rhône-Alpes ; University of Tennessee Knoxville ; Georgia Institute of Technology ; Argonne National Laboratory, Apr. 2018, pp. 1–28.

[R3] G. Aupy, A. Benoit, S. Dai, L. Pottier, P. Raghavan, Y. Robert, and M. Shantharam. *Co-scheduling Amdahl applications on cache-partitioned systems*. Research Report RR-9021. INRIA Grenoble - Rhone-Alpes ; ENS de Lyon, Feb. 2017, p. 33.

[R4] G. Aupy, A. Benoit, L. Pottier, P. Raghavan, Y. Robert, and M. Shantharam. *Co-scheduling algorithms for cache-partitioned systems*. Research Report RR-8965. INRIA Grenoble - Rhone-Alpes ; ENS de Lyon, Nov. 2016, p. 28.

[R5] A. Benoit, L. Pottier, and Y. Robert. *Resilient application co-scheduling with processor redistribution*. Research Report RR-8795. INRIA Grenoble - Rhone-Alpes ; ENS de Lyon, Oct. 2015.

Internships

2016 (3 months) **Research intern**, *Argonne National Laboratory*, Chicago, USA. I have been working with Swann Perarnau on scheduling and data management problems for the new many-core architectures that exhibit new memory hierarchies, such as Xeon Phi Knights Landing.

2015 (6 months) **Intern**, *École Normale Supérieure de Lyon*, Lyon, France. I have worked on scheduling problems and on algorithms for detecting and correcting errors, under the supervision of Yves Robert and Anne Benoit in the research team ROMA.

2013 (3 months) **Intern**, *Institut de Recherche pour le Développement (IRD)*, Sète, France. The aim was to process GPS data from fishing boats (one record every minutes in average). The data to be processed was consistent (more than one million lines). The final goal was to make a « dashboard » to represent data with a GIS (Geographic Information System).

Teaching

2017 – 2018 Master – Parallel algorithms (22h, University of Lyon)

	Master – Distributed algorithms (10h, University of Lyon)
	Bachelor – Programming 1 (32h, ENS de Lyon)
2016 – 2017	Bachelor – ASR2: Advanced Computer Architecture and Network (32h, ENS de Lyon)
	Bachelor – Programming 1 (32h, ENS de Lyon)
2015 – 2016	Master – Image Processing and Computational Geometry (20h, ENS de Lyon)
	Bachelor – ASR1 : Computer Architecture and Network (6h, ENS de Lyon)
	Bachelor – ALGO2 : Advanced Algorithms (32h, ENS de Lyon)

Languages skills

French	**Native.**	English	**Proficient.**
Italian	**Conversational.**		

Computer skills

Scientific tools	C, C++, Python, R, Bash, LaTeX.	Parallelism	OpenMP, MPI, CUDA.

Collectives responsibilities

2017-2018 Elected representative for non-tenured members at the LIP (ENS Lyon computer science laboratory) council, co-organized a two-days seminar for PhD students.

References

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