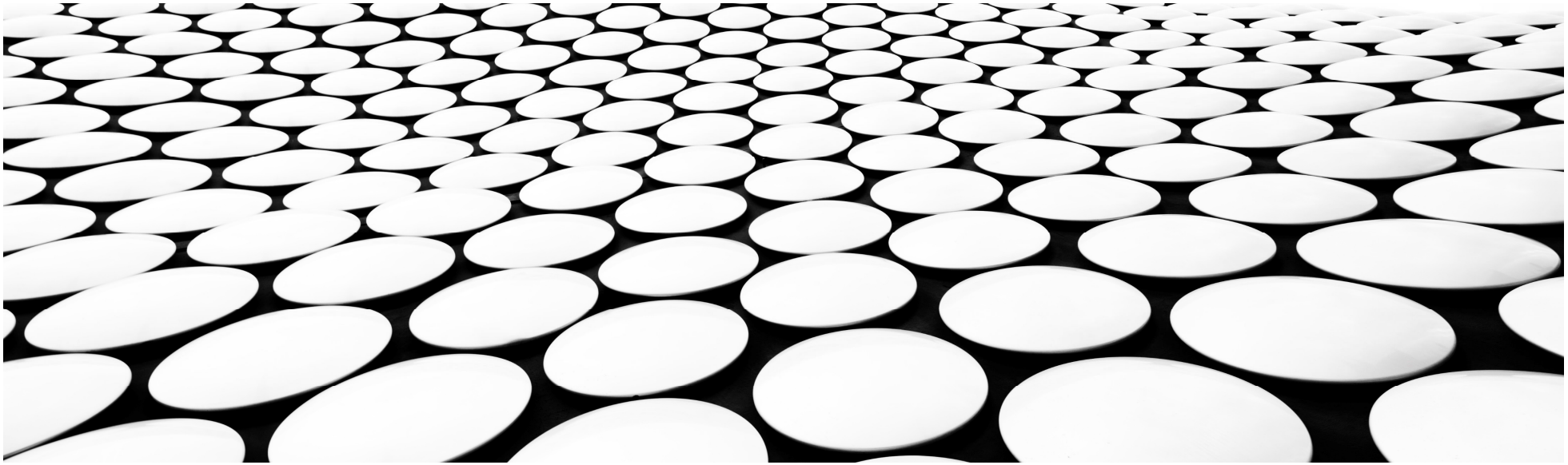
ĐẠI HỌC QUỐC GIA THÀNH PHỐ HỒ CHÍ MINH
TRƯỜNG ĐẠI HỌC KHOA HỌC TỰ NHIÊN
KHOA ĐIỆN TỬ - VIỄN THÔNG

THIẾT KẾ VI MẠCH ĐIỆN TỬ

EXCERSISES

LÊ ĐỨC HÙNG



EXERCISES

1. Find x_p, x_n, x_d, ψ_0, C_{j0}, C_j for an applied voltage of -4V of a pn diode with a step junction, N_A = $5x10^{15}/cm^3$, N_D = $10^{20}/cm^3$, and an area of 10μm by 10μm.
2. N_A = $5x10^{15}/cm^3$, N_D = $10^{20}/cm^3$, D_N = $20cm^2/s$, D_P = $10cm^2/s$, L_N = 10μm, L_P = 5μm, A = $10\mu m^2$. Calculate the saturation current of pn junction.
3. Using LTSPICE, sketch I_D-V_{DS} characteristic of NMOS and PMOS (V_{GS} steps from 1V, 2V, 3V, 4V, 5V) for each following transistor sizes: W/L = 10μm/10μm, W/L = 10μm/1μm, W/L = 1μm/10μm, W/L = 1μm/1μm.
4. Using LTSPICE, sketch I_D-V_{GS} characteristic of NMOS and PMOS (V_{DS} steps from 1V, 2V, 3V, 4V, 5V) for each following transistor sizes: W/L = 10μm/10μm, W/L = 10μm/1μm, W/L = 1μm/10μm, W/L = 1μm/1μm.
5. Using LTSPICE, sketch R_{ON}-V_{GS} characteristic of NMOS and PMOS with the following transistor sizes: W/L = 50μm/1μm, W/L = 10μm/1μm, W/L = 5μm/1μm, W/L = 1μm/1μm.

EXERCISES

6. Consider an NMOS process technology for which $L_{min} = 0.4mm$, $t_{ox} = 8nm$, $m_n = 450cm^2/Vs$, $V_t = 0.7V$.

a) Find C_{ox} and k'_n.

b) For a MOSFET with $W/L = 8mm/0.8mm$, calculate the values of v_{OV}, v_{GS}, and v_{DSmin} needed to operate the transistor in the saturation region with dc current $I_D = 100mA$.

c) For the device in (b), find the values of v_{OV} and v_{GS} required to cause the device to operate as a 1kΩ resistor for very small v_{DS}.

7. Consider an NMOS transistor fabricated in an $0.18\mu m$ process with L = $0.18\mu m$ and W = $2\mu m$. The process technology is specified to have $C_{ox} = 8.6fF/\mu m^2$, $m_n = 450cm^2/Vs$, and $V_{tn} = 0.5V$.

a) Find V_{GS} and V_{DS} that result in the MOSFET operating at the edge of saturation with $I_D = 100\mu A$.

b) If V_{GS} is kept constant, find V_{DS} that results in $I_D = 50\mu A$.

c) To investigate the use of the MOSFET as a linear amplifier, let it be operating in saturation with $V_{DS} = 0.3V$. Find the change in i_D resulting from v_{GS} changing from $0.7V$ by $+0.01V$ and $-0.01V$.

EXERCISES

8. An inverter is designed with $(W/L)_n = 10$ and $(W/L)_p = 16$, which is fabricated in a process where $K'_n = 110\mu A/V^2$, $V_{T0n} = 0.7V$, $K'_p = 50\mu A/V^2$, $V_{T0p} = -0.7V$.
   a) Calculate the middle point voltage of the inverter V_I, V_{IH}, V_{IL}. Make sure that $V_{IL} < V_I < V_{IH}$. Use LTSPICE to sketch V_{in}-V_{out} function waveform, and Voltage Transfer Characteristic (VTC) curve.
   b) Adjust $(W/L)_n$ and $(W/L)_p$ so that the the middle point voltage is at the center of VTC. Use LTSPICE to sketch V_{in}-V_{out} function waveform, and Voltage Transfer Characteristic (VTC) curve.
9. Calculate the middle point voltage V_I, of NAND-2 and NOR-2 with $(W/L)_n = 5$ and $(W/L)_p = 8$, which is fabricated in a process where $K'_n = 110\mu A/V^2$, $V_{T0n} = 0.7V$, $K'_p = 50\mu A/V^2$, $V_{T0p} = -0.7V$. Use LTSPICE to sketch Voltage Transfer Characteristic (VTC) curve of NAND2 and NOR2.

EXERCISES

10. Calculation all of the inverter characteristics with the information provided.

PMOS Parameters	NMOS Parameters
L = 1μm, W = 7μm	L = 1μm, W = 5μm
V_{Tn} = 0.7V, K'_n = 110μA/V^2	V_{Tp} = -0.8V, K'$_p$= 50μA/V^2
C_{j0} = 2.82x10^{-8}F/cm^2, ϕ_o = 0.9V	C_{j0} = 4.85x10^{-8}F/cm^2, ϕ_o = 0.92V
C_{jsw} = 4.62x10^{-12}F/cm, ϕ_{osw} = 0.95V	C_{jsw} = 1.95x10^{-12}F/cm, ϕ_{osw} = 0.97V
Oxide thickness: t_{ox} = 150 Amstrong	
Gate overlap: L_0 = 0.05μm	
Power supply: V_{DD} = 5V	
Fanout number: FO = 3	

EXERCISES

11. Calculation of setup time and hold time. Are there any violations of Setup time and Hold time?