Project Laboratory 2A Semester One Circuit Report

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Contents

I. Introduction

1.1 Aims

The aim of this report is to explain the operation of the Speech Amplifier Circuit (SAC) along with its derived component values. The report also tackles the operation and component derivations of the auxiliary Automatic Gain Control Circuit (AGCC). The purpose of the full circuit is to amplify a low-current speech signal in order for it to be digitised and recorded on a computer processor. Additionally, the AGCC allows for output regulation by boosting low input signals and attenuating large ones. All of these objectives are accomplished at a low cost.

1.2 Full Circuit Interaction

The full circuit is comprised of four sub-circuits that ultimately output to a Speech Digitizer and Recorder. The first of these is the Microphone Circuit, which outputs two out-of-phase voltages from a speech signal input. These output voltages are then fed into a differential stage where they are each amplified whilst remaining out-of-phase by $180°$. Then, they are fed into a Differential Operational Amplifier (DOA), which ultimately acts as a signal adder to produce a single-ended output. As this output is being fed into the Analog-to-Digital Converter (ADC) to be sampled for recording, it is also fed into the AGC which responds by modulating V_{Bias} (a gain-setting component in the first amplification stage) to attenuate large signals and boost small ones, with the aim of producing a final output of near-constant amplitude regardless of input amplitude. Many parameters for these circuits were given in the referenced guide, but this report focuses solely on the component values designed by the user. Brief explanations on the circuits' operations are also given [1,3,4].

II. Circuit Design

2.1 Speech Amplifier Circuit

2.1.1 Microphone Circuit

The first sub-circuit is the Microphone Circuit, which draws a 170uA DC current and can output a maximum of 3uA AC; the Mic assembly contains two plates which act as capacitors; when a signal is inputted into the microphone, one of the plates will vibrate, effectively changing its charge at a fixed voltage, and thus producing a current. The Mic is connected to two 9.1kΩ resistors (total of 18.2kΩ) - one above, and one below - to obtain two large, out-of-phase voltages [1]. These voltages are fed into the Transistor Amplifier Circuit through capacitors which set the high-pass cutoff frequency. These were selected using the RC High-Pass Filter equation with a desired cutoff frequency of 20Hz, which is the minimum for human hearing, and well below the typical 85Hz minimum of human speech [2]:
$X_c = \frac{1}{2\pi fC} \Rightarrow C = \frac{1}{2\pi f X_c} \Rightarrow C = \frac{1}{2\pi fR} \Rightarrow C = \frac{1}{2\pi(20)(9100)} \simeq 874nF$. A standard value 1uF Capacitor was chosen instead, which provides a lower cutoff frequency of 17.5Hz, just below human hearing. This lower high-pass cutoff frequency is acceptable as it is generally better to increase bandwidth.

2.1.2 Transistor Amplifier Circuit (CA-3083)

Note the symmetry in this circuit about Q3 which allows for calculations to be made on one side and mirrored (i.e, the theory and component values behind the operation of Q1 also apply to Q2). Transistor Q1 acts as an amplifier with Q3 as its current sink within the IC array; thus, Q3 sets the circuit's gain by limiting the current in Q1. Further, the current on Q3's collector is in turn set by V_{Bias} at its base, which is set to a maximum of 1V by the AGCC. V_{Bias} was selected as 1V since this is above the 0.55V required for Q3 to be fully saturated and in its linear region of operation and hence allows for room to decrease V_{Bias} for AGC [1,3]. Further, the 1V maximum is set due to the power supply restriction; Q1's Base Voltage must be higher than Q3's Collector by at least 0.6V(DC), but Q1s Collector is limited by the 5V supply; thus, if Q3's Base (and hence Q1's Base through Q3's Collector) is made too high, then Q1's Collector may dip below its Base during the input's negative AC cycle, which will chop the signal by turning Q1 off at that interval.

I_{Bias}'s maximum value was recommended to be around 1mA to meet the power consumption specification, so this was set using R_E on Q3's emitter with $R_E = \frac{V_{bias}-0.6}{I_{bias}} = 400\Omega$, the standard value of 390Ω was chosen instead, which creates an I_bias of 1.03mA, which is acceptable as it is well-within component tolerances [1]. Further, Resistor R_{B1} is used to set the base voltage on Q1. First, the minimum Base Voltage for Q1 was found by examining the components linked to each transistor base, beginning from the voltage drop across R_E; $V_{BQ_1} = V_{RE} + V_{ECQ_3} + V_{EBQ_1} = 0.4V + 0.25V + 0.6V = 1.25V$, so this voltage drop was set with a potential divider between the given 6.8kΩ resistor and R_{B1} with respect to the 5V power supply; $V_{BQ_1} = \frac{5(6800)}{6800 + R_{B1}} \Rightarrow R_{B1} = \frac{5(6800)}{1.25} - 6800 = 20400\Omega$. A standard value of 20kΩ was chosen, giving a slightly higher base voltage for Q1, which is fine since the calculated value was just a minimum [1].

On the circuit's output to the DOA, resistor R_{C1} sets the DC bias and ultimately also sets the gain for each half of the Differential Stage. Note that R_{C1} must be low enough to set a voltage of at least 0.2 between Q1's Collector and Emitter, whilst remaining high enough to prevent too large of a DC bias, which would cause the amplified input signal to hit the 5V supply rail on every positive cycle, leaving only a half-cycle signal. R_{C1} is chosen based on the selected I_{Bias} of 1mA and the expected voltage drop across R_{C1}; $V_{R_{C1}} = 5V - V_{CEQ_1} - V_{CEQ_3} - V_{R_E} = 5V - 0.2V - 0.2V - 0.39V = 4.21V$. Further, from Kirchhoff's Law, note that $I_C = \frac{I_{Bias}}{2}$. Hence, $R_{C1} = \frac{V_{RC1}}{I_C} = \frac{4.21V}{0.5mA} = 8.42k\Omega$. A resistor of 8.2kΩ was chosen as this would drive the collector voltage higher, keeping the circuit within parameters of operation. Finally, it is ideal for R_{C1} to be large as it influence the gain of this stage as given by $Gain = g_m R_{C1},\ where\ g_m = \frac{I_C}{V_T},\ and\ V_T \simeq 25mV,\ although\ V_T$ is very volatile with temperature changes [1].

2.1.3 Operational Amplifier Circuit (MCP6271)

The out-of-phase Differential Stage outputs are fed into the Differential Amplifier, where they are subtracted from each other, and thus combined into one single-ended output, where the additional AC gain is set by R_F and R_{C1}. Given that the gain in the previous stage was set by $R_{C1}g_m$, then the overall AC gain of both stages is $\frac{R_F}{R_C}R_C g_m,\ where\ R_C$ is cancelled out, and the overall gain is hence described by $R_F g_m$ [1]. Note that the required second-stage gain is minimal, as most of the amplification will have been set in the previous stage, and any additional gain would amplify electrical noise. Thus, the Op-Amp Gain, set by $\frac{R_F}{R_C}$ is aimed at around 1.2, as per the recommendation of the Laboratory supervisor. Further, it is selected with the value of R_F in mind, as this will be doubled in order to create a potential divider which DC-biases the output at 2.5V to allow for positive-only outputs [1]. Hence, $R_F = 1.2R_C = 1.2(8200) = 9840\Omega$. A standard value of 10kΩ was chosen as per the need for $2R_F$.

Finally, a Low-Pass filter with a 3kHz cutoff frequency is implemented in this stage to limit the final output signal to the human speech frequency range, and to conform with the Analog-to-Digital Converter's 4kHz maximum reading frequency [1]. Hence, capacitor C_F was chosen using $C_F = \frac{1}{2\pi fR} \Rightarrow C_F = \frac{1}{2\pi(3000)(10000)} \simeq 5.3nF$. The standard value of 5.6nF was chosen as this produces a cutoff at around 2.8kHz, which somewhat limits the Band-Pass and may dampen certain phonetics like "P" and "K", but this is preferable to the 4.7nF alternative which would produce a cutoff at 3.4kHz, and may lead to a malfunction of the ADC Circuit.

2.2 Automatic Gain Control Circuit (BC557 - PNP)

The final sub-circuit is the Automatic Gain Control Circuit, which was built and tested successfully. It is fed from the Operational Amplifier Output and modulates V_{Bias} to try and create a constant final output amplitude regardless of input amplitude. Hence, V_{Bias} is automatically decreased to attenuate output, and increased to boost it. The AGC Circuit operates mainly as a trough-detector with a fast attack and slow decay [3]. The PNP-Transistor-based AGC Circuit was chosen, as it doesn't require a diode or an additional Op-Amp like the alternative, and it also uses a leftover Q5 Transistor within the Transistor array. Thus, it is potentially cheaper, and less prone to failure due to component tolerances.

When V_{Out} falls, this fall is translated through the 1uF capacitor, ultimately bringing down the PNP's Base Voltage. The Emitter's 10uF capacitor will attempt to hold $V_{Emitter}$ constant, causing a sharp rise in $V_{Base\ to\ Emitter}$, and turning the PNP fully ON, where it can be treated as a near-short-circuit. This will lead the 10uF capacitor to quickly discharge into the 470Ω resistor, causing a fast fall in V_{Bias}, as given by the time constant $470\Omega \times 10\mu F = 0.0047sec$ [3].

When V_{Out} rises, this rise is translated through the 1uF capacitor, ultimately increasing the PNP's base voltage. The Emitter's 10uF capacitor will attempt to hold $V_{Emitter}$ constant, causing a sharp fall in $V_{Base\ to\ Emitter}$, and turning the PNP fully OFF, where it can be treated as a near-open-circuit. This will lead the 10uF capacitor to slowly charge up to the supply voltage through the 47kΩ resistor, causing a slow rise in V_{Bias}, as given by the time constant $47k\Omega \times 10\mu F = 0.47sec$ [3].

The only user-designed component here is the Potential Divider which sets the PNP's Base Voltage, which sets the maximum V_{Bias}; The maximum target voltage is 1V, as decided earlier [1,3]. Hence, noting that the power supply is at 5V, $1 = 5\frac{R_2}{R_1+R_2} \Rightarrow R_1 = 4R_2$. It was advised by the tutors to simply pick an R_2 value that would multiply nicely into R_1 whilst allowing for some further tuning with a potentiometer, R_3. Hence $R_2 = 10k\Omega$, $R_1 = 39k\Omega$, and $R_3 = 0 \Leftrightarrow 1k\Omega$.

III. Circuit Testing

During testing, the microphone was disconnected, and the top 9.1kΩ Resistor was disconnected from the 5V supply, and instead connected to a grounded Signal Generator Output with a switch-activated -40dB attenuation [1]. All measured values are with no AGC unless specified, and the set V_{Bias} is 1V. This setup was also simulated on LTSPICE for comparison purposes. The experimental input signal had a peak-to-peak voltage of 0.11V for all cases, except during AGC testing, where numerous voltage inputs were required to test AGC response. For qualitative testing, the circuit is connected to the PCB as per the provided instructions, and a set of speech inputs is recorded, and they are then played back for assessment [4].

3.1 Speech Amplifier Circuit

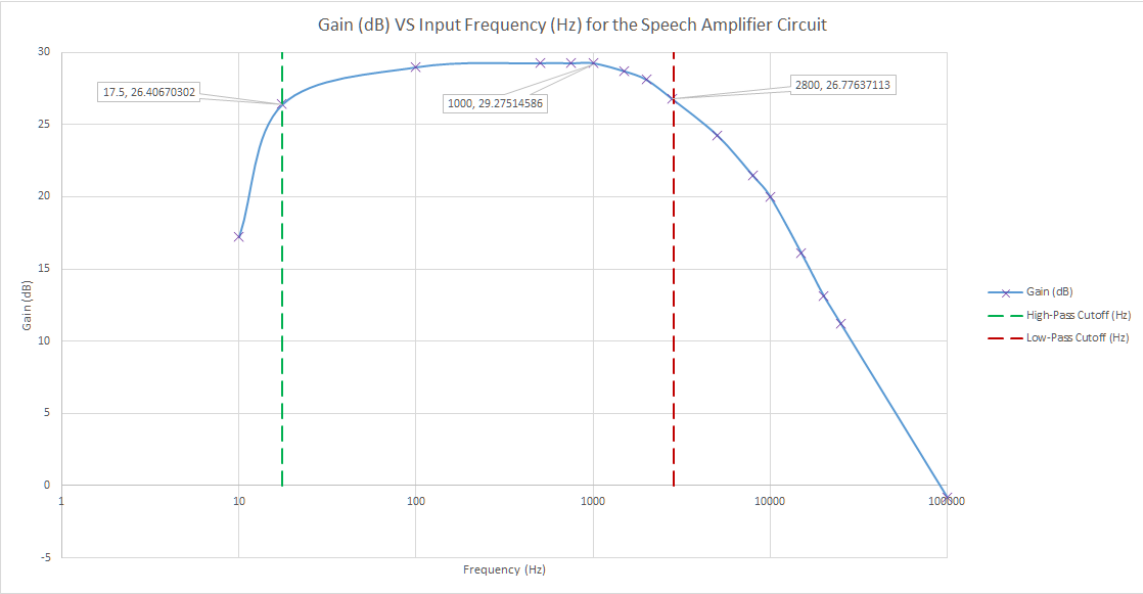
3.1.1 Outputs from Q1 and Q2 (Disconnected from Operational Amplifier)

First, the Transistor Amplifiers were optimized by ensuring the same Base Voltage for both Q1 and Q2, this was done by splitting one of the 6.8kΩ resistors used in the potential divider into one 6.2kΩ resistor, and one 1KΩ potentiometer in series, as per the lab guide. V_{Bias} was also set to 1V using a similar setup connected to the supply rail. The optimization was verified by measuring the base voltages of each to ensure that they were the same. Then, the outputs were each measured and found to be out-of-phase by 180°, with a peak-to-peak voltage difference of only 15mV. This sub-circuit's operation was then further verified by confirming the 17.5Hz cutoff frequency, as well as a varying gain with a changing V_{Bias} [1].

3.1.2 Operational Amplifier Circuit

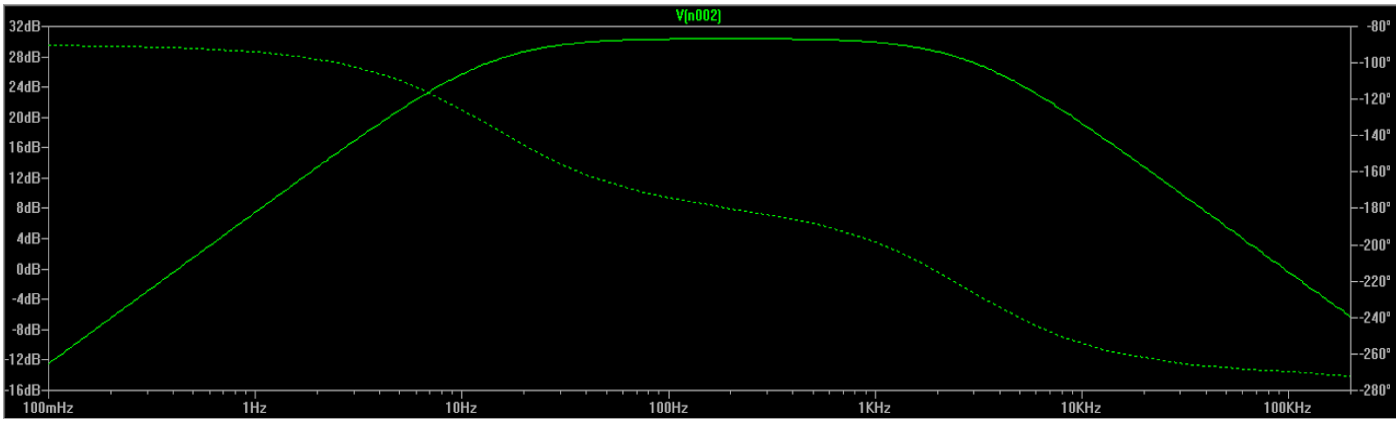
Here, the outputs from the previous circuit were fed into the Op-Amp, as described in the design section of this report. The output was measured against a constant Signal-Generator input with a 0.11V peak-to-peak voltage. A Bode Plot was created from this data, and was compared to the simulated LTSPICE Circuit data.

Figure 1: Experimental Gain VS Input Frequency for the Speech Amplifier Circuit



As per the above graph, the attenuation found at the theoretical high-pass cutoff was 2.87dB (4.3% lower than expected), meaning that the cutoff frequency was, in practice, lower than 17.5Hz. Similarly, the attenuation found at the theoretical low pass cutoff was 2.49dB (16.7% lower than expected), meaning that the cutoff frequency was in fact higher, which is, in retrospect, a good thing. Note that these differences can be accounted for by component tolerances, as well as inherent inaccuracy of measurements when reading from an oscilloscope. The maximum Gain was found to be 29.275dB from approximately 150Hz to 1800Hz. Note that values below 10Hz were not recorded, as these were impossible to trigger with the provided oscilloscopes. Further, values above 100kHz were also excluded from the plot as they did not provide any new information, and would only make the graph harder to read.

Figure 2: Theoretical (LTSPICE) Gain VS Input Frequency for the Speech Amplifier Circuit

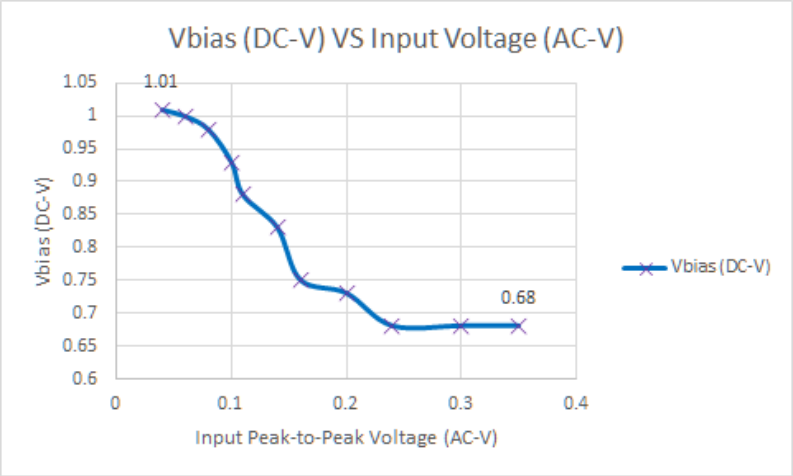


The simulation serves as a benchmark for comparison as it behaves perfectly on all fronts, including bandwidth and maximum overall gain. The maximum gain was found to be 30.405, as opposed to the experimental 29.275, which is almost 1.13dB lower. In linear terms, this means that the theoretical circuit amplifies the signal 1.16 times more than what was found experimentally. A 16% dip in real performance is reasonable, especially considering component tolerances, measurement inaccuracy and the various factors which affect transistor operation, notably temperature.

3.2 Automatic Gain Control Circuit

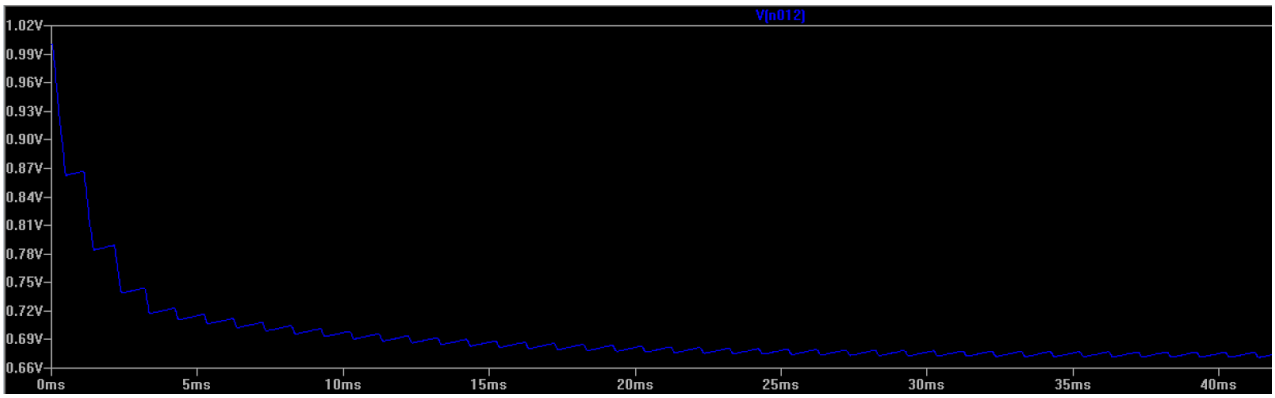
The AGC Circuit was found to perform extremely well, with its V_{Bias} variations matching closely to the simulated circuit, and its minimum value converging to, and never deceeding 0.68V (which is above the 0.55V required for Q3's linear operation). Further, the maximum theoretical V_{Bias} of around 1V was also achieved in both the simulation and the real circuit, as expected.

Figure 3: Experimental V_{Bias} VS Input Voltage



the LTSPICE data was acquired by inputting 0.5V (peak-to-peak) into the simulation; the focus in this comparison is the maximum value, as well as the minimum value for V_{Bias}, which is why it wasn't necessary to mimic the exact data collection process used in measurement-based plot.

Figure 4: Theoretical (LTSPICE) V_{Bias} VS Time for a Large Input Voltage (0.5V Peak to Peak)



Note that the theory also predicts a maximum V_{Bias} of around 1V (before the large input has been registered) and a minimum of 0.67V (after it has been registered). This is in line with the measured results. As for Qualitative Analysis, it was evident that the AGC Circuit improved recording quality, as my test involved loud iterations, as well as soft iterations of the word "test", where both iterations came out at almost the same volume during playback, with the only difference being my tone of voice. The circuit did not pick up many ambient sounds, and the sound was adequately clear, considering how inexpensive the microphone is.

IV. Conclusion

The circuit was successfully built and tested with Automatic Gain Control. Although the maximum linear gain was found to be 16% lower than expected, and the experimental cutoff frequencies were different than expected, the circuit ultimately performed well, considering the various component tolerances and the circuit's inherent weakness to temperature changes, which may have arisen during prolonged operation. It is also noteworthy that the low-pass cutoff was higher than expected (>2.8kHz) in practice, restoring the bandwidth closer to what was originally intended with the design and improving quality. To further prove this point, the results from the Qualitative Analysis of assessing the recording playback were very encouraging; the circuit did not register many ambient noises, and my speech input was mostly clear, clipping only if I spoke very loudly into the microphone. High-frequency phonetics were also adequately registered. Further, the AGCC was found to work extremely well, as the playback for loud and soft inputs was nearly identical in volume.

Aside from measuring Gain in the Bode Plot, it would not have been useful to identify the phase or gain margin for this circuit, as the output is never directly fed back to the input; technically, the AGC circuit does influences the input gain as a form of "feedforward", but this does not cause worries of unstable operation.

V. Bibliography

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VI. LTSPICE Circuit Diagram

Figure 5: Full LTSPICE Circuit Diagram