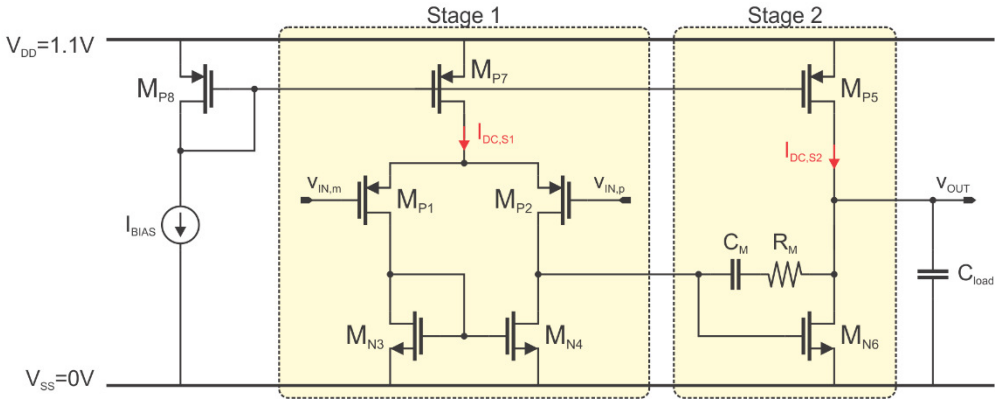
Analog Electronic Circuits – 2015-2016
Design Project Report

1. Group data

Group number	8
Name – Student 1	Gauthier Duchêne
Name – Student 2	Nathan Dwek
Name – Student 3	Sacha Maes

2. Circuit Schematic



3. Performance summary

Metric	Units	Specification	Matlab	Spectre
C_{load}	pF	50		
DC gain	dB	48	52.53	51.86
f_{GBW}	MHz	70	82.72	84.69
Phase margin	°	>60	83.78	90.78
Output swing	V	>0.8	0.871	0.866
Dominant pole	kHz		195.4	191
Input common mode range	V		0.688	0.724
Current consumption ($I_{DC,S1}$+ $I_{DC,S2}$)	A		1.89m	2.02m
FoM (f_{GBW}.C_{load}/($I_{DC,S1}$+ $I_{DC,S2}$))	MHz.pF/mA	Maximize	2184.4	2094
(input-referred noise)	V_{rms}	Minimize	0.903m	1.3m

4. Device sizes and bias point parameters

Device	W [µm]	L [nm]	I_{ds} [µA]	$V_{overdrive}$ [V]	g_m [S]	g_{ds} [S]	g_m/g_{ds} [-]	$V_{ds,sat}$ [V]	V_{ds} [V]
M_{p1}	497	212	241	0.05	5.4m	119u	43.8	-0.055	-0.508
M_{p2}	497	212	241	0.05	5.4m	119u	43.8	-0.055	-0.508
M_{n3}	75.1	400	241	0.128	4.53m	162u	28.7	0.073	0.252
M_{n4}	75.1	400	241	0.128	4.53m	162u	28.7	0.073	0.252
M_{p5}	229	500	1540	-0.2	12.5m	364u	23.8	-0.182	-0.681
M_{n6}	493	132	1540	0.01	35m	1339u	33.6	0.05	0.418
M_{p7}	80.4	500	482	-0.2	3.9m	246u	15	-0.184	-0.338
M_{p8}	0.767	500	4.51	-0.194	38u	1.64u	23.16	-0.176	-0.434

Device	Units	Value
C_M	pF	10
R_M	Ω	213.6
I_{BIAS}	A	4.51u

5 Considerations Taken into Account for Device Sizing

Sizing of M_{n6} g_{m6} was chosen in order to bring p_2 further than GBW so that GBW is mainly determined by p_1. V_{ov6} was chosen very low based on output swing and power efficiency. L_6 was chosen as long as possible in order to get good intrinsic gain and linearity. It is limited by $W_6 < 500\,\mu m$ in order to limit parasitic capacitances. This limit is quickly reached since we need g_m and weak inversion at the same time. V_{ds6} was chosen a bit higher than $\frac{V_{DD}}{2}$, to have almost symmetric swing and to get a little more gain and linearity from the higher saturation.

Sizing of M_{p5} $i_{ds5} = i_{ds6}$. V_{ov5} was chosen low based on the output swing. $V_{ds5} = V_{ds6} - V_{DD}$. L_5 was chosen very long to have a current source as ideal as possible. To ensure matching and linearity, every transistor in the current mirror should have the same length. L_5 is thus limited by the width and the parasitic capacitances of any of M_{p_5}, M_{p_7}, M_{p_8}.

Sizing of M_{p1}, M_{p2} Those transistors should have the same sizing and biasing so that the pair is symmetric. g_m is chosen based on f_{GBW}. V_{ov} is chosen low based on power efficiency. $V_{db} = V_{gs_6}$. V_{gb} was chosen so that $|V_{ds}| > |V_{dsat}| \simeq |V_{ov}|$. L was chosen as long as possible to maximize intrinsic gain and linearity. It is limited by W. The same consideration as for M_{p6} stands.

Sizing of M_{n3}, M_{n4} Those transistors should have the same sizing and biasing so that the pair is symmetric. $i_{ds} = i_{ds1} = i_{ds2}$. $V_{ds} = V_{gs} = V_{gs_6}$. L was chosen very long to minimize g_{ds} and maximize linearity.

Sizing of M_{p7} $i_{ds7} = 2i_{ds1}$. $L_7 = L_5$ to reduce distortion within the current mirror. L was chosen long to have current sources as ideal as possible. $V_{gs_7} = V_{gs_5}$. $V_{ds7} = V_{sb2}$.

Sizing of M_{p8} $V_{gs_8} = V_{ds8} = V_{gs_5} = V_{gs_7}$. $L_8 = L_7 = L_5$ to reduce distortion within the current mirrors. i_{ds8} was chosen 100 times smaller than the smallest stage current, because M_{p8} should not contribute to the power consumption, since i_{ds8} is wasted current.

Sizing of C_m C_m was chosen 5 – 10 times smaller than C_L so that the Miller pole is the dominant one. On the one hand, a too large Miller capacitance would load the first stage too much to meet the spec on GBW. On the other hand, a too small Miller capacitance would load the transistor M_{n6} too much in order to meet the spec on A_v, if the spec on GBW is strictly respected.

Sizing of R_m The nulling Miller resistance was chosen in order to cancel the second pole of the OTA and thus increase its phase margin.

6 Simulation Results

6.1 Frequency Response

6.1.1 Final Design

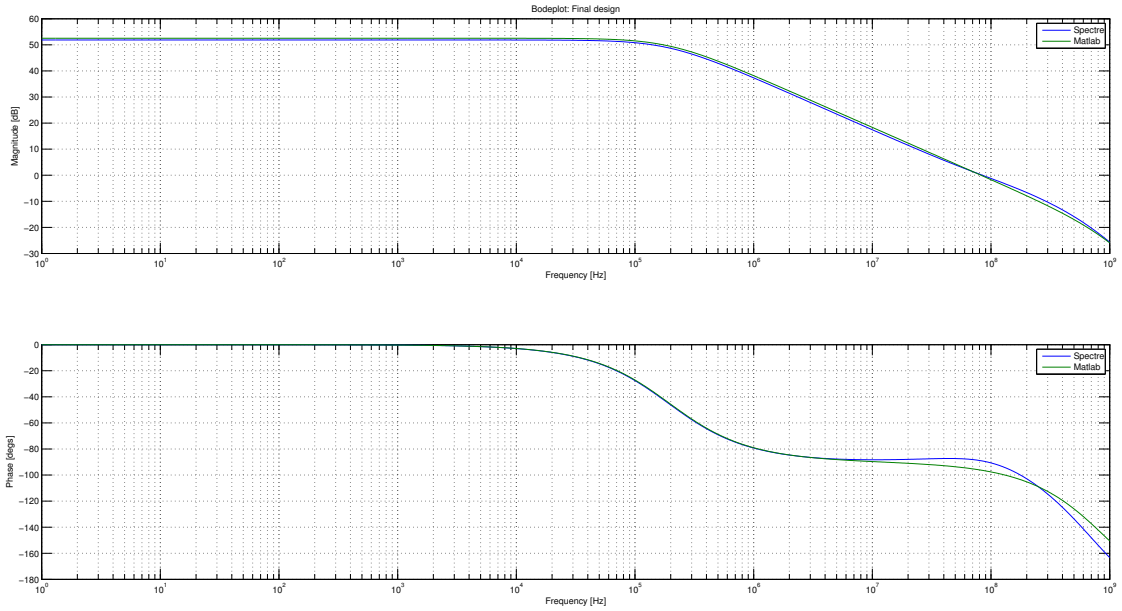


Figure 1: Bodeplots: final design

Figure 1 shows the bodeplots of the final OTA, as simulated by Matlab and Spectre. We observe that the matlab simulation was mostly accurate and that the design, as simulated Spectre seems to meet all the specs. We see however that Spectre shows that the Miller zero is a bit slower than the second stage pole, and that the next pole is a bit slower than predicted. This appears mostly on the phase graph, where we see that the phase rises up a little after the first pole, rather than staying flat. The phase then starts to decrease again at a lower frequency than was predicted using Matlab.

On figure 1, we read a phase margin of 90.78° as per Spectre and of 83.8° as per Matlab.

6.1.2 Effect of the Compensation Network

Figure 2 shows the effect of the compensation network. With no compensation, we see that the OTA becomes externally compensated: the dominant pole is set by the output node and depends on C_L. This increases f_{GBW} but degrades the phase margin a lot, since, as we can see on the phase graph, the next poles follow nearly immediately. The phase margin is reduced to 0.62° as per Spectre and to 2.88° as per Matlab. The bode curves differ between Matlab and Spectre, which is expected since parts of the Matlab simulation rely on the OTA being internally compensated.

With only the Miller capacitor, we see that the OTA becomes internally compensated, and the bodeplot before $f = 2\,\text{MHz}$ is satisfyingly shaped. However, the lack of nulling resistor means it is not possible to cancel the second pole in order to increase the phase margin and the

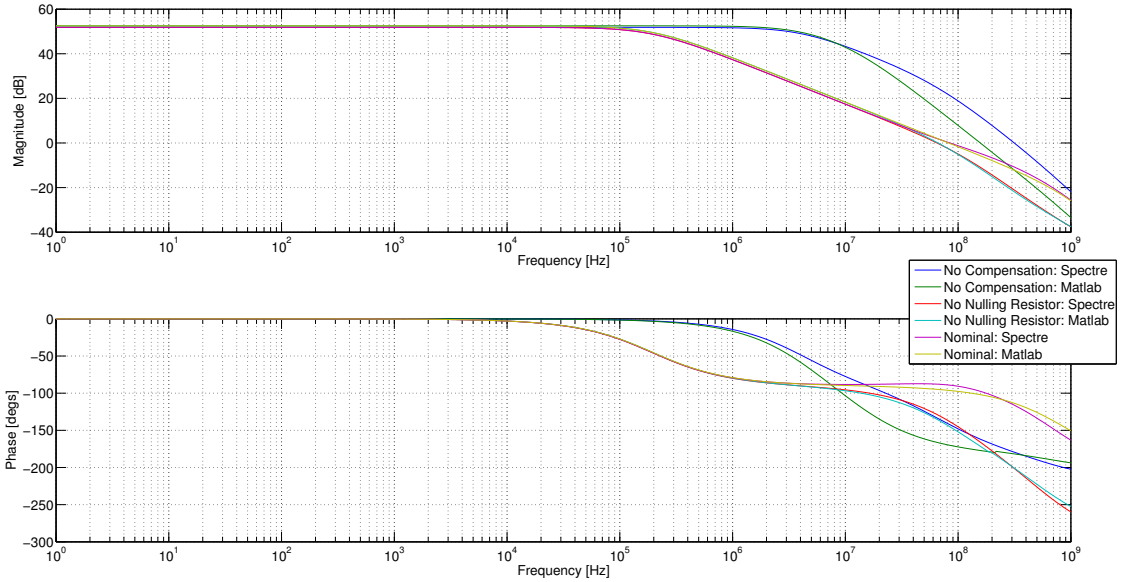


Figure 2: Bodeplots: effect of the compensation network

bandwidth in which the OTA behaves as a first order circuit. The phase margin is 51.5° as per Spectre and 44.1° as per Matlab.

With both the compensation capacitor and the compensation resistor, we come back on our final design, which was analyzed in 6.1.1.

6.1.3 Effect of the Load Capacitance

Figure 3 shows the effect of the load capacitance C_L. We see that it doesn't affect the frequency response before 2 – 4 MHz, which is normal since it doesn't appear in the DC gain, and since the OTA is internally compensated. With every parameter of the OTA fixed, decreasing C_L makes the second stage pole faster[1], which improves the high frequency response: the gain decreases at a slower rate and the phase margin is higher: 107.3° as per Spectre and 85.4° as per Matlab. Since the Miller zero does not move, its effect becomes very clear when the second stage pole is brought to higher frequencies.

Conversely, increasing C_L makes the second stage pole slower, which degrades the high frequency response: the gain decreases at a faster rate and the phase margin is lower: 80.0° as per Spectre and 82.2° as per Matlab.

In conclusion, we see that, as expected, the OTA works better as the load input impedance is closer to ideal, or in terms of transistor characteristics, as the next stage has a lower total parasitic capacitance. However, we also see that since the OTA is internally compensated, its frequency response is not impacted too much at the end of the day by a 50 % change on the load, which is a real advantage.

6.1.4 Effect of the Miller Capacitance

Figure 4 shows the effect of the Miller capacitance C_m. We see that it directly affects the f_{GBW}

[1] In first approximation, we have $p_1 = \frac{g_{m6}}{C_L}$

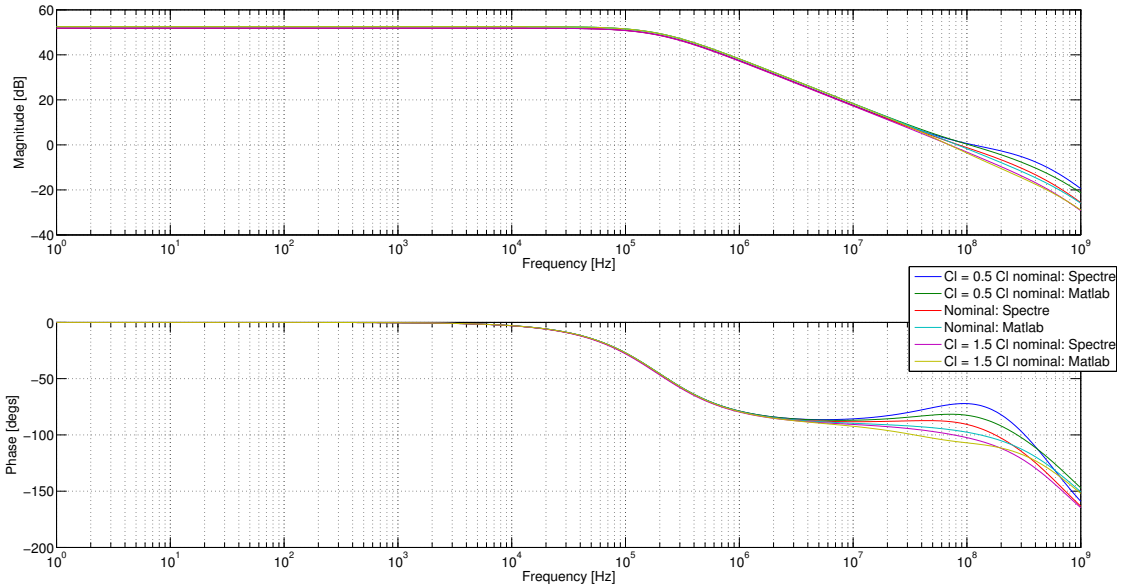


Figure 3: Bodeplot: effect of the load capacitance

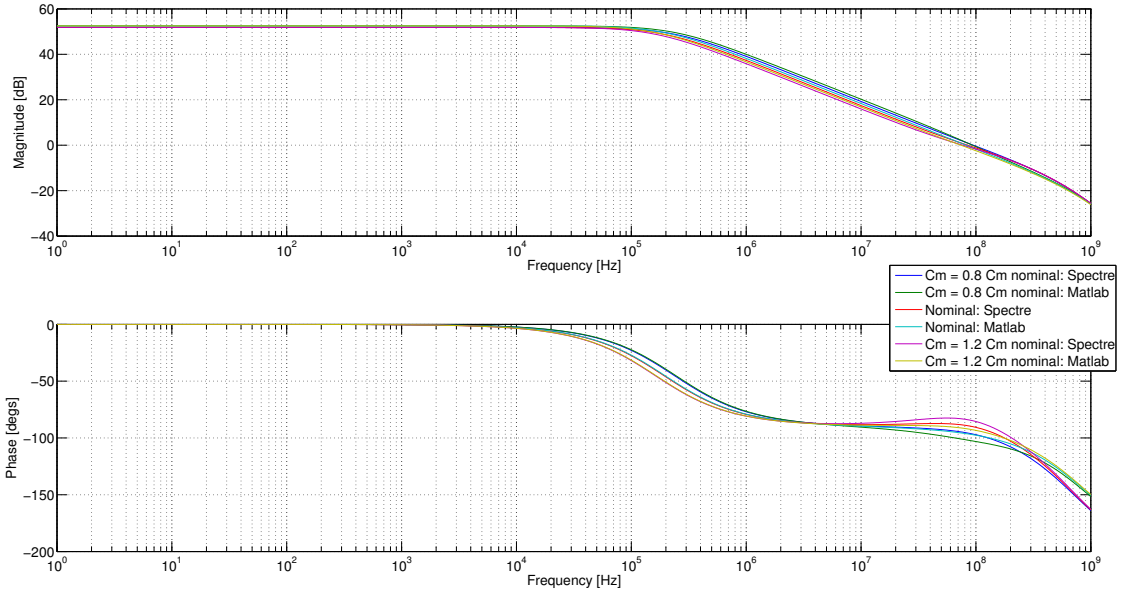


Figure 4: Bodeplots: Effect of the Miller Capacitance

which is expected since decreasing C_m brings the dominant pole to higher frequencies[2]. However, since the second stage pole is then left unchanged $\frac{p_1}{p_2}$ is reduced, and this leads to a degradation of the phase margin. With $C_m = 8\,\text{pF}$, the phase margin is 83.7° as per Spectre and 81.2° as per Matlab.

Conversely, increasing C_m reduces f_{GBW} and increases the phase margin: for $C_m = 12\,\text{pF}$, the phase margin is 96.7° as per Spectre and 85.3° as per Matlab. The effect of C_m is pretty direct to predict.

6.2 Noise and Large Signal Distortion

6.2.1 Input Noise Voltage

Figure 5 shows the input referred voltage noise power spectral density from 1 Hz to 100 GHz.

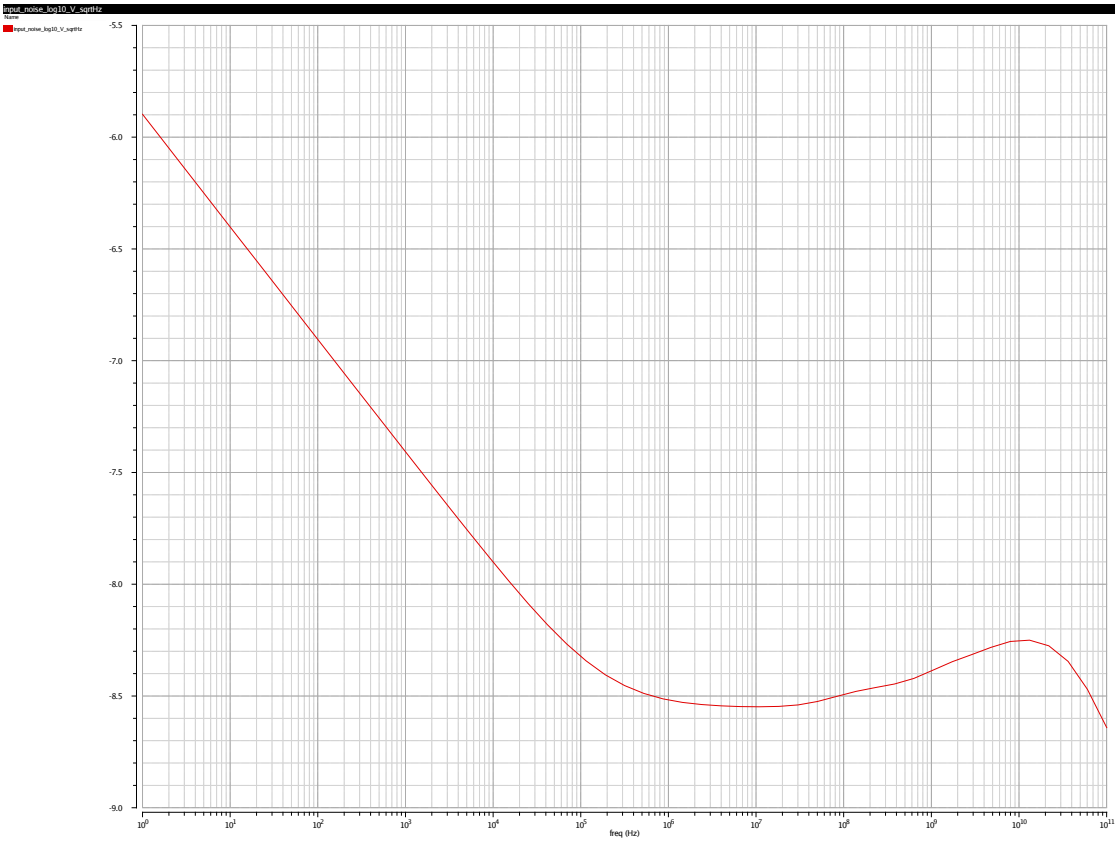


Figure 5: Input referred voltage noise power spectral density

The shape is easy to predict up to 10 GHz: if we consider a second order circuit affected by pink output noise, this shape can be produced when the turning point is between the first and second pole of the circuit or even if the turning point is after the two poles, as shown on the asymptotic magnitude plots of figure 6. The input noise dip at around 10 GHz is most probably due to higher order zeroes in the OTA as well as inaccuracies in the solver for such high frequencies.

[2] In first approximation, we have $p_2 = \frac{g_{m2}}{C_m}$

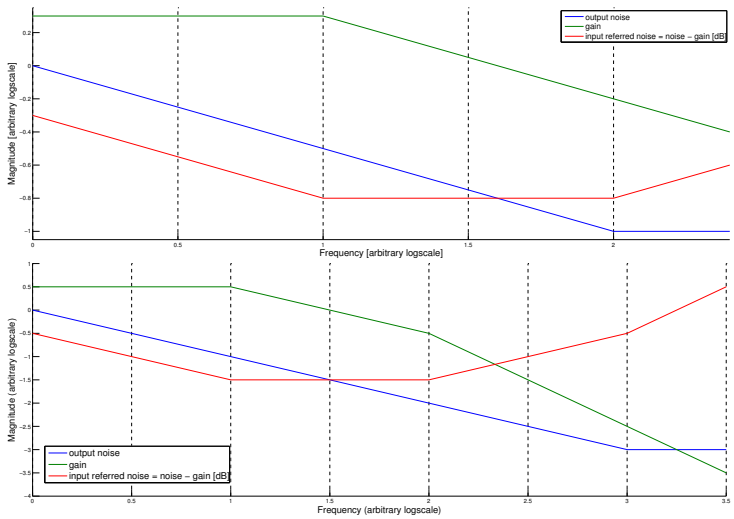


Figure 6: Asymptotic magnitude plot predicting the noise density shape (arbitrarily scaled)

6.2.2 Total Input Referred Noise Voltage

Table 1 shows the noise summary of the OTA and the top 10 contributors to the input voltage noise power integrated from 1 Hz to 100 GHz. We see that, as expected, the noise from the input stage is the dominant factor. At the output, the $^1/_f$ noise seems to dominate over the white noise. Additionally, the matlab simulation shows that at the input, the white noise is the dominant factor. This is due to the gain decrease at high frequencies, as we've explained in subsection 6.2.1.

6.2.3 Large Signal Distortion

Figure 7 shows the voltage gain and the output voltage as a function of the input signal amplitude. On the output voltage curve, we see that the operation is linear up until approximately 1 mV. We then observe significant distortion, until the output stage leaves saturation, at which point the output voltage is nearly unchanged by an increase in input voltage.

The voltage gain curve shows similar information. We read a 1-dB compression point of 1.18 mV.

Device	Param	Noise Contribution	% Of Total
/DUT/MP2	fn	0.0011608	39.71
/DUT/MP1	fn	0.00115934	39.61
/DUT/MN4	fn	0.000411413	4.99
/DUT/MN3	fn	0.000387043	4.41
/DUT/MN4	id	0.000323408	3.08
/DUT/MN3	id	0.000304224	2.73
/DUT/MP2	id	0.000297441	2.61
/DUT/MP1	id	0.000297087	2.60
/DUT/MP8	fn	6.55117e-05	0.13
/DUT/MP7	fn	5.25513e-05	0.08

Integrated Noise Summary (in V) Sorted By Noise Contributors
Total Summarized Noise = 0.00184217
Total Input Referred Noise = 0.00129607
The above noise summary info is for noise data

Table 1: Noise summary of the final OTA

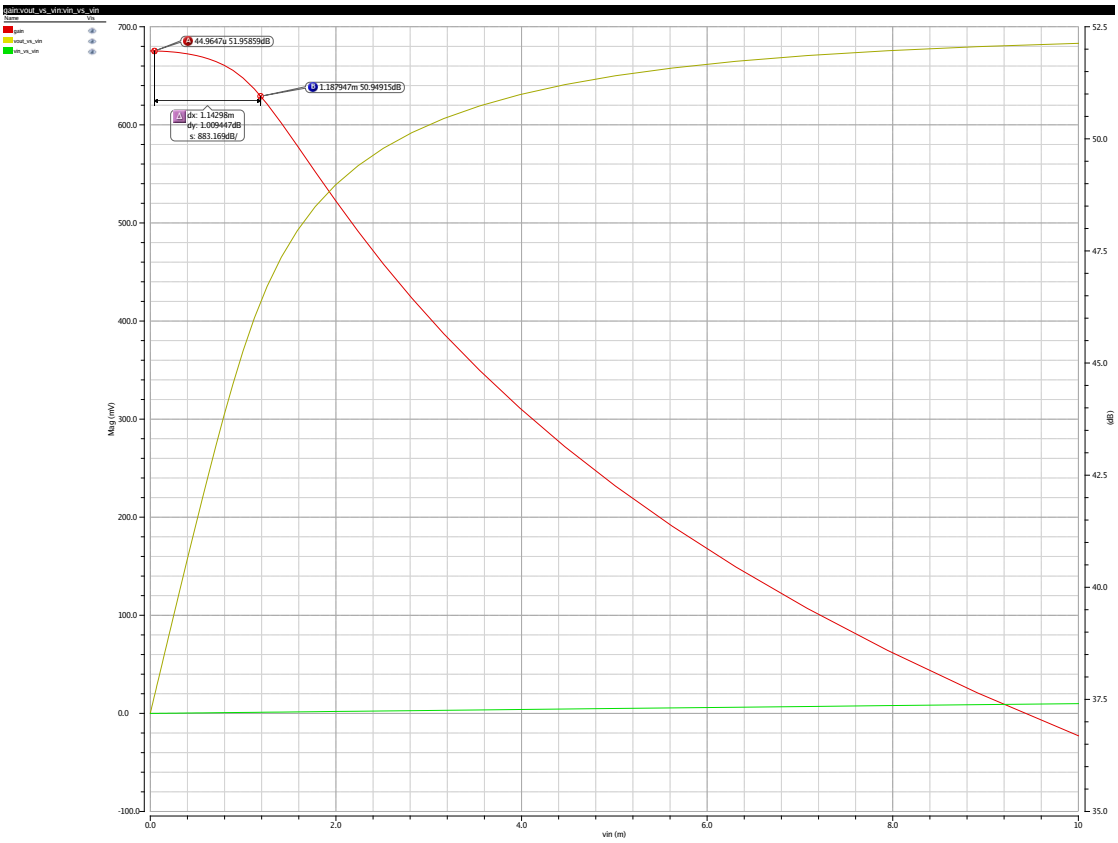


Figure 7: Large signal operation of the final OTA