Analog Electronics Circuits — 2015 – 2016
Design Project Report

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5 Considerations Taken into Account for Device Sizing

Sizing of M_{n6} g_{m6} was chosen in order to bring p_2 further than GBW so that GBW is mainly determined by p_1. V_{ov6} was chosen based on output swing and power efficiency. L_6 is chosen as long as possible in order to get good intrinsic gain and linearity. It is limited by $W_6 < 500\,\mu m$ in order to limit parasitic capacitances. V_{ds6} was chosen a bit higher than $\frac{V_{DD}}{2}$, to have almost symmetric swing and to get some more gain and linearity from the higher saturation.

Sizing of M_{p5} i_{ds5} was chosen based on i_{ds6}. V_{ov5} was chosen based on the output swing. $V_{ds5} = V_{ds6} - V_{DD}$. L_5 was chosen large to have a current source as ideal as possible. To ensure matching and linearity, every transistor in the current mirror should have the same length. L_5 is thus limited by the width and the parasitic capacitances of any of those transistors.

Sizing of M_{p_1}, M_{p_2} Those transistors should have the same sizing and biasing so that the pair is symmetric. g_m is chosen based on f_{GBW}. V_{ov} is chosen based on power efficiency. $V_{db} = V_{gs_6}$. V_{gb} was chosen so that $|V_{ds}| > |V_{dsat}| \simeq |V_{ov}|$. L was chosen based on intrinsic gain and linearity, and limited by W.

Sizing of M_{n3}, M_{n4} Those transistors should have the same sizing and biasing so that the pair is symmetric. $i_{ds} = i_{ds1} = i_{ds2}$. $V_{ds} = V_{gs} = V_{gs_6}$. L was chosen to minimize g_{ds} and maximize linearity.

Sizing of M_{p7} $i_{ds7} = 2i_{ds1}$. $L_7 = L_5$ to reduce distortion within the current mirror. L was chosen large to have current sources as ideal as possible. $V_{gs7} = V_{gs5}$. $V_{ds7} = V_{sb2}$.

Sizing of M_{p8} $V_{gs8} = V_{ds8} = V_{gs5} = V_{gs7}$. $L_8 = L_7 = L_5$ to reduce distortion within the current mirrors. i_{ds8} was chosen 100 times smaller than the smallest stage current, because M_{p8} should not contribute to the power consumption, since i_{ds8} is wasted current.

Sizing of C_m C_m was chosen 5–10 times smaller than C_L so that the Miller pole is the dominant one. On one hand, a large Miller capacitance would load too much the first stage. On the other hand, a small Miller capacitance would load the transistor M_{n6} too much.

Sizing of R_m The nulling Miller resistance was chosen in order to cancel the second pole of the OTA and thus increase its phase margin.