ALPHA RF TRANSCEIVER

ALPHA-TRX433S
ALPHA-TRX915S

- FM Transceiver Module
- Low cost, high performance
- Fast PLL lock time
- Wakeup timer
- 2.2V – 3.8V power supply First test @ 3V
- Low power consumption
- 10MHz crystal for PLL timing
- Clock and reset signal output for external MCU use
- 16 bit RX Data FIFO
- SPI interface
- Internal data filtering and clock recover
- Analog and digital signal strength indicator (ARSSI/DRSSI)
- Programmable TX frequency deviation (from 15 to 240 KHz)
- Programmable receiver bandwidth (from 67 to 400 kHz)
- Standby current less than 0.3uA
- Two 8 bit TX data registers
- High data rate up to 115.2 kbps
- Operates from -45 to +85^{O}C

Introduction

The Alpha Modules are extremely cost effective but high performance radio modules. Supplied in a miniature Surface mount package this Transceiver module can Transmit/Receive at up to 115Kbps at a maximum of 300m.

Operating at 2-5V, the module monitors its battery voltage and can sleep with very low standby current. The module can wake intermittently and provide direct control outputs to a microcontroller making it ideally suited to battery applications.

These Modules will suit one to one multi-node wireless links in applications including car and building security, POS and inventory tracking, remote process monitoring.

Part Numbers

Part Number	Description
ALPHA-TRX433S	FM Transceiver Module, preset to 433MHz
ALPHA-TRX868S	FM Transceiver Module, preset to 868MHz
ALPHA-TRX915S	FM Transceiver Module, preset to 915MHz

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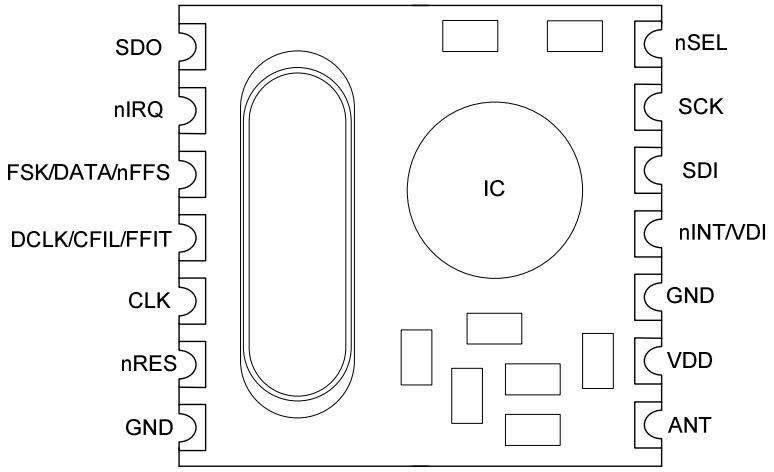
Pin Description



Pin	definition	Type	Function
11	nINT/VDI	DI/ DO	Interrupt input (active low)/Valid data indicator
9	VDD	S	Positive power supply
12	SDI	DI	SPI data input
13	SCK	DI	SPI clock input
8	ANT	IN	Antenna Connection
1	SDO	DO	Serial data output with bus hold
2	nIRQ	DO	Interrupts request output (active low)
3	FSK/DATA/nFFS	DI/DO/DI	Transmit FSK data input/ Received data output (FIFO not used)/ FIFO select
4	DCLK/CFIL/FFIT	DO/AIO/DO	Clock output (no FIFO)/ external filter capacitor(analog mode)/ FIFO interrupts(active high)when FIFO level set to 1, FIFO empty interruption can be achieved
5	CLK	DO	Clock output for external microcontroller
6	nRES	DIO	Reset Input (active low)
7, 10	GND	S	Power ground
14	nSEL	DI	Chip select (active low)

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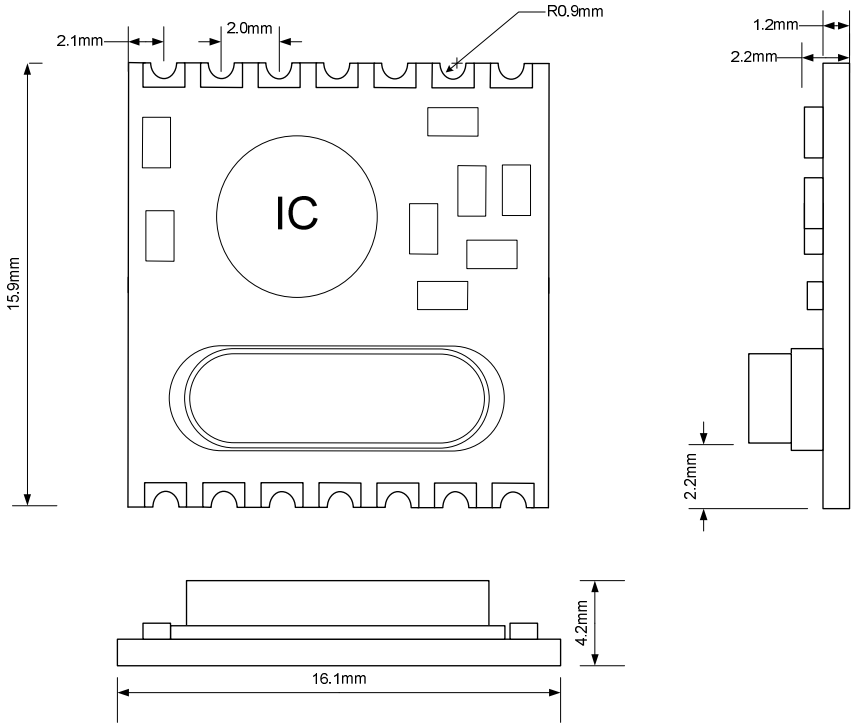
Mechanical Dimensions



Electrical Parameters

Maximum (not in working mode)

symbol	parameter	minimum	maximum	Unit
V_{dd}	Positive power supply	-0.5	6.0	V
V_{in}	All pin input level	-0.5	Vdd+0.5	V
I_{in}	Input current except power	-25	25	mA
ESD	Human body model		1000	V
T_{st}	Storage temperature	-55	125	□
T_{ld}	Soldering temperature(10s)		260	□

Recommended working range

symbol	parameter	minimum	maximum	Unit
V_{dd}	Positive power supply	2.2	3.8	V
T_{op}	Working temperature	-40	85	□

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DETAILED FEATURE-LEVEL DESCRIPTION

The Alpha transceiver Module is designed to cover the unlicensed frequency bands at 433, 868 and 915 MHz. The device facilitates compliance with FCC and ETSI requirements.
The receiver block employs the Zero-IF approach with I/Q demodulation, allowing the use of a minimal number of external components in a typical application. The Alpha transceiver Module incorporates a fully integrated multi-band PLL synthesizer, PA with antenna tuning, an LNA with switchable gain, I/Q down converter mixers, baseband filters and amplifiers, and an I/Q demodulator followed by a data filter.

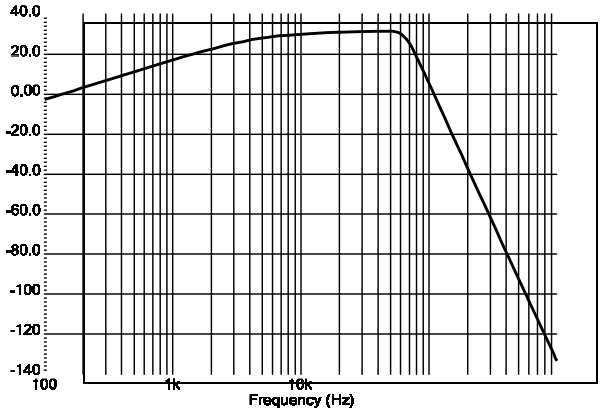
PLL

The programmable PLL synthesizer determines the operating frequency, while preserving accuracy based on the on-chip crystal-controlled reference oscillator. The PLL's high resolution allows the usage of multiple channels in any of the bands.

Baseband Filters

The receiver bandwidth is selectable by programming the bandwidth (BW) of the baseband filters. This allows setting up the receiver according to the characteristics of the signal to be received.
An appropriate bandwidth can be chosen to accommodate various FSK deviation, data rate and crystal tolerance requirements. The filter structure is 7th order Butterworth low-pass with 40 dB suppression at 2 · BW frequency. Offset cancellation is done by using a high-pass filter with a cut-off frequency below 7 kHz.

Full Baseband Amplifier Transfer Function
BW=67 kHz



Data Filtering and Clock Recovery

Output data filtering can be completed by an external capacitor or by using digital filtering according to the final application.

Digital operation: A digital filter is used with a clock frequency at 29 times the bit rate. In this mode, there is a clock recovery circuit (CR), which can provide synchronized clock to the data. Using this clock the received data can fill a FIFO. The CR has three operation modes: fast, slow, and automatic. In slow mode, its noise immunity is very high, but it has slower settling time and

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requires more accurate data timing than in fast mode. In automatic mode, the CR automatically changes between fast and slow mode. The CR starts in fast mode, then after locking, it automatically switches to slow mode

Data Validity Blocks

RSSI

A digital RSSI output is provided to monitor the input signal level. It goes high if the received signal strength exceeds a given pre-programmed level. The RSSI can be monitored by reading the status register.

DQD

The operation of the Data Quality Detector is based on counting the spikes on the unfiltered received data. High output signal indicates an operating FSK transmitter within baseband filter bandwidth from the local oscillator. DQD threshold parameter can be set by using the Data Filter Command.

AFC

By using an integrated Automatic Frequency Control (AFC) feature, the receiver can minimize the TX/RX offset in discrete steps, allowing the use of:

- Narrower receiver bandwidth (i.e. increased sensitivity)
- Higher data rate
- Inexpensive crystals

Crystal Oscillator

The Alpha transceiver Module has a single-pin crystal oscillator circuit, which provides a 10 MHz reference signal for the PLL.
The transceiver can supply a clock signal for the microcontroller; so accurate timing is possible without the need for a second crystal.
When the microcontroller turns the crystal oscillator off by clearing the appropriate bit using the Power Management Command, the chip provides a fixed number (192) of further clock pulses (“clock tail”) for the microcontroller to let it go to idle or sleep mode. If this clock output is not used, it is suggested to turn the output buffer off by the Power Management Command.

Low Battery Voltage Detector

The low battery detector circuit monitors the supply voltage and generates an interrupt if it falls below a programmable threshold level. The detector circuit has 50 mV hysteresis.

Wake-Up Timer

The wake-up timer has very low current consumption (1.5 µA typical) and can be programmed from 1 ms to several days with an accuracy of ±10%.
The wake-up timer calibrates itself to the crystal oscillator at every start-up. For proper calibration of the wake-up timer the crystal oscillator must be running before the wake-up timer is enabled. The calibration process takes approximately 0.5ms. For the crystal start up time (tsx).

Event Handling

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In order to minimize current consumption, the transceiver supports different power saving modes. Active mode can be initiated by several wake-up events (negative logical pulse on nINT input, wake-up timer timeout, low supply voltage detection, on-chip FIFO filled up or receiving a request through the serial interface).
If any wake-up event occurs, the wake-up logic generates an interrupt signal, which can be used to wake up the microcontroller, effectively reducing the period the microcontroller has to be active. The source of the interrupt can be read out from the transceiver by the microcontroller through the SDO pin.

Interface and Controller

An SPI compatible serial interface lets the user select the frequency band, centre frequency of the synthesizer, and the bandwidth of the baseband signal path. Division ratio for the microcontroller clock, wake-up timer period, and low supply voltage detector threshold are also programmable. Any of these auxiliary functions can be disabled when not needed. All parameters are set to default after power-on; the programmed values are retained during sleep mode. The interface supports the read-out of a status register, providing detailed information about the status of the transceiver and the received data.
The transmitter block is equipped with two 8-bit wide TX data registers. It is possible to write 8 bits into the register in burst mode and the internal bit rate generator transmits the bits out with the predefined rate. For further details, see the TX Register Buffered Data Transmission section.
It is also possible to store the received data bits into a FIFO register and read them out in a buffered mode.

Pin vs. Operation mode

Mode	Bit setting	Function	Pin 3	Pin 4
Transmit	El=0	Internal TX data register disabled	TX data	Not used
	El=1	Internal TX data register enabled	nFFS input (TX data register can be accessed)	
Receive	Ef=0	Receiver FIFO disabled	RX data	RX data clock output
	Ef=1	Receiver FIFO disabled	nFFS input (RX data FIFO can be accessed)	FFIT output **FIFO interrupt**

The *el* and *ef* bits can be found in the *Configuration Setting Command*. Bit *el* enables the internal TX data register. Bit *ef* enables the FIFO mode.

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DC characteristic

symbol	parameter	Remark	minimum	typical	maximum	Unit
$I_{dd\_TX\_0}$	Supply current (TX mode, P_{out} = 0dBm)	433MHz band 915MHz band		13 17		mA
$I_{dd\_TX\_PMAX}$	Supply current (TX mode, P_{out} = P_{max})	433MHz band 915MHz band		21 25		mA
I_{dd_RX}	Supply current (RX mode)	433MHz band 915MHz band		10 13		mA
I_x	Stand by current	Crystal and base band on		3□0	3□5	mA
I_{pd}	Sleep mode current	All blocks off		0.3		uA
I_{lb}	Low battery detection			0.5		uA
V_{lb}	Low battery step	0.1V per step	2.2		5.3	V
V_{lba}	Low battery detection accuracy			75		mV
V_{il}	Low level input				$0.3*V_{dd}$	V
V_{ih}	High level input		$0.7*V_{dd}$			V
I_{il}	Leakage current	V_{il}=0V	-1		1	uA
I_{ih}	Leakage current	$V_{ih}=V_{dd}$, V_{dd}=5.4V	-1		1	uA
V_{ol}	Low level output	I_{ol}=2mA			0.4	V
V_{oh}	High level output	I_{oh}=-2mA	V_{dd}-0.4			V

AC characteristic

symbol	parameter	remark	min	typical	max	Unit
f_{ref}	PLL frequency		8	10	12	MHz
f_{LO}	frequency (10MHz crystal used)	433 MHz band,2.5KHz step 915 MHz band,7.5KHz step	430.24 900.72		439.75 929.27	MHz
f_{LO}	frequency (8MHZ crystal used)	433 MHz band,2.5KHz step 915 MHz band,7.5KHz step	344.19 720.57		351.80 743.41	MHz
f_{LO}	frequency (12MHZ crystal used)	433 MHz band,2.5KHz step 915 MHz band,7.5KHz step	3516.28 1080.8		527.71 1115.1	MHz
BW	Receiver bandwidth	1 2 3 4 5 6	60 120 180 240 300 360	67 134 200 270 350 400	75 150 225 300 375 450	KHz
t_{lock}	PLL lock time	After 10MHz step hopping, frequency error <10 kHz		20		us
BR	Data rate	With internal digital	0.6		115.2	kbp

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		demodulator				s
BR_A	Data rate	With external RC filter			256	kbps
		BW=134KHz,BR=1.2kbps,433MHz band		-106	-100	
		BW=134KHz,BR=1.2kbps,915MHz band		-102	-95	
AFC_{range}	AFC working range	df_{FSK} FSK deviation in the received signal		0.8* df_{FSK}		
RS_A	RSSI accuracy			±5		dB
RS_R	RSSI range			46		dB
C_{ARSSI}	ARSSI filter			1		nF
RS_{STEP}	RSSI programmable step			6		dB
RS_{RESP}	DRSSI response time	RSSI output high after valid , CARRSI=5nF		500		us

AC characteristic (Transmitter)

symbol	parameter	remark	min	typical	max	Unit
		433MHz band	3	5		
		915MHz band	-2	0		
P_{out}	Typical output power	Selectable in 3 dB steps	P_{max}-21		P_{max}	dbm
C_o	Output capacitance (set by the automatic antenna tuning circuit)	In low bands In high bands	2 2.1	2.6 2.7	3.2 3.3	pf
Q_o	Quality factor of the output capacitance	In low bands In high bands	13 8	15 10	17 12	
L_{out}	Output phase noise	100 kHz from carrier 1 MHz from carrier			-75 -85	dbc/HZ
BR	FSK bit rate				256	kbps
df_{fsk}	FSK frequency deviation	Programmable in 15 kHz steps	15		240	kHZ

AC characteristic (Turn-on/Turnaround timings)

symbol	parameter	remark	min	typical	max	Unit
T_{st}	Crystal oscillator start-up time	Crystal ESR < 100			5	ms
$T_{tx\_rx\_XTAL\_ON}$	Transmitter - Receiver turnover time	Synthesizer off, crystal oscillator on		450		us
$T_{rx\_tx\_XTAL\_ON}$	Receiver - Transmitter turnover time	Synthesizer off, crystal oscillator on		350		us

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$T_{tx\_rx\_SYNT\_ON}$	Transmitter - Receiver turnover time	Synthesizer on, crystal oscillator on		425		us
$T_{rx\_tx\_SYNT\_ON}$	Receiver - Transmitter turnover time	Synthesizer on, crystal oscillator on		300		us
C_{xl}	Crystal load capacitance	Programmable in 0.5 pF steps, tolerance+/- 10%	8.5		16	pf
t_{POR}	Internal POR timeout	After V_{dd} has reached 90% of final value			100	ms
t_{PBt}	Wake-up timer clock period	Calibrated every 30 seconds	0.96		1.05	ms
$C_{in, D}$	Digital input capacitance				2	pf
$t_{r, f}$	Digital output rise/fall time	15pF pure capacitive load			10	ns

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
C xl	Crystal load capacitance, see crystal selection guide	Programmable in 0.5 pF steps, tolerance ± 10%	8.5		16	pF
t POR	Internal POR timeout	After V dd has reached 90% of final value			100	ms
t PBt	Wake-up timer clock accuracy	Crystal oscillator must be enabled to ensure proper calibration at the start up.		± 10		%
C inD	Digital input capacitance				2	pF
t r , t f	Digital output rise/fall time	15 pF pure capacitive load			10	ns

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CONTROL INTERFACE

Commands to the transmitter are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g. bit 15 for a 16- bit command). Bits having no influence (don't care) are indicated with X. Special care must be taken when the microcontroller's built- in hardware serial port is used. If the port cannot be switched to 16-bit mode then a separate I/O line should be used to control the nSEL pin to ensure the low level during the whole duration of the command or a software serial control interface should be implemented. The Power-On Reset (POR) circuit sets default values in all control and command registers.
The receiver will generate an interrupt request (IT) for the microcontroller - by pulling the nIRQ pin low - on the following events:

- The TX register is ready to receive the next byte (RGIT)
- The RX FIFO has received the pre-programmed amount of bits (FFIT)
- Power-on reset (POR)
- RX FIFO overflow (FFOV) / TX register under run (RGUR)
- Wake-up timer timeout (WKUP)
- Negative pulse on the interrupt input pin nINT (EXT)
- Supply voltage below the pre-programmed value is detected (LBD)

FFIT and FFOV are applicable when the RX FIFO is enabled. RGIT and RGUR are applicable only when the TX register is enabled. To identify the source of the IT, the status bits should be read out.

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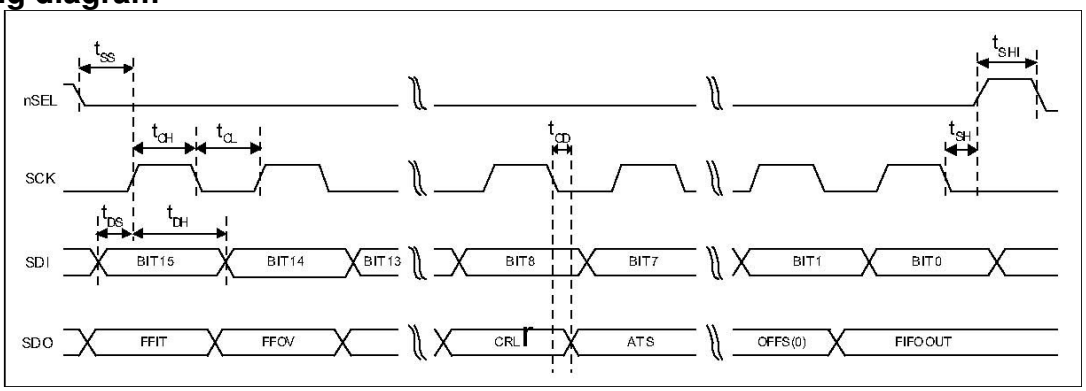
Timing Specification

Max 20 MHz

Symbol	Parameter	Minimum value [ns]
t	Clock high time	25
t	Clock low time	25
t	Select setup time (nSEL falling edge to SCK rising edge)	10
t	Select hold time (SCK falling edge to nSEL rising edge)	10
t	Select high time	25
t	Data setup time (SDI transition to SCK rising edge)	5
t	Data hold time (SCK rising edge to SDI transition)	5
t	Data delay time	10

Timing diagram



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Control Commands

	Control Command	Related Parameters/Functions	Related control bits
1	Configuration Setting Command	Frequency band, crystal oscillator load capacitance, RX FIFO and TX register enable	el, ef, b1 to b0, x3 to x0
2	Power Management Command	Receiver/Transmitter mode change, synthesizer, crystal oscillator, PA, wake-up timer, clock output enable	er, ebb, et, es, ex, eb, ew, dc
3	Frequency Setting Command	Frequency of the local oscillator/carrier signal	f11 to f0
4	Data Rate Command	Bit rate	cs, r6 to r0
5	Receiver Control Command	Function of pin 16, Valid Data Indicator, baseband bandwidth, LNA gain, digital RSSI threshold	p16, d1 to d0, i2 to i0, g1 to g0, r2 to r0
6	Data Filter Command	Data filter type, clock recovery parameters	al, ml, s, f2 to f0
7	FIFO and Reset Mode Command	Data FIFO IT level, FIFO start control, FIFO enable and FIFO fill enable, POR sensitivity	f3 to f0, sp, ff, al, dr
8	Synchron Pattern Command	Synchron pattern	b7 to b0
9	Receiver FIFO Read Command	RX FIFO read	
10	AFC Command	AFC parameters	a1 to a0, rl1 to rl0, st, fi, oe, en
11	TX Configuration Control Command	Modulation parameters, output power	mp, m3 to m0, p2 to p0
12	PLL Setting Command	CLK out buffer speed, dithering, PLL bandwidth	ob1 to ob0, ddit, dly, bw0
13	Transmitter Register Write Command	TX data register write	t7 to t0
14	Wake-Up Timer Command	Wake-up time period	r4 to r0, m7 to m0
15	Low Duty-Cycle Command	Enable and set low duty-cycle mode	d6 to d0, en
16	Low Battery Detector and Microcontroller Clock Divider Command	LBD voltage and microcontroller clock division ratio	d2 to d0, v3 to v0
17	Status Read Command	Status bit readout	

In general, setting the given bit to one will activate the related function. In the following tables, the POR column shows the default values of the command registers after power-on.

Control Register Default Values

	Control Register	Power-On Reset
1	Configuration Setting Command	8008
2	Power Management Command	8208
3	Frequency Setting Command	A680
4	Data Rate Command	C623
5	Receiver Control Command	9080
6	Data Filter Command	C22C
7	FIFO and Reset Mode Command	CA80
8	Synchron Pattern Command	CED4
9	Receiver FIFO Read Command	B000
10	AFC Command	C4F7
11	TX Configuration Control Command	9800
12	PLL Setting Command	CC77
13	Transmitter Register Write Command	B8AA
14	Wake-Up Timer Command	E196
15	Low Duty-Cycle Command	C80E
16	Low Battery Detector and Microcontroller Clock Divider	C000
17	Status Read Command	0000

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Configuration Setting Command

	2							8								
	0	0	1	0	0	1	0	1								
bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	0	0	0	0	0	el	ef	b1	b0	x3	x2	x1	x0	8008h

e l: Enable TX register
e f: Enable RX FIFO buffer

```
1010 = A for Tx REG
0110 = 6 for Rx REG
```

b1..b0: select band

b1	b0	band[MHz]
0	0	Reserved
0	1	433
1	0	868
1	1	915

x3..x0: select crystal load capacitor

x3	x2	x1	x0	load capacitor [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
1	1	1	0	15.5
1	1	1	1	16.0

```
x = b1000 : 12.5 pF
```

Power Management Command

													1	0	0	1	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	0	0	0	1	0	er	ebb	et	es	ex	eb	ew	dc	8208h

Bit	Function of the control bit	Related blocks
er	Enables the whole receiver chain	RF front end, baseband, synthesizer, crystal
ebb	The receiver baseband circuit can be separately	Baseband
et	Switches on the PLL, the power amplifier, and starts the transmission (If TX register is	Power amplifier, synthesizer, crystal oscillator
es	Turns on the synthesizer	Synthesizer
ex	Turns on the crystal oscillator	Crystal oscillator
eb	Enables the low battery detector	Low battery detector
ew	Enables the wake-up timer	Wake-up timer
dc	Disables the clock output (pin 8)	Clock output buffer

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The ebb, es, and ex bits are provided to optimize the TX to RX or RX to TX turnaround time.

The RF frontend consist of the LNA (low noise amplifier) and the mixer. The synthesizer block has two main components: the VCO and the PLL. The baseband section contains the baseband amplifier, low pass filter, limiter and the I/Q demodulator.

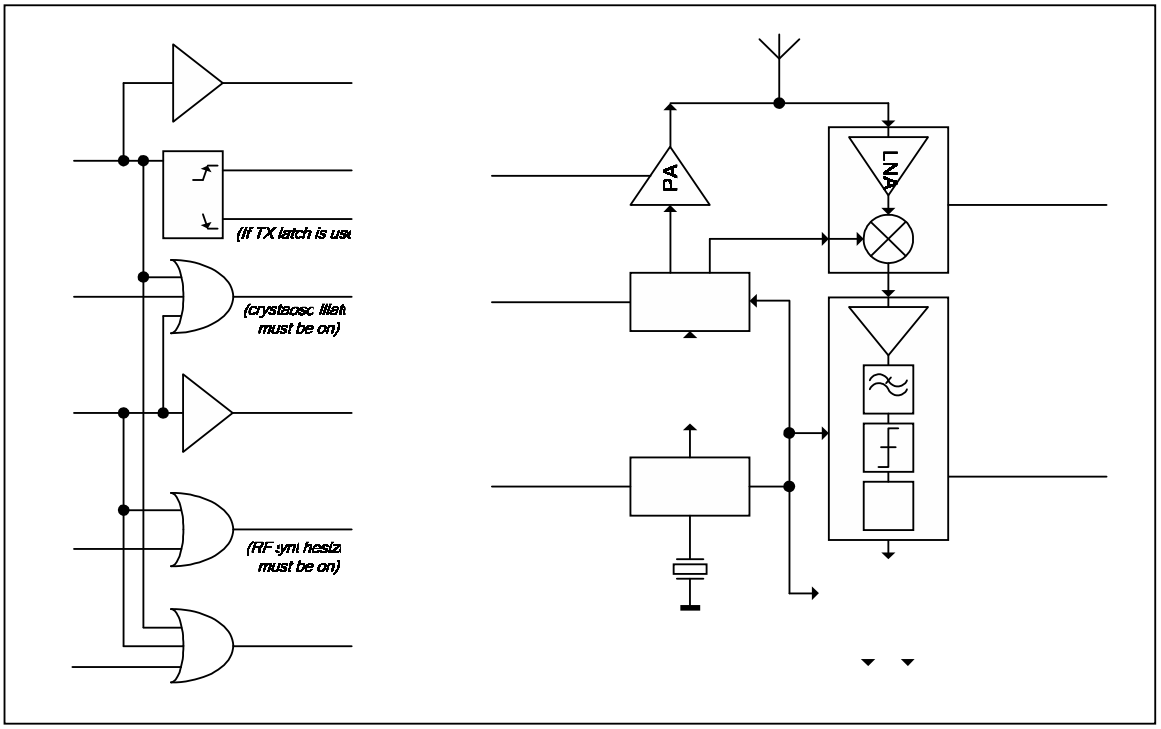
To decrease TX/RX turnaround time, it is possible to leave the baseband section powered on. Switching to RX mode means disabling the PA and enabling the RF frontend. Since the baseband block is already on, the internal start-up calibration will not be performed, the turnaround time will be shorter.

The synthesizer also has an internal start-up calibration procedure. If quick RX/TX switching needed it may worth to leave this block on. Enabling the transmitter using the et bit will turn on the PA, the synthesizer is already up and running. The power amplifier almost immediately produces TX signal at the output.

The crystal oscillator provides reference signal to the RF synthesizer, the baseband circuits and the digital signal processor part. When the receiver or the transmitter part frequently used, it is advised to leave the oscillator running because the crystal might need a few milliseconds to start. This time mainly depends on the crystal parameters.

It is important to note that leaving blocks unnecessary turned on can increase the current consumption thus decreasing the battery life.

Logic connections between power control bits:



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Note:

- If both et and er bits are set the chip goes to receive mode.
- FSK / nFFS input are equipped with internal pull-up resistor. To achieve minimum current consumption, do not pull this input to logic low in sleep mode.
- To enable the RF synthesizer, the crystal oscillator must be turned on
- To turn on the baseband circuits, the RF synthesizer (and this way the crystal oscillator) must be enabled. Leave synthesizer ON
- Setting the er bit automatically turns on the crystal oscillator, the synthesizer, the baseband circuits and the RF fronted.
- Setting the et bit automatically turns on the crystal oscillator, the synthesizer and the RF power amplifier.

Provide 1MHz clock (POR setting) to MCU

Clock tail feature: When the clock output (pin 8) used to provide clock signal for the microcontroller (dc bit is set to 0), it is possible to use the clock tail feature. This means that the crystal oscillator turn off is delayed, after issuing the command (clearing the ex bit)
192 more clock pulses are provided. This ensures that the microcontroller can switch itself to low power consumption mode. In order to use this feature, a Status Read Command must be issued before the ex bit set to zero. If status read was not performed then the clock output shuts down immediately leaving the microcontroller in unknown state.
Automatic crystal oscillator enable/disable feature: When an interrupt occurs, the crystal oscillator automatically turns on – regardless to the setting of the ex bit – to supply clock signal to the microcontroller. After clearing all interrupts by handling them properly (see the Interrupt Handling section) and performing Status Read Command, the crystal oscillator is automatically turned off. The clock tail feature provides enough clock pulses for the microcontroller to go to low power mode. Due to this automatic feature, it is not possible to turn off the crystal by clearing the ex bit if any interrupt is active. For example, after power on the POR interrupt must be cleared by a status read then writing zero to the ex bit will put the part into sleep mode. Very important to clear all interrupts before turning the ex bit off because the extra current required by running crystal oscillator can shorten the battery life significantly.
Disabling the clock output (bit dc=1) turns off both the clock tail and the automatic crystal oscillator enable/disable feature, only the
ex bit controls the crystal oscillator (supposing that both the er and et bits are cleared), the interrupts have no effect on it.

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Frequency Setting Command default = 868.32 MHz

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	A680h

The 12-bit parameter F (bits *f11* to *f0*) should be in the range of 96 and 3903. When F value sent is out of range, the previous value is kept. The synthesizer centre frequency f0 can be calculated as:

f0 = 10 · C1 · (C2 + F/4000) [MHz]

Band [MHz]	C1	C2
433	1	43
868	2	43
915	3	30

Band	Minimum	Maximum	PLL Frequency
433	430.2400 MHz	439.7575 MHz	2.5
868	860.4800 MHz	879.5150 MHZ	5.0
915	900.7200 MHz	929.2725 MHz	7.5

f11..f0: Set operation frequency:
433band: Fc=430+F*0.0025 MHz
868band: Fc=860+F*0.0050 MHz
915band: Fc=900+F*0.0075 MHz
Fc is carrier frequency and F is the frequency parameter. 36≤F≤3903

Data Rate Command default = approx. 9600 bps

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	1	0	cs	r6	r5	r4	r3	r2	r1	r0	C623h

r6..r0: Set data rate:
BR=10000000/29/□R+1□/□1+cs*7□

0x06 = 57600, 0x09 = 38400
0x0C = 28800, 0x12 = 19200
0x18 = 14400

The actual bit rate in transmit mode and the expected bit rate of the received data stream in receive mode is determined by the 7-bit parameter R (bits r6 to r0) and bit cs.

BR = 10000 / 29 / (R+1) / (1+cs · 7) [kbps]

In the receiver set R according to the next function:

R= (10000 / 29 / (1+cs · 7) / BR) – 1, where BR is the expected bit rate in kbps.

Apart from setting custom values, the standard bit rates from 600 bps to 115.2 kbps can be approximated with small error. Data rate accuracy requirements:

Clock recovery in slow mode: □BR/BR < 1/ (29 · N bit)

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Clock recovery in fast mode: □BR/BR < 3/ (29 · N bit)

BR is the bit rate set in the receiver and □BR is the bit rate difference between the transmitter and the receiver. Nbit is the maximum number of consecutive ones or zeros in the data stream. It is recommended for long data packets to include enough 1/0 and 0/1 transitions, and to be careful to use the same division ratio in the receiver and in the transmitter.

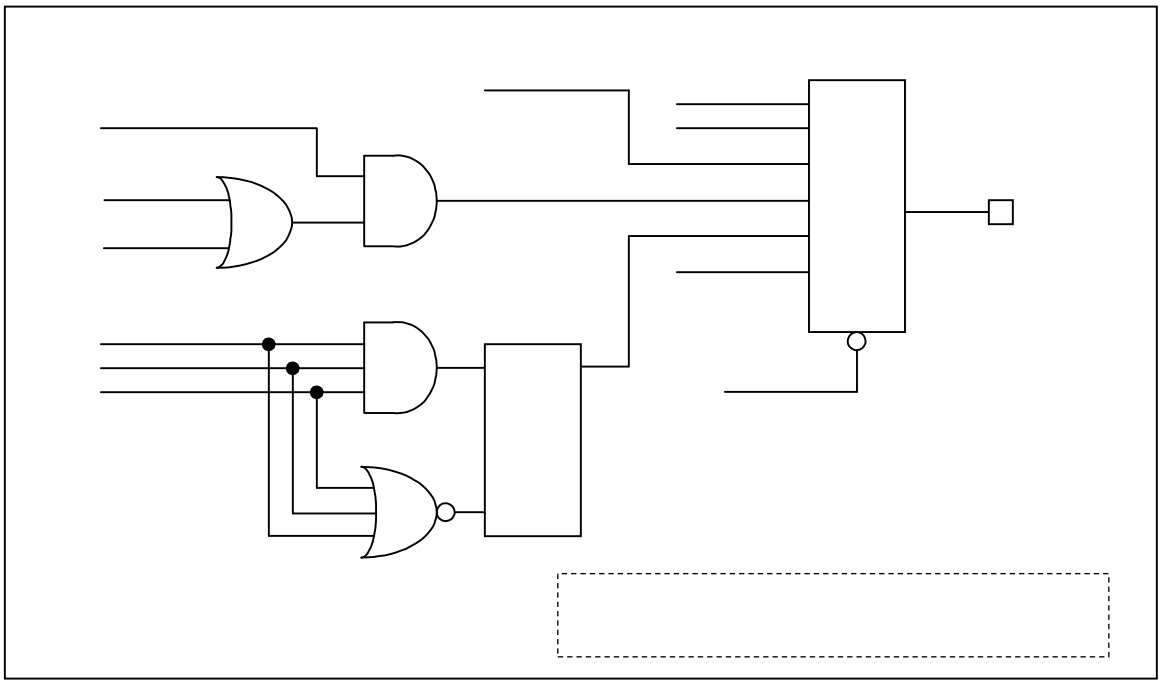
Receiver Control Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	1	0	P16	d1	d0	i2	i1	i0	g1	g0	r2	r1	r0	9080h

P16: select function of pin16

P16	Function of pin 16
0	Interrupt input
1	VDI output

VDI Logic diagram:



Slow mode: The VDI signal will go high only if the DRSSI, DQD and the CR_LOCK (Clock Recovery Locked) signals present at the same time. It stays high until any of the abovementioned signals present; it will go low when all the three input signals are low.

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Medium mode: The VDI signal will be active when the CR_LOCK signal and either the DRSSI or the DQD signal is high. The valid data indicator will go low when either the CR_LOCK gets inactive or both of the DRSSI or DQD signals go low.

Fast mode: The VDI signal follows the level of the DQD signal.

Always mode: VDI is connected to logic high permanently. It stays always high independently of the receiving parameters

Select receiver baseband bandwidth:

I2	i1	i0	Baseband Bandwidth [kHz]
0	0	0	reserved
0	0	1	400
0	1	0	340
0	1	1	270
1	0	0	200
1	0	1	134
1	1	0	67
1	1	1	reserved

Select VDI response time:

d1	d0	Response
0	0	Fast
0	1	Medium
1	0	Slow
1	1	Always on

Select LNA gain

g1	g0	LNA gain (dBm)
0	0	0
0	1	-6
1	0	-14
1	1	-20

Select DRSSI threshold

r2	r1	r0	$RSSI_{setth}$ [dBm]
0	0	0	-103
0	0	1	-97
0	1	0	-91
0	1	1	-85

Careful of the AFC range hysteresis (p. 25)

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1	0	0	-79
1	0	1	-73
1	1	0	Reserved
1	0	1	Reserved

The actual DRSSI threshold is related to LNA setup: $SSI_{th} = RSSI_{setth} + G_{LNA.}$

Data Filter Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	al	ml	1	s	1	f2	f1	f0	C22Ch

Bit 7 (al): Clock recovery (CR) auto lock control

1: auto mode: the CR starts in fast mode, after locking it switches to slow mode. Bit 6 (ml) has no effect.
0: manual mode, the clock recovery mode

is set by Bit 6 (ml) Bit 6 (ml): Clock recovery lock control

1: fast mode, fast attack and fast release (4 to 8-bit preamble (1010...) is recommended)
0: slow mode, slow attack and slow release (12 to 16-bit preamble is recommended)
Using the slow mode requires more accurate bit timing (see Data Rate Command).
Bit 4 (s): Select the type of the data filter:

s	Filter Type
0	Digital filter
1	Analog RC filter

Digital: This is a digital realization of an analog RC filter followed by a comparator with hysteresis. The time constant is automatically adjusted to the bit rate defined by the Data Rate Command.

Note: Bit rate cannot exceed 115 kpbs in this mode.

Analog RC filter: The demodulator output is fed to pin 7 over a 10 kOhm resistor. The filter cut-off frequency is set by the external capacitor connected to this pin and VSS.

The table shows the optimal filter capacitor values for different data rates

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Data Rate [kbps]	1.2	2.4	4.8	9.6	19.2	38.4	57.6	115.2	256
Filter Capacitor	12 nF	8.2 nF	6.8 nF	3.3 nF	1.5 nF	680 pF	270 pF	150 pF	100 pF

Note: If analog RC filter is selected the internal clock recovery circuit and the FIFO cannot be used.

Bits 2-0 (f2 to f0): DQD threshold parameter.

The Data Quality Detector is a digital processing part of the radio, connected to the demodulator - it is an indicator reporting the reception of an FSK modulated RF signal. It will work every time the receiver is on. Setting this parameter defines how clean incoming data stream would be stated as good data (valid FSK signal).

If the internally calculated data quality value exceeds the DQD threshold parameter for five consecutive data bits for both the high and low periods, then the DQD signal goes high.

The DQD parameter in the Data Filter Command should be chosen according to the following rules:

- The DQD parameter can be calculated with the following formula: DQD par = 4 x (deviation – TX-RXoffset) / bit rate
- It should be larger than 4 because otherwise noise might be treated as a valid FSK signal
- The maximum value is 7.

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FIFO and Reset Mode Command Using SYNCHON bytes for network identification

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	1	0	f3	f2	f1	f0	sp	al	ff	dr	CA80h

Bits 7-4 (f3 to f0): FIFO IT level. The FIFO generates IT when the number of received data bits reaches this level.

Bit 3 (sp): Select the length of the Synchron pattern:

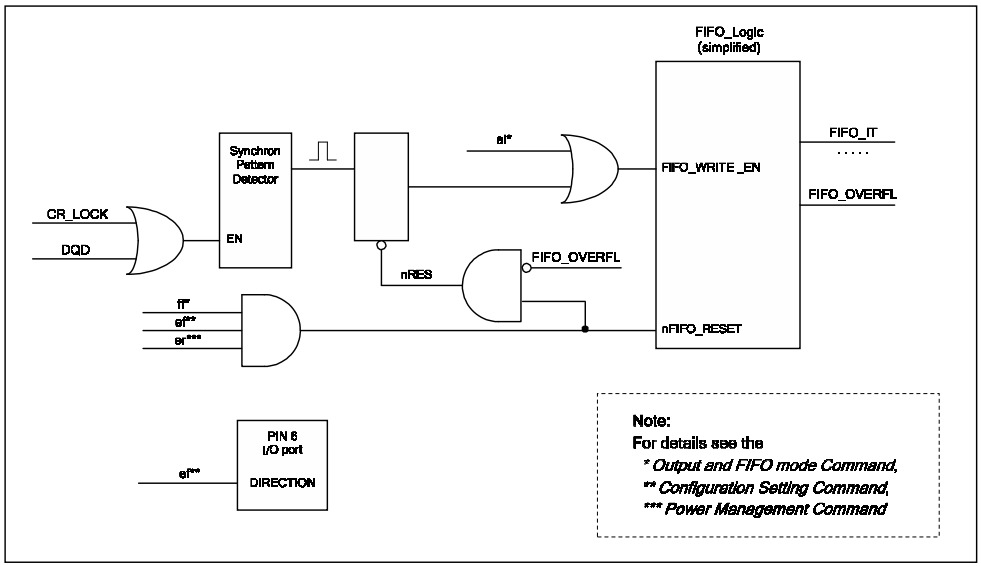
P	Byte 1	Byte0 (POR)	Synchron Pattern (Byte1+Byte0)
0	2D	D4	2DD4
1	Not used	D4	D4

Note: The synchron pattern consists of one or two bytes depending on the sp bit. Byte1 is fixed 2Dh, Byte0 can be programmed by the Synchron Pattern Command.

Bit 2 (al): Set the input of the FIFO fill start condition:

al	FIFO fill start
0	Synchron
1	Always

Fifo is filled once the last netID byte is received



Bit 1 (ff): FIFO fill will be enabled after synchron pattern reception. The FIFO fill stops when this bit is cleared. or if ef is cleared

Bit 0 (dr): Disables the highly sensitive RESET mode.

dr	Reset mode	Reset triggered when
0	Sensitive reset	V dd below 1.6V, V dd glitch greater
1	Non-sensitive	V dd below

Note: To restart the synchron pattern recognition, bit 1 (ef, FIFO fill enable) should be cleared and set.

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Synchron pattern Command

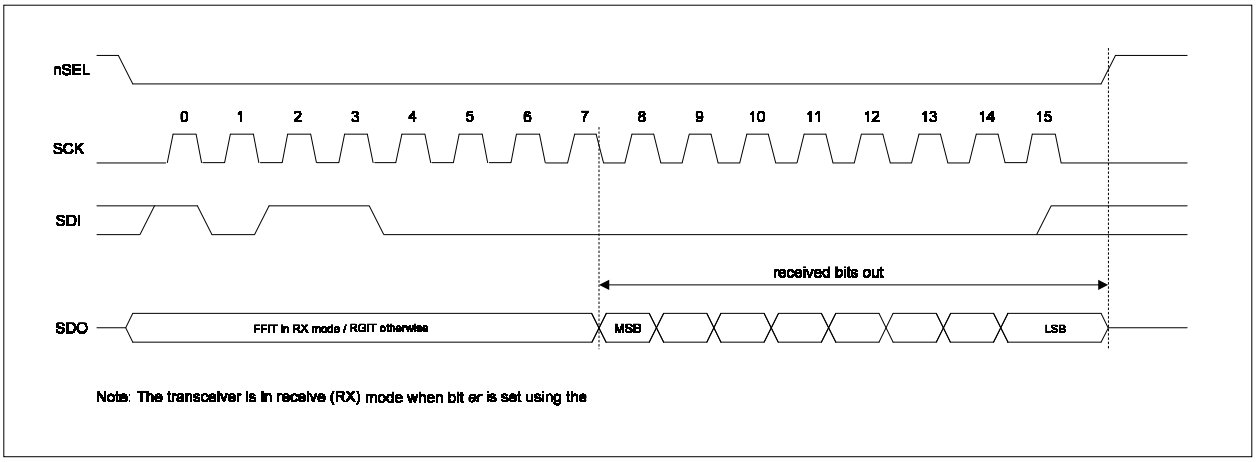
bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	1	0	b7	b6	b5	b4	b3	b2	b1	b0	CED4h

This command is used to reprogram the synchronic pattern; `netID`

Receiver FIFO Read Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	B000h

This command is used to read FIFO data when FFIT interrupt generated. FIFO data output starts at 8th SCK period.



Note: During FIFO access fSCK cannot be higher than fref /4, where f ref is the crystal oscillator frequency. When the duty-cycle of the clock signal is not 50 % the shorter period of the clock pulse width should be at least 2/fref .

AFC Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	0	0	a1	a0	rl1	rl0	st	fi	oe	en	C4F7h

Bit 7-6 (a1 to a0): Automatic operation mode selector:

a1	a0	Operation mode
0	0	Auto mode off (Strobe is controlled by microcontroller)
0	1	Runs only once after each power-up
1	0	Keep the f offset only during receiving (VDI=high)
1	1	Keep the f offset value independently from the state of the VDI signal

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Bit 5-4 (rl1 to rl0): Range limit. Limits the value of the frequency offset register to the next values:

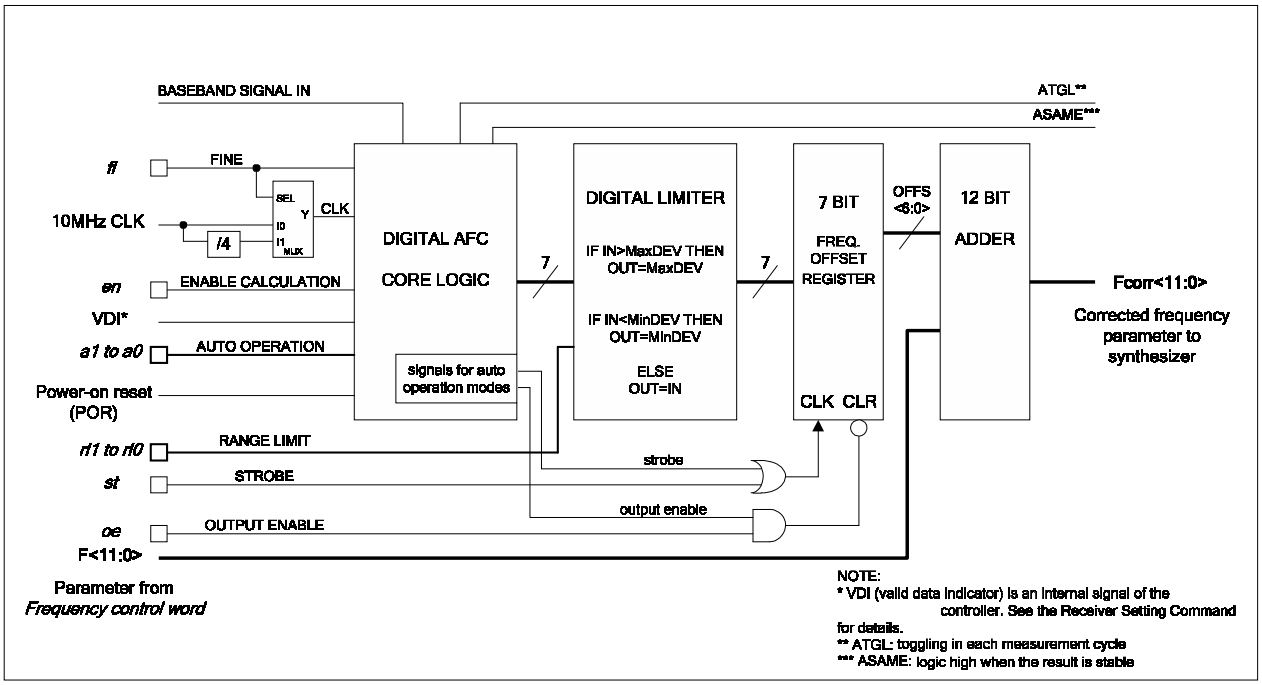
F res:
433 MHz bands: 2.5 kHz
868 MHz band: 5 kHz
915 MHz band: 7.5 kHz

Bit 3 (st): Strobe edge, when st goes to high, the actual latest calculated frequency error is stored into the offset register of the AFC block.

Bit 2 (fi): Switches the circuit to high accuracy (fine) mode. In this case, the processing time is about twice as long, but the measurement uncertainty is about half.

Bit 1 (oe): Enables the frequency offset register. It allows the addition of the offset register to the frequency control word of the PLL.

Bit 0 (en): Enables the calculation of the offset frequency by the AFC circuit.



In manual mode, the strobe signal is provided by the microcontroller. One measurement cycle (and strobe) signal can compensate about 50-60% of the actual frequency offset. Two

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measurement cycles can compensate 80%, and three measurement cycles can compensate 92%. The ATGL bit in the status register can be used to determine when the actual measurement cycle is finished.

In automatic operation mode (no strobe signal is needed from the microcontroller to update the output offset register) the AFC circuit is automatically enabled when the VDI indicates potential incoming signal during the whole measurement cycle and the circuit measures the same result in two subsequent cycles.

Without AFC the transmitter and the receiver needs to be tuned precisely to the same frequency. RX/TX frequency offset can lower the range. The units must be adjusted carefully during production, stable, expensive crystal must be used to avoid drift or the output power needs to be increased to compensate yield loss.
The AFC block will calculate the TX-RX offset. This value will be used to pull the RX synthesizer close to the frequency of the transmitter. The main benefits of the automatic frequency control: cheap crystal can be used, the temperature or aging drift will not cause range loss and no production alignment needed.

There are four operation modes:

1. (a1=0, a0=0) Automatic operation of the AFC is off. Strobe bit can be controlled by the microcontroller.

2. (a1=0, a0=1) The circuit measures the frequency offset only once after power up. This way, extended TX-RX distance can be achieved. In the final application, when the user inserts the battery, the circuit measures and compensates for the frequency offset caused by the crystal tolerances. This method allows for the use of cheaper quartz in the application and provides protection against tracking an interferer.

3. (a1=1, a0=0) The frequency offset is calculated automatically and the centre frequency is corrected when the VDI is high. The calculated value is dropped when the VDI goes low. To improve the efficiency of the AFC calculation two methods are recommended:

a. The transmit package should start with a low effective baud rate pattern (i.e.: 00110011) because it is easier to receive. The circuit automatically measures the frequency offset during this initial pattern and changes the receiving frequency accordingly. The further part of the package will be received by the corrected frequency settings.

b. The transmitter sends the first part of the packet with a step higher deviation than required during normal operation to ease the receiving. After the frequency shift was corrected, the deviation can be reduced.

In both cases (3a and 3b), when the VDI indicates poor receiving conditions (VDI goes low),

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the output register is automatically cleared. Use this “drop offset” mode when the receiver communicates with more than one transmitter.

4. (a1=1, a0=1) It is similar to mode 3, but suggested to use when a receiver operates with only one transmitter. After a complete measuring cycle, the measured value is kept independently of the state of the VDI signal. When the receiver is paired with only one transmitter, it is possible to use this “keep offset” mode. In this case, the DRSSI limit should be selected carefully to minimize the range hysteresis.

TX Configuration Control Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	1	1	0	0	mp	m3	m2	m1	m0	0	p2	p1	p0	9800h

m: select modulation polarity
m2..m0: select frequency deviation:

m3	m2	m1	m0	frequency deviation [kHz]
0	0	0	0	15
0	0	0	1	30
0	0	1	0	45
0	0	1	1	60
0	1	0	0	75
0	1	0	1	90
0	1	1	0	105
0	1	1	1	120
1	0	0	0	135
1	0	0	1	150
1	0	1	0	165
1	0	1	1	180
1	1	0	0	195
1	1	0	1	210
1	1	1	0	225
1	1	1	1	240

p2..p0: select output power

p2	p1	p0	Output power[dBm]
0	0	0	0
0	0	1	-3
0	1	0	-6
0	1	1	-9
1	0	0	-12
1	0	1	-15
1	1	0	-18
1	0	1	-21

Note: The output power given in the table is relative to the maximum available power, which depends on the actual antenna impedance.

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PLL Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	0	0	0	ob1	ob0	lpx	ddy	ddit	1	bw0	CC67h

Bits 6-5 (ob1-ob0): Microcontroller output clock buffer rise and fall time control. The ob1-ob0 bits are changing the output drive current of the CLK pin. Higher current provides faster rise and fall times but can cause interference.

Microcontroller output clock buffer rise and fall time control.

ob1	ob0	Selected uC CLK frequency
0	0	5 or 10 MHz (recommended)
0	1	3.3 MHz
1	X	2.5 MHz or less

Note: Needed for optimization of the RF performance. Optimal settings can vary according to the external load capacitance. Bit 3 (dly): Switches on the delay in the phase detector when this bit is set.

Bit 2 (ddit): When set, disables the dithering in the PLL loop.

Bit 0 (bw0): PLL bandwidth can be set for optimal TX RF performance

Select low power mode of the crystal oscillator.

lpx	Crystal start-up time (typ)	Power consumption (typ)
0	1 ms	620 uA
1	2 ms	460 uA

ddy: phase detector delay enable.
ddi: disables the dithering in the PLL loop.
bw1-bw0: select PLL bandwidth

bw0	Max bit rate [kbps]	Phase noise at 1MHz offset [dBc/Hz]
0	86.2	-107
1	256	-102

Note: POR default settings of the register were carefully selected to cover almost all typical applications. When changing these values, examine thoroughly the output RF spectrum. For more information, contact Silicon Labs Support.

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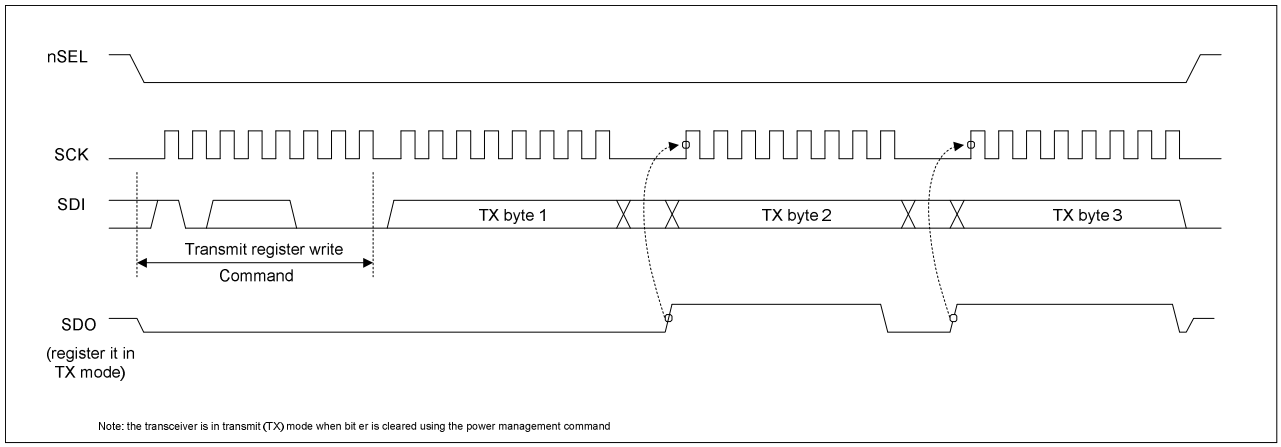
Transmitter Register Write Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	1	1	0	0	0	t7	t6	t5	t4	t3	t2	t1	t0	B8AAh

This command is use to write a data byte to module and then transmit it

With this command, the controller can write 8 bits (t7 to t0) to the transmitter data register. Bit 7 (el) must be set in Configuration Setting Command.

Multiple Byte Write with Transmit Register Write Command:



Note: Alternately the transmit register can be directly accessed by nFFS (pin6).

Wake-Up Timer Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	r4	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E196h

The wake-up time period can be calculated by (m7 to m0) and (r4 to r0): $T_{wake\text{-}up} = 1.03 \cdot M \cdot 2^R + 0.5$ [ms]

Note:

- For continual operation, the ew bit should be cleared and set at the end of every cycle.
- For future compatibility, use R in a range of 0 and 29

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Low Duty-Cycle Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	d6	d5	d4	d3	d2	d1	d0	en	C8OEh

With this command, autonomous low duty-cycle operation can be set in order to decrease the average power consumption in receive mode.

Bits 7-1 (d6-d0): The duty-cycle can be calculated by using (d6 to d0) and M. (M is parameter in a Wake-Up Timer Command, see above). The time cycle is determined by the Wake-Up Timer Command.

duty-cycle= (D · 2 +1) / M · 100%

Bit 0 (en): Enables the low duty-cycle Mode. Wake-up timer interrupt is not generated in this mode.

Note: In this operation mode, bit er must be cleared and bit ew must be set in the Power Management Command.

In low duty-cycle mode the receiver periodically wakes up for a short period of time and checks if there is a valid FSK transmission in progress. FSK transmission is detected in the frequency range determined by Frequency Setting Command plus and minus the baseband filter bandwidth determined by the Receiver Control Command. This on-time is automatically extended while DQD indicates good received signal condition.

When calculating the on-time take into account:

- the crystal oscillator, the synthesizer and the PLL needs time to start, see the AC Characteristics (Turn-on/Turnaround timings).
- depending on the DQD parameter, the chip needs to receive a few valid data bits before the DQD signal indicates good signal condition (Data Filter Command).

Choosing too short on-time can prevent the crystal oscillator from starting or the DQD signal will not go high even when the received signal has good quality.

The Alpha transceiver Module is configured to work in FIFO mode. The Alpha Module can be setup to periodically wakes up and switches to receiving mode. If valid FSK data received, the chip sends an interrupt to the microcontroller and continues filling the RX FIFO. After the transmission is over and the FIFO is read out completely and all other interrupts are cleared, the chip goes back to low power consumption mode.

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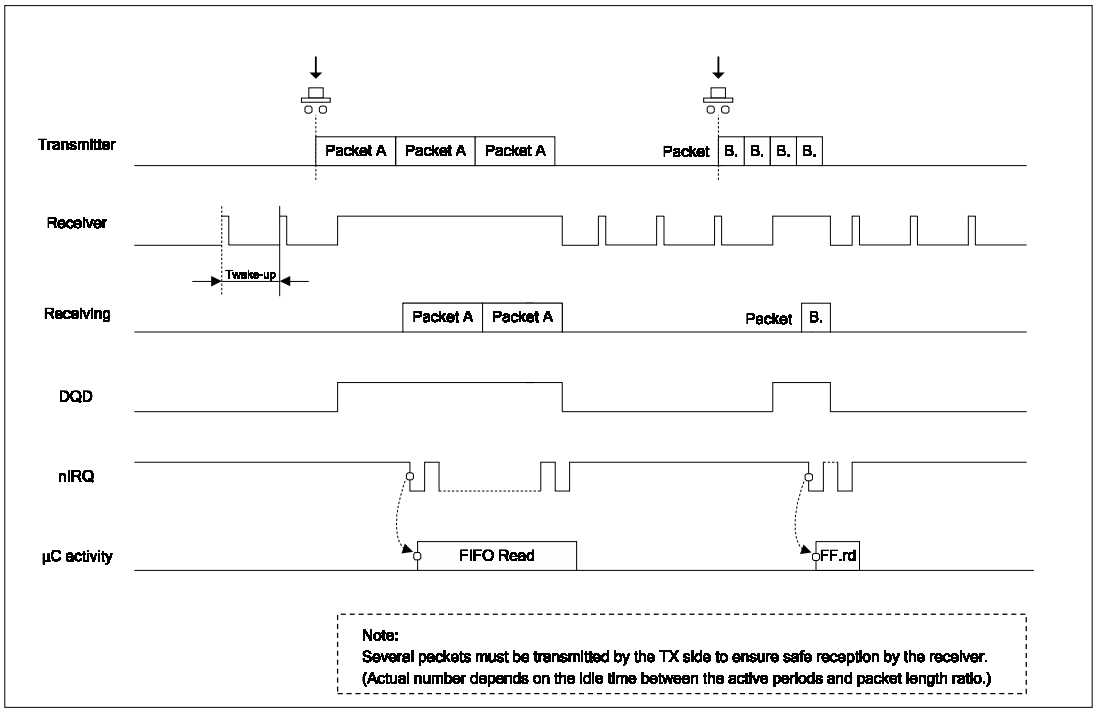
Application Proposal for LPDM (Low Power Duty-Cycle Mode) Receivers:



Low Battery Detector and Microcontroller Clock Divider Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	d2	d1	d0	0	v3	v2	v1	v0	C000h

Select frequency of CLK pin

d2	d1	d0	Clock frequency[MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

CLK signal is derive form crystal oscillator and it can be applied to MCU clock in to save a second crystal.
If not used, please set bit “dc” to disable CLK output

To integrate the load capacitor internal can not only save cost, but also adjust reference frequency by software

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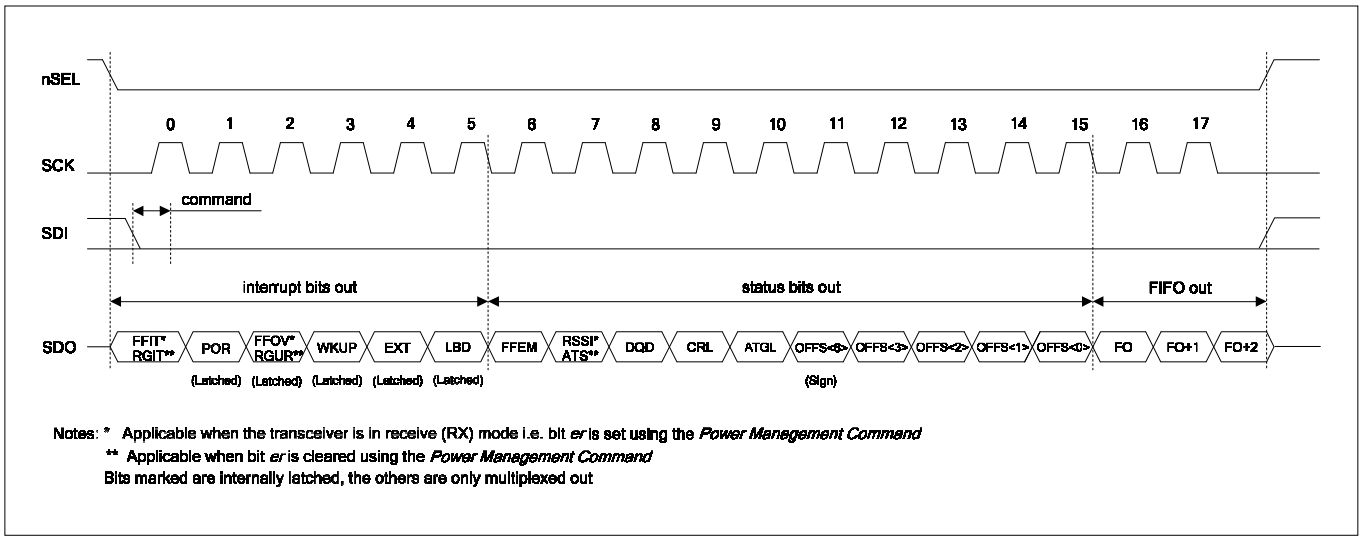
v3..v0: Set threshold voltage of Low battery detector Vlb=2.2+V*0.1 [V]

Status Read Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	-



Notes: * Applicable when the transceiver is in receive (RX) mode i.e. bit *er* is set using the *Power Management Command*
** Applicable when bit *er* is cleared using the *Power Management Command*
Bits marked are internally latched, the others are only multiplexed out

Bit	
15	TX ready for next byte or FIFO received data status
14	Power on reset status
13	TX Register under run or RX FIFO Overflow status
12	Wakeup timer overflow status
11	Interrupt on external source status
10	Low battery detect status
9	FIFO empty status
8	Antenna tuning signal strength
7	Received signal strength indicator
6	Data Quality Detector status
5	Clock Recovery Locked status
4	Toggling in each AFC cycle
3	Measured Offset Frequency Sign Value 1='+', 0='-'
2	Measured offset Frequency value (3 bits)
1	Measured offset Frequency value (3 bits)
0	Measured offset Frequency value (3 bits)

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Note: In order to get accurate values the AFC has to be disabled during the read by clearing the en bit in the AFC Control Command. The AFC offset value (OFFS bits in the status word) is represented as a two's complement number. The actual frequency offset can be calculated as the AFC offset value multiplied by the current PLL frequency step (see the Frequency Setting Command)

INTERRUPT HANDLING

In order to achieve low power consumption there is an advanced event handling circuit implemented. The device has a very low power consumption mode, so called sleep mode. In this mode only a few parts of the circuit are working. In case of an event, the device wakes up, switches into active mode and an interrupt signal generated on the nIRQ pin to indicate the changed state to the microcontroller. The cause of the interrupt can be determined by reading the status word of the device.

Several interrupt sources are available:

- RGIT – TX register empty interrupt: This interrupt generated when the transmit register is empty. Valid only when the el (enable internal data register) bit is set in the Configuration Setting Command and the transmitter is enabled in the Power Management command.
- FFIT – the number of bits in the RX FIFO reached the pre-programmed level: When the number of received data bits in the receiver FIFO reaches the threshold set by the f3…f0 bits of the FIFO and Reset Mode Command an interrupt is fired. Valid only when the ef (enable FIFO mode) bit is set in the Configuration Setting Command and the receiver is enabled in the Power Management Command.
- POR – power on reset interrupt: An interrupt generated when the change on the VDD line triggered the internal reset circuit or a software reset command was issued. For more details, see the Reset Modes section.
- RGUR – TX register under run: The automatic baud rate generator finished the transmission of the byte in the TX register before the register write occurred. Valid only when the el (enable internal data register) bit is set in the Configuration Setting Command and the transmitter is enabled in the Power Management command.
- FFOV – FIFO overflow: There are more bits received than the capacity of the FIFO (16 bits). Valid only when the ef (enable FIFO mode) bit is set in the Configuration Setting Command and the receiver is enabled in the Power Management command
- WKUP – wake-up timer interrupt: This interrupt event occurs when the time specified by the Wake-Up Timer Command has elapsed. Valid only when the ew bit is set in the Power Management Command.
- EXT – external interrupt: Follows the level of the nINT pin if it is configured as an external Interrupt pin in the Receiver Control Command
- LBD – low battery detector interrupt: Occurs when the VDD goes below the programmable low battery detector threshold level. Valid only when the eb (enable low

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battery detector) bit is set in the Power Management Command.

If any of the sources becomes active, the nIRQ pin will change to logic low level, and the corresponding bit in the status byte will be HIGH.

Clearing an interrupt actually implies two things:

- Releasing the nIRQ pin to return to logic high
- Clearing the corresponding bit in the status byte
- This may be completed with the following interrupt sources:
- RGIT: both the nIRQ pin and status bit remain active until the register is written (if under-run does not occur until the register write), or the transmitter and the TX latch are switched off.
- FFIT: both the nIRQ pin and status bit remain active until the FIFO is read (a FIFO IT threshold number of bits have been read), the receiver is switched off, or the RX FIFO is switched off.
- POR: both the nIRQ pin and status bit can be cleared by the read status command
- RGUR: this bit is always set together with RGIT; both the nIRQ pin and the status bit remain active until the transmitter and the TX latch is switched off.
- FFOV: this bit is always set together with FFIT; it can be cleared by the status read command, but the FFIT bit and hence the nIRQ pin will remain active until the FIFO is read fully, the receiver is switched off, or the RX FIFO is switched off.
- WKUP: both the nIRQ pin and status bit can be cleared by the read status command
- EXT: both the nIRQ pin and status bit follow the level of the nINT pin
- LBD: the nIRQ pin can be released by the reading the status, but the status bit will remain active while the VDD is below the threshold.

The best practice in interrupt handling is to start with a status read when interrupt occurs, and then make a decision based on the status byte. It is very important to mention that any interrupt can “wake-up” the Alpha transceiver Module from sleep mode. This means that the crystal oscillator starts to supply clock signal to the microcontroller even if the microcontroller has its own clock source. Also, the ALPHA-TRX will not go to low current sleep mode if any interrupt remains active regardless to the state of the ex (enable crystal oscillator) bit in the Power Management Command. This way the microcontroller always can have clock signal to process the interrupt. To prevent high current consumption and this way short battery life, it is strongly advised to process and clear every interrupt before going to sleep mode. All unnecessary functions should be turned off to avoid unwanted interrupts. Before freezing the microcontroller code, a thorough testing must be performed in order to make sure that all interrupt sources are handled before putting the radio device to low power consumption sleep mode. If the dc bit is set in the Power Management Command, then only the ex bit controls the crystal oscillator (supposing that both the er and et bits are cleared), the interrupts have no effect on it.

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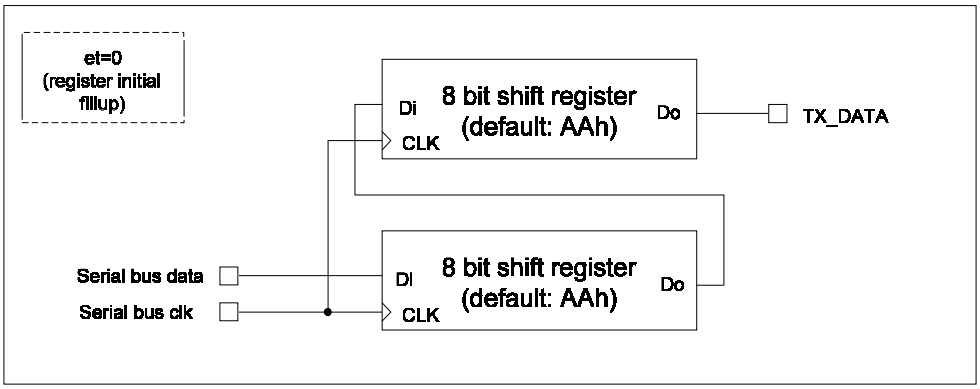
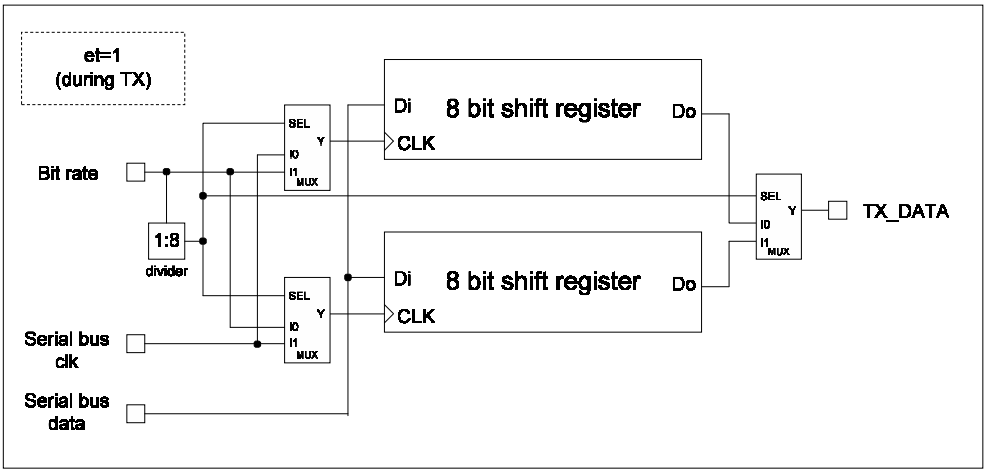
TX REGISTER BUFFERED DATA TRANSMISSION

In this operating mode (enabled by bit el, in the Configuration Setting Command) the TX data is clocked into one of the two
8-bit data registers. The transmitter starts to send out the data from the first register (with the given bit rate) when bit et is set with the Power Management Command. The initial value of the data registers (AAh) can be used to generate preamble. During this mode, the SDO pin can be monitored to check whether the register is ready (SDO is high) to receive the next byte from the microcontroller.

TX register simplified block diagram (before transmit)



TX register simplified block diagram (during transmit)



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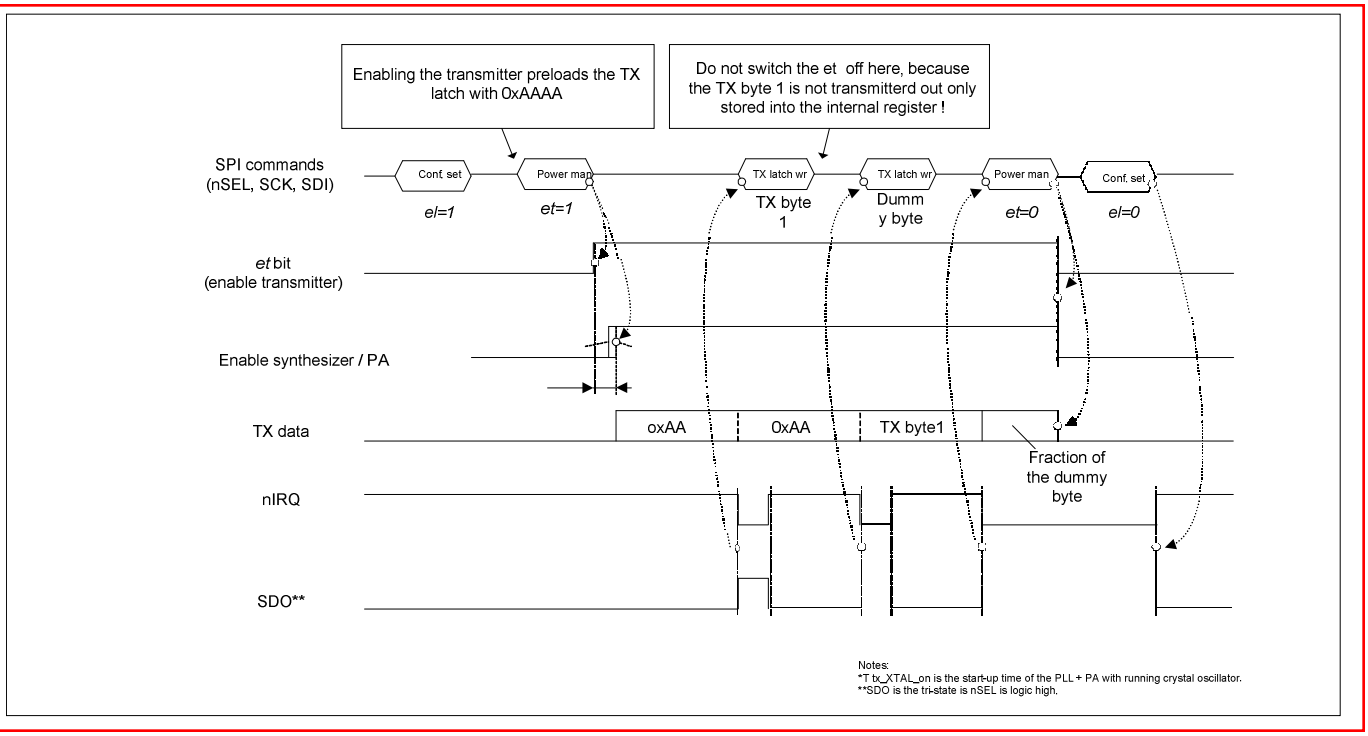
Typical TX register usage



Note: The content of the data registers are initialized by clearing bit et. A complete transmit sequence should be performed as follows:

a. Enable the TX register by setting the el bit to 1

b. The TX register automatically filled out with 0xAAAA, which can be used to generate preamble.

c. Enable the transmitter by setting the et bit

d. The synthesizer and the PLL turns on, calibrates itself then the power amplifier automatically enabled

e. The TX data transmission starts

f. When the transmission of the byte completed, the nIRQ pin goes high, the SDO pin goes low at the same time. The nIRQ pulse shows that the first 8 bits (the first byte, by default 0xAA) has transmitted. There are still 8 bits in the transmit register.

g. The microcontroller recognizes the interrupt and writes a data byte to the TX register h. Repeat f. - g. until the last data byte reached

i. Using the same method, transmit a dummy byte. The value of this dummy byte can be anything.

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j. The next high to low transition on the nIRQ line (or low to high on the SDO pin) shows that the transmission of the data bytes ended. The dummy byte is still in the TX latch.

k. Turn off the transmitter by setting the et bit to 0. This event will probably happen while the dummy byte is being transmitted. Since the dummy byte contains no useful information, this corruption will cause no problems.

l. Clearing the el bit clears the Register Underrun interrupt; the nIRQ pin goes high, the SDO low.

It is possible to perform this sequence without sending a dummy byte (step i.) but after loading the last data byte to the transmit register the PA turn off should be delayed for at least 16 bits time. The clock source of the microcontroller should be stable enough over temperature and voltage to ensure this minimum delay under all operating circumstances.

When the dummy byte is used, the whole process is driven by interrupts. Changing the TX data rate has no effect on the algorithm and no accurate delay measurement is needed.

RX FIFO BUFFERED DATA READ

In this operating mode, incoming data are clocked into a 16-bit FIFO buffer. The receiver starts to fill up the FIFO when the Valid Data Indicator (VDI) bit and the synchron pattern recognition circuit indicates potentially real incoming data. This prevents the FIFO from being filled with noise and overloading the external microcontroller.

Interrupt Controlled Mode:

The user can define the FIFO IT level (the number of received bits) which will generate the nFFIT when exceeded. The status bits report the changed FIFO status in this case.

Polling Mode:

When nFFS signal is low the FIFO output is connected directly to the SDO pin and its content can be clocked out by the SCK. Set the FIFO IT level to 1. In this case, as long as FFIT indicates received bits in the FIFO, the controller may continue to take the bits away. When FFIT goes low, no more bits need to be taken.

An SPI read command is also available to read out the content of the FIFO (Receiver FIFO Read Command).

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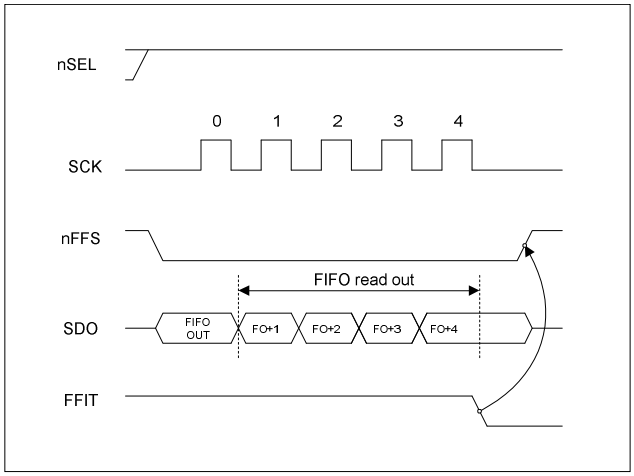
FIFO Read Example with FFIT Polling



Note: During FIFO access fSCK cannot be higher than fref /4, where f ref is the crystal oscillator frequency. When the duty-cycle of the clock signal is not 50% the shorter period of the clock pulse should be at least 2/fref .

RECOMMENDED PACKET STRUCTURES

	Preamble	Synchron word (Can be network ID)	Payload	CR C
Minimum length	4 - 8 bits (1010b or 0101b)	D4h (programmable)	?	4 bit - 1 byte
Recommended length	8 -12 bits (e.g. AAh or 55h)	2DD4h (D4 is programmable)	?	2 byte

CRYSTAL SLECTION GUIDELINES

The crystal frequency is used as the reference of the PLL, which generates the local oscillator frequency (fLO). Therefore, f LO is directly proportional to the crystal frequency. The accuracy requirements for production tolerance, temperature drift and aging can thus be

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determined from the maximum allowable local oscillator frequency error.

Whenever a low frequency error is essential for the application, it is possible to “pull” the crystal to the accurate frequency by changing the load capacitor value. The widest pulling range can be achieved if the nominal required load capacitance of the crystal is in the “midrange”, for example 16 pF. The “pull-ability” of the crystal is defined by its motional capacitance and C 0 .

Maximum XTAL Tolerances Including Temperature and Aging [ppm]

Bit Rate: 2.4 kbps

	Deviation [±						
	30	45	60	75	90	105	120
433	20	30	50	70	90	100	100
868	10	20	25	30	40	50	60
915	10	15	25	30	40	50	50

Bit Rate: 9.6 kbps

	Deviation [±						
	30	45	60	75	90	105	120
433	15	30	50	70	80	100	100
868	8	15	25	30	40	50	60
915	8	15	25	30	40	50	50

Bit Rate: 38.4 kbps

	Deviation [±						
	30	45	60	75	90	105	120
433	don't use	5	20	30	50	75	75
868	don't use	3	10	20	25	30	40
915	don't use	3	10	15	25	30	40

Bit Rate: 115.2 kbps

	Deviation [±						
	105	120	135	150	165	180	195
433	don't use	3	20	30	50	70	80
868	don't use	don't use	10	20	25	35	45
915	don't use	don't use	10	15	25	30	40

RX-TX ALIGNMENT PROCEDURES

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RX-TX frequency offset can be caused only by the differences in the actual reference frequency. To minimize these errors it is suggested to use the same crystal type and the same PCB layout for the crystal placement on the RX and TX PCBs.

To verify the possible RX-TX offset it is suggested to measure the CLK output of both chips with a high level of accuracy. Do not measure the output at the XTL pin since the measurement process itself will change the reference frequency. Since the carrier frequencies are derived from the reference frequency, having identical reference frequencies and nominal frequency settings at the TX and RX side there should be no offset if the CLK signals have identical frequencies.

It is possible to monitor the actual RX-TX offset using the AFC status report included in the status byte of the receiver. By reading out the status byte from the receiver, the actual measured offset frequency will be reported. In order to get accurate values the AFC has to be disabled during the read by clearing the en bit in the AFC Control Command.

RESET MODES

The chip will enter into reset mode if any of the following conditions are met:

- Power-on reset: During a power up sequence until the Vdd has reached the correct level and stabilized
- Power glitch reset: Transients present on the Vdd line
- Software reset: Special control command received by the chip

Power-on reset

After power up the supply voltage starts to rise from 0V. The reset block has an internal ramping voltage reference (reset-ramp signal), which is rising at 100mV/ms (typical) rate. The chip remains in reset state while the voltage difference between the actual V dd and the internal reset-ramp signal is higher than the reset threshold voltage, which is 600 mV (typical). As long as the Vdd voltage is less than 1.6V (typical) the chip stays in reset mode regardless the voltage difference between the Vdd and the internal ramp signal.

The reset event can last up to 100ms supposing that the Vdd reaches 90% its final value within 1ms. During this period, the chip does not accept control commands via the serial control interface.

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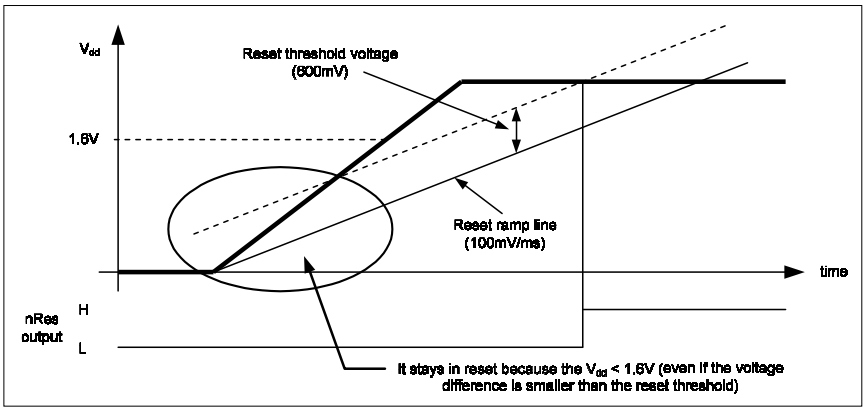
Power-on reset example:



Power glitch reset

The internal reset block has two basic mode of operation: normal and sensitive reset. The default mode is sensitive, which can be changed by the appropriate control command (see Related control commands at the end of this section). In normal mode the power glitch detection circuit is disabled.

There can be spikes or glitches on the Vdd line if the supply filtering is not satisfactory or the internal resistance of the power supply is too high. In such cases if the sensitive reset is enabled an (unwanted) reset will be generated if the positive going edge of the Vdd has a rising rate greater than 100mV/ms and the voltage difference between the internal ramp signal and the Vdd reaches the reset threshold voltage (600 mV). Typical case when the battery is weak and due to its increased internal resistance a sudden decrease of the current consumption (for example turning off the power amplifier) might lead to an increase in supply voltage. If for some reason the sensitive reset cannot be disabled step-by-step decrease of the current consumption (by turning off the different stages one by one) can help to avoid this problem.

Any negative change in the supply voltage will not cause reset event unless the Vdd level reaches the reset threshold voltage (250mV in normal mode, 1.6V in sensitive reset mode).

If the sensitive mode is disabled and the power supply turned off the Vdd must drop below 250mV in order to trigger a power-on reset event when the supply voltage is turned back on. If the decoupling capacitors keep their charges for a long time it could happen that no reset will be generated upon power-up because the power glitch detector circuit is disabled.

Note that the reset event reinitializes the internal registers, so the sensitive mode will be enabled again.

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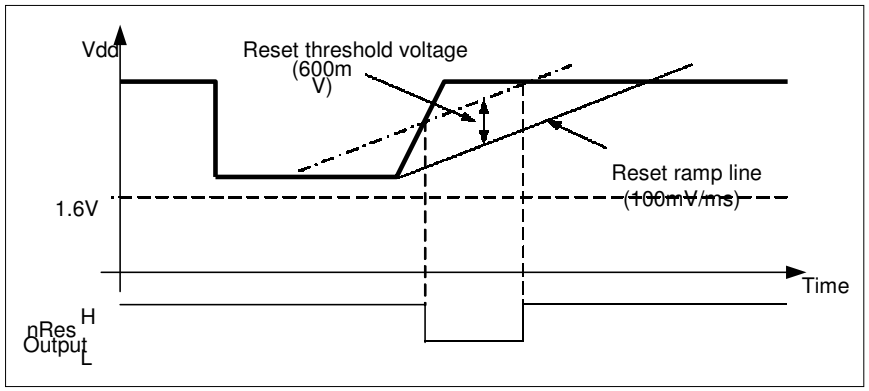
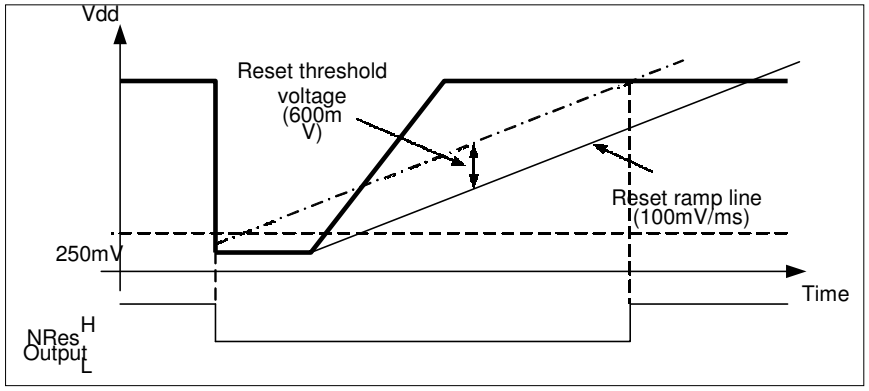
Sensitive Reset Enabled, Ripple on Vdd :



Sensitive reset disabled:



Software reset

Software reset can be issued by sending the appropriate control command (described at the end of the section) to the chip. The result of the command is the same as if power-on reset was occurred but the length of the reset event is much less, 0.25ms typical. The software reset works only when the sensitive reset mode is selected.

V dd line filtering

During the reset event (caused by power-on, fast positive spike on the supply line or software reset command), it is very important to keep the Vdd line as smooth as possible. Noise or periodic disturbing signal superimposed the supply voltage may prevent the part getting out from reset state. To avoid this phenomenon use adequate filtering on the power supply line to keep the level of the disturbing signal below 100mV p-p in the DC – 50kHz range for 200ms from Vdd ramp start.. Typical example when a switch-mode regulator is used to supply the radio, switching noise may be present on the Vdd line. Follow the manufacturer's recommendations how to decrease the ripple of the regulator IC and/or how to shift the switching frequency.

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Related control commands

FIFO and Reset Mode Command

Setting bit<0> to high will change the reset mode to normal from the default sensitive.

SW Reset Command

Issuing FE00h command will trigger software reset (sensitive reset mode must be enabled). See the Wake-up Timer Command.

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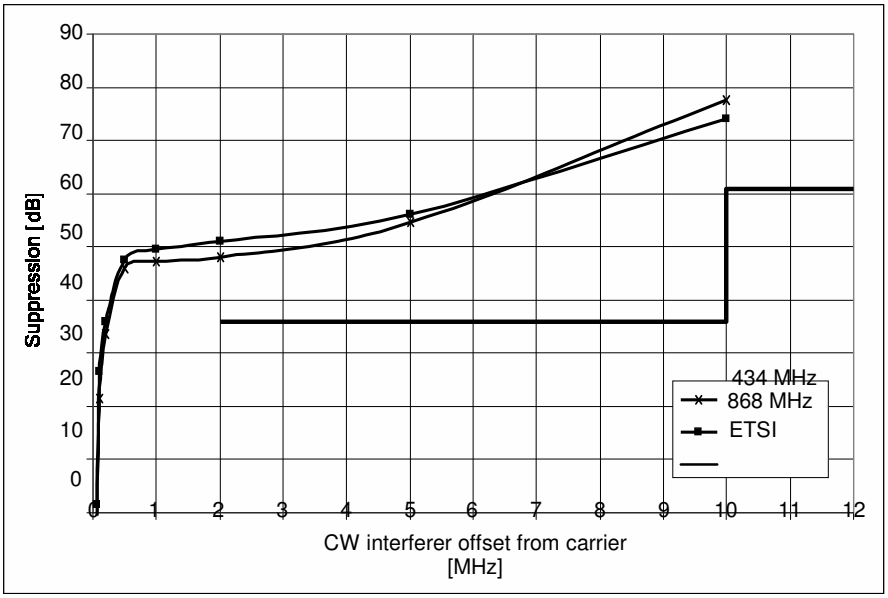
TYPICAL PERFORMANCE CHARACTERISTICS

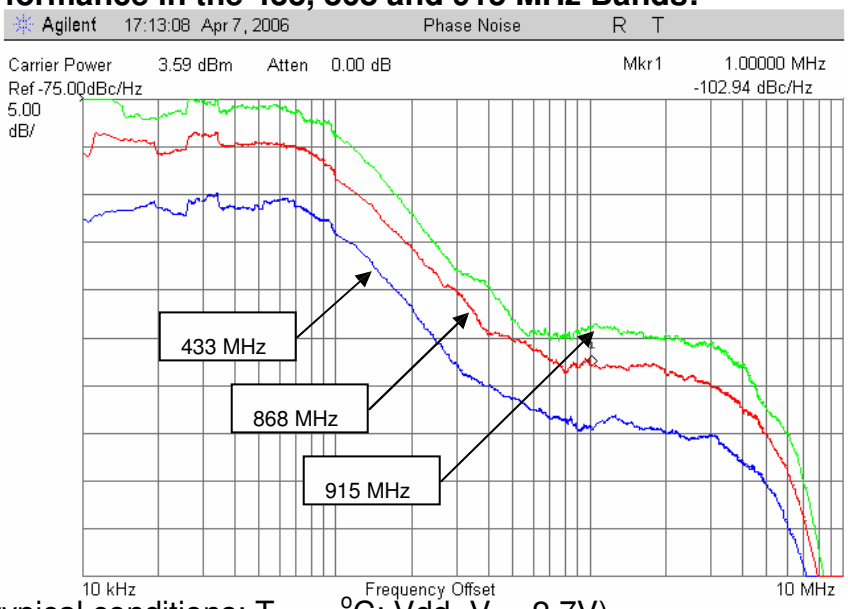
Channel Selectivity and Blocking:



Note:

- LNA gain maximum, filter bandwidth 67 kHz, data rate 9.6 kbps, AFC switched off, FSK deviation ± 45 kHz, Vdd = 2.7 V
- Measured according to the descriptions in the ETSI Standard EN 300 220-1 v2.1.1 (2006-01 Final Draft), section 9
- The ETSI limit given in the figure is drawn by taking -106dBm at 9.6kbps typical sensitivity into account, and corresponds to receiver class 2 requirements (section 4.1.1)

Phase Noise Performance in the 433, 868 and 915 MHz Bands:



(Measured under typical conditions: $T_{ep=27}$ °C; Vdd=V_{ec}=2.7V)

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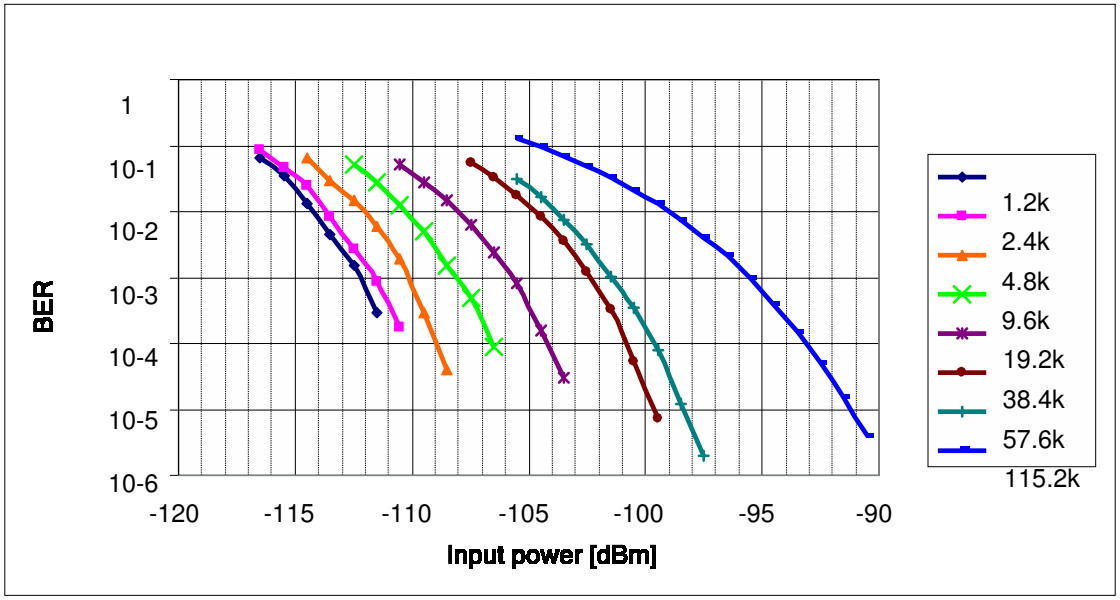
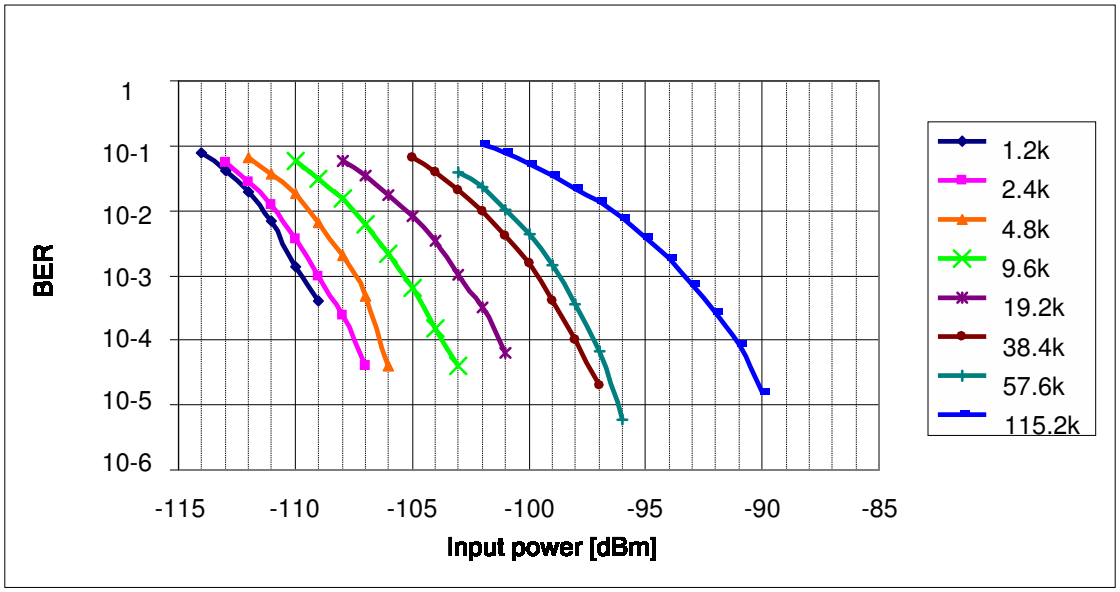
BER Curves in 433 MHz Band:



BER Curves in 868 MHz Band:



The table below shows the optimal receiver baseband bandwidth (BW) and transmitter deviation frequency (δf FSK) settings for different data-rates supposing no transmit receive offset frequency. If TX/RX offset (for example due to crystal tolerances) have to be taken into account, increase the BW accordingly.

1.2 kbps	2.4 kbps	4.8 kbps	9.6 kbps	19.2 kbps	38.4 kbps	57.6 kbps	115.2 kbps
BW=67 kHz □f FSK =45 kHz	BW=67 kHz □f FSK =45 kHz	BW=67 kHz □f FSK =45kHz	BW=67 kHz □f FSK =45 kHz	BW=67 kHz □f FSK =45 kHz	BW=134 kHz □f FSK =90 kHz	BW=134 kHz □f FSK =90 kHz	BW=200 kHz □f FSK =120 kHz

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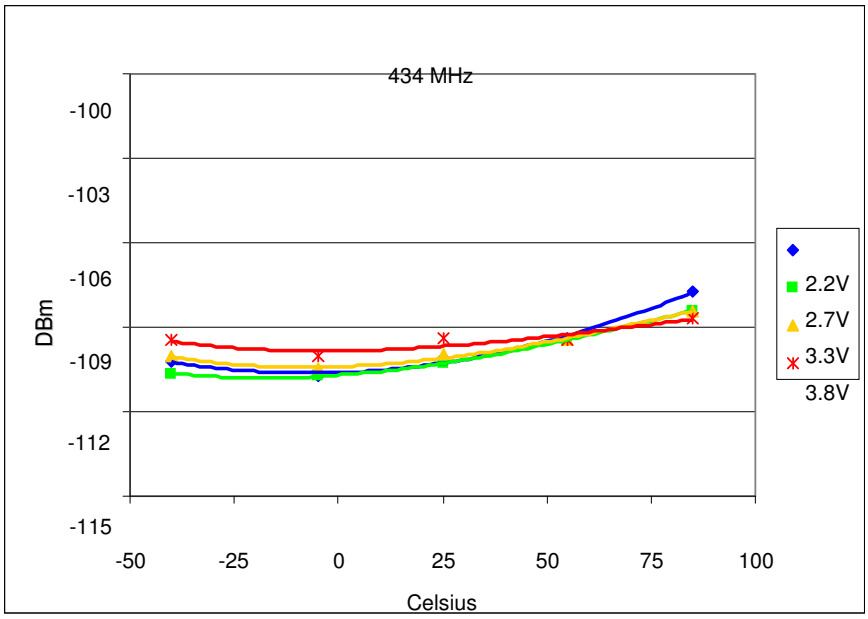
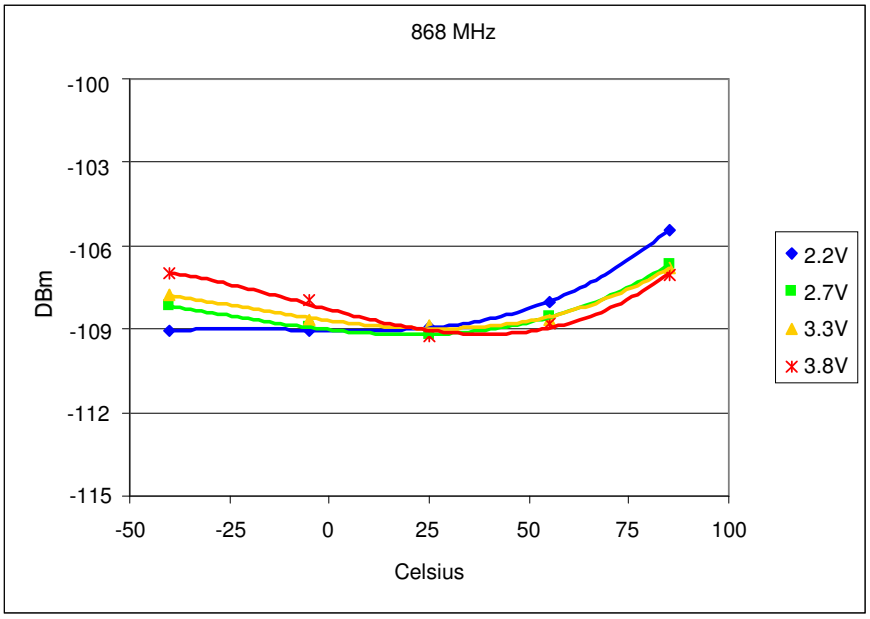
Receiver Sensitivity over Ambient Temperature (433 MHz, 2.4 kbps, fFSK: 45 kHz, BW: 67 kHz):



Receiver Sensitivity over Ambient Temperature (868 MHz, 2.4 kbps, fFSK: 45 kHz, BW: 67 kHz):



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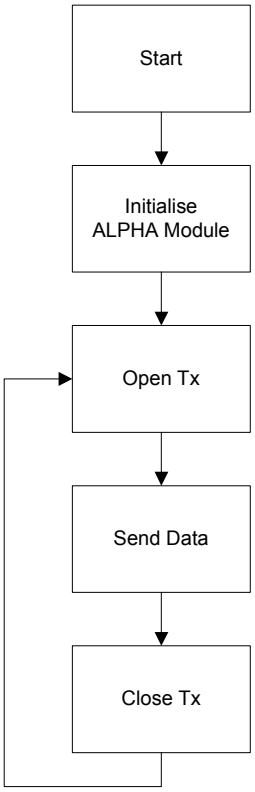
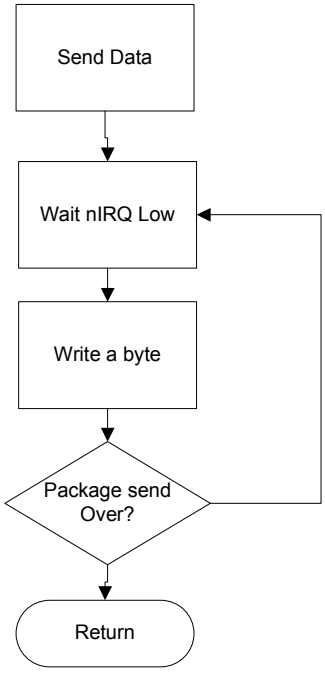
Transmitter Operation Flow





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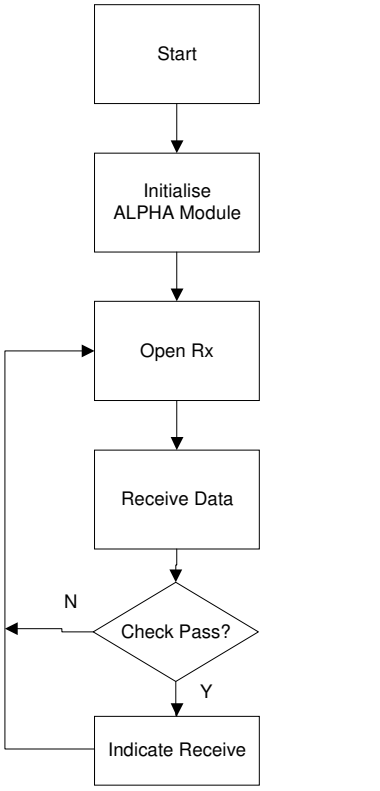
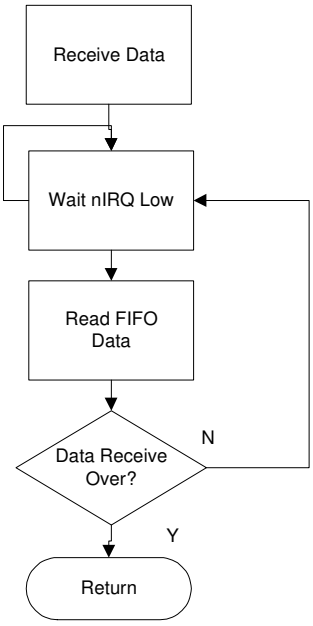
Receiver Operation Flow





After Initialisation, open FIFO receive mode and wait for nIRQ low, only then can the MCU read received and stored data in FIFO. For the next received package please reset FIFO

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