PRESS KIT

2005

ISSCC
VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency, and to network with leading experts.

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ISSCC 2005
EXECUTIVE SUMMARY

- **Activities**
- **Conference Theme**
- **Significant Results**

EXECUTIVE SUMMARY

ACTIVITIES AT ISSCC 2005

- **Tutorials, presented Sunday, February 6:**
  - Eight independent lectures presented by experts from each of the ISSCC 2005 Program Subcommittees: Analog; Digital; Imagers, MEMS, and Displays; Memory; Signal Processing; Technology Directions; Wireless Communications; Wireline Communications.

- **Advanced-Circuit-Design Forums, presented Sunday, February 6 and Thursday February 10:**
  - Informal all-day linked interaction in which circuit experts exchange information on their current research.

- **Evening Discussion Sessions, presented on Sunday through Tuesday, February 6 through 8 evenings:**
  - Five Special-Topic Sessions
  - Four Panel-Discussions

- **Technical Paper Sessions, presented Monday through Wednesday, February 7 through 9:**
  - **Three** presentations in the Plenary Session on Monday morning
  - **31** paper sessions, beginning Monday afternoon and continuing through Wednesday afternoon, including:

    185 regular-length papers

    48 short papers

- **Social Hour on Monday evening after the paper sessions:**
  - DAC/ISSCC Student-Design-Contest winners poster session
  - Technical-book display

- **Short Course, presented Thursday, February 10:**
  - **Four** linked 90-minute lectures given by experts in the field

CONFERENCE THEME:

"Entering the Nanoelectronic Integrated-Circuit Era"

With the appearance of integrated circuits having transistor dimensions less than 100nm, integrated-circuit technology is moving from the microelectronic era into the nanoelectronic era. To mark this major transition, this year's Conference highlights papers covering new circuit techniques and devices that employ transistors, or other circuit elements, with nanometer dimensions.

Sub-100-nanometer-scale transistors require circuit innovations to allow operation under ever-decreasing power-supply voltage of 1.2V or lower, while manufacturing parameters are degraded more and more. While digital chips with more than one billion transistors are realized, novel circuit concepts using the sub-100nm transistors are enabling both higher performance and lower-power digital computation. Also in the analog-circuit area, higher speed analog-to-digital converters are enabling new transmission rates and application services for both wired and wireless communications. Circuit innovations using sub-100nm transistors for the solution of problems in computing, memory, imaging, communications will be featured at the Conference.

In support of this theme, there are:

Plenary Session, with three presentations :

- Nanoelectronics for the Ubiquitous Information Society
- Ambient Intelligence: Gigascale Dreams and Nanoscale Realities
- Innovation and Integration in the Nanoelectronics Era

Technical-paper sessions, amongst which sample topics include:

- Very-low supply voltages and 90nm technology in analog-to-digital converter design **(Sessions 9 and 27)**
- Multi-core processor (Itanium®) with shared cache implemented with 1.72 billion transistors on a single die **(Session 10)**
- Next-generation multimedia processing uses multiple diverse processor cores and high-speed serial I/O techniques (CELL) **(Session 10)**
- NAND Flash breaks the 8Gb barrier **(Session 2)**
- First 256Mb SRAM **(Session 26)**
- Fully-integrated single-chip RF CMOS WLAN transceivers (with PHY and MAC) **(Session 5)**

- First Ultra-Wide-Band transceivers realized in silicon **(Sessions 11 and 24)**
- SerDes with equalization enable backplane links at 6.4Gb/s **(Session 3)**
- Chip-to-chip communication at 3Gb/s/pin implemented with RF frequency-division multiple-access interconnect which enables reconfigurability in routing **(Session 18)**

Discussion Sessions, amongst which sample topics include:

- Mobile Imaging: Paradigm or Technology Bubble? **[E1]**
- What Papers Will and Will Not Be at ISSCC in 2010? **[E2]**
- Driving Miss Ubiquity: What applications will fill tomorrow's fabs? **[E4]**
- When Processors Hit the Power Wall (or "When the CPU hits the fan") **[SE2]**
- Toward the Nanoscale Transistor – Highlights of 2004 Symposium on VLSI Technology **[SE4]**
- SRAM Design in the Nanoscale Era **[SE5]**

Circuit Design Forums:

- Advanced Dynamic Memory Design **[F2]**
- Robust Design Solutions for Nanoscale Circuits: from DFM through End-of-Life **[F4]**

SIGNIFICANT RESULTS

- **ANALOG:**
  - A 22GS/s 6b DAC pushes the DAC-speed frontier **[6.7]**
  - Low supply voltages, down to 0.5V, are demonstrated **[9.1, 27.8].**
  - Delta-Sigma Converters extend their bandwidth beyond 20MHz **[9.5, 27.6]**
- **DIGITAL:**
  - 1.7B transistors integrated on a single die **[10.1]**
  - Constant power-dissipation (100W for an Itanium®) maintained by coordinated control of voltage and frequency **[10.1]**
  - Significant increases in on-chip cache memory (26.8MB) **[10.1, 10.3, 10.4]**
  - A 32× increase in graphics processing per mW in 2 years **[10.6]**
  - On-die power measurement (never before implemented), temperature measurement, and management of each **[16.7]**
  - High-speed digital circuits operating at up to 8GHz **[20.1, 20.3, 20.4]**
  - Chip-to-chip I/O methods used in-package and on-die **[20.7, 28.7]**
- **IMAGERS, MEMS, AND DISPLAYS:**
  - A CMOS temperature sensor achieves a temperature accuracy of ±0.1°C over the temperature range of –55°C to +125°C. **[13.1]**
  - A CMOS micro-sensor that can detect less than 1ppb of lead concentration uses a few thin-film post-processing steps. **[13.4]**
  - The smallest pixel, yet announced, 1.56μm, is incorporated in a 3.1Mpixel FT-CCD optimized for mobile imaging **[19.1]**
- **MEMORY:**
  - NAND Flash breaks 8Gb barrier **[2.1, 2.2]**
  - eDRAM operating at 400MHz random cycle **[25.3]**
  - First 256Mb SRAM **[26.2]**
  - SRAMs operating at sub-0.5V **[26.3, 26.6]**

• SIGNAL PROCESSING:

- Low-power impulse-radio UWB transceiver **[24.1]**
- High-data-rate LDPC-COFDM-based UWB transceiver **[24.2]**
- Fully-integrated R/W 7XBD/16XDVD/56XCD SoC **[31.3]**

• TECHNOLOGY DIRECTIONS:

- Demonstrated microscopic interface between neural and electronic systems **[4.1]**
- MEMS-based atomic clocks which are 700× smaller than the present art **[4.5]**
- Three-dimensional integration schemes using wireless interconnects **[14.4, 14.5]**
- First-time demonstration of integrating BAW filters above BiCMOS and their connection to the RF circuits below. This technique is used for the integration of a complete WCDMA RF front-end. **[21.2 and 21.3]**
- First CMOS 60GHz direct-conversion receiver featuring folded microstrip lines realized in 0.13μm CMOS and consuming 9mW from a 1.2V supply **[21.6]**
- Organic transistors are integrated into flexible scanner and display **[32.2, 32.3]**

• WIRELESS COMMUNICATIONS:

- First truly single-chip 802.11 WLAN transceivers in CMOS **[5.2, 5.3]**
- A 24 GHz Phased-Array Transmitter on 0.18μm CMOS **[11.7]**
- A single-chip Quad-Band GSM/GPRS Transceiver in 0.18μm Standard CMOS **[17.6]**
- A 120nm CMOS DVB-T Tuner **[23.3]**

• WIRELINE COMMUNICATIONS:

- 6.25Gb/s Binary Adaptive Decision-Feedback Equalizer with First Post-Cursor Tap Cancellation **[3.5]**
- Circuit Techniques for a 40Gb/s Transmitter in 0.13μm CMOS **[8.1]**
- 3V 10.7Gb/s Differential Laser-Diode Driver with Active Back-Termination Output Stage **[12.1]**
- RF/Baseband FDMA-Interconnect Transceiver for Reconfigurable Multiple Access in Chip-to-Chip Communication **[18.6]**
- 0.94ps-rms-jitter 2.5GHz Multiphase Generator PLL for 10Gb/s Serial Links **[22.1]**

NOTES

ISSCC 2005
CONFERENCE OVERVIEW

- **Events**
- **Paper Statistics**
- **Plenary Session**
- **Technical Highlights**
- **Discussion Sessions**
- **Short Course**
- **Tutorials**
- **Advanced-Circuit-Design Forums**

EVENTS

TUTORIALS (SUNDAY, FEBRUARY 6, 2005)

- Eight 90-minute Tutorials, each taught three times, by individual circuit experts from the Program Committee, serve to meet attendees' needs for introductory material in circuit specialties.

ADVANCED-CIRCUIT-DESIGN FORUMS (SUN, FEB 6, AND THURS, FEB 10, 2005)

- In five circuit-design forums, circuit experts exchange information on their current research in an all-day informal linked-topic environment.

TECHNICAL SESSIONS (MON. TO WED., FEBRUARY 7 THROUGH 9, 2005)

- **Three invited talks** presented in the Plenary Session and **233 technical papers** presented in **31** Regular Sessions, highlight the latest circuit developments.

DISCUSSION SESSIONS (SUN, MON. & TUES., FEBRUARY 6 THROUGH 8, 2005)

- Five Special-Topic presentations, in which multiple experts provide, linked insights and background on a subject of current importance.
- Four Panels in which experts debate a selected topic and field audience questions in a semi-formal atmosphere.

SOCIAL HOUR (MONDAY, FEBRUARY 7, 2005)

- Opportunities to network with experts in a wide range of circuit specialties; meet colleagues in an informal exchange; view of the Poster Session (see below) browse the technical-book exhibits!

POSTER SESSION (MONDAY, FEBRUARY 7, 2005)

- Five DAC/ISSCC Student-Design-Contest winners will make poster presentations during the Social Hour.

SHORT COURSE (THURSDAY, FEBRUARY 10, 2005)

- Intensive all-day course on a single topic, taught by world-class instructors, can serve to "jump start" a change in an engineer's circuit specialty.

PAPER STATISTICS

OVERALL:

- **3** papers invited
- **579** papers submitted to ISSCC 2005
- **233** papers accepted, including:
    - **101** papers from North America, including
        - **55** Industry papers
        - **46** University papers
    - **79** papers from the Far East, including
        - **50** Industry papers
        - **29** University papers
    - **53** papers from Europe, including
        - **32** Industry papers
        - **21** University papers
- **32** Sessions, over 3 days

INTERNATIONAL SCOPE:

- Americas: **43%**
- Far East: **34%**
- Europe: **23%**

TECHNICAL COVERAGE:	2005	2004
• Analog	**16%**	**18%**
• Digital	**12%**	**11%**
• Imagers, MEMs and Displays	**9%**	**8%**
• Memory	**8%**	**10%**
• Signal Processing	**10%**	**10%**
• Technology Directions	**11%**	**10%**
• Wireless Communications	**18%**	**20%**
• Wireline Communications	**16%**	**13%**

PLENARY SESSION

[1.1] NANOELECTRONICS FOR THE UBIQUITOUS INFORMATION SOCIETY

Daeje Chin,
Minister of Information and Communications, Korea

- Nanoelectronics will truly lead to a ubiquitous information society, where electronics enables new information-based services for consumers, and becomes invisible to everyday life.
- This “invisible silicon” will require dramatically lower-power lower-cost and smaller-size electronics that can only be realized through nanoelectronic ICs.
- Nanoelectronics development has many technical and economic challenges. The primary technical challenges for nanoelectronics product development are the process and device parameter variations. The economic risks and challenges are the high cost of process-technology development and manufacturing production.
- The only way to manage the risk and successfully introduce high-volume nanoelectronics products is to create a tight collaboration between semiconductor manufacturers, system-infrastructure providers, and service industries. The talk will describe how government can play a key role in enabling and supporting the development phases of products for the future ubiquitous information services society based upon nanoelectronics.

[1.2] AMBIENT INTELLIGENCE: GIGASCALE DREAMS AND NANOSCALE REALITIES

Hugo De Man,
Senior Research Fellow, IMEC; Professor Katholieke Universiteit Leuven, Belgium

- Dreams of countless intelligent electronic devices, that are sensitive to, and adapt to, our human needs will be made possible by breaking through constraining complexity barriers, including: low-power software at the top of the product-development chain, and nanoscale-device quantum physics and parameter-variation control at the atomic level.
- This state of being surrounded by numerous intelligent electronics devices, called ambient intelligence, will require two-orders-of-magnitude-lower power dissipation than today’s processors, at one twentieth the cost. All levels of the design hierarchy, from circuits to architecture, and software, will be needed to address the low-power issue.
- But there is an architectural gap in the power-efficiency performance for processors – there is two orders of magnitude improvement required in computational power efficiency. Ways of addressing this gap will be described.

- At the same time, there is a physical gap due to the realities of devices and interconnects at the nanoscale level, such as gate and source-drain leakage, and transistor-parameter variability.
- In addition to “more-Moore” transistor-density growth for power-efficient computation, there is also a class of products that will require “more-than-Moore”, more than just transistor-density improvement, such as MEMS structures, and new materials and devices, for sensors and wireless sensor networks.

[1.3] INNOVATION AND INTEGRATION IN THE NANOELECTRONICS ERA

Sunlin Chou,
Senior Vice President and General Manager
Technology and Manufacturing Group, Intel, Hillsboro, OR

- Silicon technology and scaling remain keys to progress, with transistors and circuit elements already at nanoscale dimensions. Innovation will accelerate as nanotechnology renews and extends silicon technology through skillful integration of new materials, processes, and device structures.
- Hardware and software are evolving to enable new applications and usage modes, by offering features like multitasking, parallel processing, mobility, and wireless connectivity.
- Efficient use of power in nanoelectronics will call for holistic solutions involving systems, circuits, processes, devices, and packaging.
- Through innovation and integration of nanotechnology, Moore’s Law will extend into, and beyond, the next decade.

TECHNICAL HIGHLIGHTS

ANALOG:

- A 22GS/s 6b DAC pushes the DAC-speed frontier **[6.7]**
- Low supply voltages, down to 0.5V, are demonstrated **[9.1, 27.8].**
- 90nm technology enters analog design, forcing low-voltage techniques **[9.2, 9.3, 15.2, 27.3, 27.4]**
- Delta-Sigma Converters extend their bandwidth beyond 20MHz **[9.5, 27.6]**

DIGITAL:

- 1.7B transistors integrated on a single die **[10.1]**
- Constant power dissipation (100W for an Intanium®) maintained by coordinated control of voltage and frequency **[10.1]**
- Performance goals increasingly achieved through multiple cores with mixed architectures on single die **[10.2, 10.6, 10.7]**
- Significant increases in on-chip cache memory (26.8MB) **[10.1, 10.3, 10.4]**
- Next-generation multimedia processing using diverse cores and I/O techniques **[10.2, 10.5, 10.6, 10.7, 10.8]**
- A 32× increase in graphics processing per mW in 2 years **[10.6]**
- Dynamic voltage scaling with adaptive frequency control **[16.4, 16.5, 16.6]**
- On-die power measurement (never before implemented), temperature measurement, and management of each **[16.7]**
- High-speed digital circuits operating at up to 8GHz **[20.1, 20.3, 20.4]**
- Chip-to-chip I/O methods used in-package and on-die **[20.7, 28.7]**
- Asynchronous low-voltage design for a 1.47 billion-transistor cache **[26.8]**
- Clock generator that achieves 15× adjustable variation in clock rate with a cycle time of only 3 gate delays **[28.4]**
- High-speed I/O links up to 6.4Gb/s/ch **[28.6, 28.9]**
- A parallel interface tolerates up to 7 bits of skew between pins **[28.9]**

TECHNICAL HIGHLIGHTS (CONTINUED)

IMAGERS, MEMS AND DISPLAYS:

- A CMOS temperature sensor achieves a temperature accuracy of ±0.1°C over the temperature range of –55°C to +125°C. **[13.1]**
- A CMOS micro-sensor that can detect less than 1ppb of lead concentration uses a few thin-film post-processing steps. **[13.4]**
- The smallest pixel, yet announced, 1.56µm, is incorporated in a 3.1Mpixel FT-CCD optimized for mobile imaging **[19.1]**
- A dense 1Mpixel CMOS image sensor, created using a 3D fabrication technique, shows a possible direction for optimizing combinations of different technologies **[19.6]**
- A neural-monitoring system provides a significant amount of data compression (92%) for a three-dimensional 256-sensor site. **[30.4]**

MEMORY:

- NAND Flash breaks 8Gb barrier **[2.1, 2.2]**
- Multi-level NOR Flash operates at 166MHz **[2.6]**
- 2Gb DDR2 SDRAM achieves 800Mb/s/pin **[25.6]**
- eDRAM operating at 400MHz random cycle **[25.3]**
- First 256Mb SRAM **[26.2]**
- SRAMs operating at sub-0.5V **[26.3, 26.6]**
- Embedded L3 Cache increases to 24MB **[26.8]**

SIGNAL PROCESSING:

- Real-time high-definition H.264 video encoder **[7.1]**
- Low-power impulse-radio UWB transceiver. **[24.1]**
- High-data-rate LDPC-COFDM-based UWB transceiver. **[24.2]**
- WLAN-baseband transceiver w/MRC and Tx beamforming **[24.6]**
- Robust improved-throughput WLAN using a wideband approach for the Access Point. **[24.7]**
- Fully-integrated R/W 7XBD/16XDVD/56XCD SoC **[31.3]**

TECHNICAL HIGHLIGHTS (CONTINUED)

TECHNOLOGY DIRECTIONS:

- Demonstrated microscopic interface between neural and electronic systems **[4.1]**
- MEMS-based atomic clocks which are 700× smaller than the present art **[4.5]**
- Fully-functional MEMS gyroscope on conventional CMOS logicchip **[4.7]**
- A Rectifier IC for wireless power transmission up to 10m-distance **[14.1]**
- Three-dimensional integration schemes using wireless interconnects **[14.4, 14.5]**
- RF receiver architecture integrating on-chip MEMS-based high-Q inductors and tunable varactors, together with an array of parallel cantilever beams combining downconversion mixers and channel filters **[21.1]**
- First-time demonstration of integrating BAW filters above BiCMOS and their connection to the RF circuits below. This technique is used for the integration of a complete WCDMA RF front-end. **[21.2 and 21.3]**
- New RF communication devices and systems based on MEMS **[21.1, 21.2, 21.3, 21.5]**
- First CMOS 60GHz direct-conversion receiver featuring folded microstrip lines realized in 0.13µm CMOS and consuming 9mW from a 1.2V supply **[21.6]**
- New cascaded multi-stage distributed amplifier in 90nm CMOS achieves better than 7dB gain with a bandwidth of 70GHz **[21.7]**
- Organic transistors are integrated into flexible scanner and display **[32.2, 32.3]**

WIRELESS COMMUNICATIONS:

- First truly single-chip 802.11 WLAN transceivers in CMOS **[5.2, 5.3]**
- A 24 GHz Phased-Array Transmitter on 0.18µm CMOS **[11.7]**
- Ultra-Wide-Band Transceivers **[11.8, 11.9]**
- A single-chip Quad-Band GSM/GPRS Transceiver in 0.18µm Standard CMOS **[17.6]**
- A 120nm CMOS DVB-T Tuner **[23.3]**
- A CMOS TV Tuner/Demodulator IC with Digital Image Rejection **[23.4]**
- A Broadband 21 to 26 GHz SiGe BiPolar PA MMIC **[29.1]**
- A Noise-Cancellation Technique in Active RF-CMOS Mixers **[29.8]**

TECHNICAL HIGHLIGHTS (CONTINUED)

WIRELINE COMMUNICATIONS:

- 6.4Gb/s CMOS SerDes Core with Feed-Forward and Decision-Feedback Equalization **[3.2]**
- 6.25Gb/s Binary Adaptive Decision-Feedback Equalizer with First Post-Cursor Tap Cancellation **[3.5]**
- Circuit Techniques for a 40Gb/s Transmitter in 0.13μm CMOS **[8.1]**
- 3V 10.7Gb/s Differential Laser-Diode Driver with Active Back-Termination Output Stage **[12.1]**
- 20Gb/s VCSEL Driver and Regulated Output Impedance in 0.13μm CMOS **[12.2]**
- RF/Baseband FDMA-Interconnect Transceiver for Reconfigurable Multiple Access in Chip-to-Chip Communication **[18.6]**
- 0.94ps-rms-jitter 2.5GHz Multiphase Generator PLL for 10Gb/s Serial Links **[22.1]**
- 101dBc/Hz at 1MHz, 44GHz Differentially-Tuned VCO with 4GHz Tuning Range in 0.12μm SOI CMOS **[22.4]**

DISCUSSION SESSIONS

There are nine Discussion Sessions in all, three on each of Sunday, Monday and Tuesday Evenings. Of these, there are five Special-Topic Sessions, providing insight and background in a topical area.

SUNDAY

SE1 Powerline LAN: Is There a Concrete Wall Dividing Wireless from Wireline?

SE2 When Processors Hit the Power Wall (or "When the CPU hits the fan")

SE3 Integration in the 3rd Dimension: Opportunities and Challenges

MONDAY

E1 Mobile Imaging: Paradigm Shift or Technology Bubble?

E2 What Papers Will and Will Not Be at ISSCC2010?

SE4 Toward the Nanoscale Transistor - Highlights of 2004 Symposium on VLSI Technology

TUESDAY

SE5 SRAM Design in the Nanoscale Era

E3 RF MEMS: Fact or Stiction

E4 Driving Miss Ubiquity: What applications will fill tomorrow’s fabs?

SHORT COURSE:

Thursday, February 10, 2005

RF CIRCUIT DESIGN FROM TECHNOLOGY TO SYSTEMS

COURSE OBJECTIVE:

This Short Course is intended to provide both entry-level and experienced engineers with practical approaches to the design of RF circuitry in CMOS and BiCMOS technologies. Completing the course provides the attendee with an overall perspective of the technology considerations, circuit design issues and detailed design strategies for circuit building blocks for wired and wireless communication applications.

OVERVIEW:

- Technology Options for RF-ICs

  S. Simon Wong, *Stanford University* [8:00am, 10:00am]

- Wireless IC Building Blocks in CMOS/BiCMOS

  John Long, *Delft University of Technology* [10:00am, 12:00pm]

- Effects of Substrate on the RF Performance of Silicon Integrated Circuits

  Kenneth O, *University of Florida* [1:00pm, 3:00pm]

- Front-End Design for Wireless Systems

  Ranjit Gharpurey, *University of Michigan* [3:00pm, 5:00pm]

TUTORIALS:

Sunday, February 6, 2005

T1 INTEGRATED POWER MANAGEMENT
Roy Kaller, *SMSC*

T2 INTRODUCTION TO I/O DESIGN FOR DIGITAL SYSTEMS
Thucydides Xanthopoulos, *Cavium Networks*

T3 RF MEMS: DEVICES, CIRCUITS AND PACKAGING
Farrokh Ayazi, *Georgia Institute of Technology*

T4 PHASE-CHANGE MEMORY
Giulio Casagrande, *ST Microelectronics*

T5 DSP CIRCUIT TECHNOLOGIES FOR THE NANOSCALE ERA
Ram Krishnamurthy, *Intel*

T6 NANOTECHNOLOGY 101
H.-S. Philip Wong, *Stanford University*

T7 POLAR MODULATORS FOR LINEAR WIRELESS TRANSMITTERS
Antonio Montalvo, *Analog Devices*

T8 HIGH-SPEED ELECTRICAL INTERFACES: STANDARDS AND CIRCUITS
Yuriy M. Greshishchev, *PMC*

CIRCUIT DESIGN FORUMS:

Sunday, February 6, 2005

F1 CLOCK AND FREQUENCY GENERATION FOR WIRELINE AND WIRELESS APLLICATIONS

- Introduction
  Rudolf Koch, *Infineon,*
- Formulating Design Criteria for Frequency Generation for Wireless Applications
  Derek Shaeffer, *Aspendos Communications*
- Formulating Design Criteria for Clock Generation for Wireline Applications
  Takehiko Nakao, *Toshiba*
- Multiphase Ring Oscillators and Oscillator Phase Noise Modeling Techniques
  Robert Renninger, *Agere*
- VCO Design and Phase Noise Modelling
  Ali Hajimiri, *California Institute of Technology*
- Supply and Substrate Noise in VCOs
  Jan Craninckx, *IMEC*
- System Analysis, Simulation, Design and Optimization of PLL Frequency Synthesizers for Communication Systems
  Cicero Vaucher, *Philips*
- Design, Simulation, and Bandwidth Extension Methods for Fractional-N Frequency Synthesis
  Michael Perrott, *Massachusetts Institute of Technology*
- Spread Spectrum PLLs; Direct Modulation with Wideband PLLs
  Ivan Bietti, *STMicroelectronics*

F2 ADVANCED DYNAMIC MEMORY DESIGN

- Introduction
  Jinyong Chung, *POSTECH*
- High-Speed DRAM Design
  Young-Hyun Jun, *Samsung*
- DRAM I/O Interface
  Terry Lee, *Micron Technology*
- High Performance Embedded DRAM and test structures
  John Barth, *IBM*
- DRAM Design for Mobile Applications
  Martin Brox, *Infineon*
- Sub-1V DRAM Design
  Takayuki Kawahara, *Hitachi*
- DRAM in Nanoscale Era
  Tomoyuki Ishii, *Hitachi*

CIRCUIT DESIGN FORUMS:

Thursday, February 10, 2005

F3 CHARACTERIZATION OF SOLID-STATE IMAGE SENSORS

- Introduction
  Albert Theuwissen, *DALSA*
- Optics
  Nobukazu Teranishi, *Matsushita*
- Device Physics
  Dave Sackett, *Eastman Kodak*
- Design For Testability
  Bjornar Hernes, *Nordic Semiconductor*
- Electronic Circuits
  Lindsay Grant, *ST Microelectronics*
- Technology
  Shou-Gwo Wuu, *TSMC*
- ISO Sensitivity
  Rick Baer, *Agilent*
- Standardization
  Hirofumi Sumi, *Sony*

F4 ROBUST DESIGN SOLUTIONS FOR NANOSCALE CIRCUITS: FROM DFM THROUGH END-OF-LIFE

- Introduction
  Norman Rohrer, *IBM*
- Modelling DFM
  Clive Bittlestone, *Texas Instruments*
- VLSI Reliability Mechanisms - Considerations for Circuit Design
  Ron Bolam, *IBM*
- Optimization Techniques for Robust Design
  Jack Pippin, *Intel*
- Robust Circuit Designs, Flawed Circuit Designs
  David Greenhill, *Sun Microsystems*
- Robust SRAM Design
  Hyun-Geun Byun, *Samsung*
- Multi-Gb/s I/O Design Challenges in 65nm and Beyond
  Gerry Talbot, *AMD*
- Tolerant Architectures
  Hisashige Ando, Hitachi

CIRCUIT DESIGN FORUMS:

Thursday, February 10, 2005

F5 ATAC: AUTOMOTIVE TECHNOLOGY AND CIRCUITS

- Introduction
  Herman Casier, *AMIS*
- Automotive Systems and Markets
  Patrick Leteinturier, *Infineon*
- Semiconductor Technologies Support New Generation Hybrid Car
  Masayuki Hattori, *Toyota*
- SMARTMOS, the Ultimate Power, Analog, Mixed Signal Technology for Automotive Applications
  Hak-Yam Tsoi, *Freescale*
- In Vehicle Image Processing LSI for Driver Assistant Systems
  Shorin Koy, *NEC*
- Overview and Challenges of Data Communication in the Vehicle
  Stefan Poledna, *TTTech*
- A LIN Transceiver, a Case Study of Automotive Design
  Koen Appeltans, *AMIS*
- Future Lighting Systems for Vehicles
  Gunther Leising, Lumitech
- Smart Sensors for Automotive Applications
  Dirk Hammerschmidt, *Infineon*

ANALOG

- **Overview**
- **Featured Papers**
- **Panel**
- **Tutorial**

ISSCC 2005 – ANALOG

Subcommittee Chair: *David Robertson, Analog Devices, Wilmington, MA*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- Power-saving techniques pave the way to portable applications **[6.5, 15.3, 27.1]**
- A 22GS/s 6b DAC pushes the DAC-speed frontier **[6.7]**
- Low supply voltages, down to 0.5V, are demonstrated **[9.1, 27.8].**
- 90nm technology enters analog design, forcing low-voltage techniques **[9.2, 9.3, 15.2, 27.3, 27.4]**
- Delta-Sigma Converters extend their bandwidth beyond 20MHz **[9.5, 27.6]**

APPLICATIONS AND ECONOMIC IMPACT

- High-speed DACs provide direct synthesis of radio signals, enabling multiband transmitters and "software radio" architectures **[6.4, 6.7]**
- Mobile applications require ever-lower power and ever-increasing bandwidth to accommodate modern broadband technologies (3G cellular, WLAN, and beyond) **[6.5, 9.5, 15.2, 15.3]**
- Very-low-voltage techniques suggest the possibility of even-deeper submicron designs **[9.1, 27.8]**
- Very-low-voltage techniques are ideal for battery-operated analog design **[9.1, 27.8]**
- As Moore's law drives digital circuits to the deep submicron region, implementing analog functions on the same process node allows integration of SoCs for low-cost and small-footprint designs. **[9.2, 9.3, 27.7]**

PANEL

What Papers Will Be (and Will NOT Be) at ISSCC 2010? [E2]

TUTORIAL

Integrated Power Management [T1]

Response to the High Cost of Energy? Power Saving Rules ISSCC 2005

A 350MHz Low-OSR Delta-Sigma Current-Steering DAC with Active Termination in 0.13μm CMOS [6.5]

Infineon Technologies

A 50MS/s (35mW) to 1kS/s (15μW) Power-Scalable 10b Pipeline ADC with Minimal Bias-Current Variation [15.3]

University of Toronto

A 3mW 74dB SNR 2MHz Continuous-Time Delta-Sigma ADC with a Tracking-ADC Quantizer in 0.13μm CMOS [27.1]

Infineon Technologies

PRESENT STATE OF THE ART *(THE PROBLEM)*

- High-frequency or high-dynamic-range applications usually require lots of power due to high-speed or low-noise circuits.
- Power saving is crucial for portable applications, as well as for achieving high packing density.

NOVEL CONTRIBUTIONS

These papers work with several different techniques:

- Paper **6.5** provides a clever combination of Return-to-Zero coding and time interleaving to achieve top analog performance at a reduced switching rate.
- Paper **15.3** adapts not only bias currents, as others do, but extends that with a current-modulation technique. This leads to a total current variation range of 50000 to 1.
- Paper **27.1** eliminates most comparators usually needed in multibit ADCs in exploiting the signal statistics within a Sigma-Delta converter.

CURRENT AND PROJECTED SIGNIFICANCE

- Power saving: Enables wearable electronics.
- Power saving: Enables next-generation cellphones
- Power saving: Reduces size and weight
- Power saving: Keeps the lights on in California!

High-Speed D/A Converters

A 1.2GS/s 15b DAC for Precision Signal Generation [6.1]

Agilent Technologies

A 1.6GS/s Return-to-Zero GaAs RF DAC for Multiple Nyquist Operation [6.2]

Rockwell Scientific

A 1.7GHz 3V Direct-Digital Frequency Synthesizer with an On-Chip DAC in 0.35μm SiGe BiCMOS [6.3]

Rockwell Scientific

A 22GS/s 6b DAC with Integrated Digital Ramp Generator [6.7]

Nortel Networks; Institut fuer Mikroelektronik

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Speed of 6b D/As limited to about 10GS/s
- Direct-synthesis signal frequency limited to 700MHz.

NOVEL CONTRIBUTIONS

- Presampling and Return-to-Zero schemes achieve high signal quality at unprecedented speeds **[6.1, 6.2]**
- Improved state-of-the-art in signal generation **[6.2, 6.3]**
- New algorithm to calculate the DAC-codes in an energy-efficient way **[6.3]**
- Double the conversion speed of the current art, using a mainstream SiGe process **[6.7]**

CURRENT AND PROJECTED SIGNIFICANCE

- Enables direct synthesis of multi-carrier signals at higher IF, and even allows RF direct synthesis **[6.4, 6.7]**
- Another important step toward “software radio” **[6.4, 6.7]**

High-Bandwidth Delta-Sigma ADCs

An 80MHz 4x Oversampled Cascaded Delta-Sigma-Pipelined ADC with 75dB DR and 87dB SFDR [9.5]

ST Microelectronics; University of Pavia

A 43mW Continuous-Time Complex Delta-Sigma ADC with 23MHz of Signal Bandwidth and 68.8dB SNDR [27.6]

University of Toronto

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Sigma-Delta converters are known to be very power-efficient. However, due to the required oversampling, they are limited in signal bandwidth

NOVEL CONTRIBUTIONS

- Combination of a sigma-delta with a pipelined converter employing digital background algorithms **[9.5].**
- Improved complex noiseshaper **[27.6]**.

CURRENT AND PROJECTED SIGNIFICANCE

- High-bandwidth sigma-delta converters enable high-speed communication services like VDSL, WLAN baseband, as well as direct digitization of low-IF receivers, which is important for “software radio” **[9.5, 27.6]**

90nm Technology Enters Analog Design, Enforcing Low-Voltage Techniques

A Low-Power Multi-Bit Delta-Sigma Modulator in 90nm Digital CMOS without Dynamic Element Matching [9.2]

Texas Instruments and University of Texas

A 66dB DR 1.2V 1.2mW Single-Amplifier Double-Sampling 2nd-order Delta-Sigma ADC for WCDMA in 90nm CMOS [9.3]

Texas Instruments

A 3.3mW 12MS/s 10b Pipelined ADC in 90nm Digital CMOS [15.2]

University of Toronto; Texas Instruments

A 0.5V Filter with PLL-Based Tuning in 0.18μm CMOS [27.8]

Columbia University

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Deep-sub-micron CMOS demands analog-circuit operation with lower supply voltages.
- SoCs in 90nm CMOS require analog circuits to consume even less power.

NOVEL CONTRIBUTIONS

- Designs achieving excellent figures of merit despite low-voltage operation **[9.2, 27.8]**
- New architecture which modifies the $\Delta\Sigma$ feedback loop to truncate ADC output **[9.2]**.
- Use of a single amplifier with double switching **[9.3]**.
- Switched input buffers and op-amps enable lower power dissipation **[15.2]**.

CURRENT AND PROJECTED SIGNIFICANCE

- Implementations in 90nm CMOS is becoming a mainstream technology.
- Analog circuits begin to adapt to 90 nm **[9.2, 9.3, 15.2, 27.3, and 27.4]**.
- Operation at voltages down to 0.5V. **[27.8]**

Panel

What Papers Will Be (and Will NOT Be) at ISSCC 2010?

Organizer: ***Axel Thomsen****, Silicon Laboratories*
Moderator: ***David Robertson****, Analog Devices*

OBJECTIVE

- What will be the hot technology topics 5 years from now?
- How will the Conference need to evolve to effectively capture these technology shifts?

CHALLENGE

- Moore's Law and market demand will force higher integration, higher performance, and more features. IC design is moving increasingly from a device-level to a system-integration challenge.
- MOSFET device properties deteriorate from an analog perspective – leakage and low output impedance become significant as supply voltages are reduced.
- The business environment for integrated circuits is changing—global competition, expensive mask sets, and short product-life cycles, cloud the horizon. Regrettably, these conditions may not be conducive to publication: Is industry likely to withdraw from publishing their new ideas?

CONTROVERSY

- Will advanced process technologies force new efforts in transistor-level "subcircuit" design, or will a few circuit topologies survive and thrive, limiting advances mainly to those attributable to the level of integration (corresponding to the evolution of digital design in the 1980s)?
- Is all meaningful innovation reduced to the choice of system integration required to achieve the usual objectives of more features and higher integration? Will papers on transistor-level design fade from the Conference?
- What are the most important technology changes to be expected over the next 5 years? Is the Conference set up to capture these changes effectively?

Tutorial

Integrated Power Management

Roy Kaller, SMSC, Phoenix, AZ

OVERVIEW

Technology advance in integrated circuits means shrinking lithography and an increasing level of integration. Shrinking lithography means reduced supply voltages, and increasing integration means bringing more functionality onto a single chip. Inevitably, a critical part of the integration problem is the generation and management of the variety of supply voltages required in today's system-on-a-chip products. This tutorial explores the basics of modern integrated-power management circuits, including:

- Trade-offs between modern power-conversion technologies
- Integrated power-management strategies for CMOS systems-on-a-chip
- New and future power sources for mobile consumer products

SPEAKER BIOGRAPHY

Roy Kaller is Vice President of Engineering at SMSC in Phoenix, AZ, where he is responsible for analog-technology development and design automation. He joined SMSC as part of the company's acquisition of Gain Technology Corporation in June 2002. Prior to joining Gain Technology in 2000, he was the founder and director of National Semiconductor's Power-Management design center in Grass Valley, CA. From 1992 until 1995, Roy was a design-engineering manager for Silicon Systems. He started his career at Burr-Brown Corporation in 1983, where he developed a broad range of products including precision op-amps, MUXs, DACs, and ADCs. Roy has been a member of the ISSCC Analog Sub-Committee since 2002, has published eight papers, and holds one patent in the area of analog integrated circuits and solid-state chemistry. Roy earned his BSEE from the University of Arizona, and is a graduate of the University's Arizona Executive Program.

NOTES

DIGITAL

- **Overview**
- **Featured Papers**
- **Special-Topic Session**
- **Tutorial**
- **Forum**
- **Trend Charts**

ISSCC 2005 – DIGITAL

Subcommittee Chair: *William J. Bowhill, Intel, Shrewsbury, MA*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- 1.7B transistors integrated on a single die **[10.1]**
- Chip-level multiprocessing focused on parallelism and power efficiency **[10.1, 10.3, 10.4]**
- Significant increases in on-chip cache memory **[10.1, 10.3, 10.4]**
- Next-generation multimedia processing using diverse cores and I/O techniques **[10.2, 10.5, 10.6, 10.7, 10.8]**
- Advances in Power Management:

  Typically, microprocessors are designed for a specific frequency target, leading to increased variation between average and peak power consumption, and uncontrolled junction temperature. In addition, due to the fixed-frequency requirement, voltage margin is required, leading to additional power consumption. The Itanium® microprocessor featured in this Conference employs integrated control mechanisms that keep the power dissipation constant at 100W, while varying the frequency. In this fashion, power is minimized by the removal of the voltage margin, and frequency is maximized, given the power-design target. **[10.1, 16.2, 16.7]**. This approach has cut the power dissipation of a 1.75B-transistor dual-core Itanium® processor **[10.1]** to one third (to 100W from 300W)

  As a result, processor power density has fallen below the trend predicted by past published processor disclosures *(see the Watts/mm^2 Trend Chart)*
- Dynamic voltage scaling with adaptive frequency control **[16.4, 16.5, 16.6]**
- High-speed circuits operating at up to 8GHz **[20.1, 20.3, 20.4]**
- Chip-to-chip I/O methods used in-package and on-die **[20.7, 28.7]**
- High-speed I/O links up to 6.4Gb/s/ch **[28.6, 28.9]**

APPLICATIONS AND ECONOMIC IMPACT

- Multi-core multi-threaded processors enable higher parallelism, and improve application processing **[10.1, 10.2, 10.3, 10.4]**
- Large on-chip caches improve memory bandwidth for "big tin" applications such as massive web servers, database management, and deep science **[10.1, 10.3, 10.4]**
- Next-generation multimedia processors slash the time required for content-creation and digital media **[10.2, 10.5, 10.6, 10.7, 10.8]**
- Improved methods for adapting voltage and frequency enable processors to eke out maximum performance without over-heating **[16.4, 16.5, 16.6]**
- Bringing chip-to-chip I/O methods on-die breaks through the RC barrier **[20.7, 28.7]**
- High-speed I/O links take system bandwidths to a higher level **[28.6, 28.9]**

SPECIAL-TOPIC SESSION

When Processors Hit the Power Wall (or "When the CPU hits the fan") [SE2]

TUTORIAL

Introduction to I/O Design for Digital Systems [T2]

FORUM

Robust Design Solutions for Nanoscale Circuits:
From DFM through End-of-Life [F4]

CELL Processor from IBM, Sony, Toshiba:

A High-Frequency Multi-Core System-on-a-Chip

Five papers as detailed in the attached figure [7.4, 10.2, 20.3, 26.7, 28.9]

PRESENT STATE OF THE ART

- General-Purpose processors are inefficient for multimedia streaming workloads
- Multichip systems are expensive, limited by chip-to-chip communication bottlenecks
- Power-performance concerns arise with conventional multi-processor systems
- Low-frequency ASIC designs provide insufficient processing power

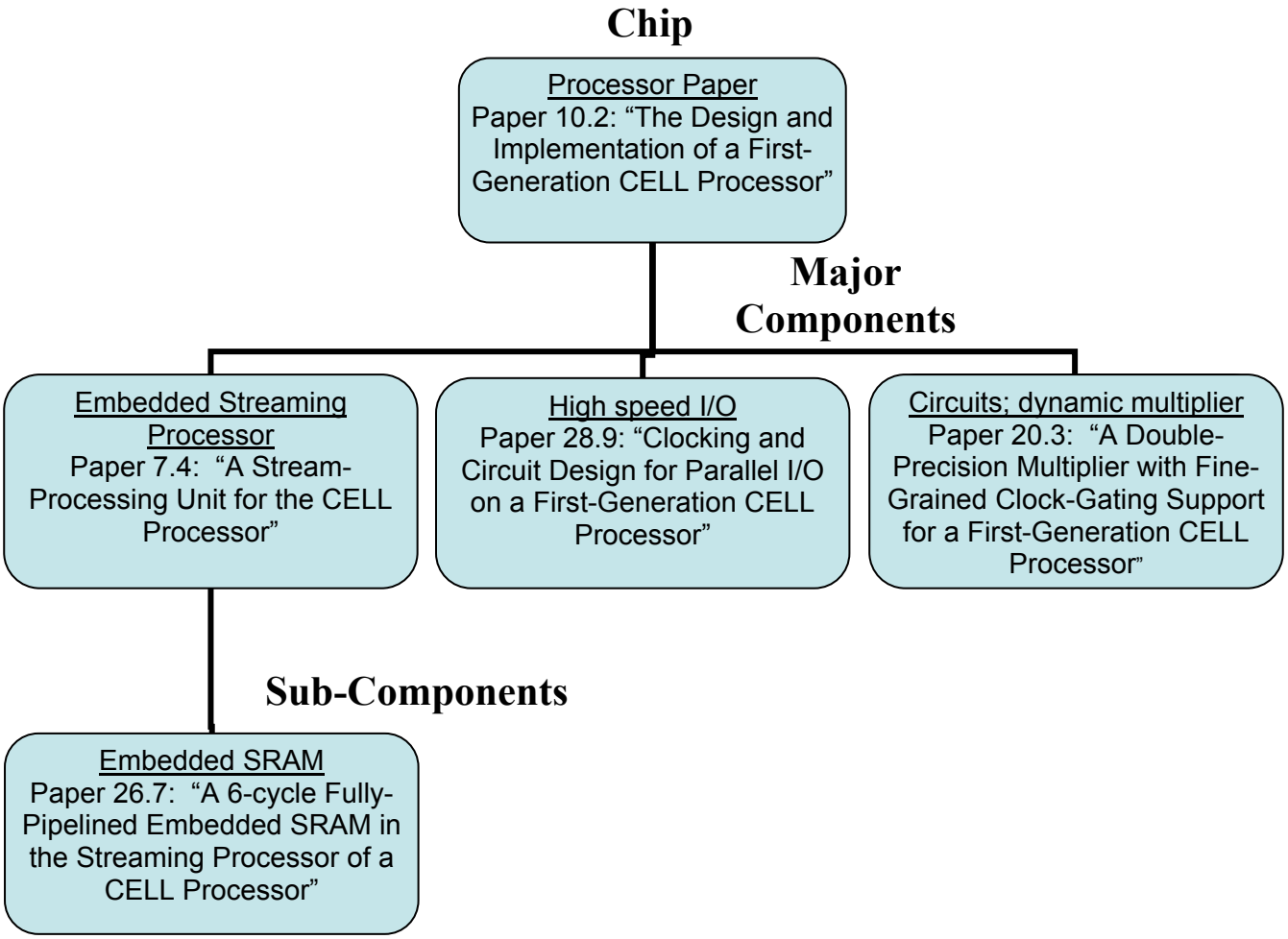
NOVEL CONTRIBUTIONS

- Streaming processor emphasizing performance per unit area, and power **[7.4]**
- High level of integration on-chip: general-purpose processor, specialized streaming processors, memory controller, flexible high-speed I/O **[10.2]**
- High-speed circuit elements: dynamic multiplier **[20.3],** SRAM **[26.7]**
- 6.4 Gb/s/link I/O for high-bandwidth off-chip communication **[28.9]**

CURRENT AND PROJECTED SIGNIFICANCE

- New level of performance for multimedia content creation and processing **[7.4,10.2]**
- Single-chip power-optimized solution for high-speed computing **[10.2]**

CELL Processor: Paper Breakdown and Organization



Itanium Breaks New Ground in Both Complexity and Power Consumption

See the next two pages for paper organization and breakdown [10.1, 16.1, 16.2, 16.7, 26.8]

PRESENT STATE OF THE ART

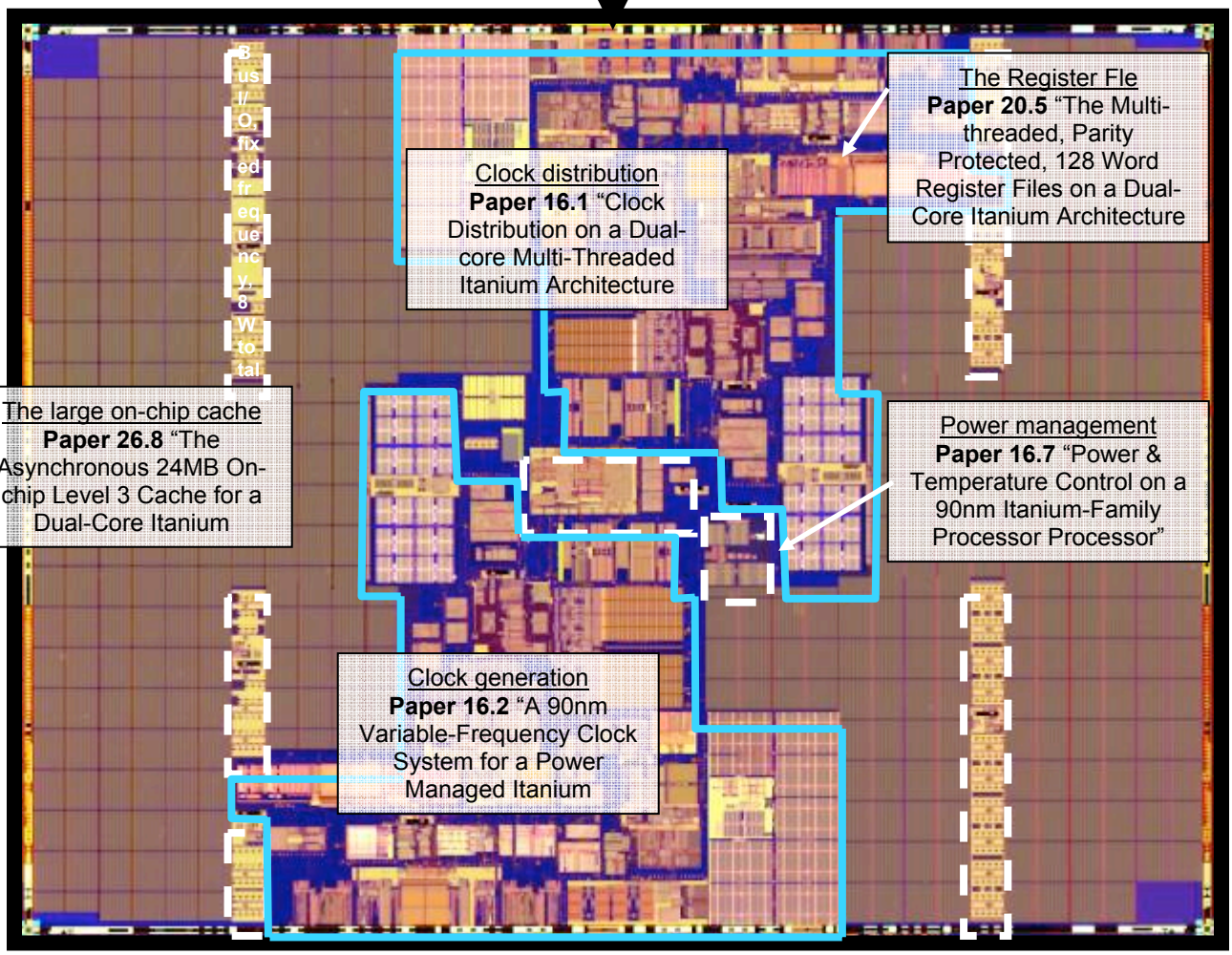
- In the processor world, size is always associated with high power, so that to exploit the large number of transistors provided by Moore's law, improved performance has traditionally required low-power design.
- Truly managing power requires measuring power, but this is difficult for high-power VLSI, and has not been done before
- Squeezing the most performance per watt requires continuously-varying voltage and frequency, but, in conflict, the resulting unstable chaotic behavior has run into insurmountable barriers for commercial designs, due to associated manufacturing and implementation issues.

NOVEL CONTRIBUTIONS

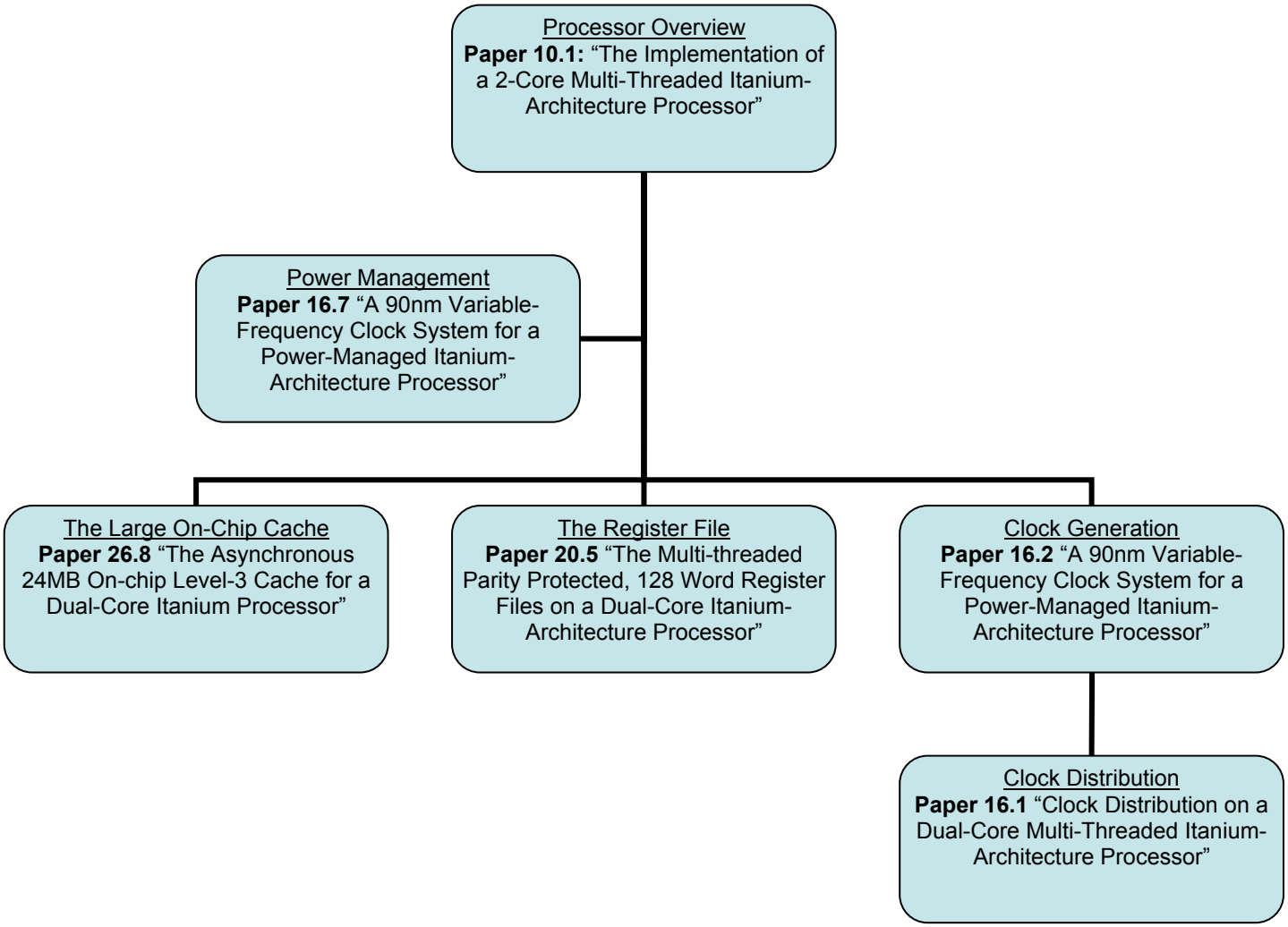
- Unprecedented integration (1.72 billion transistors), combined with adaptive power management, result in high performance at low power levels (100W). **[10.1]**
- Dynamic frequency generation and management to provide the optimal power efficiency for a given voltage **[16.2, 16.1]**
- On-die power measurement (never before implemented), temperature measurement, and management of each **[16.7]**
- Asynchronous low-voltage design for a 1.47 billion-transistor cache. **[26.8]**

Itanium-Processor-Paper Breakdown and Organization

Processor Overview
Paper 10.1 "The Implementation of a 2-core Multi-Threaded Itanium-Architecture Processor"



Itanium-Processor-Paper Breakdown and Organization



New Processors Focus on Parallelism and Power Efficiency

The Implementation of a 2-Core Multi-Threaded Itanium®-Family Processor [10.1]

Hewlett Packard; Intel

The Design and Implementation of a First-Generation CELL Processor [10.2]

IBM, Sony, Toshiba

Implementation of a 4th-Generation 1.8GHz Dual-Core SPARC V9 Microprocessor [10.3]

Sun Microsystems

Creating the BlueGene/L Supercomputer from Low-Power SoC ASICs [10.4]

IBM

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Design teams continue to struggle with the best use of (now) billions of transistors
- Power density and thermal challenges provide major design constraints
- Support of leading-edge applications requires increasingly diverse and specialized computational hardware support

NOVEL CONTRIBUTIONS

- 1.7 billion transistors on die, with over 1 billion transistors of cache **[10.1]**
- Power-density stabilizing in high-end processors via novel power-management techniques **[10.1, 10.3]**
- Multithreading and multi-core techniques proliferate **[10.1, 10.2 10.3, 10.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- Diverse-core implementations bridge the space between the general-purpose and DSP domains **[10.2]**
- Integrated power management and low-power design allow next-generation servers to remain within current thermal envelopes **[10.1, 10.3]**
- Dual-core chip forms a building block for the Top500 list's fastest computer **[10.4]**

Launching Next-Generation Multimedia: Diversity in Cores

The Design and Implementation of a First-Generation CELL Processor [10.2]

IBM, Sony, Toshiba

An SoC with 1.3 Gtexels 3D-Graphics Full-Pipeline Engine for Consumer Applications [10.5]

KAIST; Samsung

A 50 Mvertices/s Graphics Processor with Fixed-Point Programmable Vertex Shader for Mobile Application [10.6]

KAIST

A 51.2 GOPS 1.0 GB/s-DMA Single-Chip Multi-Processor Integrating Quadruple 8-Way VLIW Processors [10.7]

Fujitsu

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Insatiable demand continues for increased multimedia performance, including 3D graphics.
- Fundamental tension heightens between performance, energy???, and flexibility.
- DSP applications demand mixed-signal I/O.

NOVEL CONTRIBUTIONS

- Dedicated special-purpose-processor arrays for multimedia **[10.2]**
- Performance goals increasingly achieved through multiple cores with mixed architectures on single die **[10.2, 10.6, 10.7]**
- A 32x increase in graphics processing per mW in 2 years **[10.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- Media processors approaching the complexity of last-generation microprocessors, with continued growth in on-chip cores **[10.2, 10.5, 10.6, 10.7]**
- Specialized functional units allow power densities to fall an order of magnitude below general-purpose counterparts **[10.5, 10.6]**
- Continued march toward goal of high-resolution video on portable devices such as cell phones and PDAs **[10.6]**

Processor Self-Discipline: On-Die Systems Manage Power, Frequency, and Temperature Dynamically

A 90nm Variable-Frequency-Clock System for a Power-Managed Itanium®-Family Processor [16.2]

Hewlett Packard; Intel

Deterministic Inter-Core Synchronization with Periodically-All-in-Phase Clocking for Low-Power Multi-Core SoCs [16.3]

NEC

Power and Temperature Control on a 90nm Itanium®-Family Processor [16.7]

Hewlett Packard; Intel

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Advanced low-voltage CMOS technologies suffer from high current consumption.
- Variation due to manufacturing-process effects on transistor features, on-die supply voltage, and localized temperature, cause degradation of power and frequency of high-performance processing circuits.
- Use of multiple on-die supply voltages, to alleviate power and temperature variation, causes difficulty in intra-die communication between modules using different supply voltages.

NOVEL CONTRIBUTIONS

- Dynamic on-die frequency adjustment as a function of internal supply-voltage transients yields up to 10% increase in processor frequency relative to fixed-supply-voltage systems. **[16.2]**
- Periodically-all-in-phase clocking and deterministic synchronous bus wrappers enable communication for multi-core DVFS SoCs that run at different supply voltages. A maximum of 60% power reduction in MPEG4 decoding with 1.5 to 2x throughput is achieved. **[16.3]**
- Embedded feedback and control system maximizes performance while staying within target power and temperature constraints. The system utilizes on-die sensors and an embedded micro-controller to measure power and temperature, and modulate the processor's voltage and frequency. **[16.7]**

CURRENT AND PROJECTED SIGNIFICANCE

- Dynamic frequency adjustment, as a function of supply voltage increases product performance and helps extend Moore's Law. **[16.2]**
- The ability to adjust the communication-link properties of internal sections of a chip running at different voltages enables lower energy consumption and possible increases in system throughput. **[16.3]**
- "Self-Controlling" (i.e. adaptive) temperature and power processing increases performance and reduces energy. **[16.7]**

High-Performance Arithmetic Units

An 8GHz Floating-Point Multiply [20.1]

IBM

A Double-Precision Multiplier with Fine-Grained Clock- Gating Support for a First-Generation CELL Processor [20.3]

IBM

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Balancing floating-point speed with power dissipation is always a high priority in microprocessor design. Circuit designers strive to improve these two figures of merit.

NOVEL CONTRIBUTIONS

- 2 to 8 GHz multiplication speed with 150mW to 1.8W power dissipation, respectively. **[20.1]**
- Single-phase clocking used with same-polarity level-sensitive latches to minimize cycle time. **[20.1]**
- Bit replication in the partial-product-generation process is used to reduce wire lengths and improve speed. **[20.3]**

CURRENT AND PROJECTED SIGNIFICANCE

- Good engineering can still lead to substantial performance improvements without resorting to exotic circuit designs. **[20.1, 20.3]**

On-Chip Interconects

A 3Gb/s/ch Transceiver for RC-limited On-Chip Interconnects [20.7]

University of Twente; Philips

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Using standard repeaters for long on-chip interconnections has bandwidth and latency limitations. In addition, such a design costs power and is susceptible to noise and crosstalk.

NOVEL CONTRIBUTIONS

- Transmitter can drive 10mm of minimum-size wire without repeaters at 3Gb/s, consuming 6mW at 1.2V **[20.7]**
- Off-chip techniques, such as pre-emphasis using a simple 2-tap digital filter, are used **[20.7]**

CURRENT AND PROJECTED SIGNIFICANCE

- On-chip interconnects without standard repeaters may appear in future chips due to bandwidth and power constraints. This work proposes a viable alternative to repeaters using a simple transmitter/receiver design and minimum-size wires **[20.7]**

High-Precision Clock Generation and Distribution for Processors and I/O

A CMOS DLL-Based 120MHz to 1.8GHz Clock Generator for Dynamic Frequency Scaling [28.4]

Korea University

Clocking and Circuit Design for Parallel I/O on a First-Generation CELL Processor [28.9]

Rambus; Stanford University

PRESENT STATE OF THE ART

- Processors need to maximize performance and minimize power dissipation for different workloads. As a result, on-chip supply voltage and frequency need to be dynamically adjusted as a result.
- High operating frequencies require low timing noise from the variable-frequency clock.
- Processors need multi-gigabytes-per-second transfer rates between chips to satisfy off-chip data-bandwidth requirements. Timing noise and alignment between I/O pins are critical.

NOVEL CONTRIBUTIONS

- A dynamic frequency step can be adjusted within one cycle of operation without glitches. **[28.4]**
- Clock generator that achieves 15× adjustable variation in clock rate with a cycle time of only 3 gate delays. **[28.4]**
- A dynamic-frequency clock demonstrates peak-to-peak uncertainty of less than 1/10 of a logic-gate delay. **[28.4]**
- Energy per bit transferred is 20pJ. **[28.9]**
- An aggregate data transfer rate that exceeds 0.5 terabits-per-second. **[28.9]**
- A parallel interface tolerates up to 7 bits of skew between pins. **[28.9]**

CURRENT AND PROJECTED SIGNIFICANCE

- Dynamic frequency scaling enables 2 to 4× power reduction for next-generation processors. The adaptable frequency also leads to 10 to 20% improvement in processor performance. **[28.4]**
- Low-jitter clock generation and distribution enables ultra-short-cycle-time processor designs. **[28.4, 28.9]**
- Low I/O power combined with high transfer rates enables future multi-terabits-per-second aggregate off-chip data bandwidth. **[28.9]**

SPECIAL-TOPIC SESSION

When Processors Hit the Power Wall (or "When the CPU hits the fan")

Organizer: ***Sam Naffziger****, Hewlett Packard, Fort Collins, CO*
Chair: ***James Warnock****, IBM, Yorktown Heights, NY*

OVERVIEW

- Power consumption and heat removal have become first-order limiters of the "Moore's Law" predictions of the growth of processor performance. This limitation has bubbled up from mobile devices to the desktop, and, now, even server processors are investing heavily in technology that manages and reduces power consumption. The result is a fundamental shift in how circuit designers and architects attempt to extract higher performance from each new design generation. No aspect of the processor-design ecosystem goes untouched: silicon process technology, circuit design, computer architecture, packaging, and cooling, are all facing fundamental shifts in their methodologies and priorities.

OBJECTIVE

- This Special-Topic Session explores the power-consumption problem of leading-edge processors, and possible technology directions in architecture, circuits and cooling.

CHALLENGE

- Power consumption, as a primary limiter of the historical increase in computing capability, requires a host of innovations to address it.
- There is no "silver bullet" solution to enable sufficient power efficiency to provide historic silicon-scaling benefits. The problem must be addressed at many levels, from the way designers architect the processors, to the circuit choices made, along with the incorporation of new power and thermal-management capabilities.

STRUCTURE

- **Hendrik Hamann, IBM: *"Spatially-Resolved Imaging of Microprocessor Power"***

  This talk presents static and dynamic temperature and power distributions, as a function of clock frequency, core voltage, and workload. The impact of high-power density regions and hot spots in microprocessor circuits is discussed.

- **T. Sakurai, University of Tokyo: *"Adaptive Techniques for Managing Power Consumption"***

  In this talk, adaptive techniques are explained from the viewpoints of what to monitor (power? temperature?), how to monitor, what to control (voltage?, frequency?), how to control, and granularity of control.

- **Dave Ditzel, Transmeta: *"Low-Power High-Performance Architectures"***

  This talk will review a variety of high- performance "so-called" low-power PC processors, identify what they mean by low-power, and identify various mechanisms used to lower power for high-performance PC-compatible systems.

- **Bill Dally, Stanford University: *"Power Efficient Stream Architectures"***

  This talk describes how a power-efficient stream architecture minimizes data movement and instruction overhead to give efficiency comparable to ASIC solutions.

- **Ken Goodson, Stanford University: *"Advanced Cooling for High-Performance VLSI"***

  This talk will illustrate low heat transfer within the microprocessor chip influences circuit performance and reliability of high-performance VLSI systems. This issue is motivating much research on advanced cooling technologies, ranging from chip-integrated micro-channel cooling, thermoelectric management of localized hotspots, and advanced materials with high thermal conductivity.

RECAP

- This session will provide insights into what the brightest minds in industry and academia are thinking in regard to solving the problems that increasing power consumption creates for the computer industry.

Tutorial

Introduction to I/O Design for Digital Systems

Thucydides Xanthopoulos, Cavium Networks, Marlboro MA

OVERVIEW

- Transmission-Line Fundamentals
- Elements of Transmitter/ Receiver Design
- Electrostatic-Discharge-Protection Overview
- Advanced Techniques (Differential Design, PVT Compensation, On-Die Termination)
- Clocking for I/O Design

SPEAKER BIOGRAPHY

Thucydides Xanthopoulos received his BS, MS and PhD degrees in Electrical Engineering and Computer Science from the Massachusetts Institute of Technology in 1992, 1995, and 1999, respectively. From 1999 to 2001, he was a consulting engineer with the Alpha Development Group, Compaq Computer, in Shrewsbury MA, where he designed the clock- generation and distribution network for the Alpha 21364 server processor (EV7). Since 2001, he has been a Principal Member of Technical Staff with Cavium Networks in Marlboro MA, where he co-leads silicon implementation of security- and-network-services processors, and is primarily responsible for I/O, clocking, power distribution, and package design.

Advanced Circuits Forum

Robust Design Solutions For Nanoscale Circuits: From DFM through End-of-Life

Objective

Circuit and design techniques for robust and reliable designs in sub-100nmtechnologies. Attendance is limited, and pre-registration is required. This all-day workshop encourages open interchange in a closed forum.

Audience

The forum is targeted at circuit designers working on the advanced development and design of chips in 90nm and 65 nm technologies, who need to understand how circuit and device manufacturability and reliability limits will impact their designs.

Scope

65nm and 90nm technologies are putting the squeeze on CMOS circuit design, requiring careful design for manufacturability (DFM) and reliability. From product concept through design to end-of-life, the need for improved modeling and design margining continues to increase. For example, device voltage-operating-range is limited at the upper-end by hot electron effects and gate- oxide failure, while the lower voltage bounds are constrained by functionality and SRAM stability. This forum will address DFM, reliability-design tools, design styles and architectures, to provide high-quality reliable products.

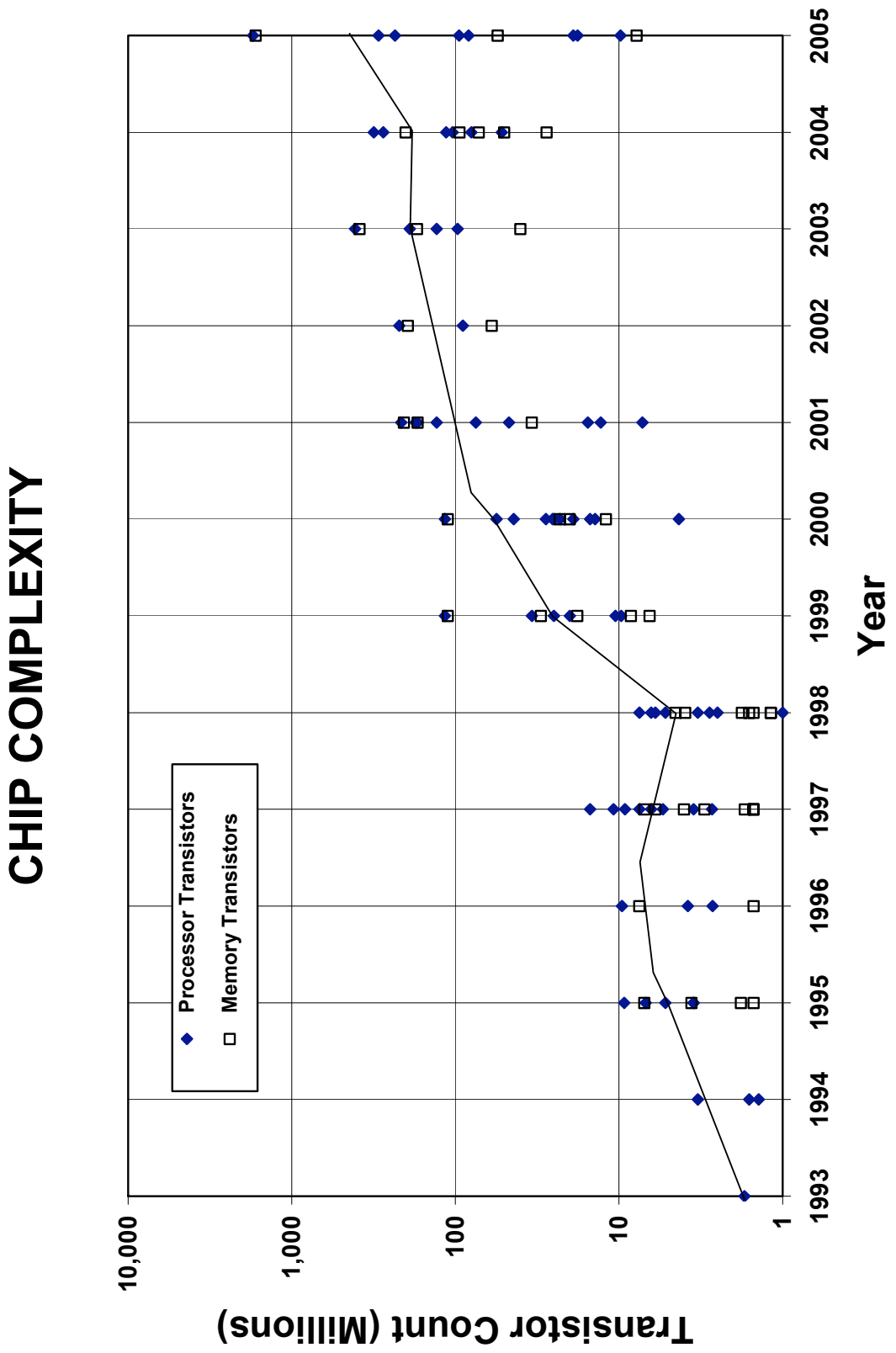
Program

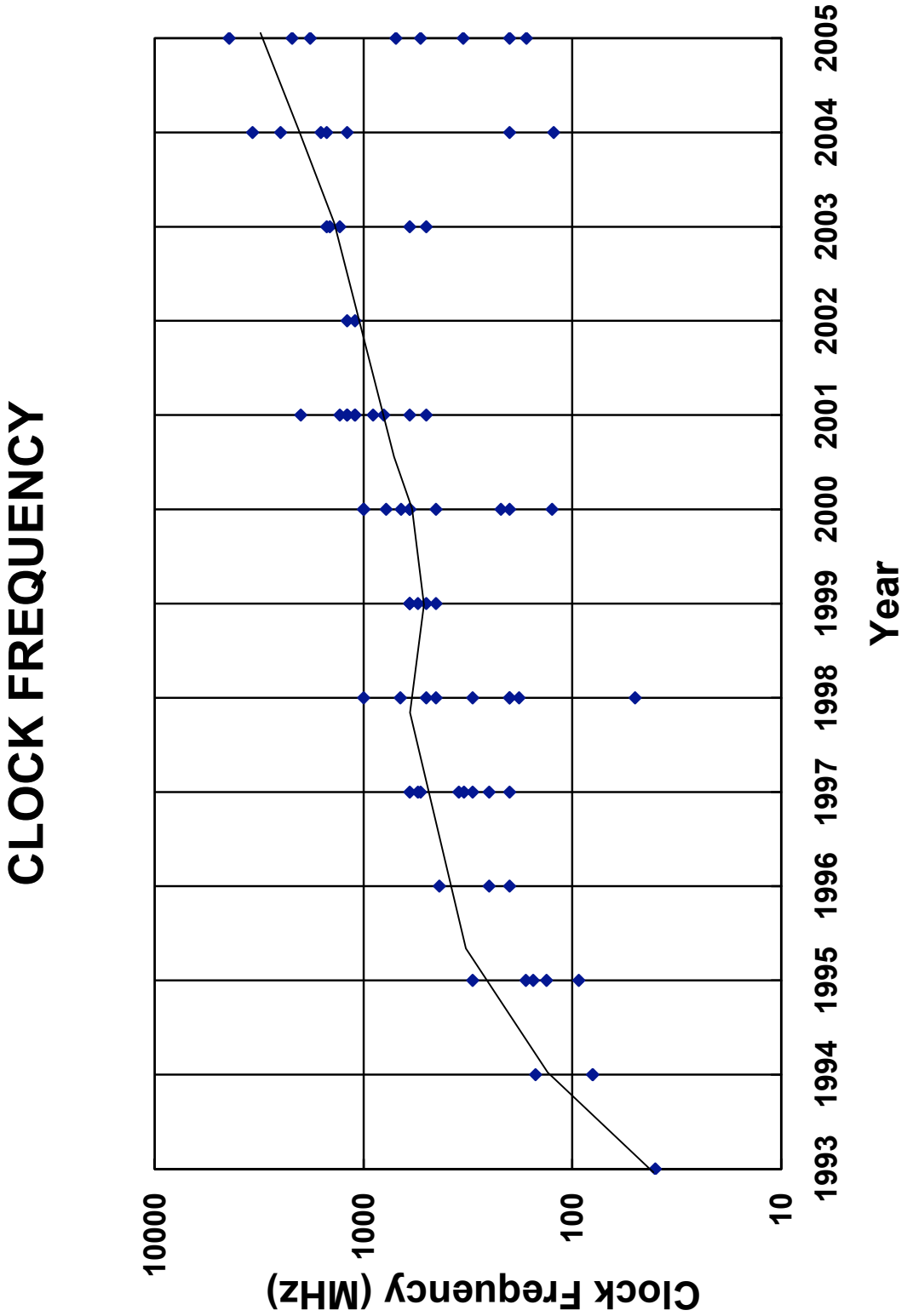
Design for manufacturability is a critical step for advanced lithography. **Clive Bittlestone** will start the forum by discussing Optical Proximity Correction (OPC) techniques. **Ron Bolam** will provide details of nano-scale reliability mechanisms and trends for hot-electron effects, NBTI, gate oxide reliability and electromigration pertinent to circuit design.

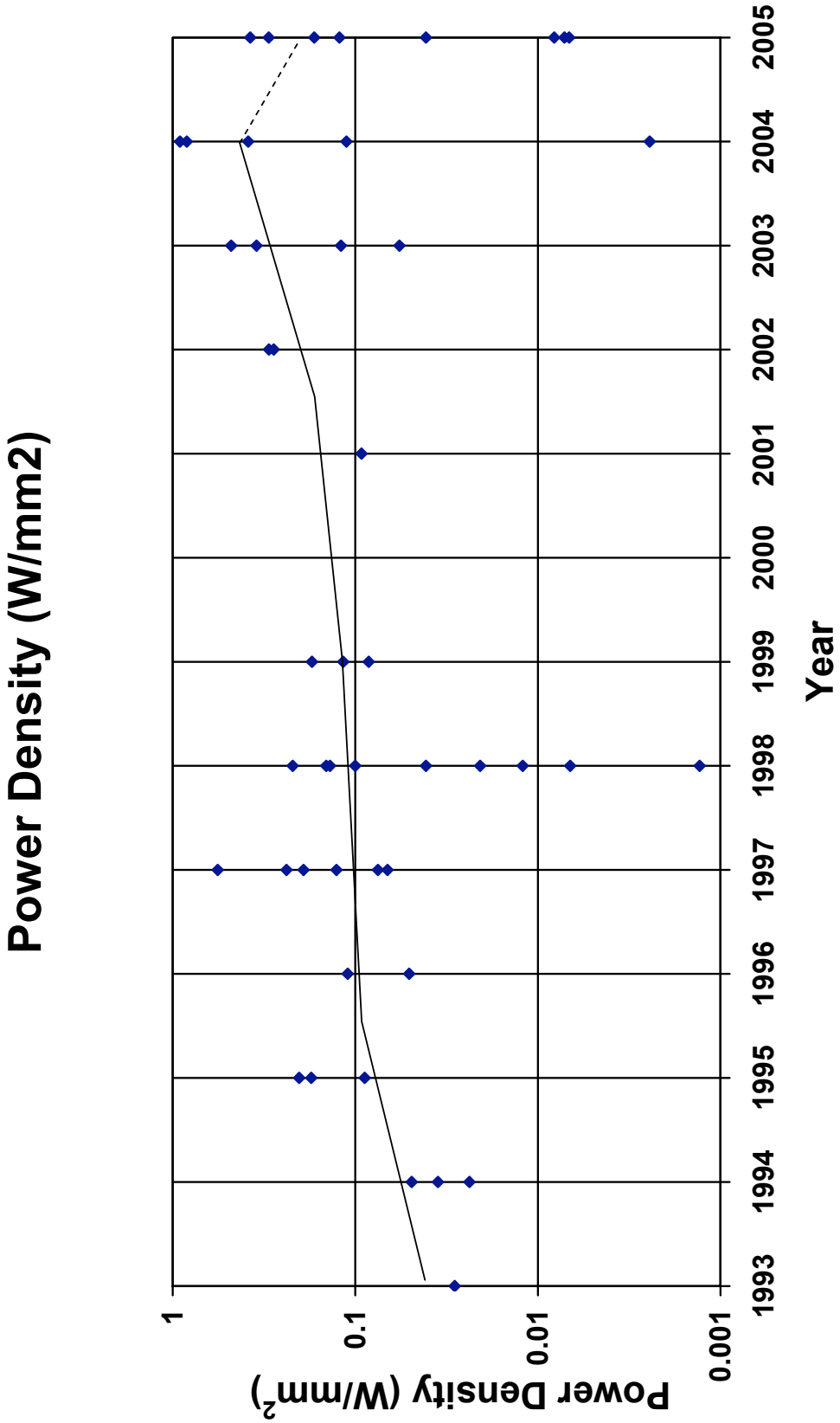
Jack Pippin's will focus on the tools and techniques of circuit analysis required to optimize circuits within reliability constraints. **David Greenhill** will show which circuit design styles are the most robust across the device operating life. **Hyun-Geun Byun** will focus on SRAM reliability and methods to cover SER and low-voltage stability. Included with the SRAM discussion will be a new cell and the methods of testing.

High-speed I/O design issues that will be discussed include the use of logic devices, and the increasing demand for higher data rates. **Gerry Talbot** will present solutions and methods for I/O design in 65nm technologies. Finally, **Hisashige Ando** will present architectures that are tolerant to failures–in-time in SRAM and logic functions.

The full-day expert analysis and presentation will conclude with a question-and-answer discussion.







IMAGERS, MEMS & DISPLAYS

- **Overview**
- **Featured Papers**
- **Panel**
- **Tutorial**
- **Forum**

ISSCC 2005 – IMAGERS, MEMS & DISPLAYS

Subcommittee Chair: *R. Daniel McGrath, Eastman Kodak, Rochester, NY*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- A CMOS temperature sensor achieves a temperature accuracy of ±0.1°C over the temperature range of –55°C to +125°C. **[13.1]**
- A CMOS micro-sensor that can detect less than 1ppb of lead concentration uses a few thin-film post-processing steps. **[13.4]**
- The smallest pixel, yet announced, 1.56μm, is incorporated in a 3.1Mpixel FT-CCD optimized for mobile imaging **[19.1]**
- A dense 1Mpixel CMOS image sensor, created using a 3D fabrication technique, shows a possible direction for optimizing combinations of different technologies **[19.6]**
- A neural-monitoring system provides a significant amount of data compression (92%) for a three-dimensional 256-sensor site. **[30.4]**

APPLICATIONS AND ECONOMIC IMPACT

- Low-cost accurate temperature measurement at the low power levels needed in many applications including wireless sensor networks **[13.1]**
- Low-cost low-power heavy-metal micro-detectors provide a possibility of remote interrogation **[13.4]**
- Digital imaging, for smaller and higher-resolution camera-phones and Digital Still Cameras in a multi-billion-dollar market **[19.1]**
- 3D fabrication provides many possibilities for technology optimization. The techniques demonstrated could allow more functions to be integrated within an imager, making it smarter and of higher quality **[19.6]**
- Basic research on neural activity and brain operation, aimed, for example, at healing of nerve-related diseases **[30.4]**

PANEL

Mobile Imaging: Paradigm Shift or Technology Bubble? [E1]

TUTORIAL

RF MEMS: Devices, Circuits & Packaging [T3]

FORUM

Characterization of Solid-State Sensors [F3]

Temperature Sensing

A CMOS Temperature Sensor with a 3σ Inaccuracy of ±0.1°C from –55°C to 125°C [13.1]

Delft University of Technolgoy

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Low-cost and accurate temperature measurement at low power levels is needed in many applications.
- Difficulty of maintaining temperature accuracy better than 0.5°C over the military and industrial temperature range of –55°C to 125°C.

NOVEL CONTRIBUTIONS

- Five times improvement over prior art **[13.1]**
- Chip area of 4.5mm^2 **[13.1]**
- Requirement of 75μA from a 2.5 to 5.5V supply **[13.1]**

CURRENT AND PROJECTED SIGNIFICANCE

- Low-power precision temperature sensing using microwatts of power **[13.1]**
- Ideal temperature sensor for low-cost wireless-sensor networks **[13.1]**

Toxic-Metal Monitoring

A Microsystem for Trace Environmental Monitoring [13.4]

University of Michigan; Analog Devices; University of Utah

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Heavy metals such as lead and mercury can cause long-term health problems, even at trace levels.
- There is a need for remotely-locatable heavy-metal detectors in a variety of industrial and commercial applications.

NOVEL CONTRIBUTIONS

- A CMOS microsensor that can detect 0.8ppb of lead **[13.4]**
- Achieves this sensitivity this by adding a few thin-film post-processing steps to standard CMOS **[13.4]**
- Implemented in 0.5μm CMOS, the chip occupies 36mm^2 and consumes 15mW of power **[13.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- Sensor enables low-cost low-power heavy-metal microdetectors with a possibility of remote interrogation **[13.4]**
- Application to wireless-sensor networks for continuous environmental monitoring **[13.4]**

Smallest Pixel, Yet!

A 1/4.5" 3.1M Pixel FT-CCD with 1.56μm Pixel Size for Mobile Applications [19.1]

Sanyo Electric

PRESENT STATE OF THE ART *(THE PROBLEM)*

- At present, the smallest pixel size is 2.35μm x 2.35μm for IT-CCD, and 2.25μm for CMOS. For FT-CCD, it is difficult to reduce smear and power when the number of pixels is increased, and it is difficult to achieve a high-resolution small-pixel-size CCD imager with video modes
- In an FT-CCD, it is difficult to reduce smear (the vertical lines at high light levels) and power when the number of pixels is increased

NOVEL CONTRIBUTIONS

- Achieves 1.56μm x 1.56μm pixels with 7V operation **[19.1]**
- Significantly reduces smear to -75dB using a 9-phase vertical-transfer technique **[19.1]**
- Provides a video mode by combining pixels **[19.1]**

CURRENT AND PROJECTED SIGNIFICANCE

- Pixel pitch provides potential for more compact higher-resolution Camera Phones and DSC **[19.1]**
- Potential to force competing imaging technologies to improve **[19.1]**

The Big Picture in 3D

Megapixel CMOS Image Sensor Fabricated in Three-Dimensional Integrated-Circuit Technology [19.6]

MIT Lincoln Laboratories

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Conventional Image sensors (CCD/CMOS) in planar technologies require a trade-off of area for readout electronics with area for image sensing
- 3D stacking based on flip-chip bump-bonding leads to large pixel size and large dark current.

NOVEL CONTRIBUTIONS

- Wafer bonding with small 2μm x 2μm x 7.5μm 3D vias **[19.6]**
- Low dark current of less than 3nA **[19.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- May allow high-performance sensors with optimized 100%-fillfactor photodiodes separated from optimized readout structures **[19.6]**
- May allow complex signal processing behind every pixel for motion detection, feature extraction, and adaptive dynamic-range enhancement **[19.6]**

Neural-Data Compression

A Three-Dimensional Neural-Recording Micro-System with Implantable Data-Compression Circuitry [30.4]

Sandia National Labs; University of Michigan

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Available monitoring systems with full-analog information transmission produce a huge amount of data. While data transmission and real-time processing present a bottleneck, but only a small portion of transferred data carries relevant information

NOVEL CONTRIBUTIONS

- Spike detection recognizes relevant events only, reducing data by 92% **[30.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- As neural monitoring becomes more efficient, longer and more complex frames can be monitored and signal-processed **[30.4]**

Mobile Imaging: Paradigm Shift or Technology Bubble?

Organizer: ***Boyd Fowler****, Agilent Technologies, Santa Clara California, USA*
Chair: ***Jed Hurwitz****, ST Microelectronics, Edinburgh, Scotland*

OBJECTIVE

- Determine if mobile imaging is here to stay, or is it just another technology bubble.
- If mobile imaging is here to stay, determine the "killer application" or applications that will enable everyone in the value chain to profit.
- Determine what key technologies will be required to enable the "killer applications".

CHALLENGE

- The image quality that customers have come to accept in one-time-use film cameras is quickly colliding with the cost requirements for mobile imaging.
- The continued reduction in pixel size, to meet cost and size requirements, is having a detrimental effect on image quality.
- Lens and packaging technologies must be developed to achieve the image quality and cost required by customers.

CONTROVERSY

- Will mobile imaging survive the cost-quality tradeoffs required by customers?
- Is there a realistic minimum pixel size and minimum camera cost?
- Will mobile imaging replace low-end digital cameras and one-time-use film cameras

Tutorial

RF MEMS: Devices, Circuits, and Packaging

Farrokh Ayazi, Georgia Institute of Technology, Atlanta, GA

OVERVIEW

RF MEMS devices, including micromechanical switches, resonators, 3D high-Q inductors and micromachined antennas, can enable ultra-low-power wireless architectures in ultra-small microsystems. High-Q micromechanical resonators in the VHF and UHF range have become available, and wafer-level-packaged MEMS switches have demonstrated reliable operation for billions of cycles. This tutorial presents an introduction to RF MEMS devices, reviews the latest advances in the field, and discusses their manufacturing, performance, and packaging.

SPEAKER BIOGRAPHY

Farrokh Ayazi is an Assistant Professor in the School of ECE at Georgia Tech. He received his BSEE from the University of Tehran in 1994, and the MSEE and Ph.D degrees from the University of Michigan, in 1997 and 2000, respectively. His research interests are in the areas of micro/nano-electromechanical resonators, RF MEMS, VLSI analog ICs, MEMS inertial sensors, and packaging. He is a 2004 recipient of the NSF CAREER award, the 2004 Richard M. Bass Outstanding Teacher Award, and the Georgia Tech College of Engineering Cutting- Edge Research Award for 2001-2002. He has served on the technical program committees of ISSCC, and the MEMS and Sensors conferences.

Characterization of Solid-State Image Sensors

Objective

Solid-state image sensors are complex devices, a fact that is especially apparent when it comes to the issue of thorough characterization. With the introduction of CMOS image sensors, about a decade ago, this evaluation and testing process became even more complicated, because CMOS image sensors have an increased functionality on-chip. This is in contrast to CCD imagers which are limited to an analog pixel matrix in combination with a simple output amplifier on-chip. In the case of the CCD circuit, any additional functionality is located off-chip.

Audience

For CMOS imagers, both the analog circuitry and digital circuitry are integrated on the same imaging chip, with photons as the input signal and processed digital bits as the output. Where full-functional testing of the component is needed, the evaluation and testing discipline encompasses optical, analog-circuit, and digital-circuit testing.

Scope

In many cases, image sensors are fabricated in CMOS processes that are in some way tweaked to result in better imaging performance. The optimization of these CMOS processes involves semiconductor physics, semiconductors processing, and characterization know-how. All of these different parameters need to be characterized throughout the fabrication process.

Program

Taken all together, the quality and performance of CCD and CMOS image sensors rely on a very-extensive multi-disciplinary characterization activity.

It is the intention of this forum to give an in-depth overview of the issues associated with the different parts of the image-sensor evaluation process. Each talk in the Forum addresses the characterization of a single discipline within the field of solid-state imaging: optics, device physics, electrical circuitry, design for testability, semiconductor technology, sensitivity, and standardization of testing. The organizing committee has invited key specialists in each of these fields to contribute to this Forum.

NOTES

MEMORY

- **Overview**
- **Featured Papers**
- **Special-Topic Session**
- **Tutorial**
- **Forum**

ISSCC 2005 – MEMORY

Subcommittee Chair: *Katsuyuki Sato, Elpida Memory, Tokyo, Japan*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- NAND Flash breaks 8Gb barrier **[2.1, 2.2]**
- Multi-level NOR Flash operates at 166MHz **[2.6]**
- 2Gb DDR2 SDRAM achieves 800Mb/s/pin **[25.6]**
- eDRAM operating at 400MHz random cycle **[25.3]**
- First 256Mb SRAM **[26.2]**
- SRAMs operating at sub-0.5V **[26.3, 26.6]**
- Embedded L3 Cache increases to 24MB **[26.8]**

APPLICATIONS AND ECONOMIC IMPACT

- Flash memory passes DRAM in bit density **[2.1, 2.2]**
- Higher density meets storage demands of digital cameras and MP3 players **[2.1, 2.2]**
- eDRAM replaces eSRAM in CMOS-compatible process **[25.3]**
- High-density DRAM keeps pace with DDR2 bandwidth **[25.6]**
- SRAM shatters 100Mb barrier **[26.2, 26.8]**
- Stability issues solved for ultra-low-voltage SRAM **[26.3, 26.6]**

SPECIAL-TOPIC SESSION

SRAM Design in the Nanoscale Era [SE5]

TUTORIAL

Phase-Change Memory [T4]

FORUM

Advanced Dynamic-Memory Design [F2]

Flash Memory Doubles Density

A 146mm^2 8Gb NAND Flash Memory in 70nm CMOS Technology [2.1]

Toshiba; SanDisk

An 8Gb Multi-Level NAND Flash Memory in 63nm CMOS Process [2.2]

Samsung

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Highest-density NAND Flash Memory reported to date has 4Gb capacity
- Present-day NAND Flash Memory technology is 90nm
- Fastest write performance for a multi-level NAND Flash reported to date is 2.3MB/s

NOVEL CONTRIBUTIONS

- Fabrication in 70nm CMOS technology **[2.1]**
- Fabrication in 63nm CMOS technology **[2.2]**
- Achieves 6MB/s write performance **[2.1]**
- Achieves 4.4MB/s write performance **[2.2]**

CURRENT AND PROJECTED SIGNIFICANCE

- Multi-Level techniques offer a significant increase in bit density for portable electronics **[2.1 2.2]**
- High-speed programming for digital cameras and audio players. **[2.1 2.2]**

A New Breakthrough in Non-Volatile-Memory Performance

A 90nm 512Mb 166MHz Multi-Level-Cell Flash with 1.5MByte/s Programming [2.6]

Intel

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Fastest-Read NOR Multi-Level Flash Memory(at 125MHz) reported to date
- Present-day NOR Multi-Level Flash Memory is in 130nm technology.
- Fastest-Write NOR Multi-Level Flash Memory (at 200KB/s) reported to date.

NOVEL CONTRIBUTIONS

- 166MHz continuous-burst operation for fast read throughput. **[2.6]**
- Achieves 1.5MB/s write performance **[2.6]**
- Capable of concurrent 166MHz read and 1.5MB/s write. **[2.6]**
- Fabricated in 90nm CMOS technology **[2.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- Significant increase in frequency for fast direct-code execution. **[2.6]**
- Significant improvement in write throughput for communications and multimedia applications. **[2.6]**
- Multi-level techniques offer lowest bit cost for memory subsystems requiring fast code execution and fast non-volatile data storage. **[2.6]**

Fastest Random-Cycle Embedded DRAM

A 400MHz Random-Cycle Dual-Port Interleaved DRAM with Striped-Trench Capacitor [25.3]

Matsushita Electric Industrial

PRESENT STATE OF THE ART *(THE PROBLEM)*

- 312MHz random-cycle DRAM was announced at ISSCC 2004.
- eDRAM process dedicated to large cell capacitance of 20fF.

NOVEL CONTRIBUTIONS

- 400MHz random-cycle DRAM with dual-port interleaved operation **[25.3]**
- Sense-signal-loss-compensating technologies for 5fF cell **[25.3]**
- CMOS-compatible Striped-Trench Capacitor (STC) cell **[25.3]**

CURRENT AND PROJECTED SIGNIFICANCE

- 400MHz Random-Cycle RAM device replaces SRAM **[25.3]**
- Increases maximum embedded-memory capacity **[25.3]**

First Commercially Viable 2Gb DRAM

An 800Mb/s/pin 2Gb DDR2 SDRAM Using an 80nm Triple- Metal Technology [25.6]

Samsung

PRESENT STATE OF THE ART *(THE PROBLEM)*

- 4Gb was announced at ISSCC 2001
- Chip areas reported have been prohibitively large

NOVEL CONTRIBUTIONS

- Creative use of triple metal enables die-size reduction **[25.6]**
- Chip outline optimized to fit industry-standard (JEDEC) package **[25.6]**
- On-chip clock doubling for test-cost reduction **[25.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- Commercially-viable 2Gb DRAM device **[25.6]**
- Increases maximum system memory **[25.6]**

Largest SRAM ever reported

A 256Mb Synchronous-Burst DDR SRAM with Hierarchical Bit-Line Architecture for Mobile Applications [26.2]

Samsung

PRESENT STATE OF THE ART *(THE PROBLEM)*

- High-density SRAM limited by cell size and leakage-induced power dissipation.
- Decreasing cell read current has pushed core architectures into inefficient hierarchical-bitline structures.

NOVEL CONTRIBUTIONS

- 256Mb SRAM uses 0.16μm^2 (25F^2) stacked single-crystal silicon thin-film transistor cell introduced at the VLSI Symposium in June 2004. **[26.2]**
- Use of stacked single-crystal silicon thin-film transistor as local column select eliminates inefficiency of hierarchical-bitline architecture. **[26.2]**
- 17mA operating current at 140MHz burst operation makes chip suitable for mobile applications **[26.2]**

CURRENT AND PROJECTED SIGNIFICANCE

- Lower cost and higher performance for mobile applications, such as cell phones, PDAs, etc. **[26.2]**
- Raised barrier to penetration by SRAM "wannabe" technologies such as 1T1C and 3T pseudo-SRAM. **[26.2]**

3X increase in Itanium® L3 Cache Size

The Asynchronous 24MB On-Chip Level-3 Cache for a Dual-Core Itanium® Processor [26.8]

Hewlett Packard; Intel

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Higher-frequency operation places greater demands on embedded memory- systems.
- Multi-core architecture also requires larger memory.
- Increasing memory size stresses power-dissipation limits.
- Increasing cache size must keep up with frequency demands of the processor.

NOVEL CONTRIBUTIONS

- 24MB L3 cache is largest embedded memory ever reported **[26.8]**
- Lower core-voltage operation limits 24MB cache power to 4.2W **[26.8]**
- Change to asynchronous memory operation reduces L3 cache pipeline from 8 to 5 cycles of latency **[26.8]**

CURRENT AND PROJECTED SIGNIFICANCE

- Higher-performance server and CPU applications **[26.8]**
- Density supports dual-core architectures **[26.8]**

SPECIAL-TOPIC SESSION

SRAM Design in the Nanoscale Era

Organizer: ***Sreedhar Natarajan****, MoSys, Kanata, Canada*
Chair: ***Alexander Shubat****, Virage Logic, Fremont, CA*

OVERVIEW

- SRAM Engineers in 90nm face enormous challenges to keep up with performance and power requirements.
- Innovative circuit design and process techniques address these issues, and enable the potential of future SRAMs.

OBJECTIVE

- To expose the critical bottlenecks in the design of SRAMs at 90nm and below.
- To highlight current research on the impact of SER on 90nm SRAMs.
- To highlight industrial approaches to resolving leakage and performance issues in 90nm SRAMs.
- To highlight the need for mandatory test of 90nm embedded SRAMs to improve yield.

CHALLENGE

- The challenges in embedded SRAM design at 90nm include:

  Increased standby leakage, and gate leakage.

  Maintaining performance as Ion/Ioff decreases.

  Improving immunity to radiation-induced events caused by lower operating voltage and reduced node capacitances.

  Impact of dopant V_t variation.

  Impact of SRAM yield at 90nm.

STRUCTURE

- *Contents*:

The first two talks will highlight the impact of leakage and soft errors on SRAMs; The final two talks will address the design difficulties and test solutions required to improve yield and quality of SoCs shipped.

- *Speakers and Specialties*
  - **Soon Moon Jung, Samsung: *"SRAM Leakage-Reduction Techniques"***

    A discussion of the leakage mechanisms and the impact of leakage on SRAM functionality, followed by approaches by which to control leakage and reduce power consumption.
  - **Robert Baumann Texas Instruments: *"Soft Error Rates in SRAM"***

    A discussion of the three dominant radiation-impact mechanisms responsible for single-event effects in advanced technologies; the scaling trends for soft error sensitivity; and the applications that require mitigation strategies for SER.
  - **Harold Pilo IBM: *"SRAM Design Issues in the 90nm Era"***

    A discussion of how some of the emerging trends (including increased Ion/Ioff, gate leakage, and random dopant fluctuations) are driving changes in design style and architecture of SRAMs at 90nm and below.
  - **Yervant Zorian Virage Logic: *"Test Solutions to Improve SRAM Yield"***

    A discussion and analysis of the impact of 90nm fabrication on SRAM yield, and present embedded test solutions required to guarantee the quality of shipped SoCs.

RECAP

- To educate attendees concerning critical issues preventing SRAMs from scaling, and conerning present approaches to solutions.
- To highlight the potential impact of the problem, and invite attendees to participate in the discussion on the creation of more innovative solutions.

Tutorial

Phase-Change Memory

Giulio Casagrande, ST Microelectronics, Milan, Italy

OVERVIEW

- Phase-change memory (PCM) concepts
- Memory cells and electrical characteristics
- Scaling perspectives
- Design aspects
- MOS vs. BJT for array selection

SPEAKER BIOGRAPHY

Giulio Casagrande graduated in Electronic Engineering in 1977 from the University of Padova, Italy. He joined ST Microelectronics, Milano, as a designer of EPROMs and EEPROMs, and then he led the design and engineering team that developed the first generations of Flash Memories at ST. He is presently the Director of R&D of the Memory-Products Group at ST Microelectronics, focusing on advanced Flash design for embedded applications, assessment and development of disruptive emerging memories, CAD, and design methodology. Giulio is a member of the ISSCC Memory Sub-Committee.

FORUM

Advanced Dynamic-Memory Design

Objective

This all-day forum is dedicated to the design and architecture of DRAMs developed to meet the requirements of tomorrow's demanding applications and diverse environments. Attendance is limited, and pre-registration is required. This all-day event encourages open interchange in a closed forum.

Audience

Target participants are circuit designers involved in the development of next-generation DRAMs. Such individuals need to understand which functionalities are required in the future, and how their requirements can be met in a design.

Scope

Recently, DRAM has expanded from a mere commodity-product into more specialized devices adapted to multiple application environments. Low-power and high-speed environments require unique design solutions to solve their specific challenges. Successful designers will require detailed knowledge of these solutions. In this forum, a solid base of DRAM design will be given, and expanded by techniques which enable the required high-bandwidth or low-power behaviour.

Program

The forum will begin with a presentation by **Jinyong Chung,** from POSTECH, Korea, who will review important general aspects of DRAM design. Building on these basics, **Young-Hyun Jun,** from Samsung, will focus on high-speed applications which meanwhile extend into the GHz regime. On-chip clock-generation is the key to a successful high-speed design, and DLL/PLL circuits will consequently be a focus of his presentation. Circuits and applications will be discussed from basic to advanced technologies.

In addition, high-speed designs require precise and clearly-defined I/O-interfaces. These will be discussed in the talk by **Terry Lee**, Micron Technology, I/O- and protocol-optimization of DRAMs can, however, only be performed while considering general DRAM constraints. The talk will, therefore, also extend to the system environment and its impact on I/O-interfaces.

The next talk, by **John Barth,** from IBM, will focus on the embedded use of DRAMs. Large, on-die SRAM caches are reaching their limits as is made obvious by the rising number of SRAM publications struggling with leakage and SER limitations. Here, high-performance eDRAM is an attractive replacement, and the relevant design techniques will be presented. Special DFT and BIST techniques need to be employed for embedded memories, which will also be covered.

The remaining part of the Forum will be dedicated to low-power applications. Power-reduction can be achieved by voltage reduction or by changes in the architecture. The first part, presented by **Martin Brox,** from Infineon, will cover architectural solutions. Here, strategies are described to minimize refresh, stand-by, and leakage currents. Further changes to standard devices will be discussed which enable optimized use of DRAMs in power-sensitive and space-constrainted mobile applications.

The next talk by **Takayuki Kawahara,** from Hitachi, will focus on the special challenges imposed on DRAMs by the necessity to lower operating voltages while staying on the shrink-path for the memory cell. Recent advances in sub-1V DRAMs will be presented which promise to enable these devices with their low, available memory-cell charge.

The last talk by **Tomoyuki Ishii** introduces future challenges for DRAM technology in the nanoscale process generation. From an operational-stability point-of-view, DRAM has better scalability than SRAM. However, the standard 1T1C type DRAM has serious difficulties in maintaining adequate retention time and storage capacitance, as the process scales. Several non-1T1C approaches for scalable DRAM are introduced, along with new device structures. Investigation of a memory cell using only 10 electrons per bit is discussed.

NOTES

SIGNAL PROCESSING

- **Overview**
- **Featured Papers**
- **Panel**
- **Tutorial**

ISSCC 2005 – SIGNAL PROCESSING

Subcommittee Chair: *Wanda Gass, Texas Instruments, Dallas, TX*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- Real-time high-definition H.264 video encoder **[7.1]**
- Low-power impulse-radio UWB transceiver. **[24.1]**
- High-data-rate LDPC-COFDM-based UWB transceiver. **[24.2]**
- WLAN-baseband transceiver w/MRC and Tx beamforming **[24.6]**
- Robust improved-throughput WLAN using a wideband approach for the Access Point. **[24.7]**
- Fully-integrated R/W 7XBD/16XDVD/56XCD SoC **[31.3]**

APPLICATIONS AND ECONOMIC IMPACT

- High-definition digital-video discs (BD, HD-DVD), HD camera, DVB-H. **[7.1]**
- High-throughput low-power short-range wireless communications. **[24.1, 24.2]**
- Robust multimedia-streaming-capable WLAN applications. **[24.6]**
- Robust-wireless-network hotspot performance and network management. **[24.7]**
- Multi-format high-rate low-cost mass-storage solutions. **[31.3]**

PANEL

Driving Miss Ubiquity: What applications will fill tomorrow's fabs? [E4]

TUTORIAL

DSP Circuit Technologies for the Nanoscale Era [**T5]**

Real-Time High-Definition H.264 Video

A 1.3TOPS H.264/AVC Single-Chip Encoder for HDTV Applications [7.1]

National Taiwan University; Chip Implementation Center, Vivotek; Chin Fong Machine Industrial; MediaTek

PRESENT STATE OF THE ART *(THE PROBLEM)*

- The new H.264/AVC video standard provides the best video quality for HD-DVD and other HD-video applications.
- No single-chip implementations of an H.264/AVC video encoder have previously been reported.

NOVEL CONTRIBUTIONS

- The world's first single-chip real-time video encoder for the H.264/AVC standard. **[7.1]**
- Provides real-time encoding for 1280×720-pixel HD videos at 108MHz (YUV420, 1280x720, 30fps, 1 reference frame, search range H[-64,+63]/V[-32,+31]) **[7.1]**
- Supports full-compression tools in baseline profile, including multiple reference frames, variable block sizes, all intra-prediction modes, DCT/HT/Q/IQ/IHT/IDCT, CAVLC, deblocking, and rate-distortion-optimized mode decision **[7.1]**
- 2048-parallel-integer motion-estimation architecture eliminates 86% of the external memory accesses (reducing from 1.14Gbytes/s to 0.16Gbytes/s) and 88% of the on-chip SRAM accesses (reducing from 13.41Gbytes/s to 1.63Gbytes/s) **[7.1]**
- Power dissipation is 785mW at 1.8V and 108MHz for HDTV 1280×720-pixel videos, and chip core size is 31.72mm^2 in 0.18μm CMOS technology. **[7.1]**

CURRENT AND PROJECTED SIGNIFICANCE

- High-definition digital-video disc (BD, HD-DVD), HD camera, digital-video broadcasting for handheld terminals (DVB-H). **[7.1]**

Ultra-Wide-Band (UWB) Enables Novel Wireless Networks

A 1.2V 6.7mW Impulse-Radio UWB Baseband Transceiver [24.1]

National Taiwan University

A 480Mb/s LDPC-COFDM-Based UWB Baseband Transceiver [24.2]

National Chiao Tung University

PRESENT STATE OF THE ART *(THE PROBLEM)*

- UWB standard (s are) under development
- Two competing system concepts: OFDM and Impulse-radio
- Early prototypes in industry and academia
- Note the special evening session and panel at ISSCC 2004 ???

NOVEL CONTRIBUTIONS

- Low-power (7 mW) transceiver **[24.1]**
- First digital baseband processors for UWB reported at ISSCC **[24.1, 24.2]**
- High-speed (480 Mb/s) transceiver **[24.2]**

CURRENT AND PROJECTED SIGNIFICANCE

- Short-distance (personal-area and intra-room network) high-data-rate (~0.5 Gb/s) communication **[24.1]**
- Wireless connectivity for computer peripherals and consumer-electronics equipment **[24.1]**

Pushing the WLAN Envelope

A WLAN SoC for Video Applications Including Beam Forming and Maximum-Ratio Combining [24.6]

Atheros

A 180MS/s 162Mb/s Wideband Three-Channel Baseband and MAC Processor for 802.11a/b/g [24.7]

Engim; MIT

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Non-idealities of wireless channels limit reliability and range, resulting in widely- varying transmission latencies which limit WLAN's ability to deliver streaming media (e.g., video).
- Current WLAN solutions are limited in data rate (54 Mbps) without proprietary extensions. As well, sharing the channel with slow clients (1 Mbps) greatly reduces overall network performance.

NOVEL CONTRIBUTIONS

- First-reported application of maximum-ratio combining and transmit beamforming to WLAN 802.11-compliant baseband. **[24.6]**
- Description of a jitter-removal system for enabling variable-bit-rate video streams over wireless channels. **[24.6]**
- First-reported multi-channel wideband WLAN solution capable of >54Mb/s for 802.11-compliant operation. **[24.7]**
- Real-time spectral-monitoring capability for monitoring interferers and rogue clients, allowing advanced network-management capabilities. **[24.7]**
- First-reported wideband WLAN baseband solution incorporating 3 completely asynchronous 802.11a/b/g-compliant modems. **[24.7]**

CURRENT AND PROJECTED SIGNIFICANCE

- Robust streaming multimedia over wireless networks. **[24.6]**
- Wide-coverage-area high-rate WLANs. **[24.6]**
- Advanced wireless-network management. **[24.7]**
- Robust wireless-network hotspot performance with fast and slow clients. **[24.7]**

Panel

Driving Miss Ubiquity: What applications will fill tomorrow's fabs?

Organizer: ***Toru Shimizu****, Renesas Technology, Tokyo, Japan*
Moderator: ***Robert Brodersen****, University of California at Berkeley, CA*

OBJECTIVE

- To identify the applications that will drive the demand for advances in silicon technology and integrated-circuit design.

CHALLENGE

- Integrated-circuit devices that will fuel the need for technology advances in the future will be portable, and so pervasive that many semiconductor companies will be drawn to this market by the promise of large-volume sales.
- This ubiquitous driver will involve the transmission and reception of information.
- The kind of information will be communicated is an item of debate.

CONTROVERSY

- Will next-generation cell phones be the driver, as the demand for multimedia continues to grow?
- Will identification-code communication become pervasive, as a way to satisfy the need for security, safety, and reliability?
- Will there be new applications which collect and transmit environmental information which will enrich our life and improve our health and safety?

Tutorial

DSP Circuit Technologies for the Nano-Scale Era

Ram Krishnamurthy, Intel, Hillsboro, OR

OVERVIEW

- Sub-65nm scaling challenges, and new paradigm shifts in next-generation DSP
- Emerging trends in the wireless and embedded-DSP industry
- Special-purpose accelerators, co-processor arrays, and reconfigurable DSP engines
- Energy-efficient arithmetic-circuit techniques, and multi-supply/multi-V_t design

SPEAKER BIOGRAPHY

Ram Krishnamurthy is a Senior Staff Research Engineer at Intel Corporation's Circuit Research Labs, in Hillsboro, OR, where he leads the high-performance and low-voltage circuits research group. He holds 41 patents and has published over 75 papers. He serves on the SRC ICSS task force and the ISSCC, CICC, and SoC program committees. Since 1999, he has been an adjunct faculty member at Oregon State University, where he teaches VLSI-system design. He received his PhD from Carnegie Mellon University in 1998.

TECHNOLOGY DIRECTIONS

- **Overview**
- **Featured Papers**
- **Special-Topic Session**
- **Tutorial**

ISSCC 2005 – TECNOLOGY DIRECTIONS

Subcommittee Chair: *Anantha Chandrakasan. Massachusetts Institute of Technology*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- Demonstrated microscopic interface between neural and electronic systems **[4.1]**
- MEMS-based atomic clocks which are 700X smaller than the present art **[4.5]**
- Fully-functional MEMS gyroscope on conventional CMOS logicchip **[4.7]**
- A Rectifier IC for wireless power transmission up to 10m-distance **[14.1]**
- Three-dimensional integration schemes using wireless interconnects **[14.4, 14.5]**
- RF receiver architecture integrating on-chip MEMS-based high-Q inductors and tunable varactors, together with an array of parallel cantilever beams combining downconversion mixers and channel filters **[21.1]**
- First-time demonstration of integrating BAW filters above BiCMOS and their connection to the RF circuits below. This technique is used for the integration of a complete WCDMA RF front-end. **[21.2 and 21.3]**
- New RF communication devices and systems based on MEMS **[21.1, 21.2, 21.3, 21.5]**
- First CMOS 60GHz direct-conversion receiver featuring folded microstrip lines realized in 0.13µm CMOS and consuming 9mW from a 1.2V supply **[21.6]**
- New cascaded multi-stage distributed amplifier in 90nm CMOS achieves better than 7dB gain with a bandwidth of 70GHz **[21.7]**
- Organic transistors are integrated into flexible scanner and display **[32.2, 32.3]**

APPLICATIONS AND ECONOMIC IMPACT

- A path for integrating electronics and neural functions **[4.1]**
- Electronic sensory capabilities in a human form-factor **[4.2]**
- Industrial bio-electronic processing of living cells **[4.3]**
- Portable positioning systems with high-accuracy clocks **[4.5]**
- Dramatic reduction in cost and form-factor from hybrid integrations **[4.5, 4.7]**
- Integrated on-chip antennas **[14.8]**
- New transceiver architectures for multi-band wireless applications **[21.1, 21.2 and 21.3]**
- New low-cost miniaturized wireless-communication systems **[21.1, 21.2, 21.3, 21.5]**
- Low-cost CMOS mm-wave circuits for high-data-rate communications **[21.6, 21.7, 21.8]**
- Flexible plastic display (electronic paper) and scanner **[32.2, 32.3]**

SPECIAL-TOPIC SESSION

Integration in the 3rd Dimension: Opportunities and Challenges [SE3]

TUTORIAL

Nanotechnology 101 [T6]

MIXED-DOMAIN SYSTEMS

Joining Ionics and Electronics: Semiconductor Chips with Ion Channels, Nerve Cells and Brain Tissue [4.1]

Max Planck Institute for Biochemistry

An Analog Bionic-Ear Processor with Zero-Crossing Detection [4.2]

MIT

An IC/Microfluidic Hybrid Microsystem for 2D Magnetic Manipulation of Individual Biological Cells [4.3]

Harvard University; Harvard Medical School

Towards Chip-Scale Atomic Clocks [4.5]

DARPA; NIST

Processing of MEMS Gyroscopes on Top of CMOS ICs [4.7]

IMEC; ASM; IMSE-CNM; Philips; Bosch

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Hybrid interdisciplinary technologies are being integrated in compatible processes

NOVEL CONTRIBUTIONS

- Analog speech processor generates stimulus directly to auditory nerve **[4.2]**
- CMOS digital-circuit operation can be used to manipulate tagged individual living cells **[4.3]**
- New capabilities and functions are realized on a single die **[4.5, 4.7]**

Low-Power Wireless and Advanced Integration

A 1V 433MHz/868MHz 25kb/s FSK 2kb/s OOK RF Tranceiver SoC in Standard Digital 0.18μm CMOS [14.2]

CSEM, Xemics; Texas Instruments

A 195Gb/s 1.2W 3D-Stacked Inductive Inter-Chip Wireless Superconnect with Transmit-Power Control Scheme [14.5]

Keio University; University of Tokyo

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Sensor interface is not integrated into wireless modules **[14.2]**
- Power consumption of RF systems too high for distributed-sensor applications **[14.2]**
- Communication bandwidth and power distribution among chips in a 3-D stack is a major bottleneck **[14.5]**

NOVEL CONTRIBUTIONS

- Sensor interface and processor integrated with radio electronics **[14.2]**
- Ultra-low-power demonstration of sensor integration **[14.2]**
- Power control eliminates interference and optimizes power dissipation **[14.5]**

CURRENT AND PROJECTED SIGNIFICANCE

- Distributed sensing applications enabled by ultra-low-power integrated-sensor node **[14.2]**
- 1Terabit/sec wireless communication among chips in a package **[14.5]**

RF TRENDS: ABOVE-IC INTEGRATION

Integration of High-Q BAW Resonators and Filters above IC [21.2]

Swiss Centre for Electronics and Microtechnology (CSEM); CEA-LETI

A SiGe:C BiCMOS WCDMA Zero-IF RF Front-End Using an Above-IC BAW Filter [21.3]

ST Microelectronics; CEA-LETI; CSEM

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Need for integration of high-Q passive components, such as BAW filters, on top of an IC to avoid external components, reduce the BOM, and decrease the transceiver cost
- Need for transceiver architectures for multi-band and multi-standard wireless communication

NOVEL CONTRIBUTIONS

- First-time demonstration of integrating BAW filters above BiCMOS, and connecting them to the RF circuits below. This technique is used for the integration of a complete WCDMA RF front-end **[21.2, 21.3]**
- Increased integration avoiding off-chip components in transceivers for single- chip RF transceiver **[21.2, 21.3]**

CURRENT AND PROJECTED SIGNIFICANCE

- Highly-integrated radios for multi-band and multi-standard wireless **[21.2, 21.3]**
- Several different radio front-ends replaced by a single one **[21.2, 21.3]**

RF TRENDS: CMOS REACHES mm-WAVE

A 60GHz Direct-Conversion CMOS Receiver [21.6]

UCLA

A 70GHz Cascaded Multi-Stage Distributed Amplifier in 90nm CMOS Technology [21.7]

National Taiwan University; TSMC

A 114GHz VCO in 0.13 µm CMOS Technology [21.8]

National Taiwan University

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Need for low-cost mm-Wave integrated circuits for high-data-rate communication and other consumer applications, such as automotive radars for collision avoidance.

NOVEL CONTRIBUTIONS

- 60GHz direct-conversion receiver in 0.13µm CMOS consuming 9mW from a 1.2V supply. Voltage gain is 28 dB with a noise figure of 12.5 dB **[21.6]**
- Amplifier in 90nm CMOS technology, achieving better than 7dB gain with a bandwidth of 70GHz **[21.7]**
- First 110 to 170GHz CMOS VCO in standard-bulk 0.13µm CMOS, featuring a phase noise of -107.6dBc/Hz at 10MHz offset, and consuming only 8.4mW **[21.8]**

CURRENT AND PROJECTED SIGNIFICANCE

- Aggressive scaling of CMOS and SiGe allows performance traditionally reserved for III-V compound semiconductors. **[21.6, 21.7, 21.8]**

SCALABLE MEMORY TECHNOLOGY

Memory Technologies in the Nano-Era : Challenges and Opportunities [32.1]

Samsung

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Transistor size, interaction between adjacent cells, and leakage current, limit the scaling of conventional memories.

NOVEL CONTRIBUTIONS

- Use of the FinFET enables nanometer scaling of conventional memories **[32.1]**

CURRENT AND PROJECTED SIGNIFICANCE

- DRAM, Flash, and SRAM, can be scaled down to technologies below 50 nm **[32.1]**

ORGANIC ELECTRONICS BECOME PRACTICAL

A Flexible 240x320-Pixel Display with Integrated Row Drivers Manufactured in Organic Electronics [32.2]

Philips

A Sheet-Type Scanner Based on a 3D-Stacked Organic Transistor Circuit using Double Word-line and Double Bit-line Structure [32.3]

University of Tokyo

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Large-scale integration of organic transistors has not yet been achieved

NOVEL CONTRIBUTIONS

- A 240-stage shift register is integrated onto a flexible organic active-matrix display **[32.2]**
- A sheet-type scanner is manufactured with 3D-stacked organic transistors and photodiodes **[32.3]**

CURRENT AND PROJECTED SIGNIFICANCE

- Integration in organic electronics opens up new application fields **[32.2, 32.3]**

SPECIAL-TOPIC SESSION

Integration in the 3rd Dimension: Opportunities and Challenges

Organizer: ***Larry Pileggi****, Carnegie Mellon University, Pittsburgh, Pennsylvania*
Chair: ***Werner Weber****, Infineon, Munich, Germany*

OVERVIEW

- Integration in three dimensions holds great promise for improving the performance and scale of integration.
- Manufacturing costs and thermal concerns are critical considerations for making 3D integration a reality.
- Additional opportunities for layering non-traditional integrated components on top of CMOS-based SoCs are available.

OBJECTIVES

- To highlight some of the current research in industry and academia directed at integration in 3D.
- To examine the cost issues for 3D integration.
- To highlight emerging applications, such as above-IC integration of non-traditional components.

CHALLENGES

- The challenges of 3D integration are:
  - Cost of manufacturing.
  - Removal of heat, and increased power density.
  - Testing, interconnecting, and stacking of unpackaged silicon die.

STRUCTURE

- Contents:
  The first two talks will introduce cost-based arguments for 2.5D integration, a structure based on stacking of traditional 2D integrated circuits. The latter two talks will explore design in the 3rd dimension via above-IC RF-MEMS components, and integration of antennas and other microwave components.

- Speakers and Specialities.
  - **Wojciech Maly CMU:** ***"Exploring Cost and Performance Advantages of 2.5-D Integration"*** will construct and apply a cost-analysis framework to compare different integration schemes, including the monolithic System-on-Chip and non-monolithic methods.
  - **Wilfried Haensch IBM:** ***"3D Integration's Architectural and Circuit Design Opportunities"*** will describe the advantages and disadvantages of 3D-integration which "folds" the chip into multiple active layers to reduce lateral dimensions.
  - **Pascal Ancey ST Microelectronics:** ***"Above IC & Embedded RFMEMS Platform for SoC Integration: Status and Prospects"*** will discuss the feasibility of integration of an above-IC BAW filter.
  - **Hermann Schumacher University of Ulm：** ***"A Wafer-Level Integration Technology for On-Wafer Antennas and Microwave Components"*** will describe a silicon-based wafer-level integration technique for microwave and millimeterwave structures.

RECAP

- To introduce the potential benefits and challenges of 3D-integrated silicon systems.

Tutorial

Nanotechnology 101

Philip H. S. Wong, Stanford University

OVERVIEW

This presentation is an introduction to the emerging opportunities in novel nanoscale devices and fabrication techniques, with particular emphasis on the implications for circuit and system designers. Topics covered include: fundamentals of device physics and materials science at the nanoscale, the ITRS Emerging Research Devices (memory & logic), nanotubes, nanowires, and nanoparticles, molecular devices, and nanofabrication techniques and their impact on device layout. An assessment of the level of maturity of the proposed devices will be given.

- Nanoscale Device physics and materials behavior
- ITRS Emerging Devices Research Projections
- Nanotubes, Nanowires, Nanoparticles, Molecular Devices
- Nanofabrication Techniques, Layout Impacts

SPEAKER BIOGRAPHY

H.-S. Philip Wong joined the IBM T. J. Watson Research Center, Yorktown Heights, New York, in 1988. In September, 2004, he joined Stanford University as Professor of Electrical Engineering.
While at IBM Research, he was a Senior Manager having the responsibility of shaping and executing IBM's strategy on nanoscale science and technology, and on semiconductor technology. His current research interests are in nanotechnology and electronic imaging
(URL: http://www.stanford.edu/~hspwong).
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NOTES

WIRELESS AND RF COMMUNICATIONS

- **Overview**
- **Featured Papers**
- **Panel**
- **Tutorial**
- **Forum**

ISSCC 2005 – WIRELESS AND RF COMMUNICATIONS

Subcommittee Chair: *Trudy Stetzler, Texas Instruments, Stafford, TX*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- First truly single-chip 802.11 WLAN transceivers in CMOS **[5.2, 5.3]**
- A 24 GHz Phased-Array Transmitter on 0.18μm CMOS **[11.7]**
- Ultra-Wide-Band Transceivers **[11.8, 11.9]**
- A single-chip Quad-Band GSM/GPRS Transceiver in 0.18μm Standard CMOS **[17.6]**
- A 120nm CMOS DVB-T Tuner **[23.3]**
- A CMOS TV Tuner/Demodulator IC with Digital Image Rejection **[23.4]**
- A Broadband 21 to 26 GHz SiGe BiPolar PA MMIC **[29.1]**
- A Noise-Cancellation Technique in Active RF-CMOS Mixers **[29.8]**

APPLICATIONS AND ECONOMIC IMPACT

- Lower-cost high-performance WiFi for portable units with higher reliability. **[5.2, 5.3]**
- Elimination of the rat's nest behind your home entertainment system. **[11.8]**
- Cheap wireless Gigabit Ethernet and low-cost RADAR-on-a-chip **[11.7, 29.1]**
- One step closer to low-cost single-chip cell phones. **[17.6, 29.8].**
- Ubiquitous cheap TV tuners for your phone, watch, etc. **[23.3, 23.4]**

PANEL

RF MEMS: Fact or Stiction? **[E3]**

TUTORIAL

Polar Modulators for Linear Wireless Transmitters [T7]

FORUM

Clock and Frequency Generation for Wireline and Wireless Applications [F1]

Highly-Integrated 802.11b/g SoC

A (Single-Chip) 802.11g WLAN SoC [5.2]

Atheros Communications; Stanford University

A Fully-Integrated SoC for 802.11b in 0.18μm CMOS [5.3]

Broadcom

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Existing transceivers consist of RF/Analog IC(s) and Baseband/MAC IC(s).
- Existing transceivers require numerous off-chip components.

NOVEL CONTRIBUTIONS

- The first single-chip 802.11g SoC that fully integrates the RF front-end, baseband analog, digital baseband, and MAC, on one die **[5.2]**
- The first single-chip 802.11a SoC that fully integrates the RF front-end, baseband analog, digital baseband, and MAC, as well as PA, antenna switch, balun and loop filter, on one die **[5.3]**

CURRENT AND PROJECTED SIGNIFICANCE

- Highly-integrated low-cost transceiver SoCs have immediate significance, enabling high-volume low-cost WLANs **[5.2, 5.3]**
- Single-chip SoC enables significant reduction of form factor, penetrating mobile and embedded appliances **[5.2, 5.3]**
- Broadband connection of consumer electric appliances will result in a seamlessly-connected world

Highly-Integrated Ultra-Wideband Transceivers

A 24GHz Phased-Array Transmitter in 0.18μm CMOS [11.7]

California Institute of Technology

A 3.1 to 5GHz CMOS Direct-Sequence Spread-Spectrum UWB Transceiver for WPANs [11.8]

Sony; Mixed Signal Systems

A 0.13μm CMOS UWB Transceiver [11.9]

University of California, Los Angeles; RealTek

PRESENT STATE OF THE ART *(THE PROBLEM)*

- UWB solutions are currently coming out of the definition phase, now that the FCC has allocated spectrum. Early proof-of-concept circuits, just now being reported, show encouraging performance. Full system functionality and verification of system specs remains to be seen, primarily due to anticipated 802.11a co-existence issues.
- UWB applications require wideband frequency synthesizers with very fast (1ns) switching times. A wealth of synthesizer architectures have been developed for cellular and WiFi systems, but these architectures can't switch fast enough for UWB applications. New approaches need to be developed.
- No fully-integrated UWB transceivers exist today, due to the radically different signaling technique and wideband nature of the signal.
- Current 54Mb/s WiFi data rate is inadequate for enterprise applications. This will drive demand for the bit rates that UWB intends to offer.

NOVEL CONTRIBUTIONS

- 500Mb/s data transfer at 24GHz using a phase-array **[11.7]**
- The first-reported UWB transmitters and receivers. **[11.8, 11.9]**

CURRENT AND PROJECTED SIGNIFICANCE

- It is impossible to imagine the full range of possibilities and conveniences that will be enabled by UWB. One example is very-high-rate data transfer over short ranges to transfer several Gigabytes of information off a hard drive or other digital device. **[11.7, 11.8, 11.9]**
- UWB hardware will ultimately allow the wireless connection of bandwidth-hungry computer peripherals and audio-video equipment. This will eliminate the rats-nest of wires and cables that currently connect computer peripherals and home entertainment equipment. **[11.8,11.9]**
- Of course, all of this wireless bandwidth will also create security issues that need to be addressed. A new class of eavesdropping will be born unless these issues are addressed early**.**

RF Cellular ICs

All-Digital PLL and GSM/EDGE Transmitter in 90nm CMOS [17.5]

Texas Instruments

A Single-Chip Quad-Band GSM/GPRS Transceiver in 0.18μm Standard CMOS [17.6]

Berkana Wireless

PRESENT STATE OF THE ART *(THE PROBLEM)*

- GSM is the most-popular worldwide cellular standard in use today, with over 75% of the total cellular market. Existing solutions, based mainly on Bipolar and SiGe technology, employ separate transmitter, receiver, and synthesizer chips, as well as requiring many external components.
- The demand for high-data-rate services has spurred the development of new cellular standards such as GSM/EDGE that require more-linear transmitters that can result in high power consumption and low battery life. Existing solutions are based on SiGe technology, which does not lend itself well to high levels of integration at low cost.

NOVEL CONTRIBUTIONS

- First polar modulator implemented in deep sub-micron 90nm CMOS technology suitable for GSM/EDGE. **[17.5]**
- GSM CMOS transceivers on the market today are based on multi-chip solutions. However, several single-chip solutions have been announced recently. But, this chip is the first published fully-integrated quad-band GSM transceiver in 0.18μm CMOS, and has the best sensitivity-and-power- dissipation tradeoff on the market today for CMOS transceivers. **[17.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- Maintaining power and extended talk time will become increasingly challenging for future multimedia handsets and smart phones that must support power- hungry features such as color LCD, 5Mpix cameras, and multimedia applications. The increased integration capability of 90nm CMOS technology can enable the integration of a complete RF

CURRENT AND PROJECTED SIGNIFICANCE *(continued)*

transceiver, as well as digital signal processing, in a single-chip, to dramatically reduce power for extended battery life. **[17.5]**

- Efficient polar transmitter extends talk time for GSM/EDGE cellular phones **[17.5]**
- The demand for multi-media handsets with voice, data, and video streaming, require high levels of integration in deep-submicron CMOS to implement the increased digital-signal-processing functionality required for feature-rich handsets. Unlike SiGe or bipolar implementations, a CMOS RF transceiver can be integrated with digital logic to reduce overall system cost and provide a smaller form factor. **[17.6]**

Wireless Receivers for Consumer Electronics

UMTV: A Single-Chip TV Receiver for PDAs, PCs, and Cell Phones [23.2]

ItoM; Eindhoven University of Technology; University of Twente

A 120nm CMOS DVB-T Tuner [23.3]

ST Microelectronics

A CMOS TV Tuner/Demodulator IC with Digital Image Rejection [23.4]

University of California at San Diego; Chrontel

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Analog television and radio have been in use for a large part of the last century, but are increasingly susceptible to random interference, have limited capacity, and limited picture and sound quality. Moreover, it is not easy to program new features for the user.
- Integration of radio and TV circuitry into the small size typical of modern PCs, PDAs, and hand-held devices such as cellphones, is limited by the size and cost constraints of traditional (analog) technologies.
- Cost, cost, cost! Wireless chips that address mass-consumer-market applications must be inexpensive to manufacture and test, offer high picture and sound quality under many (often harsh) conditions, and run for as long as possible on a fresh battery charge in a hand-held device.

NOVEL CONTRIBUTIONS

- Battery lifetime in a single-chip TV receiver for use in PDAs, PCs, and cell phones, is improved by up to 6×, and size is reduced by a factor of 50, using no external components **[23.2]**
- First DVB-T tuner offered in CMOS with the potential for integration with a digital demodulator **[23.3]**
- First wideband (48 to 860MHz) TV tuner in CMOS technology, with 60dB of image rejection, done digitally **[23.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- Convergence of personal computing and home entertainment **[23.1, 23.2, 23.3, 23.4, 23.6].**
- TV goes mobile! TV-tuner ICs enable systems with small enough form factor and low enough power dissipation for inclusion in battery-operated devices, such as cellular phones and PDAs **[23.1, 23.3].**
- Radio that is truly global in reach: Satellite broadcast radio will reach the widest- possible audience **[23.6].**

Circuit Sophistication Propels VLSI Technologies for RF

A 21 to 26GHz SiGe Bipolar PA MMIC [29.1]

University of Toronto; Delf University of Technology; IBM

A Noise-Cancellation Technique in Active RF-CMOS Mixers [29.8]

Broadcom

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Power amplifiers are typically realized in specialized technologies such as GaAs or LDCMOS, which have limited integratability
- The higher the radio frequency, the more difficult it is to deliver power linearly to an antenna. The majority of amplifiers capable of delivering 100mW of power are realized for frequencies below 6GHz.
- MOS transistors have much higher flicker noise than BJT transistors. Flicker noise is the main obstacle for mixers needed to convert radio signals directly to audio frequencies, in a signal processor known as a direct-conversion receiver.
- CMOS technologies offer low cost and high integration levels, as does a direct-conversion receiver. A direct-conversion receiver in RF CMOS is therefore the holy-grail of wireless-terminal developers.

NOVEL CONTRIBUTIONS

- The first SiGe power amplifier to deliver more than 100mW at 26GHz, 5 times higher than prior art. The amplifier has 20dB gain and a good efficiency (of more than 12.5%). To achieve this, metal layers in the technology (that are normally used for connecting transistors) are stacked to form transformers. Such transformers are then cleverly applied repeatedly to the input and output of individual amplifier stages to achieve progressively higher power levels toward the output stage. Such an interplay of transistor circuits and improvised transformers is only possible with VLSI technology, where sophistication in design techniques, rather than costly processing technology, enables an extremely useful device at a very high frequency **[29.1]**

- In another demonstration of a clever technique for overcoming the most fundamental CMOS technology limitations, a dynamic current-steering scheme is used. The novel technique steers away the flicker-noise current at brief intervals within the signal waveform. This results in a dramatic improvement (10 times) in noise performance for a direct-conversion mixer, without sacrificing other performance metrics, such as gain or linearity. **[29.8]**

CURRENT AND PROJECTED SIGNIFICANCE

- Cost-effective power amplifiers (PA) operating at 24GHz open the way to wireless Internet and other high-speed data services with much higher bandwidth than is available today. **[29.1]**
- A low-flicker-noise direct-conversion mixer is a significant step toward very-low- cost and miniaturized radio receivers. It overcomes the fundamental limitations of CMOS for RF transceivers, enabling higher integration and lower cost for applications such as cell phones and WiFi terminals. This will result in smaller and cheaper products for consumers. **[29.8]**

Panel

RF MEMS: Fact or Stiction?

Organizer: ***Ken Cioffi****, Discera Inc., San Jose, CA*
Moderator: ***Bob Puers****., K.U. Leuven ESAT-MICAS, Leuven, Belgium*

OBJECTIVE

- To determine the prospects for RF MEMS in circuit and system design
- To examine the issues and time frames needed for bringing these products to market

CHALLENGE

- Reliability issues, such as stiction, have plagued some MEMS devices and have caused concern over all MEMS devices
- MEMS RF components have not yet shown either the performance or cost required to satisfy the mass market
- Packaging of MEMS devices has been a concern

CONTROVERSY

- Will the availability of low-cost MEMS components drive new system architectures, or will new system architectures drive out the need for MEMS?
- Will RF MEMS become a mainstream technology, or will their use be limited to a few niche applications?
- Can the performance of RF MEMS devices match or exceed the performance of the components that they need to replace, or do they need to?

Tutorial

POLAR MODULATORS FOR LINEAR WIRELESS TRANSMITTERS

Antonio Montalvo, Analog Devices Inc.

OVERVIEW

- Review of linear transmitter topologies
- Justification of polar modulators: lower noise compared to traditional linear modulators, and higher power efficiency
- Analysis of polar-modulator-implementation challenges
- Case studies of polar modulators for EDGE
- Polar-modulator limitations and opportunities

SPEAKER BIOGRAPHY

Antonio Montalvo has been the director of Analog Devices' Raleigh Design Center in Raleigh, NC, since 2000. He is also an Adjunct Professor at North Carolina State University. He was with Ericsson from 1995 to 2000, where he led the RF IC group, and with Advanced Micro Devices from 1987 to 1991, where he was involved in the design of Flash memories. He received a Ph.D. from North Carolina State University in 1995, an M.S.E.E. from Columbia University in 1987, and a B.S. Physics from Loyola University in 1985.

GIRAFE Forum

Clock and Frequency Generation for Wireline and Wireless Applications

Objective

This full-day workshop is dedicated to the understanding of the requirements for clock and frequency generation in wireline and wireless applications, and of circuit and design techniques, particularly for various types of oscillators and phase-locked loops. This event encourages open interchange in a closed forum.

Audience

The target participants are circuit designers working on the development and design of advanced time-references and synchronisation circuits, in applications such as gigabit Ethernet, fiberoptics, GSM, WCDMA, ultrawideband, and so on

Scope

The quality of various frequency or clock generation has a crucial impact on the total performance of communication systems. Various system concepts can provide widely differing specifications for VCOs and PLLs, even for the same application. A satisfactory compromise between contradictory requirements, such as low phase noise and wide bandwidth, is required to fulfill system specs. This forum discusses system requirements, noise models, VCO design examples, and PLL/DLL systematic design and optimization. A goal is to enable the attendees to better understand and be able to optimize clock and frequency synthesizers.

Program

The forum will begin with two talks some from **Derek Shaeffer**, from Aspendos Communications, and one from **Takehiko Nakao**, from Toshiba, that will discuss the design requirements in wireline wireless applications, respectively and thereby build a bridge between system requirements and design aspects.

The next three talks will focus on oscillator design and noise considerations. **Robert Renninger**, from Agere, will present the design of Multiphase Ring Oscillators, and also discuss phase-noise modeling techniques for them. Then **Ali Hajimiri** from Caltech will do the same for LC-based voltage-controlled oscillators. **Jan Craninckx**, from IMEC, will conclude with an analysis supply and substrate noise in VCOs.

Phase-locked loops and delay-locked loops will be in the focus of the last three presentations. **Cicero Vaucher**, from Philips, will more generally cover system analysis, design and optimization of frequency synthesizers for communication systems. Design, simulation, and bandwidth extension methods, especially for fractional-N frequency synthesis will be treated in detail by **Michael Perrott** from MIT. Finally, **Ivan Bietti** from STM will present special aspects of PLLs for wireless communications, particularly for spread-spectrum generation, and for (DAC-free) direct modulation.

NOTES

WIRELINE COMMUNICATIONS

- **Overview**
- **Featured Papers**
- **Special-Topic Session**
- **Tutorial**
- **Forum**

ISSCC 2005 – WIRELINE

Subcommittee Chair: *Franz Dielacher, Infineon, Villach, Austria*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- 6.4Gb/s CMOS SerDes Core with Feed-Forward and Decision-Feedback Equalization **[3.2]**
- 6.25Gb/s Binary Adaptive Decision-Feedback Equalizer with First Post-Cursor Tap Cancellation **[3.5]**
- Circuit Techniques for a 40Gb/s Transmitter in 0.13μm CMOS **[8.1]**
- 3V 10.7Gb/s Differential Laser-Diode Driver with Active Back-Termination Output Stage **[12.1]**
- 20Gb/s VCSEL Driver and Regulated Output Impedance in 0.13μm CMOS **[12.2]**
- RF/Baseband FDMA-Interconnect Transceiver for Reconfigurable Multiple Access in Chip-to-Chip Communication **[18.6]**
- 0.94ps-rms-jitter 2.5GHz Multiphase Generator PLL for 10Gb/s Serial Links **[22.1]**
- 101dBc/Hz at 1MHz, 44GHz Differentially-Tuned VCO with 4GHz Tuning Range in 0.12μm SOI CMOS **[22.4]**

APPLICATIONS AND ECONOMIC IMPACT

- Further improvements on equalization techniques in the receiver allow higher data rates for legacy backplane connections. **[3.2, 3.5, 18.1]**
- Demonstration of a 40Gb/s CMOS transmitter and MUX/DEMUX circuits accelerate efforts toward implementing 40Gb/s transceiver and logic circuits in CMOS. **[8.1, 8.2]**
- Spread-spectrum clock generators with both low EMI and low jitter, can be used for the reliable chip implementation of SATA and other serial-link standards. **[8.6, 8.7]**
- Optical communications benefit from low-power and low-voltage laser drivers and high-speed and low-power burst mode receivers. **[12.1, 12.2, 12.4, 12.5]**
- Advanced technology and new circuit techniques are used to lower power and jitter and to increase the speed of the basic building blocks such as VCO, DCXO and PLL. **[22.1, 22.2, 22.4, 22.5,]**
- Shrinking CMOS linewidths enable increasingly complex and integrated transceivers.
- CMOS is taking over more and more from BiCMOS, SiGe, and GaAs, for the electrical and optical interconnections between chips, over backplanes, and between systems.
- The increase in transmission speed from 6.25 Gb/s to 40 Gb/s makes it possible to transfer the content of a whole DVD within less than 1 second. Such chips will be used in the backbone of the Internet, and will significantly contribute to faster access and download for the individual user of Internet services.

SPECIAL-TOPIC SESSION

Powerline LAN : Is There a Concrete Wall Dividing Wireless from Wireline? [SE1]

TUTORIAL

High-Speed Electrical Interfaces: Standards and Circuits [T8]

FORUM

ATAC: Automotive Technology and Circuits [F5]

BACKPLANE TRANSCEIVERS

A 6.4Gb/s CMOS SerDes Core with Feedforward and Decision-Feedback Equalization [3.2]

IBM

A 6.25Gb/s Binary Adaptive Decision Feedback Equalizer with First Post-Cursor Tap Cancellation for Serial Backplane Communications [3.5]

Texas Instruments

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Need to enable recovery of data-eye fully-closed from channel losses and crosstalk at 5Gb/s and above,in CMOS
- Legacy 1 to 3Gb/s backplane channels require transmit and receive equalization techniques at 5 Gb/s and above, but they are power hungry
- Bit-error-rate (BER) requirement of 10-15 or better mandates a holistic approach to transceiver design with full link-jitter modeling and verification

NOVEL CONTRIBUTIONS

- 2-tap VGA and peaking amplifier **[3.2],** and direct feedback of 1st tap **[3.5]** in receiver to cancel ISI
- Adaptation of equalizer coefficients to channel characteristics **[3.2, 3.5]**
- 2-path VGA design in receiver enables linear operation up to 1.2V p-p differential input signals **[3.2]**

CURRENT AND PROJECTED SIGNIFICANCE

- Doubles bit rate from existing 3Gb/s (XAUI) to 6Gb/s (Optical Internetworking Forum /CEI-CEI-6G+) backplanes **[3.2, 3.5]**

40Gb/s CMOS Transmitter Circuit

Circuit Techniques for a 40Gb/s Transmitter in 0.13μm CMOS [8.1]

Seoul National University

PRESENT STATE OF THE ART *(THE PROBLEM)*

- At 40Gb/s, integration level of CMOS is limited to small circuits such as 4:1 MUX
- Waveform degradation due to bandwidth limitation still a problem
- Power reduction required

NOVEL CONTRIBUTIONS

- Single-chip 40Gb/s transmitter with 20GHz PLL, 16:1 MUX, and PRBS generator **[8.1]**
- Judicious use of circuit techniques enables 40Gb/s transmitter with 0.13μm CMOS **[8.1]**
- Power consumption of 2.8W achieved **[8.1]**

CURRENT AND PROJECTED SIGNIFICANCE

- CMOS offers low-cost single-chip solution for up to 40Gb/s **[8.1]**
- More integration effort expected toward 40Gb/s CMOS receiver circuits **[8.1]**

OPTICAL COMMUNCATIONS

A 20Gb/s VCSEL Driver with Pre-Emphasis and Regulated Output Impedance in 0.13μm CMOS [12.2]

IBM; Cornell University; Agilent Technologies

1.25Gb/s Burst-Mode Receiver ICs with Quick Response for PON Systems [12.4]

NTT

A 12.5Mb/s to 2.7Gb/sContinuous Rate CDR with Automatic Frequency Acquisition and Data-Rate Readback [12.6]

Analog Devices

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Limited capability to handle different data rates and formats
- System interconnect now is limited to 1Gb/s and is bulky (large size) and uses expensive copper cables
- 10Mb/s Cable modem or ADSL

NOVEL CONTRIBUTIONS

- High-speed (20Gb/s) parallel optics and small light-weight low-cost cable **[12.2]**
- Burst receiver enables PON **[12.4]**
- Data rate is automatically detected and used **[12.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- Low-cost high-speed computer systems **[12.2]**
- PON is low cost for very high data rates (1G) to home **[12.4]**
- Low-cost metro-networks with the ability to transport any data formats already in use **[12.6]**

Frequency Modulation Methods for Improved Broadband Transmission

An RF/Baseband FDMA-Interconnect Transceiver for Reconfigurable Multiple Access in Chip-to-Chip Communication [18.6]

SST Communications

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Chip-to-Chip connections are fixed at design time, limiting system flexibility
- Coordinating multiple-access buses requires coordination between everyone on the bus; only one pair of chips can communicate at any one time.
- Transmission media can cause severe distortion at multi-Gb/s data rates.

NOVEL CONTRIBUTIONS

- High-bit-rate is accomplished by transmitting data at multiple frequencies. Each channel runs slower and is easier to design. **[18.6]**
- Unlike CDMA, rake filters are not needed. **[18.6]**
- No bus contention. **[18.6]**
- Connections become reconfigurable; any pair of chips can communicate uninterrupted. **[18.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- More-robust backplane transmission. **[18.6]**
- Allow smaller more-functional cheaper boards. **[18.6]**
- Alternative to ever-faster conventional serial transmission. **[18.6]**

A 0.94ps-rms-Jitter 0.016mm^2 2.5GHz Multi-Phase-Generator PLL with 360° Digitally-Programmable Phase-Shift Capability for 10Gb/s Serial Links [22.1]

IBM; Miromico

A 15mW 3.125GHz PLL for Serial Backplane Transceivers in 0.13μm-CMOS [22.2]

Synopsys

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Multi-Gigabit data transmission needs very-low-jitter clocks for low-BER operation.
- The cross-talk-rich environment of high-speed serial links makes clock requirement still more stringent.

NOVEL CONTRIBUTIONS

- A multiple-clock-phase PLL with dedicated phase detectors permits sub-ps rms tracking jitter at 10Gb/s. **[22.1]**
- Special circuit techniques and attention to loop dynamics enable a lower-power small-area PLL with 1.3ps rms-jitter at 3.125GHz. **[22.2]**

CURRENT AND PROJECTED SIGNIFICANCE

- Near-ideal multi-Gb/s clocks permit higher data rates over both new and existing links, , and enable greater transmission distances **[22.1, 22.2]**

SPECIAL-TOPIC SESSION

Powerline LAN: Is There a Concrete Wall Dividing Wireless from Wireline?

Organizer: ***Mark Ingels****, STMicroelectronics Belgium N.V., Zaventem, Belgium*
Chair: ***Michael Green****, Dept. of EECS, University of California, Irvine, CA*

OVERVIEW

- Powerline Communication (PLC) is an emerging technology that allows data transfer at high rates over existing power lines.
- The significance of PLC systems in practical situations will be highlighted
- Various existing chipsets with a potential data-transfer rate up to hundreds of megabits per se will be presented

OBJECTIVE

- To understand the significance of PLC for real-life and high-speed data communication within the home
- To present the major PLC solutions that are available today
- To investigate future technical and economic growth potential of PLC

CHALLENGE

- What is the use of PLC? Why is it viable? What is the future?
- How does PLC compete with Wireless LAN?
- How does PLC complete Wireless LAN?
- What type of data encoding should be used for high-speed communication on existing power wires?
- How to cope with emission?
- How to limit radiation?

STRUCTURE

- The first talk will provide a broad overview of PLC and will clarify its use and advantages. The following two presentations will present chipsets with data rates up to 14Mbps, and with a potential up to several hundreds of megabits. The final talk will present a narrowband system that is being deployed for remote control via power line.
- Speakers and specialties:
  - **Haniph A. Latchman, University of Florida: *"Broadband Powerline Multimedia Home Networking – Advantages and Challenges"***
  - **Jim Petranovich, Conexant Systems, Inc.: *"OFDM for Power Line Communications"***
    - In OFDM-based chipset, including challenges for practical implementation.
  - **Vincent Buchoux, LEA SA: *"Performance Analysis of a CDMA Chipset for InHouse BroadBand Powerline Communications"***
    - A new CDMA-based chipset, including performance and radiation issues
  - **Claudio Cantoro, Dora: *"Remote Control via Powerline"***
    - A narrowband system that is useful for (long-range) remote control.

RECAP

- To clarify what is PLC?
- To highlight its advantages and demonstrate its use in practical situations.
- To present various existing systems that enable real PLC transmission.

Tutorial

HIGH-SPEED ELECTRICAL INTERFACES: STANDARDS AND CIRCUITS

Yuriy M.Greshishchev, PMC Sierra Inc, Ottawa, Canada

OVERVIEW

The tutorial will review the physical level standard specification space (including standards under development), and the challenges in the multi-gigabit-range high-speed electrical-interface area, such as XFI, CEI , XAUI, Fiber-Channel, SAS, SATA, and others. Jitter requirements, signal amplitude, impedance, S-parameter specifications, and transmission-channel representation, along with equalization techniques, will be studied. Block diagrams and circuit solutions will also be discussed. This tutorial will assist attendees to understand IC design parameters, their link to standard specifications, and current and future challenges in wireline IC design of electrical interfaces for the multi-gigabit range.

SPEAKER BIOGRAPHY

Yuriy M.Greshishchev, PMC Sierra Inc, Ottawa, Canada, is a Technical Advisor on high-speed circuit design for wireline communications. His design experience is in multi-gigabit-rate CMOS, SiGe, and III-V circuits for telecom and datacom applications. He has been involved in XFI, Fiber Channel, SAS, RIO physical-level standards technical groups. He has been a member of the ISSCC Technical Program Committee for five consecutive years. He presented an ISSCC Tutorial on front-end circuit design for optical communications in 2001. He has coauthored two books and numerous technical papers in the area of high-speed communication-circuit design and data converters. He received his Ph. D. degree in Electrical and Computer Engineering from V.M. Glushkov Institute of Cybernetics, Microelectronics Division, Kiev, Ukraine, in 1984.

FORUM

ATAC: Automotive Technology and Circuits

Objective

This all-day forum is dedicated to automotive electronics, encompassing the associated high-voltage and high-power technologies, complex system developments, and robust circuit design required for automotive applications.

Attendance is limited, and pre-registration is required. This all-day forum encourages open interchange in a closed form.

Audience

The targetted participants are circuit designers working on the advanced development and design of automotive systems and chips, who want to learn about the latest developments in technology, system and circuit design for automotive applications.

Scope

While the automotive market has long been driven by innovations and improvements in the mechanical, hydraulic, and pneumatic systems of the car, this situation has changed, and the majority of innovations in cars is currently driven by electronics. Electronics will become even more pervasive for the foreseeable future, with a shift from separate electronic modules to fully- interconnected intelligent systems e.g. drive-by-wire.

This evolution, together with the growing use of high-performance sensors, requires increasingly complex and accurate electronic hardware and software in the car. At the same time, the stringent safety requirements are increasingly tightened while the harsh automotive-environment demands are further increased.

This forum discusses selected topics in automotive high-voltage and high-power technologies, complex system developments, and robust circuit design.

Program

The Forum will begin with a comprehensive overview of automotive electronic systems and market trends. **Patrick Leteinturier,** from Infineon, will discuss the challenges, and demonstrate the key elements needed, for the ongoing evolution/revolution of automotive electronics.

The next two papers will discuss semiconductor technobgies for automotive applications from the viewpoints of the car manufacturer and the semiconductor industry. First,**Masayuki Hattori,** from Toyota, will describe how several very-different semiconductor technologies are needed for their new generation of hybrid cars, including high-performance CPUs, complex high-voltage mixed-signal LSIs, and high-speed/low-saturation voltage IGBTs. In the second paper, **Hak-Yam Tsoi** from Freescale, will show

FORUM

ATAC: Automotive Technology and Circuits *(continued)*

Program *(continued)*

how high-power high-performance analog and complex digital circuits are combined in their SMARTMOS technology.

In the fourth and fifth papers, complex system-design issues and trade-offs for in-vehicle image processing and data communication, in the harsh automotive environment, will be discussed. **Shorin Kyo**, from NEC, will focus on architectural and system-design choices for image processing for driver- assistant systems, where a high computational requirement has to be balanced against a high power efficiency and system flexibility. **Stefan Poledna**, from TTTech, will then discuss the various requirements for in-vehicle data communication. Dependability of the communication channel is of major concern for the very different types of in-vehicle communications, such as interaction with smart sensors and actuators, data exchange for closed-loop control, diagnostic and repair information, multimedia and telematics.

The last three papers will focus on robust-circuit-design aspects for different automotive applications. **Koen Appeltans**, from AMIS, will first present the physical layer of a LIN (Local Interconnect Network) transceiver. He will pay attention to the non-standard aspects of integrated-circuit design for the harsh automotive environment, such as deeply-negative voltages, system ESD events, low electromagnetic emission, and high electromagnetic immunity. Gunther Leising, from LUMITECH, will then discuss the latest developments in high-luminous-flux and high-efficiency LED-packages and present current and future solutions for the thermal management and light-output shaping requirements. **Dirk Hammerschmidt,** from Infineon, will deal with the influence of automotive applications and micro-system technology on the system and circuit design of integrated magnetic-field and surface micro machined pressure sensors. These sensors have to be compatible with the IC technology on the one hand, while they require extensive signal processing to remove the sensor non-idealities, on the other.

At the end of the afternoon, all speakers will assemble in a panel format, for an open discussion with the audience, on the challenges in all aspects of automotive electronics.

ISSCC 2005

SESSION OVERVIEWS
Press-Release Material

- **Conditions of Publication**
- **Session Overviews**

CONDITIONS OF PUBLICATION

PREAMBLE

- **The Session Overviews to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2005 in February in San Francisco.**
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- **From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 52nd appearance of ISSCC, on February 6th to 10th, in San Francisco.**

This and other related topics will be discussed at length at ISSCC 2005, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 6-10, 2005, at the San Francisco Marriott Hotel.

Non-Volatile Memory

Chair: *Yair Sofer, Saifun Semiconductors, Netanya Israel*
Associate Chair: *Yukihito Oowaki, Toshiba, Kawasaki Japan*

Consumer-electronic applications such as cellular phones and digital cameras are driving a need for higher-performance and lower-cost-memory solutions. This year's Conference by is marked a strong show of non-volatile memories. In the Flash memory arena, we are seeing major breakthroughs in density, performance and cutting-edge lithography. We have seen a sprinkling of multi-level Flash papers since 1995. This year, multi-level Flash makes up the majority of the non-volatile memory presentations that report on new design approaches. Designs utilizing multi-level techniques have historically been lower-performance. With design and technology breakthroughs, we are seeing high-performance read and write times combined with multi-level storage.

This session will also look into new circuit techniques to achieve much-faster lower-power flash programming. As well, recent advancements in the area of emerging nonvolatile technologies will be reported.

In Papers 2.1 and 2.2 exhibit the highest-density Flash memories ever reported — (8Gb) — fabricated in advanced 70nm and 63nm technologies and using a multi-level approach and NAND structure. Write performance is dramatically improved to reach a level comparable with single-bit-per-cell memories.

A 1.8V 64Mb phase-change RAM (PRAM) fabricated in a 0.12μm technology is described in Paper 2.3. The paper presents techniques to improve write distribution and read margins.

An in-package inductor and capacitor are utilized for the first time to implement a hybrid voltage multiplier to improve write performance, power efficiency, and to save area, in a NOR Flash product. This scheme is described in Paper 2.4.

A 256Mb NOR Flash featuring an innovative sensing concept, based on a fast gate-voltage-ramp, which operates the cells at constant current is discussed in Paper 2.5. It overcomes the main drawbacks of multi-level NOR scaling.

A 512Mb 90nm NOR Flash, presented in Paper 2.6, has the fastest synchronous-read frequency and programming throughput ever reported.

Finally, the first 4Gb multi-level AG-AND Flash to achieve 10MB/s write throughput is reported in Paper 2.7.

Backplane Transceivers

Chair: *Mehmet Soyuer, IBM, Yorktown Heights, NY*
Associate Chair: *Muneo Fukaishi, NEC, Kanagawa, Japan*

The increasing clock rates of processing cores accompanying continuing advances in silicon technology drive the need to push electrical interconnect speeds higher. As industry-standard data rates pass 3Gb/s and approach the 5 to 12Gb/s realm, degradations from channel effects such as bandwidth loss, reflections, and crosstalk, can distort the signal to such an extent that robust data recovery requires equalizer-based backplane transceiver designs. Legacy 1 to 3Gb/s backplane channels rely on power-efficient NRZ transmit- and receive-side equalization techniques with adaptation. New signaling schemes, with better spectral efficiency, such as PAM4 and duobinary signaling, are of interest for data rates exceeding 10Gb/s. Another design challenge is the low bit-error-rate (BER) requirement of 10^{-15} or less.

As highlighted by the first five papers in this session, these requirements are currently being addressed by transceiver designs using NRZ signaling in 0.13μm CMOS, targeting data rates from 5Gb/s to approximately 10Gb/s. Overall, the transceivers described in Papers 3.1 through 3.5 employ feedforward equalization and decision-feedback equalization techniques. This combination helps to optimally compensate for bandwidth losses, providing with improved immunity to inter-symbol interference (ISI) and crosstalk.

A 5Gb/s NRZ transceiver with a 2-tap pre-emphasis network in the transmitter, along with a 1-tap FFE and 3-tap DFE in the receiver, is featured in Paper 3.1. It achieves a BER of less than 10^{-15} over 4 pairs of 1m PCB traces, in the presence of crosstalk.

A 4.9 to 6.4Gb/s transceiver core is described in Paper 3.2. The use of a 4-tap FFE, a 2-path VGA, and a peaking amplifier followed by a 5-tap DFE, enables operation on ISI channels with over 30dB loss at 3.2GHz. It achieves a power efficiency of 45mW/Gb/s.

A transceiver core operating from 0.6 to 9.6Gb/s using adaptive receive equalization with a 1-tap DFE followed by a linear equalizer, is described in Paper 3.3. The core dissipates only 150mW at 6.25Gb/s.

The 6.25Gb/s transceiver described in companion Papers 3.4 and 3.5 highlights a 4-tap DFE architecture that uses direct feedback of the first-tap output to cancel post-cursor ISI. It operates at a BER less than 10^{-16} over legacy 1Gb/s backplane channels.

The last two presentations of this session describe a 90nm CMOS 12Gb/s duobinary transceiver and a 90nm SOI 25Gb/s PAM4 transmitter. Duobinary signaling, with a 10-tap 2x-oversampled equalizer used to achieve 12Gb/s over a 75cm low-k PCB trace, is employed in Paper 3.6. The measured eye height is 3dB larger than for NRZ signaling. The PAM4 transmitter in Paper 3.7 targets short-range chip-to-chip interconnects. It features a 4-tap FIR filter, and achieves a power dissipation of 100mW at 25Gb/s.

Mixed-Domain Systems

Chair: *Kerry Bernstein, IBM, Essex Junction, VT*
Associate Chair: *Siva Narendra, Intel, Hillsboro, Oregon*

Hybrid interdisciplinary technologies enable an exciting and powerful new integration direction. Development of monolithic mixed-domain structures (such as DRAMs embedded in high-performance logic chips), so far, have focused on co-optimizing MOSFET, bipolar, and other silicon-based devices. Dimension scaling has brought CMOS to a size regime where it is now possible to exchange data with living neurons; to sense the state of individual atoms; and ultimately to reproduce human sensory function in a biological form factor. These advances are made possible by the convergence of VLSI with improvements in ancillary technologies, such as micromechanical machining, optics, and thin films. Mixed-domain systems promise to reduce latency, extend resource utilization, and increase transaction rate. Additionally, new capabilities are enabled and existing functions are realized with lower power and cost, by such mixed-domain systems.

Electrochemical as well as magnetic interaction with living tissue is explored in Papers 4.1 and 4.3. New work exploring neuro-electronic junctions is described in Paper 4.1. The interfacing between electronic and ionic systems must be examined at the ion channel, nerve cell, and extended-network/brain-tissue level in order to facilitate interchangeable signal processing, and this paper describes the unique approaches initiated to achieve these milestones. The magnetic tags, described in Paper 4.3, enable the use of CMOS logic to manipulate cells attached to these tags in a medium layered immediately above the logic. The potential impact of such a technique is readily apparent.

Direct stimulation of auditory nerves using a processor in a bionic ear is described in Paper 4.2. Much more than improving conventional hearing-aid techniques, this device maps its logarithmic-spectral-filter output to a set of topographic stimulation electrodes. By accessing the cochlea directly, the technology can emulate the fundamental biological hearing process.

The synchronous digital state machine is one of a number of architectural paradigms that are realized with current fabrication capabilities. Atomistic and, more recently, quantum-mechanical limitations arising from continued scaling require increasing timing margin and tolerance; these concerns make the analog-computer/math-co-processor advocated in Paper 4.4 very interesting and timely.

The final three papers in this session explore the integration of CMOS with MEMS and optics technologies to bring new functions on-chip. An on-chip MEMS-based low-power atomic clock is described in Paper 4.5. This chip is more than 700x smaller in volume than the state-of-the-art commercially-available atomic clocks, while delivering comparable precision. MEMS is also an enabler for realizing gyroscopes in CVD SiGe films deposited on conventional CMOS. Robust outputs are developed from larger capacitive-coupled signals, as shown in Paper 4.7. The observed improvements in signal-distribution precision in processors, and the latency-reduction realized in hardware, is presented in Paper 4.6. These improvements are achieved by the integration of optical interconnects with conventional CMOS. For the first time, less than 1ps of measured rms jitter is reported.

WLAN Transceivers

Chair: *Arya Behzad, Broadcom, San Diego, CA*
Associate Chair: *Mototsugu Hamada, Toshiba, Kawasaki, Japan*

Mass-consumer-market wireless applications set strict requirements on cost, dynamic range, power consumption, and the number of external components used in the system. These constraints have already been applied to Bluetooth chips, and the resultant chips have been reported at previous ISSCCs. This year, we see these trends being applied to WLAN ICs, and similar levels of integration being demonstrated in WLAN SoCs. As such, many of the most-integrated solutions are implemented in deep-submicron CMOS technologies which allow the full integration of the MAC and the PHY layers on the same die. These highly integrated low-cost low-power ICs open the door for the application of WLAN ICs to many new embedded and non-embedded applications, and ultimately to a seamlessly connected world.

A I/Q self-calibrating super-heterodyne CMOS 802.11g transceiver is presented in Paper 5.1. As a result of the calibration scheme, 1° phase mismatch and 0.1dB amplitude mismatch is achieved. There is only a 5% die-area penalty for implementing this calibration scheme. The die occupies an area of 10.2mm^2.

The authors present the most-integrated 802.11g SoC published to date in Paper 5.2. The chip utilizes a sliding-IF super-heterodyne architecture, and includes the RF, analog, MAC and PHY functions in a single CMOS die. The receiver achieves a sensitivity of -73dBm and -95dBm at 54Mb/s and 1Mb/s, respectively. The transmitter is capable of transmitting +4dBm. The die occupies an area of 41mm^2.

A fully-integrated direct-conversion CMOS 802.11b SoC is presented in Paper 5.3. This SoC integrates all of the radio building blocks, including the PA, loop filter, and the antenna switch, along with the analog and digital PHY and MAC blocks. The receiver achieves a sensitivity of -88dBm at 11Mb/s. The transmitter is capable of transmitting a nominal output power of +13dBm. The die occupies an area of 32.2mm^2.

A dual-band direct-conversion CMOS 802.11a/b/g transceiver is described in Paper 5.4. It achieves an RX NF of 5dB and a TX EVM of -31dB while transmitting 1dBm at 5GHz. The chip occupies only 6mm^2.

Another CMOS direct-conversion 802.11a/b/g transceiver is reported in Paper 5.5. It achieves an RX NF of 4.2dB and a sensitivity of -94dBm at 6Mb/s and 5GHz. The die occupies 17.2mm^2.

A BiCMOS SoC for bidirectional point-to-multipoint wireless digital-audio applications is described in Paper 5.6. It utilizes the 863 and 915MHz bands. It achieves an RX current consumption of 3.8dB and a sensitivity of -94dBm for the U.S. 918 kb/s mode.

A dual-band frequency synthesizer for 802.11a/b/g with a fractional-spur averaging technique is described in Paper 5.7. It achieves a 10kHz to 10MHz integrated phase noise lower than 1.25° rms for any of the synthesized channels.

A fully-integrated transformer-based RF front-end which integrates matching and T/R switch functions on the CMOS chip is reported in Paper 5.8. An example of the application of the technique to a Bluetooth IC is demonstrated. It achieves a receiver sensitivity of -90dBm and a transmitter power of +2dBm.

High-Speed and Oversampled DACs

Chair: *Robert Neff, Agilent Technologies, Palo Alto, CA*
Associate Chair: *Zhongyuan Chang, IDT-Newave Technology, Shanghai, China*

This session highlights the state-of-the-art in high-speed and oversampled DACs, including high-accuracy signal synthesis beyond 1GHz, and the doubling of sample rates for 6b-resolution DACs to 22GS/s. An oversampled ADC/DAC-based power amplifier and an RF power detector are also presented.

Signal resampling is a common technique for improving accuracy in DACs, resulting in an RTZ waveform. In baseband DACs, resampling results in unwanted signal content above the Nyquist frequency. Several refinements to resampling techniques are presented. The authors of Paper 6.1 employ two identical time-interleaved RTZ 15b DACs, resulting in an NRZ waveform with exceptional signal accuracy. An RTZ DAC with wideband performance, generating waveforms in the second and third Nyquist bands and allowing direct synthesis of RF waveforms up to 2GHz, is presented in Paper 6.2. In this DAC, the RTZ signal is a desirable resampling artifact, resulting in less sin(x)/x distortion.

These GS/s high-resolution DACs require expensive data sources with high-speed memory and/or digital signal processing and high-speed high-power data I/O. The circuit described in Paper 6.3 solves this external computation and I/O problem by integrating direct-digital frequency synthesis on-chip with a 1.7GS/s DAC.

A minimum-complexity circuit-design approach, demonstrating that a state-of-the-art high-accuracy 500 MS/s CMOS DAC can be implemented with a conventional architecture, is presented in Paper 6.4.

An oversampled RTZ DAC, presented in Paper 6.5, demonstrates that two time-interleaved DACs with two phase-adjusted data interpolators can synthesize 11.9b-accurate signals in a 29MHz bandwidth. These architectural innovations are primarily in the digital domain, and improve total DAC performance.

It is a challenge to simultaneously achieve both high accuracy and high efficiency in audio power amplifiers. The implementation in Paper 6.6 uses a $\Delta\Sigma$ modulator to create a bitstream to drive a class-D amplifier. Directly applying this bitstream would result in switching the amplifier at speeds up to 3MHz, which would result in low power efficiency. A technique to reduce the maximum frequency component to around 450kHz, and meeting both design goals, is introduced.

A 22GS/s 6b SiGe BiCMOS DAC, presented in Paper 6.7, is over twice as fast as any 6b design previously published.

The power detector presented in Paper 6.8 improves on the state-of-the-art in offset control for RF-power-detector applications, demonstrating performance that is even superior to laser-trimmed parts. It uses a chopping technique previously seen in precision amplifiers and mixers.

Multimedia Processing

Chair: *Lee-Sup Kim, KAIST, Daejeon, Korea*
Associate Chair: *Masafumi Takahashi, Toshiba, Kawasaki, Japan*

The demand to meet new standards within a tight power budget in emerging multimedia applications requires highly integrated and power-optimized solutions. This session presents a variety of subsystems with advanced multi-media features such as an H.264/AVC single-chip encoder for high-definition (HD) video, a low-power MPEG-4 advanced-simple-profile (ASP) audio/visual CODEC for HD applications, an H.264/MPEG-4 audio/visual CODEC for mobile applications, a stream processing unit of the CELL processor, a triple-CPU mobile-application processor, a multimedia-applications processor for wireless devices, and an analog CMOS auditory filter bank, for speech recognition.

Paper 7.1 implements the first H.264/AVC encoder IC. A four-stage pipelined architecture and 1.3TOPS motion estimators are used to achieve 720p HD video encoding (1280x720 @ 30 frames/s). The encoded video quality is competitive with reference software requiring 3.6 TOPS on a general-purpose processor-based platform.

An MPEG-4 video/audio CODEC for 720p HD mobile applications is presented in Paper 7.2. This is the first implementation to support MPEG-4 ASP, including B-VOPs. High-performance and cost-effective architectures are proposed.

Paper 7.3 presents an H.264/MPEG-4 video/audio CODEC LSI for mobile applications. This LSI adopts module-wise dynamic voltage/frequency scaling for the first time. It operates even during the voltage/frequency transition with no performance overhead, by using a dynamic de-skewing system and an on-chip voltage regulator with slew-rate control.

The micro-architecture of a 4-way SIMD stream-processing unit of the CELL processor is described in Paper 7.4. It minimizes instruction latency and provides fine-grain clock control to reduce power. Software controls data movement and instruction flow, and improves data bandwidth and pipeline utilization.

In Paper 7.5, three CPUs, a DSP, and several accelerators are integrated into a single chip for digital TV, web browser, and 3D graphics applications. Several techniques to increase memory bandwidth and to reduce power consumption are also described.

A new generation of multimedia-application processors is presented in Paper 7.6. An efficient set of leakage-reduction techniques, including power gating, voltage scaling, and dual V_t are adopted to reduce the standby current.

Paper 7.7 presents an ASIC that emulates the inner ear using a bank of 100 exponentially distributed asymmetric band-pass filters. Output is encoded into an auditory-nerve-like pulsed format available at a digital port.

Circuits for High-Speed Links and Clock Generators

Chair: *Hirotaka Tamura, Fujitsu Laboratories, Kanagawa, Japan*
Associate Chair: *Sung Min Park, Ewha Womans University, Seoul, Korea*

The scaling of transistor expands the territory of CMOS high-speed links toward consumer electronics, and high-end communication applications. The data rate has already reached 10Gb/s, and is approaching 40Gb/s. The keys to this technology trend are the continuous improvement in performance of component-level circuits and their integration. The papers in this session present progress in the performance and integration levels of key components like MUXes, DEMUXes and clock generators.

The authors of Paper 8.1 present a 0.13μm CMOS 40Gb/s transmitter that is composed of a 16-to-1 MUX, and clock, and a PRBS generator. Shunt-and-double series-inductive peaking, and negative feedback, are used to enhance the bandwidth of the MUX. The 38.4Gb/s (2^{31}-1) PRBS transmitted eye has a differential voltage swing of 549mV_{pp}, rise time of 14ps, and clock jitter of 0.65ps_{rms}, and 4.9ps_{pp}. A 4-to-1 MUX and a 1-to-4 DEMUX in 90nm CMOS are described in Paper 8.2. The MUX and DEMUX operate from a 1.2V single supply, and draw 110mA and 52mA, respectively.

Distributed amplifier topologies realize the wide bandwidth that is needed to amplify high-speed serial signals. In Papers 8.3 and 8.4, CMOS distributed amplifiers are described. An 80GHz distributed amplifier in 90nm CMOS is featured in Paper 8.3. The amplifier exhibits 7.4dB gain with a 3dB bandwidth of 80GHz, using both a capacitor-coupled gate and low-loss coplanar waveguide. In Paper 8.4, a non-uniform downsized distributed amplifier using 0.18μm CMOS transistors is discussed. The amplifier achieves a differential forward gain of 7.8dB over a 25GHz bandwidth, and exhibits an IIP3 of +4.7dBm while drawing 30mA from a 1.8V supply.

High-speed serial links mandate reliable clock generation; the focus of Paper 8.5 is a 1V 24GHz PLL in 0.18μm CMOS. The PLL uses transformer-feedback and a stacked frequency divider. The PLL provides an in-band phase noise of 106.3dBc/Hz at 100kHz offset, and an out-of-band phase noise of 119.1dBc/Hz at 10MHz offset, while consuming 17.5mW and occupying an area of 0.55mm^2.

The authors of Papers 8.6 and 8.7 present spread-spectrum clock generators for serial ATA that currently supports 3Gb/s serial transfer. Paper 8.6 describes a 0.15μm CMOS spread-spectrum clock generator that uses a fractional PLL controlled by the ΔΣ modulator. The clock generator achieves a peak spurious reduction level of 20.3dB, and a random jitter of 8.1ps in 250-cycle averaging period. A technique that uses 10 multi-phase clocks and a ΔΣ modulator is discussed in Paper 8.7. The deterministic jitter due to spread spectrum is 25ps, and the amount of spreading exactly conforms to the serial ATA specification.

Switched-Capacitor Delta-Sigma Modulators

Chair: *Willy Sansen, Katholieke Universiteit, Leuven, Belgium*
Associate Chair: *Andrea Baschirotto, University of Lecce, Italy*

In this session, several advances are presented in the design and realization of A/D converters, based on a ΔΣ modulator (ΔΣM) implemented with switched-capacitor techniques.

The major developments are the implementation of low-voltage (0.6V) circuits, the use of 90nm CMOS technology, the realization of wideband ΔΣMs, and the realization of two audio ΔΣMs (DR>100dB) in a 20kHz bandwidth.

The switched-RC integrator technique, which enables the operation of the ΔΣM at 0.6V without any clock-boosting, bootstrapping, or switched-opamp techniques, is introduced in Paper 9.1. In addition, low-voltage operation is enabled by the use of a feedforward topology to reduce the dynamic range at the integrator output node. These techniques are applied to a 2-2 MASH ΔΣM that achieves 82dB DR in the audio band, with 1mW power consumption.

In the next two papers, the authors report the implementation of two ΔΣMs in 90nm technology. The main issue addressed in Paper 9.2 is that a large power reduction is achieved in a 2nd-order multibit ΔΣM by truncating the quantizer output while digitally shaping and cancelling the relative error. The target of 58dB DR in a 2MHz bandwidth is achieved with good capacitor matching, which does not require the implementation of any DEM circuitry. The second ΔΣM in 90nm CMOS technology (Paper 9.3) reduces the power consumption by using a single-amplifier double-sampling 2nd-order 5b topology. The typical drawback of double-sampled structures is the path mismatch effects, which are alleviated by a proposed single-capacitor technique. This gives a 66dB DR in a 1.94MHz bandwidth, with1.2mW power consumption.

Wideband ΔΣMs with significant DR performance are reported in the next two papers. In Paper 9.4, a 2-2-0 MASH structure (with a 3b last stage) is proposed to achieve a 100dB SNR in a 1MHz bandwidth. The power consumption of the complete ADC (including ΔΣM core, input buffer, reference voltages, and decimator filter) is 475mW from a dual supply (2.5V/5V).

In Paper 9.5, several background digital linearization and noise-cancellation algorithms are introduced to improve the analog performance (in particular SNDR and SFDR) over a very large bandwidth. A 2-0 MASH structure is used, where the 1st stage uses a 4b quantizer (with DEM linearization) and the 2nd stage uses a 9b pipeline. The structure operates with an 80MHz sampling frequency, and achieves 75dB DR, and more than 87dB SFDR, in a 10MHz bandwidth. The digital algorithms are demonstrated to not degrade the analog performance.

Finally, the same overall architecture, but with different implementations, is used in the last two papers. They couple an input continuous-time stage with a switched-capacitor 2nd stage, and a 17-level quantizer to reduce clock jitter, which affects DAC feedback in continuous-time systems.

A fully-differential structure is described in Paper 9.6. It focuses on a hybrid tuning circuit to keep the RC product constant across process, supply, and sampling-rate variations. In addition, the feedback DAC ISI is eliminated by an RTZ scheme applied on the error current of the CT integrator. This allows a significant 106dB DR with 18mW power consumption (including decimator filter) in a 0.35μm CMOS technology.

An interesting solution for achieving high DR and high linearity with a single-ended input is proposed in Paper 9.7. The input stage includes an accurate CM control and a chopper structure. In this way, a 102dB SNR is achieved in the audio band with about 38mW power consumption in a 0.18μm CMOS technology.

Microprocessors and Signal Processing

Chair: *Georgios Konstadinidis, SUN Microsystems, Sunnyvale, CA*
Associate Chair: *Sung Bae Park, Samsung, Yongin-City, Korea*

Microprocessor-frequency scaling is coming up against fundamental barriers that have the potential to limit future performance gains for traditional single-processor systems. In this session, new designs are presented that incorporate extensive parallelism, or multiple processing units, to enhance overall chip performance, without the difficulties associated with higher clock frequencies. This trend is clearly illustrated in this session, where all eight papers describe chips containing multiple processor cores of various types. One of the most significant performance-limiting barriers is power consumption. Overheating and power issues have plagued recent processors, causing frequency reductions or product cancellations. New approaches to exploiting one of the most promising techniques for power reduction, namely dynamic voltage and frequency scaling, are discussed in this session.

Implementation of a next-generation Itanium® processor is described in Paper 10.1. It is comprised of two dual-threaded cores integrated on the same die with a 26.5MB cache in a 90nm. In addition to performance improvements, this design reduces susceptibility to soft errors, and improves power efficiency through low-power techniques and active power management.

The first-generation multi-core SoC CELL processor, described in Paper 10.2, combines eight streaming processors on a chip providing a high-performance platform for multimedia and streaming workloads These processors are designed with features specifically targeted for certain applications, saving power and area by this narrower application focus. Implemented in a 90nm SOI process, the chip incorporates extensive power- and thermal-management techniques.

The processor described in Paper 10.3 also follows the dual-core approach to improving performance through parallelism. This fourth-generation SPARC® processor combines two enhanced third-generation cores with expanded caches and an on-chip 2MB L2 cache. Fabricated in a 90nm technology, it operates at 1.8GHz from a 1.1V supply.

Another approach described in Paper 10.4 (BlueGene/L) uses low-cost small power-efficient processors in a massively-parallel fashion. This complex SoC ASIC includes two processor cores, embedded DRAM, SRAM and custom logic, achieving a high-power/cost-performance trade-off, suited to its role as a building block of IBM's BlueGene/L supercomputer.

Graphics and multimedia processing for portable and consumer applications are addressed in Papers 10.5 and 10.6. An SoC targeting systems such as game consoles, digital television, and next-generation DVD players, is described in Paper 10.5. The 50mm^2 chip, containing 17.9M transistors, is fabricated in 0.13μm CMOS. It integrates an ARM11 RISC processor with a dedicated 3D graphics pipeline, and supports analog-video outputs.

An IC that supports high-resolution graphics for mobile multimedia applications is discussed in Paper 10.6. This chip combines a RISC core with an SIMD graphics engine. Power-management techniques enable graphics performance of 50Mvertices/s and 200Mtexels/s while dissipating 155mW in 0.18μm CMOS.

The trend toward single-chip multiprocessors for media applications is continued in Paper 10.7. It describes the integration of four 8-way VLIW processors in a 122mm^2 chip fabricated in 90nm CMOS.

Lastly, in Paper 10.8, multiple reconfigurable logic blocks are integrated with a VLIW RISC processor and reconfigurable I/Os to improve performance and power efficiency.

Ultra Wideband Solutions

Chair: *Ali Hajimiri, California Institute of Technology, Pasadena, CA*
Associate Chair: *Tom Schiltz, Linear Technology, Colorado Springs, CO*

The last decade has seen an exponential increase in the demand for higher bit rates for existing and emerging applications. Until recently, this has been addressed by the gradual migration from low-speed dial-up to higher-speed Ethernet and fiber. Unfortunately, these broadband solutions require a wired connection that limits users' mobility. Emergence of broadband high-quality video and audio applications as well as high-speed home and enterprise networking makes it highly desirable to achieve similar bit rates in a wireless fashion. This has led to many efforts toward wireless networking solutions, e.g., 802.11x. Although they provide wireless connectivity, most are limited to bandwidths of several tens of Mb/s. However, instantaneous bit rates as high as 1Gb/s are desirable in many applications. Such an increase in data-handling capacity necessitates substantially more-aggressive approaches to signaling method, system design, and circuit design. Several approaches have been proposed to increase bit rates using broader bandwidths (e.g., 3 to 10GHz) and/or moving to higher frequencies (e.g., 24GHz and 60GHz). Recently FCC's blessing of two new UWB standards, and the availability of several higher frequency ISM bands, will likely reinvigorate new efforts in the UWB arena. This session explores the most-recent developments in UWB, and offers a broad set of solutions, ranging from OFDM-based systems operating in the 3-10GHz band, to high-frequency multiple-antenna systems taking advantage of the higher bandwidth and array gain.

The receiver chain and the frequency-generation block of an integrated UWB radio in SiGe BiCMOS are presented in the first two papers. A wideband LNA, a mixer, and the IF blocks, with an overall NF of 7.5dB, are featured in Paper 11.1. The frequency-synthesis block is presented in Paper 11.2. Frequency hopping is achieved using two PLLs and a single-sideband mixer with a fast switching time of 1ns.

A broadband CMOS frequency synthesizer capable of switching between different frequencies from 3 to 8GHz with 1ns settling time is described in Paper 11.3. A semi-dynamic regenerative frequency divider for OFDM-based UWB systems is featured in Paper 11.4.

A direct-conversion UWB receiver in SiGe BiCMOS that operates from 3.1 to 8.1GHz is reported in Paper 11.5. It has a peak conversion gain of 52dB with a NF between 3.3 and 4.1dB. The receiver has an on-chip frequency synthesizer generating the LO from 3.4 to 7.9GHz.

Multiple-antenna systems promise many performance improvements for broadband systems. The next two papers explore the numerous possibilities for higher speed using multiple antennas. A 5GHz multiple-antenna receiver implemented in 90nm CMOS is described in Paper 11.6. It can be used to extend the range of existing multiple-antenna systems. It has full 360° coverage, and achieves 6dB SNR improvement due to the array gain.

A fully-integrated four-element 24GHz phased-array transmitter in 0.18μm CMOS with integrated PAs, is featured in Paper 11.7. With a peak-to-null power ratio of 23dB and an effective isotropic radiated power (EIRP) close to 1W, it supports bit rates in excess of 500Mb/s, bringing us closer to a wireless gigabit Ethernet solution.

The final two presentations demonstrate integrated UWB transceivers in CMOS. The DSSS UWB transceiver in Paper 11.8 covers the 3.1 to 5GHz band with a programmable pulse-shaping circuit on the transmit side and a NF of 4dB in 0.18μm CMOS. Finally, a 0.13μm CMOS transceiver is presented, in Paper 11.9, that achieves a NF in the range of 5.5 to 8.4dB across the three UWB sub-bands.

Optical Communications

Chair: *Larry DeVito, Analog Devices, Wilmington, MA*
Associate Chair: *Yusuke Ohtomo, NTT, Kanagawa, Japan*

Communication using light signals over optical fiber holds great promise to lower costs for all data transport over both short and long distances. The huge bandwidth and favorable physical characteristics of optical fiber beg to be exploited: In telecom networks, transmitting high-data-rate signals over long distances becomes practical; In computer systems, high-capacity interconnect, free from electromagnetic interference and awkward bulky copper cables, is enabled by parallel optics. But, of course, practical details limit cost-effective commercial solutions. In this session, several advances in the practical art of sending and receiving optical signals, are presented. Inevitably, such advances will lead to exciting new cost-effective telecom services and higher-performance computer systems.

A 10Gb/s laser driver with impedance-matched electrical output is presented in Paper 12.1. It enables the use of a low-cost TO-can package for the laser. Previously, the hostile electrical characteristics of such a low-cost package have impaired the optical eye of the transmitted optical signal due to reflections of the electrical-drive signal.

A step towards short-distance high-capacity interconnections within a single computer system, using parallel optical fibers assembled in a ribbon format, is addressed in Paper 12.2. A backplane comprising 48 parallel channels, each operating at a data rate of 20Gb/s, is the goal of this laser driver. A low-cost vertical-cavity surface-emitting laser (VCSEL) has speed limitations that are overcome in this circuit by using pre-emphasis on the electrical-drive signal.

An astonishing new idea for long-haul telecom applications is described in Paper 12.3. Two optical carriers in quadrature are combined to compensate chromatic dispersion in the fiber: each optical carrier is modulated with a predistorted duobinary signal. This paper demonstrates the practicality of the high-speed signal processing needed for this system to transmit 10Gb/s data over 400km of fiber.

In Papers 12.4 and 12.5, a significant increase in the data rate of burst-mode communication for passive optical networks (PONs)is reported. This holds the promise of delivering high-data-rate connections to the home. A 1.25Gb/s optical front end is demonstrated in Paper 12.4. It tolerates bursts of widely different amplitudes and settles in 20 unit intervals(UIs). The first monolithic 10Gb/s burst-mode CDR with a lock time of 5UIs is presented in Paper 12.5. These circuits both represent enabling technologies for low-cost PON implementation.

A continuous-tuning CDR for the range of 12.5Mb/s to 2.7Gb/s is presented in Paper 12.6. Unaided acquisition of any data rate provides unprecedented flexibility in the provisioning of metropolitan-area networks. Alien data rates can now be transported over the public network without first being translated into a telecom standard format. This, of course, will lower the cost for end users.

The final two papers in this session are short papers. A new peak-detector circuit idea that enables implementation of very-fast offset compensation in a 3.125Gb/s optical-receiver limiting amplifier is introduced in Paper 12.7. The peak detector, implemented in 0.18μm CMOS, dramatically improves the trade-off between settling time and data-dependent jitter.

A positive-feedback boot-strap circuit to compensate the deleterious effects of both photodiode and ESD parasitic capacitances in a 2.5Gb/s fiber-optic transimpedance amplifier is shown in Paper 12.8. Inclusion of ESD protection provides more robust circuits, tolerant of real-world abuses.

Sensors

Chair: *Euisik Yoon, KAIST, Daejeon, Korea*
Associate Chair: *Navakanta Bhat, IISc, Bangalore, India*

This session highlights recent advances in a variety of sensors that interface the electronics world with the natural world. Natural signals are converted into electrical signals using integrated sensing elements with on-chip signal-conditioning electronics. System-on-a-chip mixed-signal integration enables on-chip calibration to achieve advances in higher accuracy, as well as to enable a significant amount of digital processing for intelligent decision making.

The papers in this session illustrate this process: How sensing elements can be realized in conventional CMOS technologies for magnetic sensing, for finger-print sensing, for environmental sensing, for temperature sensing and for inertial sensing.

There are multiple examples presented of the power of integrating a sensor with electronics: The first paper (13.1) realizes a smart CMOS temperature sensor with a 3σ inaccuracy of $\pm 0.1^{\circ}C$. Advances in sensor design combined with dynamic element matching and a low-offset ADC, lead to increased precision. In Paper 13.3 on a magnetic sensor, the ability to add coils along with an analog front end, enables a new reference modulation and demodulation technique leads to in-situ calibration of the magnetic sensor element, to compensate for aging. In Paper 13.5, fully-integrated electronic calibration combined with four orthogonally coupled, 8-direction spinning-current Hall-plates, allows a solid-state compass. As described in Paper 13.2, a single-chip CMOS magnetic rotary encoder integrates a split-drain MAGFET sensor array with on-chip mixed-signal electronics. As described in Paper 13.6, combining MEMS structures with $\Delta\Sigma$ closed-loop circuitry enables a high-resolution accelerometer.

A prime example of the powerful consequence of combining sensor elements with electronics is provided in Paper 13.4, which describes a microsystem which is able to perform trace environmental monitoring of heavy-metal contaminates such as lead, down to the level of 0.8 ppb.

Finally, there are two papers (13.7 and 13.8) that carry out on-chip image-enhancement preprocessing on a capacitive fingerprint-recognition sensor. In Paper 13.7, this is accomplished through the use of reconfigurable column-parallel digital processors for adaptive filter operations; in Paper 13.8, the same task is done through an embedded 32-bit RISC micro-controller.

Low-Power Wireless and Advanced Integration

Chair: *Robert Mertens, IMEC, Leuven, Belgium*
Associate Chair: *Francis Jeung, Brand in Chip, San Jose, Ca*

Low-power wireless technologies and advanced integration continue to open up new opportunities in a variety of applications. In the field of low-power wireless technologies the main challenges are the further reduction of the power and the continued system miniaturization. This session illustrates that innovative new concepts such as low power SoCs, on-chip antenna integration and more efficient rectifier ICs strongly contribute to meet these requirements. Additional challenges in the nano era include design for manufacturability of such miniaturized systems while maintaining the signal integrity. As we enter the era of ambient intelligence more electronic systems will be integrated on mechanically flexible substrates such as plastic and therefore new integration technologies need to be developed.

A rectifier IC for wireless power transmission with low-input RF power is reported in Paper 14.1. The IC achieves a 950MHz signal rectification at -14dBm input power corresponding to a 10m-distance communication. In Paper 14.2 a wireless SoC, integrating a dual 433/868MHz transceiver a RISC micro-controller, an SRAM, a sensor ADC and a power management unit is presented.

In Paper 14.3, the polysilicon gated-nanowires integrated into a CMOS process are reported. Memory cells based on this concept are among the very few reported functional hybrid CMOS-nanowire cells working at room temperature, with very low energy consumption (tens of pWs) and excellent scalability.

Three-dimensional integration schemes are proposed in Papers 14.4, and 14.5. In Paper 14.4 a new 3D integration scheme is proposed utilizing local wireless interconnect (LWI) and global wireless interconnect (GWI). LWI transfers pulses utilizing resonant coupling of spiral inductors, with 1Gb/s, 0.5ns delay and several mW power dissipation while GWI realizes over 10GHz clock with electromagnetic waves using integrated antennas through stacked chips. In paper 14.5 a wireless interface by inductive coupling is proposed that achieves an aggregate data rate of 195Gb/s among 4 stacked chips in a package with a power dissipation of 1.2W.

The substrate coupling in a 90nm CMOS technology is analyzed for frequencies above 1 GHz. The important result is that combined device-level and circuit-level analysis is required for substrate integrity beyond 1GHz.

In paper 14.7, a novel design for manufacturability method is presented to create manufacturable-by-construction designs. Silicon results show 3 to 12% improvement in the yield using this design method as compared to a traditional design flow.

An RF CMOS down-converter with integrated on-chip antennas communicating over free space up to 5m separation is demonstrated in Paper 14.8.

Finally an 8b asynchronous microprocessor fabricated using 32,000 low-temperature-processed poly-silicon thin-film transistors, transferred onto a plastic substrate is described in Paper 14.9. It draws 180μA from a 5V supply while operating at 500KHz. The power consumption is 30% of the synchronous counterpart according to the simulation.

ADCs, DC References, and Converters

Chair: *Klaas Bult, Broadcom Corporation*
Associate Chair: *Venu Gopinathan, Texas Instruments*

Power efficiency is a major concern for embedded ADCs in sub-micron CMOS technologies. The bulk of this session highlights the progress made in addressing this problem in a wide range of Nyquist-rate ADCs. The speed of the ADCs presented in this session ranges from 1MS/s to 200MS/s, while their resolution ranges from 16b to 8b. The set of ADC papers is followed by a paper on a precision voltage reference with a large programmable range and a low temperature coefficient. The session concludes with the presentation of a DC-DC converter having pseudo-continuous output regulation.

In Paper 15.1, a new ADC architecture enabling continuous digital background self-calibration, without injecting a training signal or interrupting the signal path, is described. For a 16b 1MS/s cyclic-ADC, this algorithm reduces the required number of conversion cycles for self-calibration by 3 to 5 orders of magnitude. This is achieved without any additional analog circuitry.

The low-voltage operation required in 90nm CMOS technology is addressed by Paper 15.2, using switched opamps and switched input buffers. Operating from a 1.2V supply, this ADC achieves a peak SNDR of 52.6dB, while consuming 3.3mW of power. This performance is obtained without the use of boosted voltages.

A pipelined ADC with a power consumption that adapts automatically to the sample-rate is described in Paper 15.3. The power dissipation scales with the sampling rate by over 3 orders of magnitude, while maintaining a constant SNDR of 54 to 56dB over the full range. This is achieved by rapidly powering on and off the opamps.

A judicious choice of the first-stage architecture of a pipelined ADC enables very good power efficiency, as presented in Paper 15.4. A 10b 125MS/s ADC is demonstrated in 0.18μm CMOS technology, consuming just 40mW of power.

In the final ADC paper of this session, Paper 15.5, a power-reduction technique is described. The reduction is achieved by shutting down the second-stage of a 2-stage opamp. The power efficiency is enhanced by a new rapid-recovery arrangement. This 8b 200MS/s ADC achieves state-of-the-art high-frequency performance consuming just 30mW.

A precision voltage reference based on a floating-gate technology is presented in Paper 15.6. The reference has a temperature coefficient of <1ppm/°C and an initial accuracy of 200μV. Unlike classical reference generators, this circuit can output any voltage from 0.5V to 5V without loss in precision.

This session is concluded by Paper 15.7, where a regulated switched-capacitor DC-DC converter is presented. A pseudo-continuous control enables continuous output regulation in all clock phases. This creates an attractive alternative to inductor-based DC-DC converters for low current applications, since this approach can be integrated on-chip.

Clock Distribution and Power Management

Chair: *Hoi-Jun Yoo, KAIST, Daejeon, Korea*
Associate Chair: *Sohichi Miyata, Sharp, Chiba, Japan*

Clock Distribution is an essential component of synchronous digital design. Papers in this session address techniques for the distribution of low-jitter high-quality clocks across large digital systems on a chip. The priority of power reduction in current processor designs is well-known. Power management, including methods to measure power and temperature on-chip.

Clock distribution in advanced SoCs is a major theme of the first three papers. Clock distribution and clock-frequency control of the 90nm Itanium® processor are discussed in Papers 16.1 and 16.2, respectively. A clocking scheme for on-chip interconnections is presented in Paper 16.3.

A region-based active-de-skewing clocking system to reduce PVT-related skew is described in Paper 16.1. It utilizes clock verniers to allow up to 10% clock-cycle adjustment, and supports a continuously-updating frequency with <10ps of skew across PVT changes. A clock-generator system generating fixed- and variable-frequency clocks for adaptive power control is reported in Paper 16.2. Its frequency synthesizers divide the fixed-frequency PLL clock in 1/64th cycle steps to track supply-voltage transients, resulting in a 10% improvement in CPU performance.

Periodically-all-in-phase clocking and a deterministic synchronous bus wrapper for synchronized data transfer among different frequency cores are introduced in Paper 16.3. It supports dynamic voltage and frequency scaling to obtain a maximum of 60% power reduction and 1.5 to 2X throughput increase in MPEG-4 decoding.

Advanced power-management schemes such as power switching, dynamic voltage-and-frequency control, and voltage-domain stacking are discussed in the final four papers. An interesting circuit scheme, enabling the stacked domains to operate at multiples of the supply voltage without a voltage down-converter, is proposed in Paper 16.4. Operation at 3.6V is demonstrated in the 0.18μm CMOS circuit with 93% energy efficiency.

In the chip presented in Paper 16.5, the dynamic range of voltage scaling is extended below 300mV by including sub-threshold operation in a 90nm CMOS chip. This ultra-dynamic voltage scaling leads to a 9-times energy saving over an ideal shutdown scheme. Fine-grained power-switch circuits to reduce standby power by a factor of 5500 with a 5% speed penalty, are presented in Paper 16.6. A double-switch scheme avoids power-on glitches and reduces current spikes by 38%.

An embedded feedback-control system on a 90nm Itanium® processor is described in Paper 16.7. It integrates a small microcontroller, firmware, ADC, and thermal sensors to measure power and temperature. In addition, it modulates voltage and frequency to meet the given constraints.

RF Cellular ICs

Chair: *David Su, Atheros Communications, Sunnyvale, California*
Associate Chair: *Charles Chien, SST Communications, Santa Monica, California*

At the current growth rate, the number of worldwide subscribers of cellular services is expected to exceed 1.5 billion by 2007. Today, cellular services for voice communications are primarily based on 2G systems, such as GSM and CDMA. However, with the rising demand for data services, the emerging 2.5G and 3G systems such as EDGE/GPRS and UMTS/CDMA2000, will play an increasingly important role in enabling multimedia services with feature-rich handsets. To support the enhanced functions in these handsets, RF cellular ICs must provide small-form-factor low-power solutions, while meeting stringent system-level compatibility requirements.

The nine presentations in this session represent a snapshot of the recent advances in cellular integrated circuits, ranging from highly-efficient power amplifiers to fully-integrated transceivers. It is shown in these papers that the continued scaling of silicon technologies can enable increased levels of integration and enhanced performance, while reducing overall system cost.

The first single-chip GPS receiver, that integrates both the baseband and RF functionalities in an advanced 90nm CMOS technology, is presented in the Paper 17.1. As discussed in this paper, GPS functionality can be integrated into a large digital system-on-a-chip solution.

RF buildings blocks for GSM are described in the next three papers. A very high-power GSM amplifier with 36dBm output and 54% PAE in a 0.23μm silicon LDMOS technology is presented in Paper 17.2. A 0.18μm polar-modulated CMOS GSM/EDGE power amplifier is featured in Paper 17.3. As an EDGE transmitter, this PA can deliver 23.8 dBm with 22% PAE. A unique loop bandwidth-calibration technique for a fractional-N synthesizer is showcased in Paper 17.4. The calibration technique achieves better than 2 degrees rms phase error.

The session continues with integrated transmitters and receivers. An all-digital GSM/EDGE transmitter in an advanced 90nm CMOS technology is demonstrated in Paper 17.5. This 1.2V 42mA polar transmitter consists of a digitally-controlled oscillator with digital amplitude modulation. It meets the EDGE spectral mask with an EVM of 3.5%. As in Paper 17.1, the viability of scaling RF circuits in 90 nm CMOS technology is also demonstrated in Paper 17.5.

The first-published fully-integrated GSM/GPRS transceiver in a 0.18μm CMOS technology is presented in Paper 17.6. The quad-band transceiver features a low-IF topology with no external SAW filter. A 5th-order continuous-time GmC filter with in-situ calibration, to achieve 2% tuning accuracy, is described in a companion paper (17.8).

Two direct-conversion receiver presentations round out this session. A 0.18μm CMOS direct-conversion UTMS down converter is presented in Paper 17.7. The down converter uses an LC filter to achieve a high IIP2 of 78dBm. A fully-integrated direct-conversion CDMA receiver in 0.25μm CMOS is described in Paper 17.9. This receiver has a linearized LNA that enables a high IIP2 of 75dBm.

High-Speed Interconnects and Building Blocks

Chair: *Vadim Gutnik, Impinj, Inc., Newport Beach, CA*
Associate Chair: *Michael Green, University of California, Irvine, CA*

The demand for speed and performance in broadband systems continues to increase. Circuit designers are rising to the task by designing high-speed high-performance ICs, even in standard CMOS or BiCMOS processes. Moreover, there is a strong motivation in the market to use the existing infrastructures (e.g., FR4-dielectric boards, multi-mode fiber, legacy connectors, etc.), even as bit rates continue to increase. Thus, more pressure mounts to overcome the non-idealities of the transmission channels. In this session, a number of papers address this challenge: equalization circuits are presented in two papers, one for copper, one for multi-mode fiber. Methods in which frequency modulation is employed to overcome speed limitations in the silicon are described in two other papers. Challenges associated with testing state-of-the-art transceivers, generating high-speed (PRBS), and measuring the data eye on-chip, are addressed in another three papers.

Equalization methods used in 10Gb/s receivers are presented in Papers 18.1 and 18.2. The authors of Paper 18.1 describe a 0.13μm CMOS implementation of an analog adaptive equalizer that can compensate for the loss in up to 30 inches of transmission line on an FR4 board, while dissipating only 25mW. A 0.12μm CMOS implementation of a 7-tap FIR equalizer compensates for the dispersion in up to 600m of a multi-mode optical fiber. This circuit dissipates 325mW.

The 0.13μm CMOS 10Gb/s eye-opening monitor in Paper 18.3 operates from 1Gb/s to 12.5Gb/s, consuming 330mW from a 1.2V supply. This circuit maps the input eye to a 2-dimensional bit-error diagram with 68dB mask-error dynamic range.

The authors of Paper 18.4 present an 80nm CMOS quad optical transceiver that transmits 10Gb/s per channel over multi-mode optical fiber. Each driver consumes 2mW from a 0.8V supply, and a VCSEL requires 7mA from a 2.4V supply. The receiver, excluding the output buffer, consumes 6mW from a 1.1V supply per channel, and features a transimpedance gain of 10.1k

In Papers 18.5 and 18.6, wireless-circuit architectures are borrowed that are based on modulation techniques for enhanced broadband performance. Paper 18.5 uses frequency interleaving to provide less sensitivity to clock jitter in an interleaved-sampling architecture. This circuit, realized in a 0.25μm CMOS process, occupies 4mm^2 and dissipates 1W. Paper 18.6 describes a technique in which the transmitted data signal is modulated to create two independent high-speed channels. This circuit, realized in a 0.18μm CMOS, achieves an aggregate data rate of up to 3.6Gb/s per pin, and dissipates 92mW.

A 40Gb/s 2^7-1 PRBS generator using a SiGe BiCMOS process, is described in Paper 18.7. This design makes use of a low-voltage logic family that allows 2.5V supply, and dissipates 550mW. Paper 18.8 presents a 72Gb/s 2^{31}-1 PRBS generator using a SiGe process with a 3.3V supply. This circuit dissipates 9.28W.

Imagers

Chair: *Abbas El Gamal, Stanford University, Stanford, California*
Associate Chair: *Hirofumi Sumi, SONY Corp., Japan*

This session highlights recent advancements in image sensors. Papers cover not only improvements in mainstream photographic and video applications, but also continue to demonstrate the extended range of applications that custom imagers can address.

Smaller pixels with good imaging characteristics are required for the mass markets of DSCs, camcorders, and camera phones. A CCD that contains the smallest pixel yet announced (1.56μm) and is optimized for mobile still-image and video operation is described in Paper 19.1. The smallest pixel size for CMOS imagers (2.0μm) and a new approach for color filters that uses amorphous silicon to create interference-stack filters is presented in Paper 19.2.

Three different high-dynamic-range techniques are presented in three papers from three different groups. A 19.5b dynamic sensor that combines high-speed readout and multiple exposure times is presented in Paper 19.3. A 100dB wide-dynamic-range sensor that uses one additional capacitor and one additional transistor per pixel to integrate the electrons that overflow during integration is described in Paper 19.4. In contrast, the sensor described in Paper 19.5 uses the leakage characteristics of the transfer gate during integration to create a signal that is linear up to a threshold, and then logarithmic.

A 3D fabricated 1024x1024 sensor is described in Paper 19.6. It is created by combining the readout array on one wafer of SOI, with a 100%-fill-factor photodiode array through the use of a 2μmx2μm 3D via per pixel. This approach disconnects the sensing technology from the readout technology, and is an interesting direction if it proves viable. A CMOS HDTV sensor, that uses a tapered reset technique to achieve low readout noise by design, is presented in Paper 19.7.

Three custom sensors have been developed for three different applications by three different groups, as described in the final three papers of the session. The sensor described in Paper 19.8 was developed to address automatic target tracking and ROI extraction. The sensor consists of both an active pixel array for imaging, and a distributed horizontal and vertical passive pixel array for locating the target. A temporal-change threshold detector is presented in Paper 19.9 for use in low-power low-bandwidth surveillance-network applications. An array of single-photon avalanche diodes (SPAD), combined with a micro-scanner package, create an imaging system with an enhanced resolution of 64x64, as described in Paper 19.10. It is used in a time-of-flight range finding application.

Processor Building Blocks

Chair: *Atila Alvandpour, Linköping University, Linköping, Sweden*
Associate Chair: *Fumio Arakawa, Hitachi, Tokyo, Japan*

CMOS technology shows every sign of sustaining the capability of providing functional and reliable transistors far below 70nm channel length. However, utilizing this capability for higher integration levels and larger chips requires solutions to a number of challenges, including increased power consumption, increased subthreshold and gate leakage currents, and increased interconnect RC delay. This session includes seven papers describing low-power high-performance circuit techniques for processor building blocks. Blocks that are discussed include multipliers, adders, and register-file storage arrays. Intra-chip communication is also a critical component in leveraging the speed and performance of these functional units. The final paper of the session proposes a differential-signaling scheme as an alternative to classic repeater-based wiring.

The first three papers present efficient multipliers, always a high priority in microprocessor design. The authors of Paper 20.1 describe an 8GHz floating-point multiplier utilizing a limited-switch dynamic logic with power consumption from 150mW to 1.8W for 2 to 8GHz operation. A 2's-complement multiplier fabricated in 90nm dual-V_t CMOS is presented in Paper 20.2. The multiplier delivers 110GOPS/W at 1.3V with single-cycle operation at 1GHz. The design utilizes PMOS sleep transistors enabling ultra-low stand-by power of 75μW. A double-precision multiplier for the 90nm SOI CELL processor presented in Session 10, is presented in Paper 20.3. The multiplier employs static partial-product compression utilizing replicated bits for 4.4GHz operation. In addition, an efficient clock-gating technique has been used to reduce the active power.

In Paper 20.4, a 32b parallel prefix adder in 90nm CMOS is described, demonstrating the leakage-current-reduction capabilities of skewed CMOS logic, where high-V_t and thick-gate-oxide devices have been utilized in performance-non-critical devices. The adder achieves sub-100nA device-leakage current and includes a single-cycle-activation-from-standby mode. In addition, the adder data path includes improved sense-amplifier-based flip-flops and adapted latches.

The authors of Paper 20.5 present a dual-thread 18-port 128w x 82b FPU register file and a 22-port 128w x 65b integer register file on a dual-core Itanium® processor, utilizing embedded parity to provide soft-error detection capability. In addition, the design integrates a charge-compensated thread switch and power-saving features, to operate at 1.1V and 400mW.

A method for copying memory cells to reduce the size of a 32b 64w 9-read- and 7-write-port pseudo dual-bank register file in 100nm CMOS is the focus of Paper 20.6. This has reduced the number of transistors in a memory cell by 70%, resulting in a register file, with 62% of the area of conventional register files.

Paper 20.7 describes circuit techniques for a bus-transceiver chip in 130nm CMOS using 10mm-long uninterrupted differential interconnects of 0.8μm pitch. The chip achieves 3Gb/s/ch using a pulse-width-pre-emphasis technique in combination with resistive termination with a power consumption of 6mW/ch from a 1.2V supply.

RF Trends: Above-IC Integration and mm-Wave

Chair: *Ernesto Perea, ST Microelectronics, Grenoble, France*
Associate Chair: *Christian Enz, CSEM, Neuchâtel, Switzerland*

This session highlights two important RF trends: the integration of various devices above the IC together with advanced CMOS and BiCMOS circuits, and the design of high-frequency (60GHz to 110GHz) wide-band communication circuits. On one hand, the design of wireless circuits including above-IC bulk-acoustic-wave (BAW) resonators and filters opens the door to highly-integrated transceiver architectures for multi-band and multi-standard applications. On the other hand, there is now confirmed interest in 60GHz circuits spurred in part by opening 7GHz of unlicensed bandwidth around 60GHz. This band was traditionally the domain of III-V compound semiconductors. However, aggressive scaling of CMOS technology, and the increasing capabilities of SiGe technology, make feasible the fabrication of highly-integrated CMOS or SiGe mm-wave circuits for data-communication applications.

The focus of the first four papers in this session is on the use of RF-MEMS for both increasing the integration level and reducing the power consumption of RF transceivers. An RF receiver architecture that integrates a combination of on-chip high-Q inductors and tunable MEMS varactors, together with an array of parallel cantilever-beam mixer-filters is described in Paper 21.1. All the MEMS devices are fabricated by micromachining in a standard RF foundry. Paper 21.2 demonstrates, for the first time, the feasibility of integrating BAW devices above a 0.25μm BiCMOS wafer, and connecting them to the RF circuits below. The new technology is illustrated by the design of an RF front-end lattice filter operating at 2.14GHz for WCDMA. A similar above-IC filter appears in Paper 21.3 for the integration of a complete RF front-end used in a zero-IF receiver for WCDMA. The front-end is integrated in a 0.25μm BiCMOS SiGe:C technology. It achieves a gain of 31.3dB, a 5.3dB noise figure, and consumes a total of 36mW. The authors of Paper 21.4 take advantage of the high-Q of FBAR BAWs to implement a very-low-power super-regenerative transceiver for wireless-sensor-network applications. The receiver operates at 2GHz and consumes only 450μW from a 1V supply, while achieving a −100.5dB sensitivity at 5kb/s for a 10^{-3} BER. The circuit is implemented in a 130μm CMOS technology and uses off-chip FBARs.

The second part of this session begins with Paper 21.5, in which a thin-film Cu/BCB technology with integrated inductors, resistors, and capacitors, for the realization of high quality on-chip and in-package Si-based passives, is presented. Thin-film SiP and SoC inductor and transmission-line performances are compared. A 60GHz direct-conversion receiver is presented in Paper 21.6 that features folded microstrip lines realized in 0.13μm CMOS, and consumes 9mW from a 1.2V supply. The receiver provides a voltage gain of 28dB with a noise figure of 12.5dB. The cascaded multi-stage distributed amplifier presented in Paper 21.7 is integrated in a 90nm CMOS technology, and achieves better than 7dB gain with a bandwidth of 70GHz, 10dBm output at the 1dB input compression points and 6.4dB average NF from 1 to 25GHz. The first D-band (110 to 170GHz) CMOS push-push VCO implemented in a standard bulk 0.13μm CMOS process is presented in Paper 21.8. It features a phase noise of −107.6dBc/Hz at 10MHz offset, and power consumption of only 8.4mW. The first integrated BiCMOS phase-locked loop for 60GHz applications, featuring a measured PLL lock range of 53.3GHz to 55.7GHz, is described in Paper 21.9.

PLLs , DLLs and VCOs

Chair: *Roger Minear, Agere Systems, Allentown, PA*
Associate Chair: *Thomas Burger, Swiss Federal Institute of Technology, Zurich, Switzerland*

The steadily increasing speed of chip-to-chip communication requires higher-performance PLLs, DLLs, and VCOs for high-frequency clock generation and clock recovery in multi-Gb/s transmitters and receivers.

Several key specifications must be considered in PLL design. First, PLLs must produce low phase noise, in order to have superior jitter performance in receivers and transmitters. Second, the PLL must also consume minimal power and area; clock generation and clock distribution are major contributors to overall power consumption.

Multi-phase PLLs for clock generation and clock distribution for multi-channel serial links are presented in Papers 22.1 and 22.3. The use of multi-phase PLLs in multi-channel serial links leads to very low power consumption and small area. Paper 22.1 includes a novel phase detector resulting in low phase jitter of <1ps and a power consumption of only 20mW.

The PLL in Paper 22.2 uses a new charge-pump architecture to reduce the intrinsic deterministic jitter, leading to 1.3ps rms jitter. The PLL occupies only 0.064mm^2, while consuming only 15mW.

A self-biased PLL with current-mode filter for wide-frequency-range clock generation is presented in Paper 22.6. This PLL makes the bandwidth and jitter performance independent of the multiplication factor, temperature, and process variation. This is desirable for many applications, especially for multirate transceivers.

For very-low-jitter, PLLs with narrow bandwith, fully-integrated LC-VCOs are usually needed. A 44GHz differentially-tuned VCO in 0.12μm SOI CMOS technology is described in Paper 22.4. This VCO achieves a phase noise of −101.8dBc/Hz at 1MHz offset and consumes 7.5mW from a 1.5V supply.

Applications such as GSM and WCDMA require frequency synthesis with an absolute accuracy better than 0.1ppm. DCXOs are very often used for this purpose. A DCXO that preserves the phase noise and stability of the crystal while permitting digitally-controlled tuning is described in Paper 22.5. Monotonicity of tuning and a step size of ~0.004ppm are achieved by a $\Delta\Sigma$-modulation scheme.

DLLs have become an important component for clock synthesis. ADDLLs usually provide low power but suffer from large jitter. An all-digital DLL for clock deskewing in digital ICs is demonstrated in Paper 22.7. It reduces power by nearly two orders of magnitude as compared with fast-lock mixed-mode DLLs, while also improving jitter by 36%.

Wireless Receivers For Consumer Applications

Chair: *John Long, Delft University of Technology, The Netherlands*
Associate Chair: *Tony Montalvo, Analog Devices, Raleigh, NC*

Silicon IC implementations of emerging digital TV and radio standards are promising smaller lower-cost TV- and radio-tuner chips enabling mobility and feature-rich consumer electronics. In the TV world, smaller and lower-power tuners offer attractions like picture-in-picture and mobility, while substantially driving down costs. Digital terrestrial radios boost audio quality to CD levels and extend new features to the listener, while satellite radio promises truly nationwide coverage.

Advancements in TV tuners are highlighted in the first four papers in this session. TV tuners are well-known for their extremely challenging technical requirements for RF designers. The tuning range encompasses hundreds of channels, leading to dynamic-range, local-oscillator-phase-noise, and spurious-signal-rejection requirements that are perhaps unmatched in our industry. The desire to add a tuner to hand-held portable devices, such as laptop computers and wireless PDAs, adds power consumption to the list of critical design requirements.

The session begins with a tuner designed for the digital-video-broadcasting-handheld (DVB-H) standard. The IC tunes to channels between 470 and 862 MHz, while consuming just 240mW, and does not require external filters. A tuner for a mobile standard called Universal-Mobile TV (UMTV), which is intended for deployment in PDAs, PCs, and mobile phones, is presented in the second paper (23.2). This chip features a low-noise amplifier (LNA) that includes an automatically-tuned integrated tracking filter to reduce the dynamic range required in subsequent circuits, and a low-IF topology to eliminate external passive filtering.

The digital-video-broadcasting-terrestrial (DVB-T) standard has especially stringent phase-noise requirements. A tuner for DVB-T implemented in CMOS, using a superheterodyne architecture to avoid the tracking filters used in traditional tuners, is described in the third paper of our session (23.3). The chip includes 14b ADCs and digital channel filtering to eliminate the IF SAW filter often seen in superheterodyne radio receivers.

A tuner designed for both U.S. and European set-top boxes that employs a dual-conversion topology is presented in Paper 23.4. It uses a low-IF in order to satisfy difficult image-rejection requirements by filtering in the digital domain.

Tuners for digital broadcast radio – one satellite and one terrestrial – are presented in the next two papers. An IC designed to satisfy Eureka-147, which is a European digital-audio-broadcasting (DAB) standard, that includes backward-compatibility with standard FM broadcast radio is the subject of Paper 23.5. The IC consumes only 150mW and uses a low-IF architecture to eliminate external passive filtering.

In Paper 23.6, a radio tuner for XM, which is the North American satellite radio standard, is described. The 2.3GHz received signal is converted to a low-IF using the superheterodyne topology. The low-IF allows on-chip filters to be used which eliminate bulky external filters required by earlier receivers designed for this application.

In the final paper of the session, a receiver front-end for digital-video-broadcast-satellite (DVB-S) applications is discussed. This chip uses a low-noise PLL to generate a 10.2GHz local oscillator that converts two 12GHz satellite channels to an intermediate frequency. The level of integration realized with this IC is the highest published to date for this application.

Baseband Processing

Chair: *Albert Van der Werf, Phillips Research, Eindhoven, Netherlands*
Associate Chair: *Yiwan Wong, ASTRI, Hong Kong, China*

This Baseband Processing session covers ICs for a variety of digital communication systems ranging from personal-area networks to satellite communication. The reported advances in signal-processing technology are in the area of error correction, increased application benefits of WLANs (802.11a/b/g), and ultra-wide-band communication. In addition, advances in integration offering high signal-processing performance, low standby power for cellular applications, and configurability for multiple standards, are also reported. Advanced channel-coding techniques utilizing low-density parity check (LDPC) codes are also reported, and applied to both UWB and DVB-S2 applications.

A transceiver IC for impulse-radio UWB providing 62.5Mb/s is discussed in Paper 24.1. The IC consumes 6.7mW and has a 2.72mm^2 die area in a 0.18μm CMOS technology. An LDPC-COFDM-based transceiver IC for UWB is presented in Paper 24.2. The IC is capable of 480Mb/s consuming 523mW/575mW (TX/RX) and has a die size of 42.3mm^2 in 0.18μm CMOS.

In Paper 24.3, a DVB-S2-compliant CODEC is presented including an LDPC CODEC. Two ICs are presented: one in 130nm and one in 90nm CMOS where the CODEC is integrated with ADC and demodulator. In 130nm, the CODEC area is 49.6mm^2 and consumes 1.5W at 90Mb/s; in 90nm CMOS, the CODEC area is 15.8mm^2 and consumes 700mW at 135Mb/s.

A reprogrammable EDGE-baseband and multimedia-handset IC integrating 6Mbit of embedded DRAM and programmable processors running at 156MHz is reported in Paper 24.4. The DRAM provides flexible instruction storage allowing dynamic on-the-fly downloading of new multi-media applications. The IC measures 57mm^2 in 0.13μm CMOS, and draws 336mA for GPRS communication with multi media, and draws 690μA in standby mode.

A multi-standard DSL central-office modem IC is presented in Paper 24.5. It supports 16 ADSL2+ modems, each running at 16Mb/s and configurable for multiple standards. The IC measures 145mm^2 in 0.13μm CMOS, and consumes 2.7W from a 1.2V supply at 25°C.

A WLAN IC for video applications that supports PHY rates up to 108Mb/s and can handle 802.11a/b/g is discussed in Paper 24.6. The IC measures 51.9mm^2 in 180nm CMOS, and consumes a maximum of 1.8W. In Paper 24.7 a wideband three-channel baseband and MAC processor for 802.11a/b/g is presented. The IC occupies 70.6mm^2 in 0.18μm CMOS, and consumes 2.1W when receiving three 54Mb/s channels simultaneously .

Dynamic Memory

Chair: *Hideto Hidaka, Renesas Technology, Itami, Japan*
Associate Chair: *John Barth, IBM, Burlington, VT*

Dynamic memory technologies have recently made tremendous progress in high-bandwidth applications and continue to represent the cutting-edge of memory technology intended for high-speed and high-density uses. We continue to see exploration of non-conventional memories such as SOI and dual-ported DRAMs, and high-frequency and low-power embedded memory designs. Sophisticated statistical analysis of correlated process parameters enables more accurate modeling of worst-case boundaries of device variation.

Recently-explored scalable capacitor-less DRAM on SOI is examined in Paper 25.1. A new 128Mb design highlights a new mode of cell operation employing charge-replenishing to enhance retention characteristics. A proposed high-capacity array architecture also provides a virtually-static RAM mode, reducing contention by allowing refresh interrupts.

Over 300MHz random access performance is a norm in today's embedded-DRAM arena. The authors of Paper 25.2 show that precise tuning of circuits drastically improves the sensing margins and enables 322MHz random-cycle operation. An effective dual-port approach to realizing a 400MHz random-cycle time is presented in Paper 25.3, which utilizes a shallow-trench-capacitor cell. Array noise is reduced by minimizing data-line swing.

Evolution of CAM is another promising aspect of expanding embedded-memory applications. A new AND-type CAM structure is described in Paper 25.4. It provides a power-efficient approach yielding a competitive performance advantage over conventional NOR- and NAND-type CAM configurations.

High-density 1T1C DRAM requires consideration of statistical design when dealing with multiple-billions of transistors. This topic is addressed this year by Papers 25.5 and 25.6.

A new concordant design methodology and associated tool for statistically incorporating device fluctuations into the SNR analysis in DRAM arrays is proposed in Paper 25.5 to precisely predict the minimum operating voltage. 1.4V operation in a 100nm gigabit-DRAM is demonstrated. This statistical approach is not limited to memory design, but is also well-suited to standard logic design.

A 2Gb DDR2 SDRAM, using 80nm technology, is described in Paper 25.6. Effective use of triple-level metal and statistical circuit analysis realizes a manufacturable die to cover many practical applications.

A 20GB/s interface using a precise quadrature PLL, controlled by a newly-devised tetrahedral oscillator, is presented in Paper 25.7. A 256Mb DRAM chip, implemented in an 80nm technology, incorporates a cascaded pre-emphasis transmitter to enhance the signal integrity in the multi-GHz regime.

SRAM Memory

Chair: *Alexander Shubat, Virage Logic, Fremont, CA*
Associate Chair: *Jinyong Chung, POSTECH, Pohang, Korea*

Static Random Access Memories (SRAMs) have become increasingly important to a broad spectrum of VLSI designs and applications, ranging from high-performance CPUs to low-power mobile handheld devices. While technology scaling drives the density and performance of SRAMs, it also poses design challenges in many technical areas. In this session, there is an array of papers that address some of the fundamental issues in SRAM design and considers optimization schemes to meet various product needs. It covers power and performance management, ultra-high-density SRAM design, low-voltage operation, reductions in leakage current, and improvements in cell stability.

A 65nm CMOS 3GHz 70Mb SRAM is described in Paper 26.1. To achieve balanced power and performance, it introduces a dynamic-power switching scheme that allows the SRAM to integrate two different power supplies, based on the operating mode of the memory, whether read, write, or standby. In the column direction the power-supply scheme uses various voltage levels to improve the cell read and write margins independently, leading to a higher manufacturing yield.

A 256Mb synchronous-burst DDR SRAM design-based on a 0.16μm^2 SRAM cell, using a stacked single-crystal silicon thin-film transistor, is introduced in Paper 26.2. The design adopts a hierarchical bitline architecture to achieve optimal array efficiency with a robust sensing margin. A 280Mb/s data rate is achieved with operating current of 17mA in a 61.1mm^2 chip in an 80nm process technology.

Low-voltage operation of SRAMs is limited by static-noise-margin (SNM) degradation and loss of performance due to higher-threshold transistors. These issues are addressed in Paper 26.3 by resorting to a 7-transistor cell, thus allowing low-voltage operation at the expense of a 10% increase in area.

In addition to SNM in the read mode, the write margin is now limiting scaling. This topic is discussed in Paper 26.4, which uses write-margin expansion to achieve low-voltage operation. This expansion is achieved by V_{DD} manipulation, and a special replica-tracking scheme. Operation at 450MHz is achieved with 7.8μA of leakage standby current.

Leakage control is becoming of paramount importance in SRAM designs. In fact, leakage is perhaps deemed to be the primary threat to SRAM scaling. A solution that offers 94% reduction in leakage, with only 2% performance degradation, is described in Paper 26.5. The technique involves bit-cell ground control to reduce unwanted standby current.

Another important consideration in SRAM scaling is device-parameter fluctuation. This is specifically significant when operating the device at very-low voltages, for example at 0.3V as described in Paper 26.6. Furthermore, at such low voltages, the soft-error rate needs to be significantly improved. The solution presented uses a hidden ECC scheme that does not affect the access time.

SRAM caches continue to play a key role in supporting the improvements in microprocessor performance. Cache performance of 4.8GHz utilizing a 6-cycle pipeline and a 90nm SOI technology is described in Paper 26.7. The largest on-chip SRAM-based cache memory reported to date is presented in Paper 26.8. The 24MB level-3 cache memory operates from a 2GHz from a 0.8V supply while consuming 4.2W.

Filters and Continuous-Time ΔΣ Converters

Chair: *Raf Roovers, Philips, Eindhoven, The Netherlands*
Associate Chair: *Bill Redman-White, Southampton, United Kingdom*

Achieving the optimum trade-off between the complexity of filtering to restrict analog bandwidth and the dynamic range in the data-conversion function with the lowest power, remains a central issue in many mobile and communication applications. Traditionally, filtering has been used in conjunction with gain control to limit the resolution bandwidth of the ADC, and hence the power consumption, but the partitioning is constantly changing as ADC technology advances.

In this session, we see how these issues are addressed using CT techniques while still pushing forward the state-of-the-art in low-voltage fine-geometry processes. CT noise-shaping can yield valuable savings in power in a ΔΣ ADC, and can also provide useful attenuation of interferes before the first sampling function. We also see, here, new techniques to reduce the power and voltage demands for providing classical filter functions for communication systems.

A multibit quantizer inside a ΔΣ ADC improves dynamic range, but the power needed for the internal quantizer grows rapidly with the number of bits. A 2MHz BW 3rd-order converter in 0.13μm CMOS for cellular receivers is described in Paper 27.1. Using an internal-tracking 4b ADC with only 3 comparators, the overhead is reduced significantly. The 78dB dynamic-range requirement in a digital-TV receiver is addressed in Paper 27.2, by incorporating some gain control within the converter itself by means of a variable SC feedback DAC. The 1.3MHz 1.2V 0.11μm single-bit design with internal mixer also gains some benefits in jitter immunity from this approach.

The next two papers are CT ΔΣ designs in 90nm CMOS. Showing another approach to power saving, a 4th-order noise-shaper employing passive poles and only 2 op-amps, is presented in Paper 27.3. Operating at 267MHz, the design consumes 5.4mW from a 1.2V supply. In Paper 27.4, the issue of excess loop delay in CT modulators is tackled by adding a digital-compensation branch at the output. Pseudo-differential OTA structures are optimized to give an input-referred noise of only 9nV/√Hz for cellular-baseband applications.

Complex ΔΣ architectures are gaining popularity for I/Q receiver processing. Optimization of the signal-transfer function against the needs of out-of-band signal rejection is the subject of Paper 27.5. The modified feedback modulator with variable gain has almost 90dB dynamic range for only 4.7mW. In Paper 27.6, the prime goal is to attain a single-sided bandwidth of 23MHz. The DR of 72.5dB and 45dB image rejection for only 42.5mW, permit direct digitization in a low-IF WLAN receiver with minimal additional analog functions.

The concluding papers of the session show that low-power filter techniques also continue to advance. A new technique that trades power and noise floor dynamically in a high-linearity GSM baseband filter path is introduced in Paper 27.7. Unlike traditional filter/AGC schemes, DR is enhanced by adding parallel paths so that impedance levels and kT/C noise are traded with power consumption. The 0.45 to 2.6mW 5th-order filters occupy 1.2mm^2 per path in 0.18μm CMOS. Finally, in Paper 27.8, it is shown that useful self-tuning filters can be realized at extremely low voltages without resorting to special device thresholds. Employing a new transconductor design with body bias tuning, the 135kHz filter achieves a DR of 57dB with only 0.5V supply.

Clocking and I/O

Chair: *Dennis Fischette, AMD, Sunnyvale, CA*
Associate Chair: *Hannu Tenhunen, KTH Royal Institute of Technology, Stockholm, Sweden*

Low jitter and low power are competing demands on the clock networks of systems running at GHz speeds. In addition, testability concerns require that low jitter be verified accurately, quickly, and at low cost. The papers in the first half of this session address high-speed clock generation, distribution, and testing. The second half of the session looks at three multi-Gb/s/pin I/O interfaces, and an innovative approach to interfacing today's deep-submicron chips with high-voltage legacy systems.

A multi-phase sampling system employing an analog DLL and two-level phase interpolation is presented in Paper 28.1. Redundancy and digital error correction reduce the effects of manufacturing mismatches by 6x, allowing sampling edges to be placed with 10ps accuracy. An analog on-chip jitter-measurement circuit that eliminates the need for a reference clock is described in Paper 28.2. It improves the measurement range and sensitivity using a combination of programmable delay elements and current sources, and reduces circuit activity with an interleaving architecture.

In Paper 28.3, on-chip global clock-network wires are replaced by lossless package interconnects to distribute a clock across a chip. The chip-package hybrid approach combines an on-chip DLL with package-level routing to reduce peak-to-peak clock jitter by more than 50%. In Paper 28.5, a differential global clock-network, based on distributed on-chip LC-tank oscillators, reduces jitter by an order of magnitude, while using three times less power at speeds ranging from 1.1 to 1.6GHz.

Pressing low-power concerns demand instantaneous clock frequency changes, a difficult feat for a PLL-based clock generator. A DLL-based clock generator for dynamic frequency scaling is described in Paper 28.4. This 120MHz-to-1.8GHz clock generator in 0.35μm CMOS can change its output frequency in one clock cycle with only 13ps peak-to-peak jitter at 1.3GHz.

In the second half of the session, high-performance I/O issues are presented. A 3Gb/s/pin performance for a 4-drop DRAM interface is demonstrated in Paper 28.6. Receiver equalization and digital offset-cancellation are employed, while a DLL loop with phase interpolation allows for data de-skew. In Paper 28.7, a pulsed AC-coupled receiver capable of 3Gb/s performance across a 15cm FR4 circuit-board interconnect with only 15mW/pin and a 60mV input swing is presented. The receiver incorporates clock recovery from the data stream using a semi-digital DLL with phase interpolation. A parallel 6.4Gb/s/pin I/O interface with an aggregate bandwidth of more than 0.5Tb/s is described in Paper 28.9. The parallel I/O is incorporated into a first-generation CELL processor and must combat the twin challenges of floating-body effects in a 90nm SOI CMOS technology, and reference-clock tracking.

In many applications, low-voltage circuits need to be interfaced to higher-voltage legacy circuits. The I/O buffer design in Paper 28.8 tolerates 3x V_{DD} input levels without gate-oxide reliability problems, using only 1x V_{DD} transistors and a single V_{DD} supply. A dynamic gate bias circuit auto-detects the received input-voltage levels.

RF Techniques

Chair: *Mario Paparo, STMicrolectronics, Catania, Italy*
Associate Chair: *Qiuting Huang, ETH Zurich, Switzerland*

New applications for silicon-based IC technologies are in the process of being defined in frequency bands well above 10GHz, including short-range automotive radar in the 24GHz ISM band, local-multipoint distribution systems (LMDS) at 28 to 30GHz (IEEE 802.16) for broadband WLAN, and multiple bands between 10 and 66GHz. In the first paper in this session (29.1), on-chip transformers are used extensively in the implementation of a 3-stage 21 to 26GHz power amplifier, implemented in 0.18μm SiGe BiCMOS. A maximum power-added efficiency (PAE) of 19% and output power of +23dBm are achieved – a very competitive result for circuits operating at these frequencies. Quadrature VCOs, used extensively in monolithic silicon transceivers, are described in Paper 29.5. The design presented extends the frequency range of such circuits beyond 30GHz, with very low quadrature phase error.

The trend towards wideband wireless transceiver circuits, for applications such as 3G cellphones and UWB systems, is supported by the circuit developments presented in Papers 29.2 and 29.4. In Paper 29.2 a new architecture for D/A conversion is applied to a high-performance direct-digital I/Q transmitter chip implemented in 0.13μm CMOS. It realizes better than −43dBc LO leakage and −47dBc image rejection. Quadrature signal generation over a wide range of frequencies is of critical importance to the successful development of UWB transceivers. In Paper 29.4, a quadrature VCO embedded in a feedback loop with a single-sideband mixer and two frequency dividers is used to implement a quadrature LO source that is continuously tunable over the 0.75 to 2.2GHz range. The ±20% tuning range of the VCO is extended to ±50% with only a 0.01mm^2 increase in die area.

Continuing evolution in the wireless-equipment domain requires extended battery life, reduced weight, and lower cost. This has stimulated the development of low-power RF building blocks in silicon. In Paper 29.6, an LC-VCO in 0.18μm CMOS is described, that operates at 2GHz with −103dBc/Hz phase noise at 100kHz offset and just 1mW power dissipation from a 1.25V supply. A low-power LNA and a quadrature VCO suitable for the 4 to 6 GHz WLAN band in 0.18μm CMOS are proposed in Paper 29.3. The LNA uses a gm-boosting technique to reach a remarkable 7.6dBm IIP3 and 2.5dB NF, while drawing just 1.9mA from a 1.8V supply. The Q VCO utilizes a modified Colpitts-oscillator architecture, and exhibits a 20% tuning range with a phase noise of −127dBc/Hz at 1MHz offset, while consuming 8.6mW.

A state-of-the-art fully-integrated low-power direct-conversion receiver for the 2.4GHz ISM band in 0.25μm CMOS is described in Paper 29.10. The receiver is intended for low-bit-rate communication and includes a complete frequency synthesizer. It draws a total of 9.5mA from a 1.8V supply, and occupies less that 1mm^2 of silicon area.

The opportunity to integrate calibration circuitry together with a wireless transceiver is open to designers using silicon IC technology. Two excellent examples of auto-calibration schemes are presented in this session. As described in Paper 29.7 over 50dB of image rejection is achieved when I and Q mismatch is adaptively minimized in a 90nm CMOS receiver chip targeted for GSM applications. A gear-shifting algorithm is employed for fast acquisition of the adaptive filter coefficients. As demonstrated in Paper 29.9, when applied to a WLAN direct up-conversion transmitter, automatic calibration can realize over 40dB of sideband suppression without the need for external circuitry or a high-precision receiver.

It is well-known that flicker noise constrains the performance of CMOS transceiver circuits. Presented in Paper 29.8, is a mixer which employs a new method of reducing the effect of 1/f noise. Reduction by an order of magnitude, with no penalty in power consumption, chip area, gain or, linearity is described. A prototype Gilbert-type mixer implemented in a 0.13μm CMOS is presented as a proof of the concept.

Displays and Biosensors

Chair: *Tiemin Zhao, Reflectivity, Sunnyvale, CA*
Associate Chair: *Roland Thewes, Infineon Technologies, Munich, Germany*

This session is the combination of two parts. The first part focuses on display technology and highlights a microdisplay for portable electronics, and driver technologies for LCD TVs. The second part focuses on biosensing, and highlights advanced approaches for neural-signal monitoring, and bio-molecule detection.

In Paper 30.1, the authors report a 360x200 CMOS-based microdisplay. It provides silicon light emitters for use in conjunction with image intensifiers to meet the low-power requirement for portable electronics.

The authors of Paper 30.2 report the first panel-sized TFT-LCD scan driver with 768 outputs, which is useful for low-cost TFT-LCD modules for large-panel LCD TV applications.

An LCD column driver using a switched capacitor DAC is described in Paper 30.3. Each DAC performs its conversion in less than 15μs and draws less than 2.5μA. This architecture allows 10b independent color control in a 17mm^2 die, for the LCD television market.

The remaining papers deal with CMOS-based biosensor applications. In Paper 30.4, a three-dimensional microsystem for monitoring neural activity on the basis of 256 sensor sites is described. Whereas data transmission in such systems represents a severe bottleneck if full analog-signal information is transferred, here an event-detection-based method decreases the volume of data by 92%.

Paper 30.5, a battery-driven low-power radio chip is described for a similar application area namely, FM-based wireless data transmission of neural signals. It requires only three off-chip components for operation.

In the final two papers, chips for detecting bio-molecules are described. In Paper 30.6 a chip is described that includes various sensors that operates in a sample solution with a wireless interface. Experimental detection of a DNA single nucleotide polymorphism is demonstrated.

Finally, in Paper 30.7, a 10x5 sensor array, fabricated in a 0.18μm CMOS technology, provides sensor sites using a variety of different detection principles. It demonstrates the versatility of an integrated sensors as enabling building blocks in important bioelectronics applications.

Mass Storage

Chair: *David Parlour, Xilinx, Pittsburgh, PA*
Associate Chair: *Ram Krishnamurthy, STMicroelectronics, Cornaredo, Italy*

Advances in materials and solid-state electronics have led to evolving standards for removable optical storage media which provide the consumer with cheap reliable read/write mass storage. The existing CD and DVD formats provide 650MB and 4.7GB capacity, respectively, while the emerging Blu-ray format offers 25GB single-layer capacity with a minimum 36Mb/s transfer rate. This session presents a variety of solutions to the challenges of supporting many formats spanning a wide range of data-transfer rates, and disk capacities, in a low-cost consumer setting.

In Paper 31.1, a DVD write channel IC, extracts additional performance from an existing format with a voltage-folding technique. Applied to the VCO loop filter, this reduces gain while expanding tuning range, thus enabling support for 1x to 16x write speed. A DLL-based clock-recovery technique is described in Paper 31.2. It has improved noise-rejection and jitter-accumulation characteristics as compared to those of implementations using PLLs. The technique is demonstrated to operate over both Blu-ray and DVD PRML read channels. A single device that can read and write multiple formats (CD, DVD, and Blu-Ray) is presented in Paper 31.3. This IC provides backward compatibility to today's popular standards, while extending Blu-ray performance to 7x read and write, compared to the 2x speed reported at ISSCC 2004.

Advanced Array Structures

Chair: *Eugenio Cantatore, Philips Research, Eindhoven, The Netherlands*
Associate chair: *Koji Kotani, Tohoku University, Sendai, Japan*

Large circuits, like stand-alone or embedded memories and addressing matrices for LED displays, that are built as an array of devices, have a paramount importance in the electronics market.

Memory arrays have to face a number of technology and circuit challenges in order to keep pace with CMOS transistor scaling. These challenges are addressed in the first part of this session.

A detailed overview of the issues related to the scaling of conventional memories (DRAM, SRAM and Flash) and emerging memories (FeRAM, MRAM, and PRAM) towards nanometer scale size is presented in Paper 32.1.

A 3T DRAM cell that combines very-low leakage with embedded gain is presented in Paper 32.2. This cell can be potentially scaled down to nanometer dimensions, allowing low-power operation and a retention time longer than 100ms, by using only 10 electrons per cell.

In the second part of the session, new large-area circuit concepts, based on organic- transistor technology, are presented. Organic transistors can be processed at low temperature on flexible and transparent substrates that can be integrated with displays or sensors to enable new applications.

A complete flexible display, based on an organic-transistor active matrix is presented in Paper 32.3. This display embodies the concept of electronic paper and is addressed by integrated row drivers to reduce the number of interconnects and the display footprint.A functional prototype is presented.

A sheet-type scanner based on the integration of an organic photodiode array with an organic TFT-based readout circuit is described in Paper 32.4. The integration is achieved by stacking three flexible layers: one foil with the image-sensor array with two foils containing the organic TFTs for the readout circuitry. A double word-line double-bit-line readout architecture allows a 5-fold improvement in speed and a 7-fold reduction in power over claims reported earlier.

NOTES

ISSCC 2005

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This and other related topics will be discussed at length at ISSCC 2005, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 6-10, 2005, at the San Francisco Marriott Hotel.

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Flash-Memory Capacity Grows and Grows

As will be reported at ISSCC 2005, both Toshiba and Samsung have developed 8Gb Flash Memories using advanced process technologies and. multi-level design techniques. Multi-level storage allows for one physical memory cell to store two bits of data, effectively cutting the cell area in half. Both 8Gb devices utilize a NAND Flash structure, which is a Flash-Memory technology well-suited to mass-storage applications, such as digital still cameras and MP3 players. NAND Flash memory, using state-of-the-art process lithography utilizing multi-level techniques, offers a low bit cost for these applications.

As will be reported in February, new process technology and new circuit-design techniques have been used to improve programming time beyond that of commercially-available multi-level NAND Flash memories. The Samsung and Toshiba memories are fabricated in sub-100nm technology, 63nm and 70nm, respectively. Both designs utilize triple-metal triple-well CMOS. More details of these developments will be revealed at ISSCC 2005, at the San Francisco Marriot, in February.

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A Breakthrough in Flash Memory Performance

At ISSCC 2005, in February, Intel will unveil 512Mb Flash Memory in a 90nm technology. It is targeted for communications and multimedia applications that demand both fast code execution and fast non-volatile data storage. To address these application needs, Intel engineers utilize a NOR Flash memory technology, along with multi-level techniques, to realize high-performance read and write throughput with a low bit cost. The memory is capable of 166MHz continuous-burst mode for fast code execution. Breakthrough circuit-design techniques, along with a technology that offers low-voltage high-performance transistors, were combined to achieve this read performance. As well, significant improvement in write performance makes this Flash Memory well-suited for fast non-volatile data storage. An 8Kb write buffer is included in the design, along with Flash cells optimized for low current and fast programming. Concurrent 166MHz read operation and 1.5MB/s programming operation is offered for memory subsystems that require simultaneous read and write operations. Details of these developments will be revealed at ISSCC 2005, at the San Francisco Marriot, in February.

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"NEW LIFE FOR OLD LINKS"

With continuing advances in silicon technology, increasing clock rates of processing cores drive the need to push electrical interconnect speeds to higher data rates. As industry-standard data rates pass 3Gb/s, signal degradation from channel effects such as bandwidth loss, reflections, and crosstalk, can distort the signal to such an extent that robust data recovery requires complex backplane transceiver designs. For example, legacy 1Gb/s backplane channels rely on power-efficient adaptive equalization techniques similar to those used in more-conventional image-scale wireline communication channels. In addition to binary pulse-amplitude modulation (PAM2), new signaling schemes with better spectral efficiency, such as PAM4 (for four-level signaling) and duobinary (or three-level signaling), are of interest for data rates exceeding 10Gb/s.

As highlighted by several presentations to be made at ISSCC 2005, these requirements are currently being addressed by transceiver designs using PAM2 signaling in 0.13μm CMOS, targeting data rates up to 10Gb/s. For higher data rates, duobinary and PAM4 solutions are implemented in 90nm CMOS and SOI technologies.

These approaches to enabling data rates up to 25Gb/s, will be described in the session on backplane transceivers at ISSCC 2005. All of these developments indicate that old-style electrical interconnects may have a much longer lifetime than expected. A rare piece of good news! But typical of much to be learned at ISSCC!

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NEUROELECTRONICS: THE NEXT FRONTIER

If you are a Star Trek fan, you may be familiar with Data, the android Lieutenant Commander, known to be first activated into operation on February 2, 2338. Surprisingly, research by Peter Fromherz of the Max Planck Institute in Germany, may lead humans to realize such capabilities before 2338! At ISSCC 2005, his presentation on neuroelectronics will describe how information exchange can be accomplished between electronics on a silicon chip and contacting neurons.

Information is transmitted in electronic systems by electrons, and in neurons by ions. Being able to achieve information exchange between these two different charge carriers is a significant challenge. The presentation (4.1) will explain a true breakthrough, a neuron-cell-to-semiconductor connection that enables neuroelectronic communication, an exchange that is noninvasive for the cells and noncorrosive for the chips, using purely-capacitive effects across the interface. Such microscopic interfacing is demonstrated between a silicon chip and snail neurons, with the diameter of the interface junction estimated to be between 10 and 100 microns.

Fromherz himself retains a relatively conservative view of the potential reach of his research: According to him, this work will enable complete spatiotemporal mapping of brain dynamics, facilitate learning networks on a chip, and allow systematic studies of memory formation. However, based on his already-startling breakthrough, he will provide a comprehensive discussion of the problems of neuroelectronic interfacing for future designs of such mixed-domain circuits. This and other bioelectronic topics will be presented at ISSCC 2005, at the San Francisco Marriott. in February.

This and other related topics will be discussed at length at ISSCC 2005, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 6-10, 2005, at the San Francisco Marriott Hotel.

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CHIP-SCALE ATOMIC CLOCKS

At ISSCC 2005, miniature atomic clocks will be reported (4.5). Such devices are needed for the accurate timing of electronic communication systems, such as the Global-Positioning System (GPS). In such applications, accurate timing is needed to precisely calculate distance and establish location. Currently, the timing systems needed for this type of application are very large, of table-top size (approaching 1 cubic meter), and consume large amounts of power, making highly-accurate portable applications difficult.

The presentation by researchers from the University of Michigan will discuss a miniaturized microsystem, smaller than a sugar cube, and consuming only 30 mW or power (approximately one thousandth that of a common light bulb). The system to be presented contains a high degree of functionality, including a cesium atomic-vapor cell, VCSEL laser, photodiode detector, polarizing optics, and a thermally-isolated heating element used to keep the cesium atoms in their vapor state. The demonstration of this type of integration is highly indicative of the potential for portable high-precision electronic communication and positioning systems.

Key Developments Include:

Microelectromechanical systems (MEMS) realization of a compact atomic-clock package including a sealed microchip with a cesium-vapor cell.

Integration of multiple components, including a cesium-vapor cell, 852 nm-VCSEL laser, photodiode detector, polarizing and focusing optics, and thermal-stabilization heater elements.

Portability and low power (<30 mW).

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WORLD'S FIRST FULLY-INTEGRATED MEMS GYROSCOPE

MEMS is increasingly used in automotive applications. Pressure sensors and accelerometers for airbag applications are well-known examples. But, future automotive applications will require an increase in performance and reduction in size of MEMS structures. One way to achieve these goals is to monolithically integrate MEMS with the driving, controlling, and signal-processing units in a single silicon chip. This integration will result in a physically smaller system, and thereby improve MEMS performance due to a reduction of the parasitics inherent in external (large-scale) connections. Such a system may also lead to lower cost. One of the approaches for achieving this level of monolithic integration is the fabrication of the MEMS devices on top of a processed CMOS wafer, allowing independent optimization of the CMOS and MEMS processes. This implies that the MEMS must be made at sufficiently low temperatures (below 400°C), so that the underlying CMOS is not degraded. In a presentation (4.7) at ISSCC 2005 this February, its Belgian developers will discuss a MEMS gyroscope integrated on top of a CMOS wafer. The combination performs both directional sensing and information processing. Integration of sensing and processing makes this the world's first single-chip miniature-gyroscope solution having excellent performance.

This and other related topics will be discussed at length at ISSCC 2005, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 6-10, 2005, at the San Francisco Marriott Hotel.

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"CMOS WIFI-ON-A-CHIP" 802.11 CMOS SYSTEM-ON-A-CHIP

Mass-consumer-market wireless applications set strict requirements on cost, dynamic range, power consumption, and the number of external components used in the system. These constraints have already been applied to Bluetooth chips, and the resultant chips have been previously reported. This year, at ISSCC 2005, we see these trends being applied to WLAN ICs, and similar levels of integration being demonstrated in WLAN SoCs. Correspondingly, many of the most integrated solutions are implemented in deep-submicron CMOS technologies which allow the full integration of the MAC and the PHY layers on the same die. These highly- integrated low-cost low-power ICs open the door for the application of WLAN ICs to many new embedded and non-embedded applications, and ultimately to a seamlessly connected world. WLAN-enabled printers, cable modems, set-top-boxes, digital cameras, cell phones, and game consoles, are just a few examples of integration of WiFi in various types of consumer electronics. The high-level of integration of such a system-on-chip changes the economics of WiFi solutions, and enables the continued price reduction of WiFi-enabled consumer electronics.

At ISSCC 2005, in February, Atheros will present the most integrated 802.11g SoC published to date [5.2]. There are many architectures to achieve such a system, Atheros utilizes a sliding-IF super-heterodyne structure, which eliminates one of the on-chip phase-locked loops required in traditional super-heterodyne radios. This SoC includes the RF, analog, ADC, DAC, MAC and PHY functions in a single CMOS die. This receiver achieves similar sensitivity as previously published for multi-chip and less-integrated solutions. The transmitter is capable of transmitting +4dBm. The die occupies an area of 41 square millimeters.

An unprecedented level of integration is demonstrated by a direct-conversion CMOS 802.11b SoC to be presented at ISSCC 2005 by its developers at Broadcom [5.3]. The direct-conversion architecture utilized in this SoC allows for very small size and low power consumption, but is quite difficult to design. This SoC integrates all of the radio building blocks including the PA, loop filter, and the antenna switch along with the analog sections, ADCs, DACs and all of the digital PHY and MAC blocks. This SoC has an antenna as its input and digital bits (to the host processor) as its output! The receiver achieves a sensitivity similar to what has been demonstrated before in multi-chip and significantly less integrated solutions. The transmitter is capable of transmitting a nominal output power of +13dBm. The die occupies an area of 32.2 square millimeters.

This and other related topics will be discussed at length at ISSCC 2005, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 6-10, 2005, at the San Francisco Marriott Hotel.

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Sigma-Delta Grows

THE BATTLE OF THE SIGMA-DELTA ADCS

While Sigma-Delta Analog-to-Digital Converters have been considered to be a mainstream technology for nearly two decades, the 2005 International Solid-State Circuits Conference (ISSCC) will set a new standard, with more than two sessions dedicated to such converters featuring oversampling techniques.

Switched-Capacitor circuit technology has been the long-standing favorite for implementing Sigma-Delta ADCs, and there are several examples which push the state-of-the-art in this area, extending the bandwidth to 24MHz for wireless-LAN applications, and pushing the technique onto 90nm processes for integration in SoCs.

An alternative technique is to implement the Sigma-Delta modulator in the continuous-time domain. ISSCC 2005 will feature a full session dedicated to these architectures, adapted to a wide variety of applications. The Continuous-Time Sigma-Delta A/D converters post some very remarkable power-efficiency numbers—the special strength of this approach.

Rounding out the attractions for the Sigma-Delta fans are two Digital-to-Analog Converters implemented with Sigma-Delta techniques.

Overall, one can conclude that Sigma-Delta converter techniques have now expanded beyond their traditional low-speed/high-resolution/audio niche to become a pervasive technology touching a broad range of evolving applications.

This and other related topics will be discussed at length at ISSCC 2005, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 6-10, 2005, at the San Francisco Marriott Hotel.

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VOLTAGE AND TECHNOLOGY CONTINUE TO DRIVE ANALOG-CIRCUIT INNOVATION

Integrated-circuit technology continues to drive itself down to finer and finer features, allowing more and more transistors to be packed onto a single chip. For digital circuits, the benefits are great—more integration, higher clock rates, and more processing muscle. With each generational advance in lithography, however, power-supply voltages are reduced. This presents a particular challenge to the analog-circuit designer, who is constantly battling to maintain her/his sensitive signal above the "noise floor".

In some cases, the analog circuitry can be moved to a separate chip with higher supply voltages, implemented in older technology. In other cases, however, the need to totally integrate is compelling: analog circuits that can operate on supply voltages below 1V are required. Furthermore, these circuits must cope with other special challenges posed by fabrication processes at 90nm, and below: high leakage currents and low gain, for example.

Much of today's analog-circuit innovation is directed toward solving the resulting problems. Correspondingly, presentations at ISSCC 2005 will reflect some of the advances in circuit techniques for very-deep-submicron design. In view of the difficulty of deep-submicron analog design, architectures where digital complexity can be added in exchange for simplification of the analog design are favored. Accordingly, Sigma-Delta converters are popular. But the Conference will also explore effective more-analog implementations of high-speed pipelined A/D converters in 90nm CMOS, as well as integrated filters. Such presentations show that, while their design is challenging, analog circuits are certainly possible in 90nm technology!

This and other related topics will be discussed at length at ISSCC 2005, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 6-10, 2005, at the San Francisco Marriott Hotel.

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BETTER AND FASTER DACS: RADIO TO AUDIO

Advances in signal processing are often measured by increasing speed (or bandwidth) and increasing dynamic range (or resolution). Digital-to-Analog Converters (DACs) are a key element in the signal chain, taking the signal from the digital domain back to the "real world" of analog signals. In many cases, the DAC can be the ultimate performance-limiting link in the signal-processing chain.

This year, ISSCC features an entire session dedicated to DACs, establishing new benchmarks in performance. In the high-speed arena, the emphasis is on DACs that can directly synthesize radio signals, a critical component in bringing more and more of the radio functionality into the digital domain. At ISSCC 2005, DACs with clock rates up to 22gigasamples per second will be presented, DACs with the ability to directly synthesize signals up to 1GHz and beyond—critical for cellular telephony and emerging broadband radio applications.

At the other end of the spectrum, Sigma-Delta techniques used in the new generation of high-performance Class-D audio amplifiers, provide a technique whereby a specially-processed digital signal directly drives the loudspeaker. A special version of this technique presented at ISSCC 2005. As usual, this year, ISSCC is the Conference at which innovation in electronics, whether audio or radio is normal fare!

This and other related topics will be discussed at length at ISSCC 2005, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 6-10, 2005, at the San Francisco Marriott Hotel.

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REAL-TIME HIGH-DEFINITION H.264 VIDEO

Due to its high compression capability at low bit rates, the latest video standard, H.264/AVC is becoming an important component in the communication and consumer-electronics industry. H.264/AVC decreases bit rates by 25% to 45% and 50% to 70% when compared with MPEG-4 ASP and MPEG-2, respectively. MPEG-2 has been adopted for DVD applications, and MPEG-4 is widely used in cellular-phone environments. H.264 employs advances in intra- and inter-prediction, as well as variable-block-size motion estimation, to provide lower bit rates. These new features will enable the possible presentation of high-definition digital-video disc (HD-DVD) and digital-video broadcasting on handheld terminals (DVB-H).

This year, at ISSCC 2005, National Taiwan University will report (7.1) the first implementation of a high-definition single-chip H.264 video encoder. The encoder contains a main controller and five engines for integer motion estimation (IME), fractional motion estimation (FME), intra prediction (IP), entropy coding (EC), and deblocking (DB). The core size of the chip is 31.72square millimeters using 0.18 micron CMOS technology. It contains 923K logic gates and 35KB SRAM. Power dissipation is 581mW for D1 video (YUV420, 720x480, 30fps), and is 785mW for HDTV 720p video.

Just as MPEG-2 has been adopted for DVD applications, H.264 will likely be adopted for HD-DVD, BD(Blu-ray Disk), and other high-quality HD-video applications, to become the next-generation video standard. Clearly, this development from Taiwan represents a key milestone for the H.264 standard.

This and other related topics will be discussed at length at ISSCC 2005, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 6-10, 2005, at the San Francisco Marriott Hotel.

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TRENDS IN WIRELINE COMMUNICATION

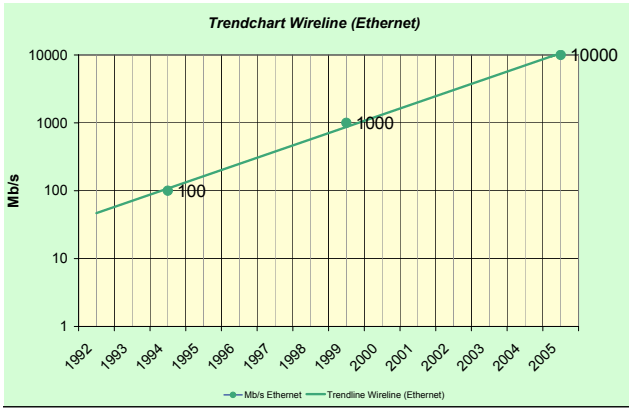
Moore's Law marches on! Such is the conclusion that can be drawn by examining performance characteristics of integrated-circuits and systems introduced over the years at ISSCC. the International Solid-State Circuits Conference, and foremost global forum for such developments.

As CMOS feature size relentlessly diminishes, increasingly-complex and more- integrated systems have been possible. Correspondingly, in the area of wired communication, the electrical and optical interconnection between chips, over backplanes, and between systems, CMOS ascends, overtaking BiCMOS, SiGe, and GaAs. This change has been dramatic, by any measure. For example, the recent increase in transmission speed from 6.25Gb/s to 40Gb/s makes it now possible to transfer the entire content of a DVD within a second! Such chips as these, to be described at ISSCC 2005 at the San Francisco Marriott, in February, will be used in the backbone of the Internet. And, in such a role, they will contribute significantly to faster access and download for the individual users of all Internet services.

The fact of Moore's-Law-led unbridled growth in wireline communications can be appreciated in the accompanying chart, where Ethernet data rates over the years are plotted. From the graph, one can see that the data rate demonstrates the exponential growth predicted by Moore. The particular rate of growth observed in this Ethernet example is doubling every two years. But, while this example has been for Ethernet, other application areas such as DSL show very similar exponential characteristics.

While the demand for this rapid increase in data rate certainly originates, in part, from the ever-growing popularity of the Internet, other applications,like high-quality video conferencing, HDTV and three-dimensional displays, also require more and more bandwidth. This trend will certainly continue, particularly because beyond such applications already with us, future technological dreams, such as virtual reality and holographic imaging, will require even-further advances in pursuit of ever-higher data rates.

While at some point in time we may reach some fundamental limit in such Moore's-Law processes, we do not see (or do not choose to think about) them, today.



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FASTER AND AT LOWER COST

Nowadays, we are facing a rapid increase in data traffic driven by the ever-increasing popularity of the Internet. Continuous scaling of transistors has pushed the performance of CMOS circuits into new regimes of speed, power consumption, and low cost. Now, we can produce transceivers allowing 40Gb/s transmission speeds. Such developments give us the opportunity to improve and further develop commercial data networks and to provide ultimate solutions for the ubiquitous-information society.

For the future, such issues and related developments will be the subject of a variety of presentations at ISSCC 2005, at the San Francisco Marriott in February. Tremendous challenges have to be resolved by engineers in various disciplines, including process, circuit, and system, creating the innovations that will achieve increasingly high speeds, well beyond the reach of conventional techniques.

At this Conference attendees will see the future—many, many ideas for—even faster, even better, and even lower cost, solutions that are already on the way.

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PARALLELISM AND MULTIPROCESSING

Microprocessor frequency scaling is running up against fundamental physical limits, which will restrict future performance gains for traditional single-processor systems. Even though technology scaling continues to provide ever-increasing circuit density, transistor leakage and power-density concerns will slow the continuing advance of peak clock frequency, forcing designers to look for new ways to achieve higher performance. As a result, chip architects are exploring ways in which to use parallelism and multiple processing units to enhance overall chip performance, while limiting the difficulties associated with higher clock frequencies. (Parallelism consists of a range of techniques in which multiple program operations execute concurrently on a system.) This trend will be clearly illustrated at ISSCC 2005 in the session on microprocessors and signal processing (Session 10). In this session, all eight papers describe chips containing multiple-processor cores of various types, employing many different approaches to specifying their concurrent operations.

As noted, several methods of employing increased parallelism for enhanced performance are illustrated in the ISSCC 2005 session on microprocessors: Two papers (10.1, 10.3) describe the continuation of the recent trend of integrating two high-performance general-purpose cores onto a single chip, in order to boost the overall single-chip performance. In particular, paper 10.1 describes a dual-core Itanium® chip which uses multithreading techniques to execute two programs concurrently within each core, as well. While these approaches help performance, they do little by themselves to mitigate the power-dissipation problems faced by the high-speed microprocessor core. Another approach, described in paper 10.2 for a CELL processor, presents a heterogeneous architecture in which multiple processors are designed with features specifically targeted for certain applications, saving power and area by this narrower application focus. In this case, special streaming processors provide a high- performance platform for multimedia and streaming workloads. Another approach, described in paper 10.4 on BlueGene/L, uses low-cost cheap small low-power microprocessor cores in a massively parallel fashion. Systems based on this approach can provide an unmatched power/cost-performance tradeoff, although only for certain workloads which can be spread across such a massively-parallel system.

The examples above illustrate some of the problems and tradeoffs inherent in single-chip multiprocessor system design. Although not all workloads can be shared or split up to run efficiently in a multi-processor environment, it is expected that these kinds of architectures represent the wave of the future. Moreover, it is likely that many new structures will appear, targeting specific applications. In the future, further innovation in both hardware and software design will allow better exploitation of larger numbers of processors, providing a path to continued performance improvement, even as microprocessor frequency trends level off.

This and other related topics will be discussed at length at ISSCC 2005, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 6-10, 2005, at the San Francisco Marriott Hotel.

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GIGABIT WIRELESS ETHERNET AT 24GHZ or "RADAR ON A CHIP"

The last decade has seen an exponential increase in the demand for higher bit rates for many existing and emerging applications. Emergence of broadband high-quality video and audio applications, as well as high-speed home and enterprise networking, makes it highly desirable to achieve very-high bit rates in wireless. While wireless-LAN systems are capable of providing bit rates of several tens of Mb/s, bit rates close to a Gigabit per second over a wireless channel have remained illusive to this date. Such an increase in data-handling capacity necessitates substantially more aggressive approaches to system and circuit design. The instrumentation, scientific, and medical (ISM) band at 24GHz offers an attractive alternative for Gigabit Wireless Ethernet (GWE).

At ISCC 2005 at the San Francisco Marriott in February, developers from the California Institute of Technology will present a fully integrated phased-array transmitter with integrated PAs (11.7) using 0.18μm CMOS. It supports bit rates in excess of 0.5Gb/s with standard QPSK modulation, and can provide rates as high as a Gigabit per second over a wireless channel, using more complex modulation schemes.

The propagation challenges at higher frequencies are overcome by using a phased-array multiple- antenna system on both the receiver and the transmitter. An integrated phased-array system uses the coherent addition of signals in free space to generate a focused beam of RF energy that can be electronically steered and pointed in different directions very quickly. The effectiveness of this beam-forming system, when compared to more traditional omni-directional transceivers, is analogous to a laser pointer compared with an incandescent light bulb. For the same amount of power used, the laser pointer produces a light spot many orders of magnitude brighter than that generated by a light bulb that illuminates everything indiscriminately. A similar concept is used for the RF signal to increase the received power at the target receiver, without "illuminating" other receivers with RF power, resulting in much higher signal-to-noise ratio at the receiver, and generating a lot less interference for other users.

The beam-forming function of the chip can also be used for ranging and sensing applications, effectively making it the world's first radar-on-a-chip. This miniaturized radar can be used in a variety of applications, such as automotive obstacle sensing and imaging.

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THERE IS FIBER IN YOUR FUTURE!

Communication using light signals over optical fibers holds great promise to lower costs for all terrestrial data transport over both short and long distances. The huge bandwidth and favorable physical characteristics of optical fiber begs to be exploited: Telecom networks, transmitting high-data- rate signals over long distances become practical; in Computer-systems high-capacity interconnect, free from electromagnetic interference and awkward bulky copper cables dissenabled by parallel optics. But, of course, practical details limit cost-effective commercial solutions. At ISSCC 2005, in February, several advances in the practical art of sending and receiving optical signals are presented. Such developments will lead inevitably to exciting new cost-effective telecom services, and higher-performance computer systems.

A 10Gb/s laser driver with impedance-matched electrical output will be presented by its developers at Analog Devices [12.1]. It enables the use of a low-cost TO-can package for the laser. Previously, the inferior electrical characteristics of such a low-cost package impaired the optical eye of the transmitted optical signal. The reason for this impairment is imperfect termination of the electrical transmission line between the driver and the laser, causing a portion of the electrical drive signal to be reflected away from the laser, and back to the driver. This reflected signal must be absorbed at the driver, or else it will just rattle around between the driver and the laser, and degrade the eye. Previous methods of absorbing this reflected signal at the driver used passive resistor termination,and wasted half of the signal power. This new circuit synthesizes a termination impedance which delivers all of the signal power to the laser diode.

As well, a step toward short-distance high-capacity interconnections within a computer will be described by its developers at IBM, Cornell and Agilent [12.2]. It uses parallel optical fibers assembled in a ribbon format. A backplane comprising 48 parallel channels, each operating at a data rate of 20Gb/s is the goal of the laser-driver design. Use of electrical signaling on copper wires for such a huge aggregate data rate would take hundreds of wires and consume many watts of power. As well, such copper wires would radiate electrical interference, as well as be a victim of such interference. Simply cooling and shielding such a system would be prohibitively expensive. Optical solutions have none of these problems. Vertical-cavity surface-emitting lasers (VCSELs) are particularly suited to this application because they are low-cost, easy-to-fabricate into an array, and low-power. However, the VCSEL has speed limitations: happily, these limitations are overcome in the design to be reported, by using pre-emphasis on the electrical drive signal. This parallel optical solution promises to remove an anticipated bottleneck in data throughput for evolving high-performance computer systems.

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SENSORS

Combined advancements in integration and in sensor-device design have led to significant advances in the performance of sensors of many kinds, including, for example, temperature, angular position, compass heading, toxicity, acceleration, and biometric identification. Perhaps unexpectedly, these developments can be accomplished using standard CMOS processing, in many cases, or using CMOS with post-processing to create sensing elements.

Specific examples of such developments, to be presented at ISSCC 2005, include the following:

(1) For temperature, the integration of a bandgap-reference circuit with other precision analog circuitry, and a Sigma-Delta ADC, within a CMOS process that allows for a 5 improvement in temperature sensing over the full military range of operation [13.1].

(2) For angular position, the integration of a directional sensor created from MOSFETs with on-chip digital processing, that achieves 0.36 degrees of rotational precision, a distinct advance in the state-of-the-art [13.2].

(3) For compass direction, the integration of a calibration coil and support circuitry within a standard CMOS process, allows self-calibration to overcome environmental effects and aging, to achieve a 6 improvement in magnetic-sensor performance. In this design, the use of on-chip circuitry allows spinning-current operation to compensate for component offset, leading to an integrated compass with an accuracy of 0.5° [13.5].

(4) For toxics-monitoring, the combination of sensor design with process enhancements, and of compensation with on-chip signal processing, leads to a toxic-metal detector, operating down to the 0.8 parts-per-billion level, a 58 improvement in detection capability per unit power [13.4].

(5) For acceleration monitoring, the combination of digital processing with feedback, and of a MEMS post process to create an enhanced sensor, enables an improved accelerometer [13.6].

(6) For fingerprint recognition, two examples of improved fingerprint sensing are provided, one using column-parallel processing, [13.7] and the other with an embedded RISC processor [13.8]. Both demonstrate how the intimate combination of a capacitive sensor array and integrated processing can provide an enhanced fingerprint image for biometric identification.

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DYNAMIC VOLTAGE MANAGEMENT

The priority of power reduction in today's processor designs is well-known. Overheating and other power issues have plagued recent processor designs, forcing frequency reductions and product cancellations. A spate of papers to be presented at ISSCC 2005, at the San Francisco Marriott in February, present new approaches to exploiting one of the most promising approaches to power reduction, namely dynamic voltage management.

A voltage must be provided to a processor (or any circuit) for it to function at all. The value of this voltage has a direct (linear) impact on the frequency at which the chip can operate, and a quadratic (square-law) impact on power consumption. Historically, the value of this voltage has been dropping, from 5 Volts, 10 to 15 years ago, down to barely over 1 volt in today's processors. It is one of the miracles of semiconductor scaling that transistor speed (and, hence, processor clock rate) has maintained its exponential increase in the face of reduced voltages. This voltage reduction, which results in a square-law reduction in power, is what has kept power from exploding. For example, today's 1V processor will burn 1/25th of the power of last decade's 5V processor at the same frequency.

Unfortunately, the days of ever-decreasing voltage are over. 1V is widely viewed as a plateau below which it will be very hard to go in the foreseeable future. This has forced designers to find ways to dynamically move a processor's voltage around to exploit the square-law behavior. Done properly, in theory a processor can provide the performance of a high-voltage design for the power consumption of a low-voltage design. One only has to raise the voltage at the relatively rare times when the processor needs to run at top speed, and to leave it low at other times. Several of the biggest challenges to doing this efficiently will be addressed by presentations to be made at ISSCC 2005. One such problem is that the processor's frequency must also be managed to obey the linear relationship between voltage and frequency. Another is that any power-managed processor really needs to know what its instantaneous power consumption is, in order to set the voltage properly.

With those challenges being met with innovative solutions, we will see dynamic voltage management provide some relief from the limit on voltage reduction possible in silicon process technologies. This will just be a temporary injunction, however. Increasing frequencies and integration will continue driving power up, and, in a few years, designers will need new breakthroughs, if they are to continue to cling to Moore's law.

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SINGLE-CHIP QUAD-BAND GSM/GPRS CMOS TRANSCEIVER

The worldwide subscriber base for cellular services is growing steadily, and is expected to exceed 1.5 billion by 2007, making it the largest market segment for the semiconductor industry. Today, cellular services for voice communications are primarily based on 2G systems, such as GSM and CDMA. Of the two, GSM is the most-popular worldwide cellular standard in use today, with over 75% of the total cellular market. With the rising demand for data services, the emerging 2.5G and 3G systems, such as EDGE/GPRS and UMTS/CDMA2000 will play an increasingly important role in enabling multimedia services with feature-rich handsets.

To support enhanced functions in current and future multimedia handsets, RF cellular ICs must provide small-form-factor low-power solutions, while meeting stringent system-level requirements, including sensitivity and linearity. High sensitivity improves the reception of an on-going call, as well as extending the distance range of the handset. High linearity improves the quality of the call in areas with high subscriber density.

Existing cellular phones are implemented in multiple-chip sets based mainly on Bipolar and SiGe technology. While current SiGe/bipolar chip-sets achieve adequate system performance, they do not lend themselves well to high levels of integration at low cost.
The increased integration capability of deep-submicron CMOS technology can enable the integration of a complete RF cellular transceiver, as well as digital signal processing, on a single chip. Such integration will dramatically reduce power, for extended battery life, while maintaining adequate system performance. Existing CMOS solutions for RF transceivers are also based on multiple chips. However, several single-chip CMOS solutions are beginning to appear.

ISSCC 2005 will showcase, for the first time, the technology of a fully-integrated quad-band GSM transceiver in mature low-cost 0.18-μm CMOS. This design has the best sensitivity/linearity and power dissipation tradeoff on the market today for CMOS transceivers. This single-chip transceiver achieves a linearity of 15dBm and a sensitivity of 110dBm, while consuming 95mA in receive mode and 112mA in transmit mode, both from a 2.7 to 3V supply. This work demonstrates the viability of integrating high-performance cellular ICs, such as GSM, in a single chip, and opens the possibility of future integration of RF transceiver functions together with baseband support in a low-cost CMOS chip.

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SPLITTING A SINGLE WIRE

Electronic signals between chips travel on fixed wires, much like trains on a track—one message in one direction at a time. Many chips can use the same wire, but they have to cooperate. First, the microprocessor talks to the memory, then, later, the memory talks to the processor. To get multiple chips talking to each other, they all have to coordinate and take turns to avoid metaphoric trainwrecks. Until now!

At 2005, its developers from SST Communications and UCLA, describe a technique that lets multiple chips talk to each other over the same wire, without interfering with each other. Using this technique, the microprocessor can talk to the memory, while the memory answers back at the same time. Or, maybe, the memory sends data to the microprocessor, while the cpu sends data to the video card, without coordination. Sharing a wire was possible before, but only if one of the signals was extremely slow, possibly thousands of times slower than the other. But there is no such slowdown now: The new chip sends data at up to 2.4Gbits/second in one direction, and 600Mbits/second in the other. (That's fast enough to transmit an entire uncompressed CD in about 10 seconds, in the slow direction.) A regular phone line also transmits speech in both directions over the same line, but it requires bulky transformers and other special hardware, which would be too expensive at these speeds.

The technique to be presented at ISSCC 2005 to split a wire has been borrowed from radio and cellphone communications: The chip uses different frequencies to send different signals, so that multiple conversations can take place at the same time. Obvious, yes? Well, it's easier imagined than done! A radio or cellphone has very carefully-tuned filters to make sure it only hears the information intended for it. Those kinds of filters are impractical in a chip, and far too expensive to use routinely. And without them, the conversations become hopelessly jumbled. The new chip manages to separate multiple data streams using only on-chip filters. That it can be cheap, without compromising data rate or integrity, is a remarkable feat!

Fewer wires, faster communication, more flexibility, cheaper…. and no data-wrecks. Such are the exciting developments to be experienced at ISSCC 2005 in February, at the San Francisco Marriott.

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TRENDS IN IMAGE SENSORS

As will be reported at ISSCC 2005, advancements continue in image-sensor design, enabling increased performance and functionality in smaller packages. These developments demonstrate several important trends:

(1) Pixels continue to shrink to allow more pixels per unit area, improving the image-resolution-to-cost tradeoff. A CCD imager with 1.56 micron pixels [19.1] and a CMOS imager with 2.0 micron pixels is to be presented [19.2].

(2) Process scaling continues, unabated, following the digital-logic lead: Image sensors use standard CMOS processes down to 0.15 micron, along with enhancements to obtain color response and increased responsivity. Such scaling allows additional integration to permit the incorporation of ADCs, providing increased functionality in signal-processing and control, to enable increased performance, and to enable additional pixel-processing in the focal plane. Examples of this direction include pixel structures providing increased dynamic range, 12b ADC for HDTV video operation, binning in a CCD for increased viewfinder sensitivity for a cell-phone camera, and region-of-interest tracking to allow high-speed readout of infracting license plates [19.3]

(3) Applications of image sensors, beyond simple photography, continue unabated. Applications to be presented at ISSCC 2005 include wide-dynamic-range imaging for automotive and surveillance, use 3D imaging with a precision of millimeters per meter, and motion detection. The increased possibilities enabled by increased integration allow multi-functional pixel arrays to provide detection as well as imaging, allow multiple exposures that can be fused into higher-quality images, and allow on-chip calibration to smoothly transition the intensity response from a linear to a logarithmic transfer function [19.4]

(4) Advancements in processing, such as wafer bonding and wafer-to-wafer vias within the pixel, enable the demonstration of a one-megapixel image sensor with processing behind every pixel [19.6].

And so, pixel pace proceeds, as presented in February, at ISSCC 2005!

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RF MEMS

Traditionally, Micro-ElectroMechanical Systems (MEMS) have been applied in accelerometers and micro-mirror displays. But, recently, CMOS MEMS have emerged to realize new communication applications. Four contributions to ISSCC 2005 at the San Francisco Marriott, in February, will describe major advances to this field (21.1, 21.2, 21.3, and 21.5):

Researchers from Carnegie Mellon University (21.1) will report on advances in RF foundry processes. These have lead to the realization of high-performance electromechanical mixer filters. Such filters enable down-conversion from the GHZ to the MHz range, with built-in frequency selectivity.

Using MEMS techniques, integrated high-quality-factor Bulk-Acoustic-Wave (BAW) resonators and filters have been developed at CSEM, Neuchâtel, Switzerland and STMicroelectronics, Grenoble, France (21.2 and 21.3). Using a process that integrates CMOS, Bipolar and BAW devices, RF passive and active devices are integrated on a single chip. This development leads directly to the realization of multi-standard and multiband communication systems.

Further advances in integrated RF components, such as inductors, resistors, and capacitors based on thin-film Cu/BCB (copper/benzo-cyclobutene), will be reported by researchers from IMEC, Leuven, Belgium (21.5). The thin-film approach to be presented allows for the realization of new classes of low-cost high-performance RF systems.

Key developments include:

The availability of enhanced quality-factors in RF MEMS capacitors and inductors.

The integration of Bulk-Acoustic-Wave Devices in an efficient above-IC process that will facilitate new types of wireless-communication systems.

The availability of a thin-film approach for realizing on-chip and in-package passive RF components.

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RF TRENDS: CMOS REACHES MILLIMETER-WAVE PERFORMANCE

Worldwide, there is now a confirmed interest in applications in the 60GHz frequency band, inspired in part by the availability of a new unlicensed 7GHz bandwidth around 60GHz. Operation in this frequency band was once the exclusive domain of III-V-compound semiconductors, such as GaAs and InP. However, aggressive scaling of CMOS technology has made the fabrication of highly-integrated CMOS mm-wave circuits a reality for data-communications. As a result, one expects a significant reduction in the projected cost of the radio chips required for high-data-rate wireless communication at home or in the office.

Another significant aspect of CMOS mm-wave circuits is in their potential application in automotive anti-collision warning systems.

The trend in the use of higher frequencies (100GHz and beyond) will continue in the years to come. As will be presented at ISSCC 2005 at the San Francisco Marriott, in February, researchers at National Taiwan University offer, for the first time, two essential building blocks (a VCO and broadband amplifier) for creating a robust 60GHz radio in a conventional CMOS technology. The VCO is in fact operational at a much higher frequency (to 114GHz).

Other essential building blocks for realizing a 60GHz receiver, to be presented at ISSCC 2005, include a low-noise amplifier and a mixer for frequency translation directly to DC. The operation of these blocks has been successfully demonstrated, as Bezhad Razavi of UCLA will described.

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PLLs' PROGRESS

Digital data communication requires clock signals (square waves) of a precisely known frequency. Time uncertainty in clock-edge position is called jitter. Excessively high jitter can cause unacceptable errors in data transmission.

Phase-locked loops (PLLs) or delay-locked loops (DLLs) are often used to generate clock signals. Considerable design effort is made to realize low-jitter clocks. As data rates rise, jitter must be reduced to permit reliable data transmission.

At ISSCC 2005, in February, papers 22.1 and 22.2 are outstanding examples of PLLs for clock generation. PLLs act as "clock multipliers" which convert an input clock signal of one frequency (for example, from a crystal oscillator) into an output clock signal of a different, usually higher, frequency, suitable for clocking the transmitted data. In these two papers, the PLLs produce precisely-controlled frequencies of 2.5 GHz and 3.125 GHz, respectively. Their clock edges are typically within about 1 picosecond (ps) of those which a mathematically-perfect clock would produce. Such PLLs are an essential part of systems which transmit data at several Gb/s.

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SINGLE-CHIP TV TUNER

Feature-rich digital TV with picture-in-picture, personal-video-recorders, crystal-clear high-resolution pictures: These are some of the benefits that consumers can reap from advanced TVs enabled by the state-of-the-art TV tuner to be presented at ISSCC 2005 by ST Microelectronics [23.3].

Traditional tuners have relied on bulky "canned" tuner modules that employ components that are not amenable to integration on a semiconductor substrate. Integrating a TV tuner in silicon is no small feat. A tuner must be capable of selecting one of over 100 channels between 48 and 862MHz. In a cable-TV set-top-box, the large number of channels available requires the tuner to distinguish both tiny and very large signals, to be insensitive to spurious signals, and to implement very-tough local-oscillator tuning-range specifications.

While there are some silicon tuners available today, they rely on relatively expensive BiCMOS technologies, implement only the analog part of the tuner, and continue to rely on a bulky SAW filter for final channel selection. The work to be presented at ISSCC 2005, by its developers at Chrontel, in San Diego, [23.3], using a 120nm digital CMOS technology has the potential of reducing costs by taking advantage of the economies-of-scale of the digital-semiconductor industry. Equally importantly, the tuner to be described includes a 14b analog-to-digital converter which allows the bulky channel-select SAW filter to be replaced by dirt-cheap on-chip digital filtering.

Mobile TV: Can't get home in time to watch the big game? Watch it on your phone! At ISSCC 2005, developers from ItoM in The Netherlands will present [23.3] a tuner IC for the mobile TV standard, Universal Mobile Tele-Vision (UMTV). Optimized for small size and low power (just 150mW), this tuner can fit comfortably into a cellular phone or a PDA, without running down the battery.

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ULTRA-WIDE-BAND (UWB) FOR NOVEL WIRELESS NETWORKS

Interest in ultra-wideband (UWB) wireless technology has exploded over the last few years, primarily driven by its promise to deliver data rates in excess of 100Mb/s over short distances, while consuming very low power at very low cost. Two such developments, which describe leading-edge UWB transceivers, will be presented in February at ISSCC 2005 in San Francisco.

While one transceiver pursues an aggressive data rate, the other focuses on ultra-low power consumption. The first solution implements a high-data-rate 480Mb/s UWB baseband transceiver based on coded-multi-carrier techniques. This design consumes a total power of 575mW, providing an energy efficiency of 1.2nJ/bit. The second design implements a 62.5Mb/s UWB transceiver which consumes only 6.7mW, and occupies an area of under 3 square millimeters in 0.18 micron CMOS technology. This corresponds to an impressive energy efficiency of 0.1nJ/bit! The novel aspects of both transceivers will be presented at ISSCC 2005.

These designs are among the fastest and lowest-power UWB transceivers reported to date, and point the way to further advances in this rapidly-developing wireless technology.

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PUSHING THE WLAN ENVELOPE

ISSCC 2005 will feature two recent innovations in WLAN baseband transceivers. They address growing issues in both the home and enterprise markets. The challenge to be met is to improve the overall quality-of-service and utility of wireless communication networks.

On the home front, the push towards wireless distribution of high-definition video has resulted in the need to improve the reliability of wireless channels, and to increase the coverage area of existing WLANs. At ISSCC 2005: Atheros will describe their multi-antenna solution which utilizes advanced signal-processing techniques to greatly increase the reliability and range of conventional WLAN channels. Atheros will also describe their advanced packet-management functions which facilitate video transmission.

In the enterprise arena, the wide range of data rates used within the same channel, results in low-rate clients severely limiting the performance of high-rate clients, yielding low overall network performance. At ISSCC, Engim will describe a wideband WLAN solution that is capable of operating on three adjacent channels concurrently. This wideband multi-channel approach allows low-rate clients to be grouped on a slow channel, while high-rate clients can operate unimpeded on a fast channel, yielding much better overall network performance. Engim will also discuss their real-time spectral-monitoring facilities that provide advanced network-management capabilities to detect interferers and rogue clients, allowing for improved performance and security. And so, WLAN developments proceed, at a characteristically astounding pace! A pace which characterizes the presentation of many developments at ISSCC!

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FASTEST RANDOM-CYCLE EMBEDED DRAM

Although a random-cycle-operated DRAM was announced at ISSCC 2004, the design was limited to operation at 312MHz and needed an expensive DRAM-dedicated fabracation process for realizing its 20fF cell capacitors. There are two major requirements imposed on any embedded-DRAM substitute for SRAM: It is required that they provide: 1) fully-guaranteed random access, with multi-port interleaved operation, while satisfying much-more tough and complex sensing-signal-integrity requirements; and 2) CMOS logic-process compatibility without using eDRAM-dedicated cell capacitors, while compensating for the lowered noise immunity caused by a smaller cell capacitance (only 5fF).

As will be reported at ISSCC 2005, to meet these requirements, a 400MHz 1.5V dual-port interleaved DRAM has been developed, with only two key additions to a 0.15μm CMOS logic process:

1) Sense-signal-loss-compensating technology, based on an intensely-detailed noise-element analysis.

2) A striped-trench capacitor (STC) cell which is fabricated by adding only one mask.

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FIRST COMMERCIALLY-VIABLE 2GB DRAM

Although a 4Gb DRAM was announced at ISSCC 2001, high-volume commercially-available DRAMs have been limited to 512Mb. While 1Gb DRAMs are available commercially, it is only in limited quantities. One impediment to effective commercialization has been that previously-announced 2Gb and 4Gb DRAMs have been too large to fit into industry-standard packages, making them unavailable for use in systems designed around industry standards.

In February, at ISSCC 2005, a presentation by memory developers at Samsung will highlight design and technology improvements enabling a smaller chip outline that conforms to the JEDEC industry standard. By the creative use of a third level of metal (typically not found in DRAMs), and an unconventional bank arrangement, it has been possible to modify the chip aspect ratio to fit the standard.

Because the DDR2 interface specification limits the maximum number of chips on the bus, total system-memory capacity is limited by chip density. Thus, the advent of a 2Gb DRAM in an industry- standard package significantly increases the maximum system-memory configuration. The impact on future computer-based products is clearly significant!

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WORLD'S LARGEST SRAM AT 256Mb

At ISSCC 2005, Samsung will introduce the largest SRAM device ever reported. Based on their 0.16μm^2 stacked single-crystal-silicon thin-film-transistor SRAM cell, introduced at the 2004 VLSI-Symposium, the 256Mb chip has an area of just 61.1mm^2. The DDR chip operates at 140MHz with a burst latency of 3 cycles, while drawing only 17mA from a 1.8V supply.

The novel design approach, to be described, uses the stacked single-crystal-silicon thin-film transistor as the local column-select transistor in a hierarchical-bitline architecture, to virtually eliminate the usual area penalty associated with this approach. An array efficiency of over 70% is achieved, while maintaining the power and speed benefits of the short hierarchical bitlines.

The 256Mb DDR SRAM to be described is organized as 16Mb x 16 to provide a total bandwidth of 4.48Gb/s. Yet with a current draw of only 17mA, the chip is ideally suited for mobile applications, opening this low-power market to the benefits of very-high-density, high-bandwidth static memory.

This and other related topics will be discussed at length at ISSCC 2005, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 6-10, 2005, at the San Francisco Marriott Hotel.

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DUAL-CORE ITANIUM® EXPANDS L3 CACHE TO 24MB

As will be reported at ISSCC 2005, designers at Hewlett-Packard and Intel have extended the Itanium® Processor to a dual-core architecture that features a 24MB L3 cache — the largest embedded SRAM array ever reported. Thanks to improvements in array design, and a reduced array operating voltage, the L3 cache consumes only 4.2W, with cache latency reduced from 8 cycles to 5.

Power dissipation in the expanded cache has been controlled by lowering the cache voltage by 300mV from that of the core supply, to reduce gate and drain leakage currents in the memory cells. A shift from the traditional synchronous-SRAM design approach to an asynchronous design also eliminates clocking power in the memory arrays.

Another benefit of the use of asynchronous design is the decrease in L3 cache latency from 8 to 5 cycles. This is possible because excess design margins for clock skews, latch delays, and marginal bits, are all eliminated.

Expanding the size of the embedded memory to support a dual-core architecture offers users the full capability of multi-CPU performance in a single chip.

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CIRCUITS FOR TERABITS PER SECOND

To maximize performance and minimize power consumption of advanced processors, their on-chip supply voltage and clock frequency are being dynamically adjusted. At ISSCC 2005,developers from Korea [28.4] will present a Delay-Locked-Loop-based clock generator which provides clock signals ranging from 120 MHz to 1.8 GHz. The frequency can be changed within this 15:1 range very quickly. In addition, great emphasis is put on providing a clean clock signal. The regular peak-to-peak uncertainty is only 13.2 ps. This performance is achieved in a 0.35μm CMOS technology. Improvements of 4 to 6 can be anticipated for a more current process technology, indicating the feasibility of systems operating at 10+GHz.

The high intrinsic speed of advanced processors makes the transfer of data on and off chip a bottleneck. Also, at ISSCC 2005, developers from Stanford [28.9] will address this issue, and present an I/O interface with a total data rate of more than 0.5 terabits/second (that is, 500 billion bits per second)! The circuit provides a twelve-byte-wide interface (seven bytes for transmitting and five bytes for receiving). Each pin operates at a data rate of 6.4 Gb/s, consuming an energy of only 20 pJ for every transferred bit. To achieve an accurate timing relationship between the I/O pins, the presenters will describe the on-chip clock-distribution technique that delivers the reference clock across the width of the I/O interface, and presents a clock-tracking architecture which allows the use of low-cost clock sources. The circuits to be presented can maintain high analog performance even in an SOI (silicon on insulator) CMOS process, by suitably handling the floating-body effects.

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PRESS COPY

TRENDS IN BIOSENSORS

Biosensing advances at a rapid pace, propelled by evolving trends in low-power electronics. Two directions for these advances will be presented this year at ISSCC 2005:

(1) One is aimed at implantable systems to enable remote access to arrays of sensors. Such systems need to be wireless, to be low-power, and to be programmable, in order to select amongst data available on many parallel channels. An ASIC incorporating a DSP is used, on the front line (so to speak) in one system to compress the raw data, by signal processing, to detect, locally, the occurrence of interesting events, resulting in compression of the data transmitted, and enabling a 12.5 increase in the number of channels that can be handled over the wireless link [30.4].

(2) A second is aimed at creating lab-on-a-chip sensors, and arrays of such sensors, to act as flexible building blocks for biological assay, and DNA analysis. In one case to be reported, this is accomplished by creating an electronic building block that supports various sensor types, allowing wireless readout that eliminates the problem of contamination from direct-wire connection. In another case, access ease is enabled by an array of detectors, each using differential sensing with respect to a local reference for calibration, and each being programmable to allow use in various modes. This allows precision tests to be carried out in parallel, enabling point-of-use and environmental tests [30.6].

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DISPLAY TRENDS

Displays provide an essential interface between two solitudes: the electronic world and the physical world. In this role, displays must respond to developments in technology that are analogous to, but reversed from, those impacting image sensors. Amongst evolving requirements, is the need to be able to provide the basic drive signals to a display in a manner sufficiently cost-effective to enable consumer applications; There is a distinct benefit in developing analog circuitry that can provide the drive in a power-efficient manner; As well, there is a distinct benefit in using the power of mixed-signal processing, and its methodologies, such as self-calibration and feedback, to provide competitive solutions and price points capable of advancing the business case.

This year, at ISSCC 2005, there will be three display papers that touch on developments in which electronics meets displays. Several trends are in evidence:

(1) One is demonstrated by an integrated microdisplay, viewable with image intensification, that demonstrates direct light emission from a silicon integrated-circuit backplane. This display is fabricated in a commercial 0.18micron CMOS process . The challenges met by the on-chip circuitry, in addition to creating and addressing the light-emitting pixels, are calibration and overdrive protection used to provide performance and reliability. Potentially, these techniques could be extended to OLED deposited materials, to provide a microdisplay with direct viewing [30.1].

(2) A second is demonstrated by an example of drive electronics using TFT-on-glass electronics. This is likely to provide a better fit to the form factor of the display than would be available using conventional bulk silicon CMOS technology. The technique is demonstrated in the context of an XVGA LCD display [30.2].

(3) The third is in response to market demand to improve the dynamic range of displays for television, from the 6b to the 8b or 10b level. This has motivated the design of a silicon IC that uses a new DAC architecture and calibration techniques to mitigate component mismatch in a 384-output device. Such self-calibration techniques represent a strong trend in many developments to be reported at ISSCC 2005 [30.3].

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SHEET-TYPE SCANNER USING 3-D ORGANIC CIRCUITS

Organic-transistor technology relies on carbon-based material, which differs greatly from mainstream silicon. Organic circuits have the potential to provide drastically cheaper electronics, using printing and/or plastic-sheet technology. Until now, the drawback of the organic approach has been its slow operation, which has appeared as a major bottleneck in enabling practical applications.

At ISSCC 2005, researchers from the University of Tokyo will describe a new circuit concept called "double word-line and bit-line structure" which dramatically reduces the delay of the circuit by a factor of 5, and the power by a factor of 7. In order to realize the new structure, two layers of organic transistors are stacked in three dimensions, for the first time, together with organic photo-detectors, using laser drilling.

The resulting faster circuit has enabled a sheet-type scanner made with flexible plastic sheets. This portable, ultra-light-weight and flexible scanner, is made possible by organic-transistor technology.

A prototype of the sheet-type scanner is less than a millimeter thick, with an area of 8 square centimeters, with 64 x 64 resolution. If 4 million pixels were to be implemented in a future design, the time for a single scan is estimated to be less than one minute using these 3-D organic circuits.

This and other related topics will be discussed at length at ISSCC 2005, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 6-10, 2005, at the San Francisco Marriott Hotel.

NOTES

ISSCC
GLOSSARY

ISSCC GLOSSARY

Rev. 11/10/2004

1T1C	1 Transistor/1 Capacitor
3G	Third Generation Wireless
3T	3-Transistor
ΔΣ	Delta-sigma
ΔΣM	Delta-sigma Modulator
A/D, ADC	Analog-to-Digital Converter
AAC	Advanced Audio Coding
ACI	Adjacent Channel Interface
ACLR	Adjacent Channel Leakage Power Ratio
ACPR	Adjacent Channel Power Ratio
ADDLL	All Digital Delay Locked Loop
ADSL	Asynchronous Digital Subscriber line
AES	Advanced Encryption Standard
AFC	Automatic Frequency Control
AFE	Analog Front End
AGC	Automatic Gain Control
ALU	Arithmetic Logic Unit
AM	Amplitude Modulation
AMPS	Advanced Mobile Phone Service
AMS	Analog Mixed Signal
APG	Algorithmic Pattern Generator
ARM	Advanced RISC Machine
ASIC	Application-Specific Integrated Circuit
ASK	Amplitude Shift Keying
ASP	Advanced Simple Profile (MPEG-4 Video)
ATA	AT Attachment
ATD	Address Transition Detection
ATE	Automatic Test Equipment
AVC	Audio Visual CODEC
BAW	Bulk Acoustic Wave
BBT	Band to Band Tunneling
BD	Blu-ray disc
BER	Bit Error Rate
BGR	Band Gap Reference
BiCMOS	Bipolar Complementary MOS
BIOS	Basic Input/Output System
BIST	Built-in Self-Test
BOM	bill of materials
BJT	Bipolar Junction Transistor
BL	Bit Line
BPF	Bandpass Filter
BPSK	Binary Phase Shift Keying
B-VOP	Bidirectional Video Object Planes
BW	Bandwidth
CAD	Computer-Aided Design
CAM	Content Addressable Memory
CAS	Column Address Strobe
CCCS	current-controlled current source
CCD	Charge-coupled Device
CCVS	current-controlled voltage source
CDMA	Code-Division Multiple Access
CDR	Clock and Data Recovery
CDS	correlated double sampling
CHE	Channel Hot Electron Injection
CISC	Complex Instruction Set Computer
CML	Current-Mode Logic
CMOS	Complementary MOS
CMRR	Common-Mode Rejection Ratio
CMU	Clock Multiplier Unit
CO	Central Office
CODEC	Coder-Decoder
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
CSMA	Carrier Sense Multiple Access
CT	continuous time
CUI	Command User Interface
CVD	Chemical Vapor Deposition
D/A, DAC	Digital-to-Analog Converter
DAB	Digital Audio Broadcasting
dBFS	dB relative to Full Scale
DCO	Digitally Controlled Oscillator
DCT	Discrete Cosine Transform
DCXO	Digitally Controlled Crystal Oscillator
DDR	Dual Data Rate
DDS	Direct Digital Synthesis
DECT	Digitally Enhanced Cordless Communication
DEM	dynamic element matching
DEMUX	Demultiplexer
DEMOS	Depletion MOS
DFE	Decision Feedback Equalizer
DFM	Design for Manufacturability
DFT	Design for Testability, Discrete Fourier Transform
DIMM	Dual In Line Memory Module
DLL	Delay-Locked Loop
DMA	Direct Memory Access
DMB	Digital Multimedia Broadcasting
DMOS	(Double-)Diffused MOS
DNA	Deoxyribonucleic Acid
DNL	Differential Non-Linearity
DRAM	Dynamic Random-Access Memory
DR	dynamic range
DRC	Design Rule Check
DSL	Digital Subscriber Line
DSP	Digital Signal Processing
DSSS	Direct Sequence Spread Spectrum
DT	Discrete Time
DTL	Diode-Transistor Logic
DUT	Device Under Test
DVB	Digital Video Broadcasting
DVB-H	Digital Video Broadcasting-Handhelds
DVB-S	Digital Video Broadcasting-Satellite
DVB-T	Digital Video Broadcasting-Terrestrial
DVD	Digital Video Disc
DVS	Dynamic Voltage Scaling
DWA	Data Weighted Averaging
ECC	Error-Correcting Code
ECL	Emitter-Coupled Logic
ECP	Emitter-Coupled Pair
EDGE	Enhanced Data rates for Global Evolution
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	Electro Magnetic Interference
ENOB	Effective Number Of Bits
EPROM	Erasable Programmable Read-Only Memory
ERBW	Effective Resolution Bandwidth
ESD	Electrostatic Discharge
EVM	Error Vector Magnitude
f_s	sampling frequency
f_T	transition frequency
FAMOS	Floating Gate Avalanche Injection MOS Transistor
FCC	Federal Communications Commission (U.S.)
FDMA	Frequency-Division Multiple Access
FDNR	Frequency Dependent Negative Resistor
FEC	Forward Error Checking
FeRAM	Ferro Electric Random Access Memory
FF	Flip Flop
FFE	Feed-Forward Equalizer
FFT	Fast Fourier Transform
FIFO	First In-First Out

FIR	Finite Impulse Response Filter
FLOTOX	Floating Gate Tunnel Oxide
FM	Frequency Modulation
FN	Fowler Nordheim
FOM	Figure Of Merit
FPGA	Field-Programmable Gate Array
FSK	Frequency Shift Keying
FSM	Finite State Machine
GBW	Gain-Bandwidth Product
GCA	Gain-Controlled Amplifier
GDDR	Graphics Double Data Rate RAM
GFSK	Gaussian Frequency-Shift Keying
GIDL	Gate Induced Drain Leakage
GMSK	Gaussian Minimum Shift Keying
GOPS	Giga-Operations Per Second
GPRS	General Packet Radio Service
GPS	Global Positioning System
GSM	Global Standard for Mobile Communication
HBT	Hetero-junction Bipolar Transistor
HCI	Host Controller Interface
HD	High Density
HDL	Hardware Description Language
HDTV	High-Definition TeleVision
HPF	High-Pass Filter
HVCMOS	High Voltage Complementary MOS
HVMOS	High Voltage MOS
I/O	Input-Output
I/Q	In Phase and Quadrature
IC	Integrated Circuit
IF	Intermediate Frequency
IIP3	Input referred Input Third-order Intercept Point
IIR	Infinite Impulse Response Filter
IMD	Inter-Modulation Distortion
INL	Integral Non-Linearity
InP	Indium Phosphide
IP	Intellectual Property
IPSEC	Internet (Network) Protocol for Security
ISI	Inter Symbol Interference
ISM	Industrial, Scientific and Medicine Band
JPEG	Joint Photographic Expert Group
JTAG	Joint Test Automation Group
LAN	Local-Area Network
LCD	Liquid Crystal Display
LDCMOS	Laterally Diffused Complementary Metal Oxide Silicon
LDMOS	Laterally Diffused Metal Oxide Silicon
LDO	Low drop-out
LDPC	Low-Density Parity Check
LED	Light Emitting Diode
LFSR	Linear Feedback Shift Register
LNA	Low-Noise Amplifier
LO	Local Oscillator
LPF	Low-Pass Filter
LSB	Least Significant Bit
LSI	Large Scale Integration
LTPS	Low Temperature Poly Silicon
LVDS	Low Voltage Differential Signalling
LVS	Layout Verification to Schematic
MAC	Media Access Controller
MASH	Multi-stage noise shaping
MB-OFDM	Multi-Band OFDM
MCM	Multi-Chip Module
MCU	Micro Controller Unit
MEMS	Micro-Electro-Mechanical System
MIM	Metal-Insulator-Metal
MIMO	Multiple Inputs, Multiple Outputs
MMIC	Monolithic Microwave Integrated Circuit
MODEM	Modulator-Demodulator
MOS	Metal-Oxide-Semiconductor
MOST	MOS Transistor
MPEG	Motion Picture Expert Group
MSB	Most Significant Bit
MRAM	Magnetic Random Access Memory
MTJ	Magnetic Tunnel Junction
MUX	Multiplexer
NF	Noise Figure
NMOS	n-channel MOS transistor
NMOST	NMOS transistor
NPN	Negative-Positive-Negative bipolar transistor
NRTZ	Non Return To Zero
NRZ	Non-Return to Zero (also NRTZ)
NVM	Non Volatile Memory
NVRAM	Non Volatile Random Access Memory
OFDM	Orthogonal Frequency Division Multiplexing
OIF	Optical Internetworking Forum
OIP3	Output referred Third-Order Intercept Point
ONO	Oxide Nitride Oxide
OOK	On-Off Keying
OSR	Over-Sampling Ratio
OTA	Operational Trans-conductance Amplifier
OTP	One Time Programmable
P_{1dB}	1dB gain compression point
PA	Power Amplifier
PAE	Power Added Efficiency
PAM	Pulse Amplitude Modulation
PAN	Personal Area Network
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PDA	Personal Data Assistant
PFD	Phase and Frequency Detector
PGA	Programmable Gain Amplifier
PHEMT	Pseudomorphic High-Electron-Mobility Transistor
PHY	Physical Layer
PLA	Programmable Logic Array
PLC	Power-Line Communication
PLD	Programmable Logic Device
PLL	Phase-Locked Loop
PMOS	p-channel MOS transistor
PMOST	PMOS transistor
PNP	Positive-Negative-Positive bipolar transistor
PON	Passive Optical Network
POTS	Plain Old Telephone Service
PPM	Pulse-Position Modulation
PRAM	Phase-change RAM
PRBS	Psuedo-Random Binary Sequence
PRML	Partial Response, Maximum Likelihood
PROM	Programmable Read-Only Memory
PSD	Power Spectral Density
PSK	Phase Shift Keying
PSNR	Peak SNR
PSRR	Power Supply Rejection Ratio
PTAT	Proportional to Absolute Temperature
PVD	Physical Vapor Deposition
PVT	Process, Voltage, Temperature
PWM	Pulse-Width Modulation
QAM	Quadrature Amplitude Modulation
QDR	Quad Data Rate
QoS	Quality of Service
QPSK	Quadrature Phase Shift Keying
QVCO	Quadrature Voltage Controlled Oscillator
QVGA	Quarter Video Graphics Array
RAM	Random-Access Memory
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
ROM	Read-Only Memory
rms	Root Mean Square

RSA	A public-key cryptographic system, named after: Ron Rivest, Adi Shamir, and Leonard Adleman
RSSI	Received Signal Strength Indicator
RTL	Resistor-Transistor Logic
RTZ	Return To Zero
RX	Receiver
RZ	Return to Zero (also denoted by RTZ)
SATA	Serail AT-Attachment
SC	Switched Capacitor
SCP	Source-coupled pair
SCR	Silicon Controlled Rectifier
SDRAM	Synchronous Dynamic Random-Access Memory
SEM	Scanning Electron Microscope
SER	Soft Error Rate
SerDes	Serializer/Deserializer
SFDR	Spurious Free Dynamic Range
SFI	Serdes Framer Interface
S/H	Sample-and-Hold
SHA	Sample-and-Hold Amplifier
SiGe	Silicon Germanium
SILC	Stress Induced Leakage Current
SIMD	Single Instruction, Multiple Data
SIP	Single Inline Package
SiP	System in a Package
SMP	Symmetric Multi-Processing
SNDR	Signal-to-Noise and Distortion Ration
SNR	Signal-to-Noise Ratio
SoC	System on a Chip
SOI	Semiconductor on Insulator
SONET	Synchronous Optical Network
SONOS	Silicon-Oxide-Nitride-Oxide-Silicon
SOS	Silicon On Saphire
SPI	System Packet Interface
SRAM	Static Random-Access Memory
SSB	Single Side Band
SSTL	Stub Series Terminated Logic
TC	Temperature Coefficient
TCAM	Ternary Content Addressable Memory
TDDB	Time Dependent Dielectric Breakdown
TDMA	Time Division Multiple Access
TEM	Tunneling Electron Microscope
TFT	Thin-Film Transistor
T/H	Track and Hold
THA	Track-and-Hold Amplifier
THD	Total Harmonic Distortion
THD+N	THD plus noise
TOPS	Tera Operations Per Second
TTL	Transistor-Transistor Logic
TX	Transmitter
UDTV	Ultra-High Definition Television
UHF	Ultra-High Frequency
UI	Unit Interval
UIPP	Unit Interval Peak-to-Peak
U-NII	Unlicensed National Information Infrastructure
UMTS	Universal Mobile Telecommunication System
UPROM	Unerasable Programmable Read Only Memory
USB	Universal Serial Bus
UWB	Ultra WideBand
VCCS	Voltage-Controlled Current Source
VCDL	Voltage-Controlled Delay Line
VCO	Voltage-Controlled Oscillator
VCVS	Voltage-Controlled Voltage Source
VCXO	Voltage-Controlled Crystal Oscillator
VCSEL	Vertical Cavity Surface Emitting Laser
VDMOS	Vertically diffused MOS
VGA	Variable-Gain Amplifier, Video Graphics Array
VLIW	Very Long Instruction Word
VLF	Very Low Frequency
VLSI	Very Large-Scale Integration
VSWR	Voltage Standing-Wave Ratio
WAN	Wide-Area Network
WCDMA	wideband Code-Division Multiple Access
WEP	Wired Equivalent Privacy
WiFi	Wireless Fideleity; an interoperability certification for WLAN products based on the IEEE 802.11 standard
WL	Word Line
WLAN	Wireless Local-Area Network
XAUI	10 Gigabit eXtended Attachment Unit Interface

PREFIXES AND UNIT ABBREVIATIONS

d	dec	k	kilo
c	centi	M	mega
m	milli	G	giga
μ	micro	T	tera
n	nano		
p	pico		
f	femto		
a	atto		

A	amperes	S	siemens
Å	angstroms	s	seconds
b	bits	v	volts
B	bytes	W	watts
C	coulombs	Ω	ohms
^{0}C	degrees Celsius		
F	farads		
ft	feet		
H	henrys		
Hz	hertz		
in.	inches		
J	joules		
K	Kelvin		
m	meters		
rad	radians		

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