[1] These capacitances are strongly bias dependent. As you found in Problem Set #3, they have slightly different values for rising and falling output, but for the purposes of back-of-the-envelope calculations, this single number will do fine.

[2] In Problem Set #3, we calculated values for "unloaded" and "fully loaded" wires. These numbers reflect an "average" cap to use for estimation.

[3] The beta ratio for balanced rising and falling delays is two.

[4] In Problem Set #4, we went to a great deal of effort to calibrate $m_n$ and $m_p$ from simulation, but found that for the "fast" input in the stack, this number was very close to the "ideal" case, so we will just use these ideal numbers in our sizings.

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EE E4321. Summary of "rules-of-thumb" for CMOS14TB

In Problem Sets #3 and #4, you calculated various "rule-of-thumb" parameters for our HP CMOS14TB technology. In the following table, we present the "blessed" value to be used in our back-of-the-envelope sizing and delay estimations.

| Transistor cap | Capacitance per $\mu$m of transistor W |
|---|---|
| gate | 2 fF/$\mu$m |
| ndiff[1] | 0.7 fF/$\mu$m |
| pdiff[1] | 0.7 fF/$\mu$m |

| Wire cap | Capacitance per unit length |
|---|---|
| poly (0.6 $\mu m$ wide) | 0.2 fF/$\mu$m |
| metal1 (0.9 $\mu m$ wide) | 0.07 fF/$\mu$m$^2$ |
| metal2 (0.9 $\mu m$ wide) | 0.07 fF/$\mu$m$^2$ |
| metal3 (1.5 $\mu m$ wide) | 0.07 fF/$\mu$m$^2$ |

| FET type | Resistance |
|---|---|
| nfet | 8 $k\Omega\mu m^3$ |
| pfet | 16 $k\Omega\mu m^3$ |

| Stack height | $m_n$ | $m_p$ |
|---|---|---|
| 2 | $2^4$ | $2^4$ |
| 3 | $3^4$ | $3^4$ |
| 4 | $4^4$ | $4^4$ |