

Peter Kinget: Research Overview

Introduction: Connecting Bits to the Physical World

The exponential increase in the density of components on integrated circuits in tandem with an exponential component cost reduction has been a tremendous driver for the development of our information society. This remarkable achievement of the electronics industry is often referred to as Moore's law. Although several important obstacles for the scaling of silicon devices have been identified, at least an additional one or two decades of exponential scaling for silicon-based electronics is widely expected. Furthermore, several technology alternatives to keep supporting this exponential growth are currently being investigated, since the desire of the information society for more powerful information devices at a progressively lower cost is not expected to stop.

The ability to realize very complex signal and information processing functions on a small silicon chip, while operating with low power, has made possible a tremendous revolution in computing and communications. The digital signal paradigm representing signals in a discrete-time, discrete-value format has enabled the efficient processing and storage of information such as sound, images and video. However, these signals appear as continuous-time, continuous-value signals, a.k.a. analog signals, in the physical world. To reap the power of digital processing and storage, high performance interfaces between the analog and digital worlds need to be designed. These interfaces capture the signals from various sensors, condition the signals and then convert them to digital; or, convert the digital signal into an analog signal, filter out conversion artifacts and drive actuators. As the performance of the digital signal processing and storage improves, the performance of the interface circuits needs to improve as well.

My research has focused on inventing design techniques and circuit principles to design efficient interfaces for various applications as technology scales. Technology scaling results in important device speed and density improvements for digital circuits. At the same time, it often makes the design of interfaces more difficult, primarily due to the need for a reduced supply voltage or the degradation of analog device performance parameters. Additionally, the improvements in digital performance gained from scaling result in more stringent requirements on the interfaces. These evolutions have led to several paradigm shifts in the field of analog and radio-frequency (RF) circuit design over the past several decades. Whereas many of interface functions being designed remain more or less the same, the implementation of these functions is using totally different principles, architectures and integrated circuit realizations.

An important part of my recent work deals with the problem of designing analog and RF circuits at ultra low supply voltages motivated by the ultra low maximum operating voltages of nanoscale devices, as well as by the desire to understand the fundamental limitations on the reduction of analog or RF supply voltages. A good understanding of the device characteristics is important to guide the designer towards efficient implementations. Part of my work has focused on characterizing and modeling errors between identically designed devices, typically called device mismatches, and their fundamental impact on the performance limits of circuits. Voltage-controlled oscillators are crucial building blocks in many interfaces such as RF receivers and transmitters and high speed digital interfaces, and in the generation of clocks or timing references in general. I have worked on understanding the fundamental trade-offs in the design of these building blocks and on the creation of efficient circuit implementations. Some of my earlier research looked at the implementation of massively parallel analog signal processing in order to obtain very efficient sensor signal processing functions.

The motivation behind all these projects is to enable the design of more efficient interfaces between the analog signals in the physical world and the digital signals or bits of silicon information processing devices while taking advantage of the benefits of technology scaling.

Research Projects

Ultra-low Voltage Analog and RF Integrated Circuits

The line widths of integrated circuit technologies currently used for the design and fabrication of integrated circuits, go from 180nm down to 65nm or even 45nm. Further scaling of these line widths to 32nm, 16nm and, around 2020, down to 9nm is foreseen by the International Roadmap of Semiconductors. As device dimensions scale deep into the nanometer scale, the maximum operating voltages for the devices need to be reduced to well below 1V to keep the electric fields inside the devices sufficiently low for reliable operation. Scaling the supply voltage has also proven to be an effective strategy to cope with the increased power density in highly integrated digital systems; supply voltages down to 0.5V or even 0.3V have been proposed for future systems. Ultra-low supply voltages also occur in circuits that operate on energy scavenged from the environment. For example, a single solar cell will provide a supply voltage between 0.3 and 0.5V. These circuits are used in applications such as sensor networks that are key enablers to the realization of ‘Ambient Intelligence’.

In the majority of analog and RF circuits, a signal is represented as the voltage swing on a particular node or the differential swing between two nodes. The supply voltage scaling thus reduces the maximum signal which makes the effect of impairments such as noise, offsets or interference more prominent and results in a reduction of the accuracy and dynamic range. Furthermore, classical analog design techniques rely heavily on the use of device stacks to improve performance, e.g., by using cascode devices to increase gain, or by using tail-current-source-degenerated differential pairs to help reject common-mode signals. In our research we have investigated novel analog design techniques that avoid device stacks so that ultra-low voltage analog and RF system functions can be built operating from a supply as low as 0.5V.

At the device level we have investigated how the dependence of the threshold voltage on the device length can be used when sizing circuits. We also used forward body biasing to reduce the threshold voltage or control the bias of devices. Traditionally, only the gate, drain and source terminal of a MOS transistor are used, but at ultra-low supply voltages the body terminal can be extensively used to process signals or control the bias without the risk of causing latch-up [1][2][3]. At the building block level we have developed topologies for operational transconductance amplifiers (OTAs) that only require stacks of two devices while still achieving sufficient gain, low common-mode gain and good common-mode rejection [1][2]. These amplifiers have then been used to develop analog functions such as continuous-time filters [1] and track-and-hold amplifiers [4] operating from an ultra-low supply of 0.5V with a dynamic range of close to 60dB.

We have also made contributions towards changing the system level implementation of analog functions in order to make ultra-low voltage operation possible. For example in the continuous-time filter [1] we use variable capacitors tuned with their body source voltage in order to implement continuously-tuneable filters. Switches are particularly difficult to implement at low voltages except if they switch to the supply or ground. For continuous-time delta-sigma modulators, we developed a new digital-to-analog feedback signal scheme named Return-to-Open, that allows to implement highly linear modulators while only needing switches to the supply or ground [3].

Recently, we have gained access to an advanced nanometer CMOS process with line widths of 90nm and have expanded our ultra-low voltage research effort towards higher speed applications including radio-frequency communication circuits. Scaling offers higher intrinsic device speeds which lets us expand the biasing regions we can apply in our circuits while maintaining sufficient speed. However, aggressively scaled devices exhibit substantial leakage currents and we developed a cascaded switching technique that significantly reduces the effects of switch leakage for the sampling operation in pipelined analog-to-digital converters; we demonstrated this improved sampling technique in conjunction with ultra-low voltage operational amplifier design in a 0.5V 8bit 10Msps pipelined ADC [18]. The higher intrinsic

speed of nanometer CMOS devices also enables us to study the design of radio-frequency communication circuits. We have developed ultra-low voltage design techniques for receivers to receive signals in the 2.4GHz ISM band [17]. These receivers operate with low power consumption and can be used in sensor network applications where they can be powered, e.g., from energy scavenging power supplies such as a single solar cell. We further developed a design technique to optimize the speed performance of ultra-low voltage divider circuits and incorporated them into an ultra-low voltage 0.65V 2.4GHz fractional-N frequency synthesizer [16].

This research has received an excellent response from our peers with the acceptance of several papers at the top conferences, like the International Solid State Circuits Conference [8][9][16], the Symposium on VLSI Circuits [14][15][18] and the European Solid State Circuits Conference [7], as well as several regular and invited journal publications in the Journal of Solid State Circuits [1][4] and IEICE Transactions on Electronics [2] which are the prime journals in our field. Additionally, we have been invited for contributions to workshops [10], a book chapter [6], for invited and plenary talks [11][12][13], and for tutorials [19][20]. A summary of a large part of our work will appear as a book published by Springer in the second half of 2007 [5]. This research has further led to the filing of four patent applications [21][22][23][24] and one provisional patent application with the U.S. Patent Office.

Device Mismatch and its Implications for Analog Circuits

Two identically designed components fabricated on the same silicon chip will exhibit small differences in their characteristics. These errors between matched components are referred to as device mismatch. It is an important factor in the design of analog integrated circuits since it can limit many of the performance characteristics of the analog circuits such as accuracy, offset, common-mode rejection, second-order harmonic distortion, etc. Once the devices are fabricated, mismatches are stationary in time, so that in some applications they can be characterized and eliminated through calibration or offset cancellation techniques. Several applications, however, are not amenable to such mismatch-mitigation techniques due to the area overhead involved, or the requirement to periodically interrupt the system operation to characterize the errors.

My involvement with device mismatch started through my Ph.D. work in the area of massively parallel analog signal processing systems [25][26]. These systems borrow some concepts from neural systems but their connectivity is typically limited to specific patterns. I focused on the IC realization of cellular neural networks which have nearest-neighbor connections with programmable weights. The efficient implementation of these systems focuses on the performance trade-offs in terms of speed, power, accuracy and area. At the time, basic models for the understanding of device mismatch had been demonstrated and the dependence of mismatch on device area was known. A trade-off between accuracy and area at the circuit and system level was a direct consequence of this device behavior. This trade-off sets the limit on the number of cells of a massively parallel analog system that could be implemented on a given chip area. I showed that a fundamental link between the speed, power and accuracy of analog computational circuits can further be derived due to the existence of device mismatches [27]. This then results in a mismatch-imposed lower limit on power consumption for a given speed and accuracy that is more restrictive (two or three orders of magnitude) than the limit due to thermal noise.

In more recent work, I further explored these power bounds for analog building blocks and circuits in general. It resulted in number of design guidelines that lead to optimal speed-power-accuracy performance for these building blocks. Both MOS and Bipolar technologies were examined and an overview paper was published in [28]. These mismatch-imposed power bounds are a fundamental limitation for the attainable performance in circuit-level analog signal processing.

During my Ph.D. work I collaborated with fellow graduate students and industrial researchers to accurately characterize and model MOS device mismatches [29][30][31].

Traditionally such device mismatch characterization and modeling work has focused on the DC characteristics of devices. Recently in my group at Columbia, we are investigating the characterization of MOS device mismatches for non-stationary operation to, e.g., estimate the mismatches in delay between different matched circuits. As technology scales, and device sizes reduce, device variation and mismatch become progressively more important. The non-stationary mismatch effects are of significant importance for high-speed analog, RF but also high speed digital circuits. We are currently developing a test strategy based on matched ring oscillators and the associated characterization methods and mismatch models. We will present an invited paper in a special topic session at ISCAS07 [32] and a regular paper at CICC07 [33] with our latest findings. A solid understanding for the matching of the dynamic operation of devices will play a very prominent role for the success of future analog and digital high speed integrated circuit design.

High Performance Integrated Oscillators

At Bell Laboratories, I shifted my research focus to communication circuits, more specifically RF circuits for wireless communications and the design of integrated voltage-controlled oscillators (VCOs). When locked to a low frequency reference signal in a phase-locked loop, they provide accurate timing signals for digital or high speed I/O applications or they provide accurate RF carriers for the reception and transmission of wireless signals. Traditionally RF circuits had been implemented using bipolar transistors in specialized bipolar or BiCMOS IC technologies. In the 1990-ies CMOS RF circuits were actively being researched in academia and industrial research labs to enable the co-integration of the RF, analog and digital functions of communication transceivers in low-cost standard CMOS technologies. Based on my earlier experience with CMOS RF transmitter building blocks [57][58] and integrated inductors [59], I started to work on extending the frequency reach of CMOS VCOs using on-chip LC resonators. Using a design methodology to carefully account for component parasitics, a 4.7GHz and 5.2GHz VCO circuit were developed in a standard digital 0.35um CMOS technology. This circuit significantly extended the operation frequency of CMOS LC VCOs and went beyond an operation frequency of 2GHz for the first time in CMOS. It was presented at the 1998 International Solid-State Circuits Conference [34].

My research further focused on the fundamental trade-offs in oscillator design and I was invited to contribute a talk to AACD99 [35]. In the talk and the associated book chapter [36], a figure of merit (FOM) for an oscillator design was defined. This FOM quantifies the power-noise-operating frequency trade-off in an oscillator. It has since been very widely used in the design community and is nowadays the standard metric to compare oscillator designs.

Due to the advances in technology and the associated speed and complexity increase of digital circuits, more and more functions for communication systems can be realized in the digital domain. However, LC VCOs are crucial RF building blocks that cannot be implemented in the digital domain. Improving the efficiency of their operation is thus essential to enable further scaling of communications circuits. Analysis techniques developed in recent years have brought more insight in some of the VCO noise mechanisms. In recent work at Columbia, we have developed a number of design principles building on, and expanding, these insights to improve the intrinsic noise performance of LC VCOs. In [37], the pulsed biasing principle was introduced, and tail-current-shaping was presented as a compact implementation. A noise improvement better than 3dB (corresponding to a factor-of-two lower noise power) was achieved. This concept was further extended to the design of quadrature oscillators in [38] [39] and offers a compact circuit implementation technique with excellent performance. Other types of pulse biased LC oscillators are currently being researched.

Advances in technology are further leading to a reduction of minimum feature sizes and as a result, to a significant area reduction for digital functions. However, the area of analog and RF circuits is typically constrained by fundamental limits imposed on component values by noise, mismatch or quality factor requirements and is not scaling as strongly. It is thus becoming a progressively more significant part of the total area of highly integrated systems. Integrated

spiral inductors and variable capacitors occupy the largest area in many RF circuits including RF LC VCOs. The area under and around integrated inductors is typically left empty in order to avoid any possible eddy current paths which would degrade the quality of the inductor. We have invented [40] and demonstrated design techniques to put circuits under the integrated inductor without degrading its quality factor and as such reclaim the space [41]. This results in significant area savings, 50% in our VCO prototype, and much larger savings can be expected in large RF circuits with many spiral inductors. We have also investigated the design of compact oscillators taking advantage of the scaling of components in nanometer CMOS technologies and in [42] have demonstrated an LC VCO for I/O applications in 90nm CMOS with the size of about two bond pads.

Our work has received very good reception with our peers and we will present an invited paper with an overview of our techniques at the Custom Integrated Circuits Conference [43].

Multi-phase oscillators have many applications and the multi-stage topology of integrated ring oscillators offers a natural way to implement them. Moreover, ring oscillators are very compact, especially compared to multi-phase oscillators built with multiple LC tanks whose large area is a significant cost limitation in scaled technologies. The phase noise of ring oscillators is however excessive for most communication applications. In [44][45] we invented a technique to combine the advantages of the low phase noise of a single-phase LC oscillator with the multi-phase capabilities of ring oscillators. The ring oscillator's noise is suppressed by injection locking it to the LC oscillator and accurate multi-phase signals are obtained. We proved that the phase accuracy is improved when using a cascade of injected ring oscillators.

The interest in applications for injection locking of integrated ring oscillators has been increasing in recent years. Models for injection locking of harmonic oscillators, such as LC oscillators, are well established using frequency domain techniques, but the injection locking of ring and relaxation oscillators was poorly understood. I have a research effort in my group developing a new approach to accurately estimate the locking range and to model the locking dynamics in differential and single ended ring oscillators using time-domain modeling techniques [46][47][48].

Ultra-wideband Pulse Radios

In recent years several system level innovations to improve the efficient use of the spectrum for wireless communications have gained wider acceptance with the regulatory agencies such as the Federal Communications Commission. Since 2002, ultra-wide band (UWB) communications have been allowed at frequencies between 3GHz and 10GHz at very low power levels, so that they do not interfere with the existing primary users of those frequency bands. Instead of modulating the information on high power, narrow-band carrier waves, the data is transmitted using short (modulated) pulses of RF energy that occupy an ultra-wideband spectrum. I am currently co-editing a book on ultra-wideband techniques which is scheduled to appear in the second half of 2007 [49].

We are investigating the efficient realization of such 'pulse radio' systems from the architectural down to the component level. Ultra-wideband systems have the unique challenge of requiring very wideband circuit design while maintaining low noise as well highly linear circuit operation. At the component level, we have introduced a design technique for the optimization of distributed amplifiers towards high dynamic range performance while maintaining a compact circuit area [50]. At the architectural level, we have developed a digital UWB architecture. The different RF pulse basis waveforms needed in the transmitter and receiver for communication in different subbands of the spectrum and to represent different data symbols, are stored in digital memories. This architecture allows for a very precise control of the pulse characteristics and for exceptionally fast switching between different pulse shapes (and thus different parts of the UWB spectrum) without requiring any changes in the up- and downconversion carrier frequencies or clock frequencies. Several architectural and circuit level innovations have further been implemented to eliminate challenges due to sampling images in the receiver and transmitter [51].

The ether is a shared resource and signals from other users operating in the same part of the frequency spectrum can be very strong and mask the reception of a weak wanted signal. This is a standard problem in wireless radio communications, but it is more prominent in ultra-wideband communications due to the use of large bandwidths occupied by primary users, and the use of very low power signals. We have developed a unique system solution to this challenge using a fast, low power and compact spectrum scanning circuit that detects large interfering signals [52]. This information is used by the communication controller to quickly jump to empty parts of the spectrum to avoid the interference which is possible thanks to our digital based agile receiver and transmitter architecture. A prototype system implementation based on a custom designed receiver, transmitter and interference detector is currently in fabrication.

Earlier Work

Part of my earlier research work has been on massively parallel analog signal processing systems for sensor signal processing [26][53]. Besides deriving fundamental speed-accuracy-power and area trade-offs due to the effects of device mismatches, as mentioned earlier, I also studied in detail the sensitivity of these parallel systems to mismatch and other implementation imperfections [54][55]. Several prototype implementations applied to image sensor [56] and tactile sensor signal processing [25] were demonstrated.

My research has further led to a number of contributions in the design of several other RF building blocks. I designed the first CMOS up-conversion mixer for RF applications [57][58]. My work was part of a larger effort at the K.U.Leuven to develop CMOS RF transceivers at a time where RF circuits were designed with bipolar devices. This work was widely recognized, resulting in a number of invited presentations [60][61]. At Bell Labs, part of my research focused on the design of high speed frequency dividers which are an important building block for phase-locked loop and besides a publication [62], this work also led to two patents [63][64].

I have worked in an industrial environment for 6 years after completing my Ph.D., first in research at Bell Laboratories and then in product IC design at Broadcom, Celight and Multi-Link. Some of the research work has led to publications whereas other contributions have only been made public through patents. At Broadcom I was involved in the design of an integrated 50MHz-850MHz CMOS receiver for TV channels for use in cable modems. The IC was very successful in the market place and several million have been sold. We also worked on the digital implementation of TV demodulators [65]. At Celight, a start-up company, I led the custom VLSI design activities and was a key contributor to the architecture definition of a high capacity optical data-transport system using phase-modulated light signals [66][67]. As an early employee and part of the management, I also participated in the growth and organization of the company, raising of venture capital and customer interactions. At Multi-Link, I participated in the design of a high speed backplane communication transceiver.

Conclusion

Four decades of aggressive scaling of the dimensions of transistors on semiconductor chips has brought about exponential improvements in integrated circuit speed, density and cost reduction. The benefits of the device scaling can only be reaped through the development of adequate circuit design techniques that take advantage of the scaled devices, while avoiding important impairments associated with scaling. The resulting circuits are at the heart of the sophisticated computing and communication devices that empower our information society. My research contributions help to enable the design of high performance analog and radio-frequency interfaces that connect the digital core of communication and computing devices to the real physical world. The foreseen continued scaling with several orders of magnitude of silicon-device performance, as well as the expected introduction of novel device paradigms to continue scaling beyond the limits of current technologies, provide exciting prospects for significant challenges and opportunities for integrated circuit and systems research in the upcoming decades.

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