IEEE JOURNAL OF SOLID STATE CIRCUITS

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Article Information

1. **Design of a High Performance 2-GHz Direct-Conversion Front-End With a Single-Ended RF Input in 0.13 mum CMOS**
Yiping Feng; Takemura, G.; Kawaguchi, S.; Kinget, P.
Solid-State Circuits, IEEE Journal of
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Digital Object Identifier 10.1109/JSSC.2009.2015824
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2. **A 1 GHz Bandwidth Low-Pass $Delta Sigma$ ADC With 20–50 GHz Adjustable Sampling Rate**
Hart, A.; Voinigescu, S.P.
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Digital Object Identifier 10.1109/JSSC.2009.2015852
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3. **Measurements and Analysis of Process Variability in 90 nm CMOS**
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4. **A Fully Integrated 0.13- mum CMOS 40-Gb/s Serial Link Transceiver**
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5. **A 0.13 mu m CMOS Quad-Band GSM/GPRS/EDGE RF Transceiver Using a Low-Noise Fractional-N Frequency Synthesizer and Direct-Conversion Architecture**
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8. **A Low Jitter Programmable Clock Multiplier Based on a Pulse Injection-Locked Oscillator With a Highly-Digital Tuning Loop**
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