PRESS KIT

2007

ISSCC
VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and use to maintain technical currency, and to network with leading experts.

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ISSCC 2007
EXECUTIVE SUMMARY

- **Activities**
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- **Significant Results**

EXECUTIVE SUMMARY

ACTIVITIES AT ISSCC 2007

- Tutorials presented Sunday, February 11:
  - 10 independent lectures presented by experts from each of the ISSCC 2007 Program Subcommittees: Analog, Data Converters, Digital, Imagers, Medical, MEMS and Displays, Memory, RF, Signal Processing, Technology Directions, Wireless, and Wireline.

- Circuit-Design Forums presented Sunday, February 11 and Thursday, February 15:
  - 7 informal all-day interaction in which circuit experts exchange information on their current research.

- Short Course presented Thursday, February 15:
  - 4 linked 90-minute lectures given by experts in the field

- Technical Paper Sessions presented Monday through Wednesday, February 12 to 14:
  - 3 presentations in the Plenary Session on Monday morning
  - 31 paper sessions beginning Monday afternoon and continuing through Wednesday afternoon
  - 182 regular-length papers
  - 52 short papers

- Evening Sessions presented on Sunday, Monday and Tuesday evenings
  - 7 Special-Topic Sessions
  - 2 Panel-Discussion Sessions
  - Social Hours on Monday and Sunday evenings after the paper sessions.

CONFERENCE THEME

"The 4 Dimensions of IC Innovation"

This theme explores the synergism between the various dimensions of integrated circuits: The continued growth of Moore's Law has pushed integrated circuits – their creation, fabrication, and application – from the micro-electronic into the nano-electronic era. This transition has created tremendous opportunities for higher-density higher-performance lower-power circuits and systems, creating cost-effective solutions for ubiquitous communications, computation, sensing, display, consumer electronics, and multimedia. However, the advent of the nano-era has blurred the traditional boundaries between the four dimensions of IC innovation: technology, devices, circuits, and system architecture. In fact, innovation in solid-state circuits requires an intricate balance between advances in process, circuit, architecture and system technology. Authors were encouraged to submit novel circuit concepts, and systems, that explore the interrelationships among the four dimensions of IC innovation.

Significant Results

Analog

- Fractional-N frequency synthesizer in 90nm CMOS runs at 2.5GHz on a 0.65V supply **[17.2]**
- CMOS hybrid-switching amplitude-modulator delivers 2W for EDGE polar transmitter **[29.1]**
- Very-power-efficient ADSL 2+ Central-Office line driver **[29.4]**
- 3GHz 90nm CMOS embedded-switching DC-to-DC converter uses charge-recycling from SoC clock-tree **[29.8]**

Data Converters

- 90nm implementations dominate the converter papers.
  [13.1, 13.3, 13.5, 25.1, 25.2, 25.3, 25.4, 25.7]
- Successive-Approximation-Register (SAR) A/D-converter topologies operate at 40MS/s.
  [13.5, 13.6]

Digital

- More than one TFLOP from a single chip **[5.2]**
- Quad-core chips with independent core-frequency control. **[5.3, 5.4]**
- Eight-core microprocessor with 64 threads. **[5.7]**
- Low-energy interconnects **[22.8, 22.9]**

Imagers, MEMS, Medical and Displays

- Single component combining display and image-sensing enables touch-screen and biometrics **[7.2]**
- Retinal stimulator realized in 0.35µm HV CMOS providing 232 channels with programmability, testability, and safety features **[8.1]**
- 8.1 Mpixel sensor with smallest commercially-available (1.75µm) pixel **[28.5]**

Significant Results (continued)

Memory

- Ultra-low-leakage SRAMs in 65nm, with 2pA/b at retention voltage, using integrated leakage-reduction schemes **[18.2]**
- SRAMs penetrate subthreshold regime with 6T, 8T, and 10T architectures **[18.4, 18.5, 18.6]**
- PRAM breaks new records with 512Mb density, and 266MB/s throughput **[26.1]**
- First high-performance 65nm embedded DRAM in SOI **[27.1]**

RF

- Millimeter-wavelength (60GHz) combined with milliwatt power consumption demonstrated by CMOS receiver front-ends [**10.1, 10.2]**
- CMOS on-chip voltage-controlled oscillators (VCOs) break the100GHz barrier, with the demonstration of a Colpitts oscillator **[10.7]**
- Clever re-use of a delay-line significantly reduces size and cost of a steerable-beam antenna for radio imaging **[23.5]**
- Highly integrated silicon-based radar IC at 79GHz **[23.7]**

Signal Processing

- GSM baseband radio integrates power-management circuits and memory with RF, digital, and analog baseband functions **[14.6]**
- First-reported 3x3 MIMO PHY/MAC processor **[14.7]**
- First implementation of a real-time 3D-display processor with a programmable 3D-graphics-rendering engine **[15.4]**

Technology Directions

- First microsystem combining energy scavenging from thermal and RF sources **[3.1]**
- First closed-loop system tracking the minimum-energy operating voltage with embedded high-efficiency DC-to-DC converter **[3.2]**
- Complementary-type carbon nanotube transistors are demonstrated, enabling CMOS-like logic gates **[3.4]**
- An ultra-thin (< 300μm) e-paper display with high-speed response (< 0.2ms) is demonstrated **[3.7]**
- Lowest-power capacitive chip-to-chip interconnect, uses 0.08pJ/b **[20.1]**
- See-through imaging camera using passive detection of millimeter and submillimeter waves, with amplifiers operating up to 300GHz **[32.3]**

Significant Results (continued)

Wireless

- An all-digital 90nm CMOS ultra-low-energy (47pJ/Pulse) UWB transmitter **[6.4]**
- The first direct-conversion cable-TV tuner chip covering the entire 48 to 860MHz band, using no external filters **[11.1]**
- Single-chip transceivers for multi-class global RFID readers **[11.5, 11.6]**
- A MEMS-enabled fully-reconfigurable Software-Defined-Radio transceiver in 130nm CMOS **[19.6]**
- The first fully-integrated dual-band CMOS direct-conversion MIMO transceiver for 802.11n/EWC, capable of supporting > 270Mb/s PHY rate **[31.2]**

Wireline

- A fully-integrated 4x10Gb/s DWDM optoelectronic transceiver in standard 0.13μm CMOS SOI **[2.1]**
- A 72mW 0.03mm^2 inductorless 40Gb/s CDR in 65nm SOI CMOS **[12.3]**
- A 14mW 6.25Gb/s transceiver in 90nm CMOS for serial chip-to-chip communication **[24.3]**
- Performance variability of a 90GHz static CML frequency divider in 65nm CMOS SOI **[30.3]**

NOTES

ISSCC 2007
CONFERENCE OVERVIEW

- **Events**
- **Paper Statistics**
- **Plenary Session**
- **Technical Highlights**
- **Discussion Sessions**
- **Short Course**
- **Tutorials**
- **Advanced-Circuit-Design Forums**

EVENTS

TUTORIALS (SUNDAY, FEBRUARY 11, 2007)

- **10** 90-minute Tutorials, each taught twice, by circuit experts from the Program Committee, serve to meet attendees' needs for introductory material in circuit specialties.

CIRCUIT-DESIGN FORUMS
(SUNDAY, FEBRUARY 11 AND THURSDAY, FEBRUARY 15, 2007)

- **7** circuit experts exchange information on their current research in an all-day informal environment.

TECHNICAL SESSIONS (MONDAY TO WEDNESDAY, FEBRUARY 12 TO 14, 2007)

- **Three invited talks** presented in the Plenary Session and **234 technical papers** presented in **31** Regular Sessions, highlight the latest circuit developments.

EVENING SESSIONS
(SUNDAY, MONDAY & TUESDAY, FEBRUARY 11 TO 14, 2007)

- **7** Special-Topic presentations, in which experts provide insight and background on a subject of current importance.
- **2** Panels in which experts debate a selected topic and field audience questions in a semi-formal atmosphere.

SOCIAL HOURS (MONDAY AND TUESDAY, FEBRUARY 12 AND 13, 2007)

- Network with experts in a wide range of circuit specialties; meet colleagues in an informal exchange; browse the technical-book exhibits!

SHORT COURSE (THURSDAY, FEBRUARY 15, 2007)

- Intensive All-Day Course on a single topic, taught by world-class instructors, can serve to "jump start" a change in an engineer's circuit specialty.

PAPER STATISTICS

OVERALL:

- **3** invited plenary papers
- **637** papers submitted to ISSCC 2007
- **234** papers accepted, including:
  - **91** papers from North America, including
    - **47** Industry papers
    - **44** University papers
  - **73** papers from the Far East, including
    - **32** Industry papers
    - **41** University papers
  - **70** papers from Europe, including
    - **36** Industry papers
    - **34** University papers
- **32** Sessions, over 3 days

INTERNATIONAL SCOPE:

- Americas: **39 %**
- Far East: **31 %**
- Europe: **30 %**

WIDE COVERAGE:

- Analog **7**%
- Data Converters **7 %**
- Digital **13 %**
- Imagers, Medical, MEMS & Displays **12**%
- Memory **8 %**
- RF **10 %**
- Signal Processing **6 %**
- Technology Directions **12 %**
- Wireless **12 %**
- Wireline **13 %**

PLENARY SESSION

[1.1] "Foundry Future: Challenges in the 21st Century",

Morris Chang
Founding Chairman
Taiwan Semiconductor Manufacturing Corporation
Hsinchu, Taiwan

- Silicon Foundries have become an integral part of the overall semiconductor supply-chain, accounting for over 20% of all wafer production.
- The Foundry business-model has been an important contributor to the health of the IC industry.
- Challenges facing the foundry industry will be described: (1) To ensure continuous growth; and (2) To maintain profitability in an increasingly more-competitive environment.
- Foundries need to expand into the IC-product market by offering a broadening range of technologies.
- Circuit designers can expect an expanded range of process- technology options tailored to various applications, such as memory, analog, high-performance-logic, image-sensors, and CMOS logic.
- Deeper and broader relationships with customers are needed, covering both design and technology engineering to allow for increasing demands fo product-cost-performance and reduced time-to-market.

[1.2] Analog and Mixed-Signal Innovation: The Process-Circuit-System-Application Interaction

Lewis Counts
Vice-President of Analog Technology and Fellow
Analog Devices
Wilmington, MA

- Analog and mixed-signal electronics becomes increasingly important to the continued growth of the IC industry.
- Designers need to exploit, more and more, the potential of process technology, in order to design circuits that minimize the impact of process variations on product performance.
- Typical examples will be reviewed of circuit techniques that have allowed the production of high-precision amplifiers and data converters.
- Process scaling has been the driving force behind a wide variety of advanced products, including multi-media cell phones, imaging systems, and sophisticated wireless systems. Analog and mixed-signal subsystems are critical in support of these advanced applications.
- A creative combination of process, design, and system architecture are more crucial than ever to ensure GHz speeds, minimizing power, and integrating multiple systems in smaller packages.

PLENARY SESSION (CONTINUED)

[1.3] "Toward a New Nanoelectronic Cosmology"

Joël Hartmann
Director, Crolles2 Alliance
STMicroelectronics, Crolles, France

- As scaling moved into the nanometer dimensions, devices performance has become difficult to predict, while performance has degraded due to leakage and dispersion.

- Increased parameter variability has caused a significant discrepancy between simulation and measurement results. This effect has become pervasive at all levels and in all segments of the IC design, including digital circuits.

- A better understanding and improved modeling of the underlying physical causes of variability is urgently needed to guarantee acceptable levels of performance, manufacturability, and yield, while feature sizes continue to shrink.

- The tight coupling between seemingly-independent dimensions of design, force the creation of a new nano-cosmology, where global optimization results from a delicate balance between process, device, and system, aspects.

- An emerging concept of Generalized Design-for-Manufacturability unifies conventional Design-for-Manufacturability, Manufacturing-for-Design, and Design-for-Yield. Tightly-coupled physical-electrical-mechanical modeling and simulation will allow early evaluation of the impact of design choices at all levels.

Technical Highlights

Analog

- Adaptive cancellation technique lowers phase noise in 2.4GHz ISM-band PLL **[17.1]**
- Fractional-N frequency synthesizer in 90nm CMOS runs at 2.5GHz on a 0.65V supply **[17.2]**
- Clock PLL in 65nm PD-SOI CMOS achieves 18GHz operation with a 1V supply **[17.6]**
- CMOS hybrid-switching amplitude-modulator delivers 2W for EDGE polar transmitter **[29.1]**
- Very-power-efficient ADSL 2+ Central-Office line driver **[29.4]**
- 3GHz 90nm CMOS embedded-switching DC-to-DC converter uses charge-recycling from SoC clock-tree **[29.8]**

Data Converters

- 90nm implementations dominate the converter papers. **[13.1, 13.3, 13.5, 25.1, 25.2, 25.3, 25.4, 25.7]**
- Oversampling-converter topologies allowing multimode operation to allow a single converter to handle multiple radio standards. **[13.1, 13.2, 13.3, 13.4]**
- Successive-Approximation-Register (SAR) A/D-converter topologies operate at 40MS/s. **[13.5, 13.6]**
- 90nm converter circuits are being designed to operate with 1V power supplies. **[25.1, 25.2, 25.3, 25.4, 25.7]**
- New topologies for low-voltage converters. **[25.2, 25.3, 25.4]**

Digital

- Dual-core microprocessor with 5GHz clock **[5.1]**
- More than one TFLOP from a single chip **[5.2]**
- Quad-core chips with independent core-frequency control. **[5.3, 5.4]**
- Eight-core microprocessor with 64 threads. **[5.7]**
- 40GHz all-digital clock generator in 90nm CMOS **[9.4]**
- Inductively-loaded standing-wave clock generator at 12GHz **[9.5]**
- Managing processor variation for power, performance, and reliability **[16.1, 16.4, 16.6, 22.1]**
- Low-energy interconnects **[22.8, 22.9]**

Technical Highlights (continued)

Imagers, MEMS, Medical and Displays

- Low-Temperature-Polysilicon Active-Matrix OLED display with integrated 8b/color DAC and driver **[7.1]**
- Single component combining display and image-sensing enables touch-screen and biometrics **[7.2]**
- Retinal stimulator realized in 0.35µm HV CMOS providing 232 channels with programmability, testability, and safety features **[8.1]**
- Advances in power and noise figures for implantable deep-brain neural-recording implant **[8.6]**
- Single-chip micro-compass with industry-standard SPI serial readout **[21.2]**
- MEMS gyroscope achieves the highest-reported accuracy of 0.2° per hour **[21.4]**
- 8.1 Mpixel sensor with smallest commercially-available (1.75µm) pixel **[28.5]**

Memory

- Clock for 65nm SRAMs for CELL processor targets 6GHz **[18.1]**
- Ultra-low-leakage SRAMs in 65nm, with 2pA/b at retention voltage, using integrated leakage-reduction schemes **[18.2]**
- SRAMs penetrate subthreshold regime with 6T, 8T, and 10T architectures **[18.4, 18.5, 18.6]**
- PRAM breaks new records with 512Mb density, and 266MB/s throughput **[26.1]**
- First 1.8V 1G Multi-Level NOR Flash memory in 65nm, with fastest read and write throughput **[26.3]**
- Largest-capacity (2Mb) Spin-Transfer-Torque-RAM (SPRAM) with optimized performance **[26.5]**
- First high-performance 65nm embedded DRAM in SOI **[27.1]**

RF

- Closed-loop impedance-mismatch-protection circuit for CMOS power amplifiers **[4.2]**
- Feed-forward filtering technique to cancel interferers in a radio receiver **[4.4]**
- Millimeter-wavelength (60GHz) combined with milliwatt power consumption demonstrated by CMOS receiver front-ends [**10.1, 10.2]**
- CMOS on-chip voltage-controlled oscillators (VCOs) break the100GHz barrier, with the demonstration of a Colpitts oscillator **[10.7]**
- SiGe BiCMOS phased-array receiver capable of beamforming (with a phased-array antenna) at 60GHz **[10.8]**

Technical Highlights (continued)

RF *(continued)*

- Novel broadband (10GHz bandwidth) beamforming technique reusing a delay-line, significantly reduces area and cost **[23.5]**
- Clever re-use of a delay-line significantly reduces size and cost of a steerable-beam antenna for radio imaging **[23.5]**
- Highly integrated silicon-based radar IC at 79GHz **[23.7]**

Signal Processing

- GSM baseband radio integrates power-management circuits and memory with RF, digital, and analog baseband functions **[14.6]**
- First-reported 3x3 MIMO PHY/MAC processor **[14.7]**
- First implementation of a real-time 3D-display processor with a programmable 3D-graphics-rendering engine **[15.4]**

Technology Directions

- First microsystem combining energy scavenging from thermal and RF sources **[3.1]**
- First closed-loop system tracking the minimum-energy operating voltage with embedded high-efficiency DC-to-DC converter **[3.2]**
- Complementary-type carbon nanotube transistors are demonstrated, enabling CMOS-like logic gates **[3.4]**
- The advantage of using carbon nanotubes rather than ultra-scaled CMOS transistors is quantified in terms of a maximum 2x better FO4-delay improvement and 30x better average energy-delay product (EDP) **[3.5]**
- An ultra-thin (< 300μm) e-paper display with high-speed response (< 0.2ms) is demonstrated **[3.7]**
- Lowest-power capacitive chip-to-chip interconnect, uses 0.08pJ/b **[20.1]**
- Lowest-power inductive chip-to-chip interconnect uses 0.14pJ/b **[20.2]**
- Adaptive Software-Defined Radios (SDRs) achieve up to 40% lower energy through run-time quality-of-service and energy management **[32.1]**
- See-through imaging camera using passive detection of millimeter and submillimeter waves, with amplifiers operating up to 300GHz **[32.3]**

Technical Highlights (continued)

Wireless

- The first 65nm CMOS WiMedia-compliant UWB transceiver **[6.1]**
- An all-digital 90nm CMOS ultra-low-energy (47pJ/Pulse) UWB transmitter **[6.4]**
- The first direct-conversion cable-TV tuner chip covering the entire 48 to 860MHz band, using no external filters **[11.1]**
- Single-chip transceivers for multi-class global RFID readers **[11.5, 11.6]**
- Direct-conversion linear-uplink WCDMA transmitters requiring no SAW filters **[19.1, 19.2]**
- A MEMS-enabled fully-reconfigurable Software-Defined-Radio transceiver in 130nm CMOS **[19.6]**
- The first Bluetooth EDR SoC implemented in 0.13µm CMOS **[31.1]**
- The first fully-integrated dual-band CMOS direct-conversion MIMO transceiver for 802.11n/EWC, capable of supporting > 270Mb/s PHY rate **[31.2]**

Wireline

- A fully-integrated 4x10Gb/s DWDM optoelectronic transceiver in standard 0.13µm CMOS SOI **[2.1]**
- A fractional-N PLL for SONET-quality clock-synthesis applications **[2.9]**
- A 72mW 0.03mm^2 inductorless 40Gb/s CDR in 65nm SOI CMOS **[12.3]**
- A 7Gb/s 9.3mW 2-tap current-integrating DFE receiver **[12.5]**
- A 12.5Gb/s SerDes in 65nm CMOS using a baud-rate ADC with digital receiver equalization and clock recovery **[24.1]**
- A 14mW 6.25Gb/s transceiver in 90nm CMOS for serial chip-to-chip communication **[24.3]**
- A 16Gb/s Source-Series-Terminated Transmitter in 65nm CMOS SOI **[24.6]**
- Performance variability of a 90GHz static CML frequency divider in 65nm CMOS SOI **[30.3]**

EVENING SESSIONS

SUNDAY

SE1 Digitally-Enhanced Analog & RF

SE2 Circuit Design in the Year 2012

MONDAY

SE3 Last-Mile Access-Options: PON/DSL/Cable/Wireless

E1 Ultimate Limits of Integrated Electronics

SE4 Automotive Signal-Processing Technologies

TUESDAY

SE5 Highlights of IEDM

SE6 Secure Digital Systems

E2 Digital RF – Fundamentally a New Technology or Just Marketing Hype?

SE7 Implantable and Prosthetic Devices: Life-Changing Circuits

SHORT COURSE:

[Thursday, February 15, 2007]

ANALOG, MIXED-SIGNAL, AND RF CIRCUIT DESIGN IN NANOMETER CMOS

COURSE OBJECTIVE:

This Short Course will explain the fundamental limitations faced by those designing such blocks as, amplifiers, mixers, data converters, and phase-locked loops, in nanometer CMOS, and present state-of-the-art circuit and system-level techniques for addressing these limitations. It is intended for both entry-level and experienced engineers.

OVERVIEW:

- **RF Transistor System Design in Nanometer CMOS** [8:00 am; 10:00 am]

  Matt Miller, *Freescale Semiconductor*

- **RF Circuit Design in Nanometer CMOS** [10:00 am; 12 noon]

  Bram Nauta, *University of Twente*

- **Continuous-Time ADCs in Nanometer CMOS** [1:00 pm; 3:00 pm]

  Michiel S.J. Steyaert, *Katholieke Universiteit Leuven*

- **Frequency Synthesizers in Nanometer CMOS** [3:00 pm; 5:00 pm]

  Robert Bogdan Staszewski, *Texas Instruments*

TUTORIALS:

[Sunday, February 11, 2007]

T1 **Embedded Power-Management Circuits** [12:30 pm; 2:30 pm]
(***Philip K.T. Mok***, *Hong Kong University of Science & Technology*)

T2 **Continuous-Time $\Delta\sum$ Data Converters** [8:00 am, 10:00 am]
(***Yiannos Manoli***, *University of Freiburg*)

T3 **Dealing with Issues in VLSI Interconnect Scaling** [12:30 pm; 2:30 pm]
(***Ron Ho***, *Sun Microsystems*)

T4 **Dynamic-Offset Cancellation Techniques in CMOS** [8:00 am, 10:00 am]
(***Kofi A.A. Makinwa***, *Delft University of Technology*)

T5 **Error-Correcting Codes for Memories** [12:30 pm; 2:30 pm]
(***Takayuki Kawahara***, *Hitachi*)

T6 **CMOS Front-End-Circuit Design** [12 :30 pm ; 2 :30 pm]
(***Marc Tiebout***, *Infineon*)

T7 **Vector Processing as an Enabler for Software-Defined Radio in Handsets** [8:00 am, 10:00 am]
(***Kees van Berkel***, *NXP Research*)

T8 **Organic-Transistor Circuit Design** [8:00 am; 10:00 am]
(***Takayasu Sakurai***, *University of Tokyo*)

T9 **Radio Design for MIMO Systems with an Emphasis on IEEE 802.11n** [12:30 pm; 2:30 pm]
(***Arya Behzad***, *Broadcom*)

T10 **Fundamentals of Electronic Dispersion Compensation [**8:00 am, 10:00 am]
(***Naresh Shanbhag***, *University of Illinois at Urbana-Champaign*)

FORUM:

F1 Non-Volatile-Memory Circuit Design and Technology

[SUNDAY, FEBRUARY 11, 2007, 8:00 AM]

TOPICS & SPEAKERS:

- Introduction and Overview
  *(**Mark Bauer**, Intel)*
- Non-Volatile Memory Technology: Present and Future Trends
  *(**Al Fazio**, Intel)*
- NOR Flash Memory Design
  *(**Kerry Tedrow**, Intel)*
- NAND Flash Memory Design
  *(**Tomoharu Tanaka**, Micron)*
- NROM Memory Design
  *(**Yair Sofer**, Saifun Semiconductors)*
- Embedded Flash Memory Design
  *(**Hideto Hidaka**, Renesas)*
- Circuits and Design Challenges for Alternative and Emerging NVM
  *(**Shine Chung**, TSMC)*
- Non-Volatile Memory Applications
  *(**Koji Sakui**, Sony)*

FORUM:

F2 Design of 3D-Chipstacks

[SUNDAY, FEBRUARY 11, 2007, 8:00 AM]

TOPICS & SPEAKERS:

- Introduction
  *(**Werner Weber**, Infineon)*

- Status, Opportunities and Trends of 3D Integration by Thru-Silicon-Via Stacking
  *(**Harry Hedler**, Qimonda)*

- New Three-Dimensional Integration Technologies Based on Water-to-Water and Chip-to-Water Bonding Methods
  *(**Mitsumasa Koyanagi**, Tohoku University)*

- Heat Removal and Power Delivery for 3D SoC
  *(**Muhannad Bakir**, Georgia Institute of Technology)*

- CMOS Proximity Wireless Communications of SiP Integration
  *(**Tadahiro Kuroda**, Keio University)*

- Applications of 3D Integration
  *(**Dan Radack**, DARPA)*

- Is 3D the Next Big Thing in Microprocessors?
  *(**Wilfried Haensch**, IBM)*

- 3D Design Opportunities and Challenges for Microprocessors
  *(**Bryan Black**, Intel)*

- 3D Chip Stacking Technology for Memory Device
  *(**Dong-Ho Lee**, Samsung)*

- 3D System-in-Package Integration of Wireless Sensor Nodes
  *(**Bert Gyselinckx**, IMEC)*

- Performance and Cost Trade-Offs for SoC, SoP and 3D Integration
  *(**Hannu Tenhunen**, Royal Institute of Technology)*

FORUM:

F3 GIRAFE: Power-Amplifiers and Transmitter Architectures

[SUNDAY, FEBRUARY 11, 2007, 8:00 AM]

TOPICS & SPEAKERS:

- Welcome
  *(**Rudolf Koch**, Infineon)*

- Introduction and Basics
  *(**David Su**, Atheros Communications)*

- Transmit Architectures and Power Amplifier Requirements
  *(**Earl McCune,** Panasonic)*

- Power Amplifier Concepts
  *(**David Pehlke**, Silicon Labs)*

- Power Supply Modulation Techniques for Power Amplifier Efficiency Enhancement
  *(**Lawrence Lawson**, University of California, San Diego)*

- Overview of Power Amplifier and Front-End Module Technologies and Solutions
  *(**Gene Tkachenko**, Skyworks Solutions)*

- Fully Integrated CMOS Power Amplifiers for Mobile Wireless Communications
  *(**Ali Hajimiri**, California Institute of Technology)*

FORUM:

F4 Noise in Imaging Systems

[THURSDAY, FEBRUARY 15, 2007, 8:00 AM]

TOPICS & SPEAKERS:

- Welcome and Overview
  *(**Albert Theuwissen**, DALSA)*
- The 4 Dimensions of Noise
  *(**Takao Kuroda**, Panasonic)*
- kT/C Noise
  *(**Boyd Fowler,** Fairchild Imaging)*
- Noise at the Device Level
  *(**Bedrabata Pain**, JPL)*
- Noise at the Circuit Level
  *(**Shoji Kawahito,** Shizuoka University)*
- Noise at the System Level
  *(**Rick Baer**, Micron Technology)*
- Perception of Noise in Imagery
  *(**Jim Larimer,** ImageMetrics)*
- Noise Reduction
  *(**Aleksandra Pizurica**, Ghent University)*

FORUM:

F5 ATAC: Automotive Bus Systems

[Thursday, February 15, 2007, 8:00 am]

TOPICS & SPEAKERS:

- Welcome and Introduction
  *(**Wolfgang Pribyl**, Graz University of Technology)*

- Overview of Systems and Standards
  *(**Herman Casier**, AMI Semiconductor)*

- The New BMW X5 – Criteria for Bus System Selection and Optimization
  *(**Martin Peteratzinger,** BMW)*

- The Physical Layer of LIN- and CAN-Bus, Driven by Cost and Automotive Requirements
  *(**Geert Vandensande**, AMI Semiconductor)*

- Physical Layer of the Flexray Bus, Characteristics & Design Considerations
  *(**Harald Gall,** austriamicrosystems)*

- Protocols & Processors for Bus Systems, Example Flexray
  *(**Shunichi Ko**, Fujitsu)*

- The MOST Network for the Multimedia Enabled Automobile
  *(**Dave Knapp,** SMSC)*

- Safety and Dependability – A System Perspective
  *(**Stefan Poledna**, TTTech & Vienna University of Technology)*

FORUM:

F6 Adaptive Techniques for Dynamic Processor Optimization

[Thursday, February 15, 2007, 8:00 am]

TOPICS & SPEAKERS:

- Welcome and Overview
  *(**Shannon Morton**, Icera)*

- Technology Challenge of Adaptive Techniques
  *(**David Scott,**, Texas Instruments)*

- Adaptive Body Bias Techniques for Low Power SoC
  *(**Koichiro Ishibashi,** Renesas)*

- Adaptive Control for High End Processor Power Management
  *(**Thomas Pflüger**, IBM)*

- Processor Support for Advanced Power & Thermal Management Techniques in Multi-Core Environments
  *(**Mike Clark,** AMD)*

- Adaptive Architectural Techniques and the Hardware/Software Interface
  *(**Dave Blaaw,** University of Michigan)*

- The Challenges of Testing Adaptive Techniques
  *(**Eric Fetzer,** Intel)*

FORUM:

F7 Low-Voltage Analog-Amplifier Design for Filtering and A/D Conversion

[Thursday, February 15, 2007, 8:00 am]

TOPICS & SPEAKERS:

- Welcome and Introduction
  *(**Peter Kinget**, Columbia University)*

- Critical OpAmp Design Aspects for Low-Voltage Active RC Filters
  *(**Andrea Baschirotto**, University of Lecce)*

- True Low-Voltage OTAs for 0.5V Active Filter,s THAs and CT $\Delta\Sigma$ Converters
  *(**Peter Kinget,** Columbia University)*

- Switched-R Applications of Low-Voltage Amplifiers
  *(**Un-Ku Moon**, Oregon State University)*

- Low-Noise Optimization for Low-Voltage Amplifiers
  *(**Willy Sansen,** Katholieke Universiteit Leuven)*

- Low Voltage Multi-Stage Amplifiers
  *(**Johan Huijsing**, Technische Universiteit Delft)*

- Calibration Techniques for Low-Voltage Amplifier Non-Idealities in Pipelined ADCs
  *(**Jieh-Tsorng Wu,** National Chiao-Tung University)*

- Low-Voltage Analog Front-End for Digital Hearing Aids
  *(**Alexander Heubi**, AMIS)*

- Performance Motivated Low-Voltage Analog Circuit Design
  *(**Corey Petersen**, Analog Devices)*

ANALOG

- **Overview**
- **Featured Papers**
- **Special-Topic Session**
  (co-sponsored by Analog/Data Converters/RF)
- **Tutorial**
- **Forum**
  (co-sponsored by Analog/Data Converters)
- **Short-Course**
  (co-sponsored by Analog/Data Converters)

ISSCC 2007 – ANALOG

Subcommittee Chair: *Bill Redman-White, NXP Semiconductors, and Southampton University, UK*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- Adaptive cancellation technique lowers phase noise in 2.4GHz ISM-band PLL **[17.1]**
- Fractional-N frequency synthesizer in 90nm CMOS runs at 2.5GHz on a 0.65V supply **[17.2]**
- Clock PLL in 65nm PD-SOI CMOS achieves 18 GHz operation with a 1V supply **[17.6]**
- CMOS hybrid-switching amplitude-modulator delivers 2W for EDGE polar transmitter **[29.1]**
- Very-power-efficient ADSL 2+ Central-Office line driver **[29.4]**
- 3GHz 90nm CMOS embedded-switching DC-to-DC converter uses charge-recycling from SoC clock-tree **[29.8]**

APPLICATIONS AND ECONOMIC IMPACT

- Lower phase noise and lower power consumption for radio links operating in the ISM bands **[17.1]**
- Viability of continued supply-voltage scaling into the next decade of Moore's law. **[17.2]**
- Faster clocks possible, for more-powerful computers **[17.6]**
- Cellular talk-time will be increased by ~2X **[29.1]**
- Battery size can be reduced **[29.1]**
- Phone form-factor can be reduced since heat generated is reduced **[29.1]**
- Rack size can be significantly reduced **[29.4]**
- Overall system cost is reduced due to decreased number of power supplies **[29.4]**
- More line drivers per board **[29.4]**
- Energy efficiency improved **[29.8]**
- System area reduced **[29.8]**

SPECIAL-TOPIC SESSION *(co-sponsored by Analog/Data Converters/RF)*

DIGITALLY-ENHANCED ANALOG & RF [SE1]

Challenging behavior of nanometer CMOS transistors makes traditional analog-design techniques hard to sustain. However, taking advantage of what the technology does best, employing embedded digital-signal-processing, control and calibration techniques enhances analog solutions with performance-yield, and design-time improvements.

TUTORIAL

Embedded Power-Management Circuits [T1]

Due to the drastic increase in system integration and power consumption of an IC with technology scaling, power management becomes a critical issue in determining the overall performance of an IC. This Tutorial starts with a brief overview of power-management circuits for embedded applications, and then deals with the operational and design issues associated with various on-chip power-converter circuits**.**

FORUM *(co-sponsored by Analog/Data Converters)*

Low-Voltage Analog-Amplifier Design for Filtering and A/D Conversion [F7]

The increased use of battery-powered devices motivates the push toward lower supply voltages in mobile applications. While threshold voltages in nanometer CMOS processes are not significantly lower, the net usable voltage range for signal swing, biasing, and device stacking, is substantially reduced. As a result, amplifier performance (e.g., speed, gain, and noise) is compromised, which then requires adjustments in the systems where they are applied. This Forum deals with specialist techniques addressing low-voltage-amplifier design for a range of key functions in mixed-signal SoCs.

SHORT COURSE *(co-sponsored by Analog/Data Converters)*

Analog, Mixed-Signal, and RF Circuit Design in Nanometer CMOS [Thursday, February 15]

This Short Course includes a session on Continuous-Time Delta-Sigma ADCs, by Michiel Steyaert of Katholieke Universitet, Leuven.

Timing Circuits

A Wide-Bandwidth 2.4GHz ISM-Band Fractional-N PLL with Adaptive Phase-Noise Cancellation [17.1]

UCSD

A 0.65V 2.5GHz Fractional-N Synthesizer in 90nm CMOS [17.2]

Columbia University

A 1V 18 GHz Clock Generator in a 65nm PD-SOI Technology [17.6]

IBM

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Fractional-N Phase-Locked Loops suffer from quantization noise due to the delta-sigma modulator. In order to keep the spectrum clean, one needs a low-bandwidth PLL, with disadvantages such as slow settling time, and large jitter from the Voltage-Controlled Oscillator. **[17.1]**
- As transistors are shrunk to nanometer sizes, tradeoffs are made which require the use of progressively-lower power-supply voltages (e.g., 1V, and below). This makes analog circuits, such as Phase-Locked Loops complex to design.
- Processors require higher and higher clocking speeds. Key building block to reach these high speeds are Phase-Locked Loops, which run at the speed limits of the technology.

NOVEL CONTRIBUTIONS

- Use of an adaptive technique to cancel the noise generated by the delta-sigma modulator, over a wide loop bandwidth (730kHz) **[17.1]**
- A Phase-Locked Loop is able to operate from a supply voltage as low as 0.65V, while major parts of the circuit can even work at 0.5V with a competitive performance at 2.5GHz. **[17.2]**
- Thanks to this architecture, the clocking speed can be increased up to 18GHz in 65nm SOI technology, without the need for integrated (and thus costly) inductors **[17.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- Provides lower phase noise and lower power consumption for radio links operating in the ISM bands **[17.1]**
- Demonstrates viability of continued supply-voltage scaling into the next decade of Moore's law. **[17.2]**
- Makes faster clocks possible in more-powerful computers **[17.6]**

Convergence of Power, Analog, and RF

A 2W CMOS Hybrid-Switching Amplitude-Modulator for EDGE Polar Transmitters [29.1]

KAIST, Magna Chip Semiconductor

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Talk-time is limited by the low power efficiency of the transmitter
- Present linear amplifiers for EDGE transmission use lots of power
- Polar Modulation brings efficiency improvement, but requires challenging power-supply control

NOVEL CONTRIBUTIONS

- Convergence of power, analog, and RF techniques in new polar modulator opens the way for high efficiency and extended talk-time for mobile transmitters **[29.1]**
- The combination of linear and switching regulation to deliver the required power envelope improves the efficiency by 2× **[29.1]**

CURRENT AND PROJECTED SIGNIFICANCE

- Talk-time will be increased by about 2× **[29.1]**
- Battery size can be reduced **[29.1]**
- Phone form-factor can be reduced, since heat generated is reduced **[29.1]**

ADSL Driver Sets New Standard for Power Efficiency

A 237mW ADSL2+ CO Line Driver in Standard 1.2V 0.13µm CMOS [29.4]

Katholieke Universiteit Leuven

PRESENT STATE OF THE ART *(THE PROBLEM)*

- DSL drivers burn too much power for further down-sizing
- The size of Central-Office (CO) equipment is limited by Line-Driver power dissipation per rack
- Fundamental limits of Class-AB-amplifier efficiency have been reached
- The DMT signal has a peak-to-rms power ratio as high as 6X

NOVEL CONTRIBUTIONS

- New ADSL driver sets new standard for power efficiency for dense central-office installations **[29.4]**
- Novel switching output stage combines PWM and FM modulation to achieve a new benchmark for efficiency **[29.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- CO Rack size can be significantly reduced **[29.4]**
- Overall system cost is reduced due to decreased number of power supplies needed **[29.4]**
- More line drivers can be installed per board **[29.4]**

3GHz Embedded DC-to-DC Converter & Clock-Tree Buffer

A 3GHz Switching DC-DC Converter Using Clock-Tree Charge-Recycling in 90nm CMOS with Integrated Output Filter **[29.8]**

University of British Columbia

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Power efficiency requirements dictate the usage of high-efficiency DC-to-DC converters
- Typical DC-to-DC converters employ external inductors to smooth the regulated voltage
- Clock generation is ubiquitous, and consumes a great deal of power
- Separate functions for DC-to-DC conversion and Clock generation inherently reduces efficiency

NOVEL CONTRIBUTIONS

- Merging of normally-separate DC-to-DC converter and Clock generation improves system efficiency **[29.8]**
- Overall system cost is reduced by the combination of functions. **[29.8]**
- Embedded inductor reduces size of Bill-of-Materials. **[29.8]**

CURRENT AND PROJECTED SIGNIFICANCE

- Energy efficiency improved **[29.8]**
- System area reduced **[29.8]**

SPECIAL-TOPIC SESSION

Digitally-Enhanced Analog & RF

Organizers: ***Kari Halonen****, Helsinki University of Technology, Espoo, Finland*
Stefan Heinen*, Infineon Technologies, Germany*
Chair: ***Robert Neff****, Agilent Technologies, Santa Clara, CA*

OVERVIEW

- As CMOS chip technologies scale to finer line widths, smaller devices, and lower voltages, the job of the analog-circuit designer is getting harder every year. Analog-circuit targets are harder to achieve with larger device mismatch, non-ideal device characteristics, and less voltage available for design. At the same time, the scaled technologies reduce power and area for digital circuits, and modern design tools make digital signal-processing and control lower-cost every year. The trends promise the replacement of high-linearity high-accuracy, but costly, analog circuits, by lower-performance lower-cost analog, enhanced by digital signal-processing. The final result is better performance, at lower cost, and lower design time.

CHALLENGE

- Where can digital assist analog?
- How can digital improve linearity and speed performance of analog-to-digital and digital-to-analog converters?
- How can digital improve linearity performance and yield for power amplifiers and direct-digital-synthesis systems?
- How does digital enhance widely-tunable multi-standard radios in cellphones and wi-fi applications?

RECAP

- Four experts with backgrounds in analog-circuit design, analog-digital converters, power amplifiers, and radio systems, will address the widening breadth of applications where digital signal-processing, control, and calibration, techniques enhance analog applications with performance, yield, and design-time improvements.

TUTORIAL

Embedded Power-Management Circuits

Philip K.T. Mok, Hong Kong University of Science & Technology, Hong Kong

OVERVIEW

Due to the drastic increases in the levels of system integration, and power consumption, of a scaled-technology IC, power management becomes a critical issue in determining its overall performance. This Tutorial starts with a brief overview of power-management circuits for embedded applications. A detailed explanation of the operation and design issues associated with various on-chip power-converter circuits will be presented. These include the design of:

- linear regulators
- switched-inductor regulators
- switched-capacitor regulators

The focus is on the analog-circuit techniques and control mechanisms for implementing these power converters.

SPEAKER BIOGRAPHY

Philip K.T. Mok is currently an Associate Professor in the Department of Electrical and Computer Engineering at the Hong Kong University of Science and Technology in Hong Kong. His current research interests include power-management integrated circuits, and low-voltage analog integrated-circuit design. He received his PhD in Electrical and Computer Engineering from the University of Toronto, Toronto, Canada, in 1995.

FORUM

Low-Voltage Analog-Amplifier Design for Filtering and A/D Conversion

Objective

Analog designers are forced to deal with continuously decreasing supply voltages. Continued process scaling is reducing device dimensions including the gate-oxide thickness, and, as a result, the breakdown voltages and maximum supply voltage, decrease for each process generation. Additionally, the increased use of battery-powered devices motivates the push toward lower supply voltages in mobile applications. Since threshold voltages are not significantly lower, the net usable voltage range for signal swing, biasing, and device stacking, is substantially reduced. As a result, amplifier performance (e.g., speed, gain, and noise) is compromised, which then requires adjustments in the systems where they are applied.

Audience

This Forum is intended for circuit designers and engineering students wishing to gain understanding of basic design issues for low-voltage amplifier circuits in the context of the applications and systems in which they operate.

Scope

A panel of researchers from academia and industry will review low-voltage-amplifier design techniques, amplifier performance degradation due to low-voltage operation, as well as filter and A/D converter-architecture solutions to mitigate the amplifier design challenges. The techniques presented will range from product-proven established techniques to more-recently-developed techniques for aggressive supply-voltage scaling.

Program

Andrea Baschirotto (University of Lecce) will discuss active-RC filter design solutions that incorporate limited opamp gain and bandwidth in the filter-design process. **Peter Kinget's** (Columbia University) talk addresses circuit-level techniques that allow amplifiers to operate at extremely low supplies in filters and converters, by utilizing techniques such as bulk biasing or bulk inputs, common-mode level shifting, and switch-elimination techniques. **Un-Ku Moon** (Oregon State University) will cover low-voltage, switched-circuit techniques for switched-capacitor filter applications. **Willy Sansen** (KU Leuven) will address the issue of noise optimization in headroom-constrained amplifiers. In low-supply environments, high-gain amplifiers need to be implemented as multistage amplifiers, and **Johan Huijsing** (TU Delft) will present class-AB techniques, as well as compensation techniques, that stabilize amplifiers with up to 4 stages. **Jieh-Tsorng Wu** (National Chiao-Tung University) addresses the performance limitations that amplifiers cause in A/D converters, and digital-calibration techniques to overcome the amplifier imperfections. The final two presentations focus on how the constraints on low-voltage amplifier design result in engineering decisions. Battery-powered hearing-aid-IC designs require both low voltage and low power, and **Alexander Heubi** (AMIS) will discuss a design using low-voltage circuits in some areas, while choosing to boost the supply voltage in others. **Corey Petersen** (Analog Devices) will review the trade-offs in low-voltage design for performance-driven applications, and discuss under what conditions low-voltage design is really beneficial.

The Forum will conclude with a panel discussion, where the attendees have the opportunity to ask questions and share their views.

NOTES

DATA CONVERTERS

- **Overview**
- **Featured Papers**
- **Special-Topic Session**
  (co-sponsored by Analog/Data Converters/RF)
- **Tutorial**
- **Forum**
  (co-sponsored by Analog/Data Converters)
- **Short Course**
  (co-sponsored by Analog/Data Converters)

ISSCC 2007 – Data Converters

Subcommittee Chair: *David Robertson, Analog Devices, Wilmington, MA*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- Data converters have made the shift to deeper-submicron technology: At ISSCC 2006, more than half the data converters were implemented in 0.18µm lithography; At ISSCC 2007, 90nm implementations dominate the converter papers. **[13.1, 13.3, 13.5, 25.1, 25.2, 25.3, 25.4, 25.7]**
- Oversampling-converter topologies continue to push to wider bandwidths **[13.1, 13.3],** and multimode operation to allow a single converter to handle multiple radio standards in a communications system. **[13.2, 13.3, 13.4]**
- Successive-Approximation-Register (SAR) A/D-converter topologies, traditionally used for medium-speed applications (<1MS/s) are being pushed to 40MS/s and above—a performance region formerly dominated by pipelined-converter technologies. The important advantage is that SAR topologies can offer smaller-area implementations and no latency. **[13.5, 13.6]**
- Increasingly, 90nm circuits are being designed to operate with 1V power supplies. **[25.1, 25.2, 25.3, 25.4, 25.7]**
- Driven by Imaging and Data-Communications requirements, there is continued improvement in power efficiency of Nyquist A/D Converters in the performance "sweet spot": of 8 to 10bits, and 50 to 250MS/s **[25.1, 25.2, 25.4, 25.5, 25.6]**
- In many converter designs, traditional circuit topologies are being adapted to lower supply voltages by using careful biasing and headroom management. **[25.1]** However, new topologies are also being explored that are explicitly designed to cope with lower supplies. **[25.2, 25.3, 25.4]**

APPLICATIONS AND ECONOMIC IMPACT

- As digital circuits continue to race to deep submicron technology, Data Converters are challenged to keep up, thereby enabling "System-on-a-Chip" integration of the analog and digital circuitry. In 2006, 90nm converter implementations were the exception, while in 2007, 90nm is the dominant technology, and in many cases, the circuit designs have been optimized to run at or below the "core-digital" supply voltage of 1.0V or 1.2V. **[13.1, 13.3, 13.5, 25.1, 25.2, 25.3, 25.4]**
- While some work continues to stretch "raw performance", **[25.7, 25.8],** many of this year's papers highlight efficient implementation of converters in the "performance mainstream" needed for multimedia and data-communications applications Here, the emphasis is on reducing power consumption and area. **[Session 13, Session 25]**
- Converters for mobile applications continue to emphasize power efficiency, but are increasingly demanding configurability to support multiple communications protocols, including 3G **[13.2, 13.3, 13.4]**, and, in some cases, even WLAN **[13.2, 13.3]** Delta-Sigma implementations continue to be the favorite topology here, featuring a variety of architectural variants—including switched-capacitor, continuous-time, and hybrid implementations.

SPECIAL-TOPIC SESSION *(co-sponsored by Analog/Data Converters/RF)*

Digitally Enhanced Analog and RF [SE1]

This Special-Topic Session explores the techniques for digital calibration and compensation of analog non-idealities, a technique becoming increasingly popular in deep-submicron CMOS converter and RF implementations.

TUTORIAL

Continuous-Time $\Delta\Sigma$ Data Converters: [T2]

FORUM *(co-sponsored by Analog/Data Converters)*

Low-Voltage Analog-Amplifier Design Techniques for Applications in Filtering and A/D Conversion [F7]

Deep-submicron design (90nm and below) implies low-voltage design (at 1V or less), and special design techniques. A series of speakers will address these issues for critical building blocks needed for Data-Converter design.

SHORT COURSE *(co-sponsored by Analog/Data Converters)*

Analog, Mixed-Signal, and RF Circuit Design in Nanometer CMOS [Thursday, February 15]

This Short Course includes a session on Continuous-Time $\Delta\Sigma$ ADCs, by Michiel Steyaert of Katholieke Universitet, Leuven.

ADCs for Multi-Mode Wireless Transceivers in Nanometer Digital CMOS

A 0.13μm CMOS EDGE/UMTS/WLAN Tri-Mode ΔΣ ADC with –92dB THD [13.2]

ETH

A 1.2V, 121-Mode Continuous-Time ΔΣ Modulator for Wireless Receivers in 90nm CMOS [13.3]

NXP Semiconductors

A 5th-Order CT/DT Multi-Mode ΔΣ Modulator [13.4]

NXP Semiconductors

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Cellular phones now must operate with several communication standards, often requiring multiple analog-to-digital converters.
- Until now, a separate ADC is required to meet the requirements for WLAN or WiMAX.
- Multi-mode converters have been in 0.18μm or 0.13μm CMOS.

NOVEL CONTRIBUTIONS

- Multi-mode converters in 90nm CMOS and below. **[13.3, 13.4]**
- Multi-mode converters now satisfy wideband (i.e. WLAN) applications, as well as cellular-communication standards **[13.2, 13.3]**
- Hybrid combination of continuous-time and discrete-time approaches, gives the benefits of both approaches **[13.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- Improvements in power efficiency result in increased battery life, reduce size, and reduced weight of handsets **[13.2, 13.3, 13.4]**
- Multi-mode ADC allow a cell phone transceivers to meet several standards, but still achieve low cost, small size, and excellent power efficiency **[13.2, 13.3, 13.4]**
- In the past, a brute-force wide-band converter might have been required, or, alternatively, several converters could be used **[13.2, 13.3, 13.4]**. Now, efficient one-stop conversion simplifies design.

Nyquist-Rate ADCs Leapfrog to 90nm CMOS

A 0.8V 10b 80MS/s 6.5mW Pipelined ADC with Regulated Overdrive Voltage Biasing [25.1]

Fujitsu

A 10b 160MS/s 84mW 1V Subranging ADC in 90nm CMOS [25.2]

UCLA

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Until recently, Nyquist-rate converters were best implemented in 0.18μm CMOS
- When converters were implemented in finer-geometry processes, they usually relied on special high-voltage transistors similar to those in 0.18μm CMOS

NOVEL CONTRIBUTIONS

- New techniques allow Nyquist-rate converters to be implemented in true nanometer CMOS processes **[25.1, 25.2]**
- New techniques, such as new biasing schemes, allow 1V (or less) supplies **[25.1, 25.2, 25.3, 25.4]**
- These converters achieve record energy efficiency, (e.g. 6.5mW, 10b at 80MS/s with a 0.8V supply) **[25.1]**

CURRENT AND PROJECTED SIGNIFICANCE

- More than half of the analog-to-digital converters at the 2007 Conference are in 90nm CMOS or below **[25.1, 25.2, 25.3, 25.4, and others]**
- The industry is leap-frogging from 0.18μm CMOS to 90nm CMOS -We believe that 90nm will provide a new standard for analog-to-digital converters **[25.1, 25.2, 25.3, 25.4]**
- Designers have developed new techniques to allow data-converter circuits to be integrated on the same substrate as the digital processing
- The energy efficiency of analog-to-digital converters continues to improve, defying skeptics **[25.1, 25.2]**

SPECIAL-TOPIC SESSION

Digitally-Enhanced Analog & RF

Organizers: ***Kari Halonen****, Helsinki University of Technology, Espoo, Finland*
Stefan Heinen*, Infineon Technologies, Germany*
Chair: ***Robert Neff****, Agilent Technologies, Santa Clara, CA*

OVERVIEW

- As CMOS chip technologies scale to finer line widths, smaller devices, and lower voltages, the job of the analog-circuit designer is getting more difficult every year. Analog-circuit targets are harder to achieve with larger device mismatch, non-ideal device characteristics, and less voltage available for design. At the same time, the scaled technologies reduce power and area for digital circuits, and modern design tools provide digital signal-processing and control at lower cost every year. The trends promise the displacement of challenging high-linearity high-accuracy analog circuits by lower-performance analog, enhanced by digital signal-processing. The ultimate achievement is better performance, at lower cost and reduced design time.

CHALLENGE

- Where can digital assist analog?
- How can digital improve linearity and speed-performance of analog-to-digital and digital-to-analog converters?
- How can digital improve linearity-performance and yield of power amplifiers and direct-digital synthesis systems?
- How does digital enhance widely-tunable multi-standard radios in cellphone and Wi-Fi applications?

RECAP

- Four experts with background in analog-circuit design, analog-to-digital converters, power amplifiers, and radio systems, will address the widening breadth of applications where digital signal-processing, controls, and calibration techniques, enhance analog applications with performance, yield, and design-time improvements.

TUTORIAL

Continuous-Time ΔΣ Data Converters

Yiannos Manoli, University of Freiburg, Germany

OVERVIEW

- The drive to finer-lithography CMOS processes pushes designs to lower supply voltages, and, inevitably, to smaller signal levels. This leads to the use of new architectures and circuit topologies better-suited to operate with lower headroom.
- Most A/D-converter applications—particularly those for communications— require filtering in front of the A/D converter to provide an "anti-alias" function, and remove or attenuate unwanted signals.
- While "switched-capacitor" delta-sigma architectures have been well-established and broadly-used for well over a decade, "continuous-time" delta-sigma A/D converters are becoming increasingly popular, particularly where low power and small area are important (as in chipsets for cellular phones). Continuous-time delta-sigma architectures offer the advantage of combining the filtering and ADC functions into one block, saving power and area.
- This Tutorial will cover the special design considerations for this important circuit topology.

SPEAKER BIOGRAPHY

Yiannos Manoli holds the Chair of Microelectronics at the University of Freiburg, Germany. His current research interests lie in the design of low-voltage and low-power mixed-signal CMOS circuits, and sensor-read-out circuits, as well as A/D and D/A converters, with over 150 papers in these areas. He holds a B.A. degree in Physics and Mathematics, an M.S. degree in Electrical Engineering and Computer Science from the University of California, Berkeley, and the Dr.-Ing. Degree in Electrical Engineering from the Gerhard Mercator University in Duisburg, Germany.

DIGITAL

- **Overview**
- **Featured Papers**
- **Special-Topic Session**
- **Tutorial**
- **Forum**
- **Trend Charts**

ISSCC 2007 – DIGITAL

Subcommittee Chair: *Samuel Naffziger, AMD, Fort Collins, CO*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- Dual-core microprocessor with 5GHz clock **[5.1]**
- More than one TFLOP from a single chip **[5.2]**
- Quad-core chips with independent core-frequency control. **[5.3, 5.4]**
- Eight-core microprocessor with 64 threads. **[5.7]**
- 40GHz all-digital clock generator in 90nm CMOS **[9.4]**
- Inductively-loaded standing-wave clock generator at 12GHz **[9.5]**
- Managing processor variation for power, performance, and reliability **[16.1, 16.4, 16.6, 22.1]**
- Low-energy interconnects **[22.8, 22.9]**

APPLICATIONS AND ECONOMIC IMPACT

- Performance growth will continue using high-frequency clocking and explicit parallelism with multiple cores and multi-threading **[5.1, 5.2, 5.7]**
- Maximizing product coverage with multiple power requirements using a single design **[5.3, 5.4, 5.5, 5.6]**
- Lower cost and improved yield with adaptive design for variation **[5.3, 5.4, 16.4, 16.6, 22.1, 22.3]**
- Faster time-to-market and portability enabled with all-digital clocking **[9.1, 9.4]**
- Power savings from clock-generation and circuit innovation **[9.5, 9.6, 22.8, 22.9]**

SPECIAL-TOPIC SESSION

Secure Digital Systems [SE6]

TUTORIAL

Dealing with Issues in VLSI Interconnect Scaling [T3]

FORUM

Adaptive Techniques for Dynamic Processor Optimization [F6]

New Record for Microprocessor Clocking

Design of the POWER6 Microprocessor [5.1]

IBM

An 80-Tile 1.28-TeraFlop Network-on-Chip in 65nm CMOS [5.2]

Intel

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Power constraints are imposing increasingly-severe limits on processor clock-frequency increases. In recent years, frequency improvements have been limited, with no new records being reported at ISSCC.

NOVEL CONTRIBUTIONS

- A record 5GHz operating frequency is reported **[5.1]**
- A large network-on-chip achieves an operating frequency of 4GHz **[5.2]**

CURRENT AND PROJECTED SIGNIFICANCE

- Demonstration that frequency improvements are still possible, even with today's power constraints **[5.1, 5.2]**
- Performance improvements from higher-frequency operation will continue, even as the number of cores per chip continues to increase **[5.1, 5.2]**

Record Multi-Processor Integration Levels

An 80-Tile 1.28-TeraFlop Network-on-Chip in 65nm CMOS [5.2]

Intel

An 8-Core, 64-Thread, 64-Bit Power-Efficient SPARC System-on-a-Chip [5.7]

Sun Microsystems

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Moore's Law continues to hold as feature sizes scale to 65nm, enabling more components to be integrated on a single chip
- More performance is derived from multi-core systems as power constraints restrict frequency increases.

NOVEL CONTRIBUTIONS

- A Network-on-Chip (NOC) architecture contains 80 tiles including floating-point cores and packet-switched routers. **[5.2]**
- One TFLOP peak performance is achieved **[5.2]**
- The Niagara-2 processor can handle up to 64 different programs simultaneously, double the number reported last year. Until recently, processors could handle only one program at a time. **[5.7]**

CURRENT AND PROJECTED SIGNIFICANCE

- 65nm technology enables higher integration levels **[5.1, 5.2, 5.4, 5.5, 5.6, 5.7]**
- Higher performance is obtained by integrating more components on one die **[5.2, 5.7]**
- The rapid rate of improvement is visible upon comparison with the papers at last year's ISSCC Conference **[5.2, 5.7]**

Core-Level Frequency Control for Power Management

A 4320MIPS Four-Processor Core SMP/AMP with Individually Managed Clock Frequency for Low Power Consumption [5.3]

Renesas; Hitachi; Hitachi ULSI; Waseda University

An Integrated Quad-Core Opteron™ Processor [5.4]

AMD

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Existing multi-core processors can adjust clock frequency only for all cores together, so that cores with lighter workloads cannot be independently slowed down to save power.
- Without individual frequency control for separate cores, individual voltage control is also unrealizable

NOVEL CONTRIBUTIONS

- Individual cores have independent dynamic-frequency control **[5.3, 5.4]**
- For single-core workloads, allowable power consumption can be increased, since idle processors can be slowed down **[5.3, 5.4]**
- Independent frequency control also enables independent voltage control of each core **[5.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- Individual core-level frequency control allows reduction of average power **[5.3, 5.4]**
- System-on-Chip control mechanisms are increasing in complexity, and, in the future, will provide many benefits by allowing more degrees of freedom for control of individual components **[5.3 ,5.4]**

LC-Based Resonant Clock-Distribution

12GHz Low-Area-Overhead Standing-Wave Clock Distribution with Inductively-Loaded and Coupled Technique [9.5]

Hiroshima University; Elpida Memory

Adaptive Low-Jitter LC-Based Clock Distribution [9.6]

University of California, Los Angeles

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Jitter in the clock distribution limits the maximum operating frequency.
- Power dissipation is a critical design concern.

NOVEL CONTRIBUTIONS

- Instead of direct metal coupling, the clock mesh is connected through magnetic links. **[9.5]**
- Inductors placed at the ends of each wire mimic a full transmission line, and enable full clock amplitude along the entire length, rather than at a single point on the wire. **[9.5]**
- Reduced power dissipation is achieved by inducing an in-phase standing-wave across the clock-distribution network at its natural frequency. **[9.5, 9.6]**
- Jitter can be optimized by adjusting the mixture of natural frequency and induced frequency, when operating away from the ideal resonance. **[9.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- Very-high-speed clocks enable higher-performance processors. **[9.5]**
- By reducing the power in the clock-distribution network, chips can be built which either operate at a higher frequency, or have less overall system cost. **[9.5, 9.6]**
- A reduction in jitter also helps to improve the power and performance of chips and systems. **[9.5, 9.6]**

High-Performance and Flexible Clock Generation

A Wide Power-Supply Range (0.5V to 1.3V) Wide-Tuning-Range (500MHz to 8GHz) All-Static CMOS All-Digital PLL in 65nm SOI [9.1]

IBM

A 40GHz DLL-Based Clock Generator in 90nm CMOS Technology [9.4]

National Taiwan University

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Analog PLLs have good jitter specifications and can achieve high frequencies, but have limited supply-voltage range, limited output dynamic-range, and porting the design to new process technologies is difficult.
- Digital clock generators are portable, have wide dynamic range, and can operate at multiple voltages, but their jitter specifications are not as good, and they traditionally cannot generate very-high frequencies.

NOVEL CONTRIBUTIONS

- An all-digital implementation of a PLL enables very-low power dissipation, less sensitivity to supply-noise, and extremely-low-voltage operation. **[9.1, 9.4]**
- Low-area designs are achieved through the use of static digital-logic techniques. **[9.1, 9.4]**
- Digital clock generators typically suffer from added jitter through interpolation, but this has been alleviated through innovative ways of increasing emphasis on digital-delay resolution. **[9.1, 9.4]**
- Locking the controlled delay-line to multiples of the reference-clock period enables significantly higher frequencies to be achieved with an all-digital generator. **[9.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- Wide operating ranges enable multiple power/performance envelopes, and designs with a big market-footprint. **[9.1]**
- High-speed processors will be enabled by very-fast low-jitter clock generators **[9.1, 9.4]**
- Low power dissipation helps reduce chip cost. **[9.1, 9.4]**

Processor Optimization Using Adaptive Techniques

On-Die Supply-Resonance Suppression Using Band-Limited Active Damping [16.1]

Intel; Haokai Microelectronics

Adaptive Frequency and Biasing Techniques for Tolerance to Dynamic Temperature/Voltage Variations and Aging [16.4]

Intel; Tyfone; Oregon State University; University of Michigan

Embedded SoC Resource Manager to Control Temperature and Data Bandwidth [16.6]

Hitachi, Renesas Technology

PRESENT STATE OF THE ART *(THE PROBLEM)*

- As processor integration grows to meet performance demands, power consumption and heat dissipation continue to increase.
- Nanometer-scale CMOS technologies show increasing performance degradation with transistor aging, as well as with variations in process, voltage, and temperature.
- Achieving optimized processor performance requires both real-time monitoring of its environment, as well as quickly adjusting the processor's operating parameters, such as voltage, frequency, body-bias, and bandwidth-allocation.

NOVEL CONTRIBUTIONS

- An active damping circuit suppresses on-die power-supply resonances, reducing voltage noise by a factor of four. **[16.1]**
- A set of sensors quickly measures temperature, voltage, and current, to enable dynamic changes in frequency, voltage, and body bias. Multi-PLL clocking systems and on-chip body-bias, enable rapid responses for power/performance optimization. **[16.4]**
- A dual-core SoC uses a thermal sensor and a resource manager to control core frequencies and core bandwidth allocation. **[16.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- Active damping of power-supply resonances allows for improved reliability, stability, and operating frequency of processors. **[16.1]**
- Rapid clocking and body-bias changes allow fast response to voltage droops. Adaptive techniques compensate for transistor aging-effects and temperature changes, significantly reducing design guardbands and improving performance. **[16.4]**
- SoC resource management allows for dynamic total-system optimization of power and performance. **[16.6]**

Managing and Exploiting Transistor Variability

A Distributed Critical-Path Timing Monitor for a 65nm High-Performance Microprocessor [22.1]

IBM

A 6.3pJ/b 96%-Stable Chip-ID-Generating Circuit Using Process Variations [22.5]

University of Washington

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Transistor variation mandates design guardbands, and thus reduce operating frequency and performance.
- Variations can themselves change across a die or wafer. This chip "tilt" further reduces margins across a die.

NOVEL CONTRIBUTIONS

- A collection of circuits that monitor critical timing margins are distributed around a 65nm SOI high-performance processor. These measure transistor variation, as well as DC power-supply droops. **[22.1]**
- A low-power dense array of sensitive circuits exploits transistor variation to generate a stable, unique chip identification number. **[22.5]**

CURRENT AND PROJECTED SIGNIFICANCE

- Distributed monitor circuits provide vital design feedback concerning DC-supply noise, across-chip and die-to-die transistor variation, and transistor aging effects. **[22.1]**
- A robust read-only stable unique chip-identification-number enables inexpensive tagging for RFIDs, sensor-node identification, and security applications. **[22.5]**

Reducing Power and Latency of On-Chip Wiring

High-Speed and Low-Energy Capacitively-Driven On-Chip Wires [22.8]

Sun Microsystems

A 0.28pJ/b 2Gb/s/ch Transceiver in 90nm CMOS for 10mm On-Chip Interconnects [22.9]

University of Twente

PRESENT STATE OF THE ART *(THE PROBLEM)*

- As technologies continue to scale, the delay of global on-chip interconnects can limit system performance.
- As chip integration increases to meet performance demands, the number of global on-chip interconnects continues to grow, thus increasing total power consumption.

NOVEL CONTRIBUTIONS

- A circuit that drives long on-chip wires through a coupling capacitor reduces energy by an order of magnitude, by lowering voltage swing. The capacitor boosts signal-swing rates, thereby compensating for wire latency, as well. **[22.8, 22.9]**

CURRENT AND PROJECTED SIGNIFICANCE

- Fast and low-power wire connections, providing lower energy and lower delay for global communication, remove a significant design complication in high-performance processors. **[22.8, 22.9]**

SPECIAL-TOPIC SESSION

Secure Digital Systems

Organizer: **David Money Harris** *Harvey Mudd College, Claremont, CA*
Chair: **Norman Rohrer** *IBM, Essex Junction, VT*

OVERVIEW

Digital security underpins the integrity of online financial transactions and of our privacy. Algorithms for secure systems are well-known among security experts, but not among the growing numbers of digital designers who need to build such systems. Public-key cryptosystems are computationally expensive, but allow communication without first sharing a secret key between the parties. Private-key cryptosystems are better-suited to encrypting large amounts of data. Hence, public-key systems are generally used to encrypt short messages, sign documents, or exchange secret keys used to encrypt longer messages. Recent advances in hardware design are dramatically improving the cost, speed, and power, of cryptographic hardware. Given a long-enough key, these systems generally cannot be broken by brute force. However, they are vulnerable to side-channel attacks that deduce information by monitoring side-effects of the encryption process, such as delay, power consumption, or electromagnetic radiation. This Session will address the algorithms and hardware implementations for private and public-key cryptosystems, the major side-channel attacks, and methods of defending against such attacks.

OBJECTIVE

- To introduce the design of secure digital systems to the semiconductor community. Specifically, to survey the leading algorithms for public and private-key cryptography, the known methods of attack, and the state-of-the-art defenses against these attacks.

CHALLENGE

- The news in the past two years has been full of stories of theft of confidential personal data, credit-card fraud, illegal surveillance, and piracy. Secure digital systems are needed to fight these problems.
- Digital systems must provide security seamlessly, inexpensively, and with low energy consumption.
- While a small cadre of security specialists has devised practical solutions, these solutions need to be communicated to a large audience of practicing engineers who can implement these solutions robustly.

STRUCTURE

- **Algorithms and Hardware Design for Private-Key Cryptography**
  Ingrid Verbauwhede, KU Leuven, Belgium

  Private-key cryptography is the most computationally efficient way to protect large amounts of data, such as communications across a wireless network. This talk explains the algorithms and hardware implementations for private-key cryptography, especially AES and DES.

- **Algorithms and Hardware Design for Public-Key Cryptography**
  Çetin Kaya Koç, Oregon State University & Istanbul Commerce University

  Public-key cryptography is a remarkable way for two parties to communicate securely without sharing a secret key in advance. However, the algorithms are computationally intensive because they involve arithmetic on very large numbers. This talk explores the algorithms and hardware implementations for private-key cryptography, especially RSA, Diffie-Hellman key exchange, and Elliptic-Curve Cryptography.

- **Side-Channel Attacks**
  Pankaj Rohatgi, IBM T. J. Watson Research Center, Yorktown Heights, NY

  Brute-force attacks against good cryptographic systems are computationally infeasible. However, side-channel attacks that exploit information leaked from the encryption processes, such as power consumption, timing, or electromagnetic radiation, have cracked many theoretically-secure systems. This talk will give examples and demonstrations of side-channel attacks.

- **Developing a Secure Chip**
  Chris Curren, EmbedICs, El Segundo, CA

  Practical cryptographic systems include countermeasures against side-channel attacks. This talk describes methods for developing integrated circuits resistant to these side-channel attacks.

RECAP

- The attendees will come away with an understanding of the most important cryptographic techniques used today, the state-of-the-art implementation techniques, and strategies to mitigate side-channel attacks.

Tutorial

Dealing with Issues in VLSI Interconnect Scaling

Ron Ho, Sun Microsystems Research Labs

OVERVIEW

Designers have recognized, for many years, that on-chip wires can limit system performance. As technologies continue to scale, the problems posed by on-chip wires continue to worsen. This Tutorial will introduce these problems, some solutions, and examine how they will scale in future technologies. The Tutorial will cover:

- Simple models for wire latency, bandwidth, power, and noise
- Scaling trends and technology projections for wire performance
- Design implications of wire scaling
- Promising circuit techniques that improve wire performance

SPEAKER BIOGRAPHY

Ron Ho is currently a Senior Research Scientist at Sun Microsystems Research labs in Menlo Park, California. He is involved in the design of on-chip and inter-chip communication for application in high-performance systems, focusing on energy-efficient designs. He received his B.S., M.S., and Ph.D. degrees in Electrical Engineering from Stanford University, in 2002. From 1993 to 2003, he was with Intel Corporation in Santa Clara, working on processors ranging from the 80486 to the 3rd-generation Itanium. He is also a Consulting Assistant Professor at Stanford University, where he has taught graduate-level classes in circuit design.

FORUM

Adaptive Techniques for Dynamic Processor Optimization

Objective

One of the most severe repercussions of device scaling in sub-100nm technologies is the large variability in device parameters. This results in a wide range of operating points for manufactured silicon. Furthermore, there is a need to limit power and thermal dissipation to meet overall-system or reliability concerns, whilst still achieving sufficient performance for each software/system application. As a result, numerous innovative techniques have been developed to allow silicon-based functions to adjust dynamically to achieve their target operating range. Implementing such techniques spans the entire spectrum of design, from devices and circuits through to testability and software/system control mechanisms. In their presentations, the experts assembled for this Forum will detail the various issues encountered in designing and utilizing dynamically-adaptive systems.

Audience

This Forum is intended for chip designers at all levels, who are interested in understanding the opportunity presented by dynamically-adaptive systems, and the techniques to implement them.

Scope

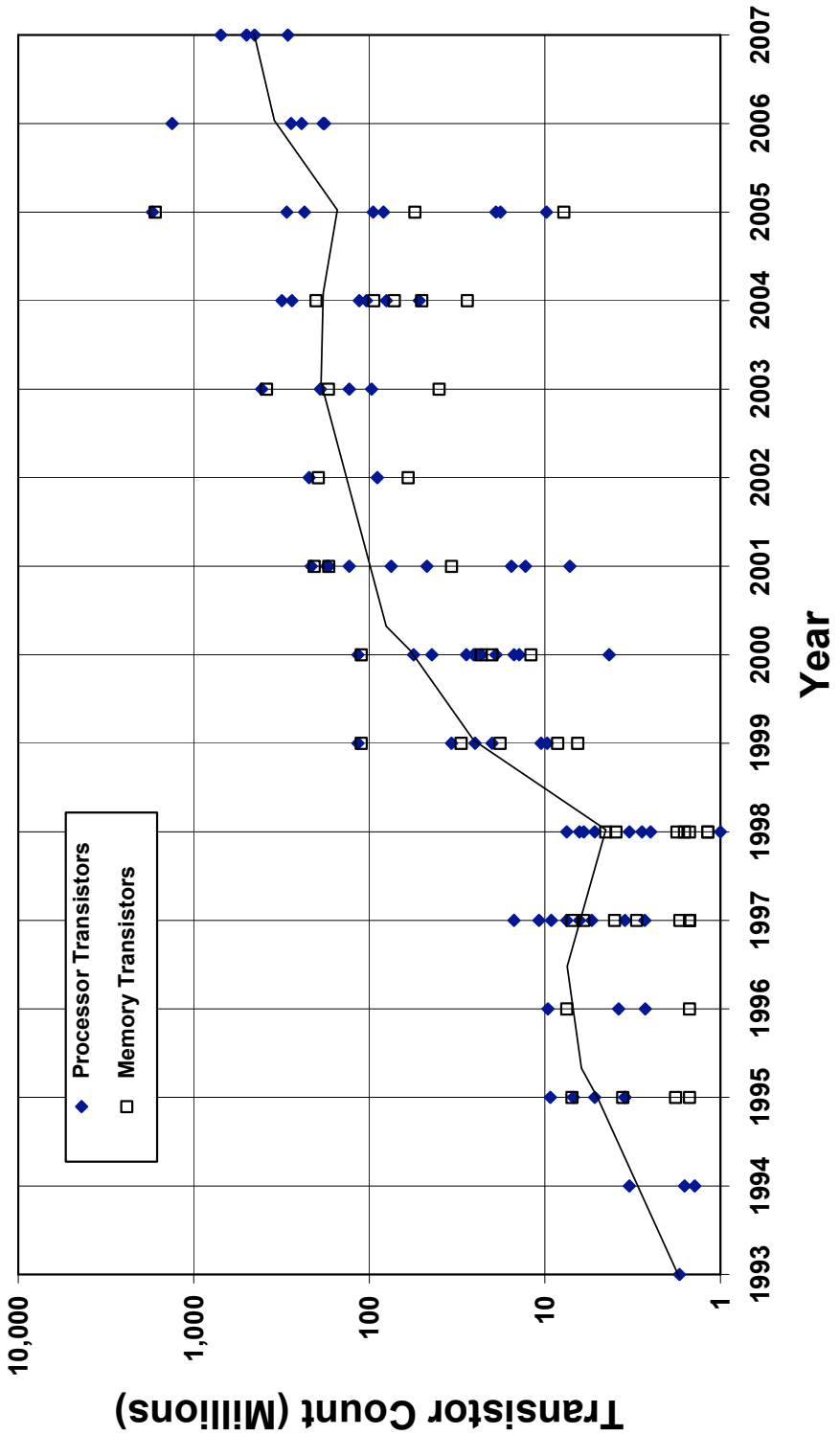
Various adaptive techniques for dynamic processor optimization will be discussed in this Forum, from a technology, circuits, systems, and, test perspective. Applications span the power/performance spectrum, from low-power SoCs to high-performance microprocessors.

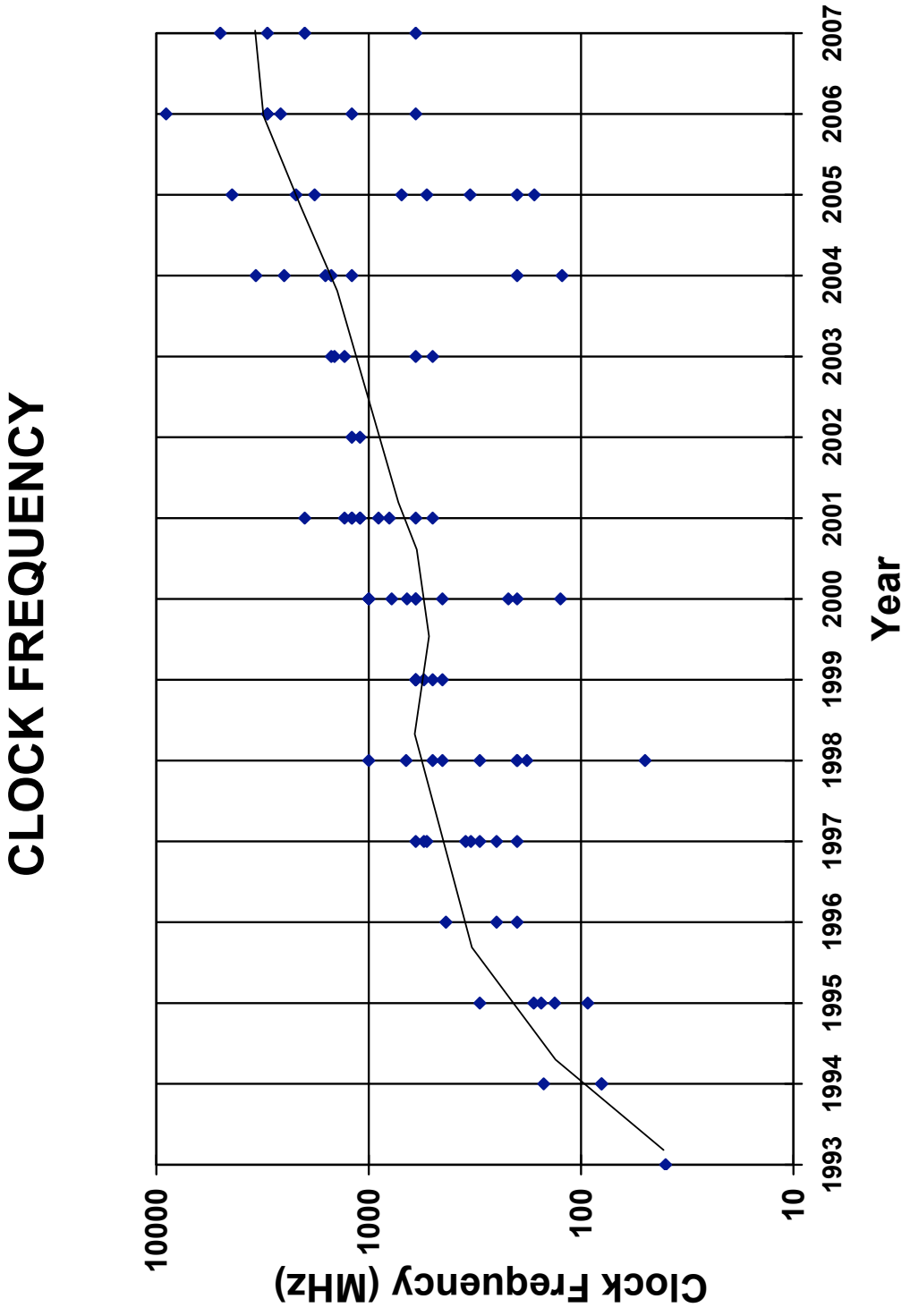
Program

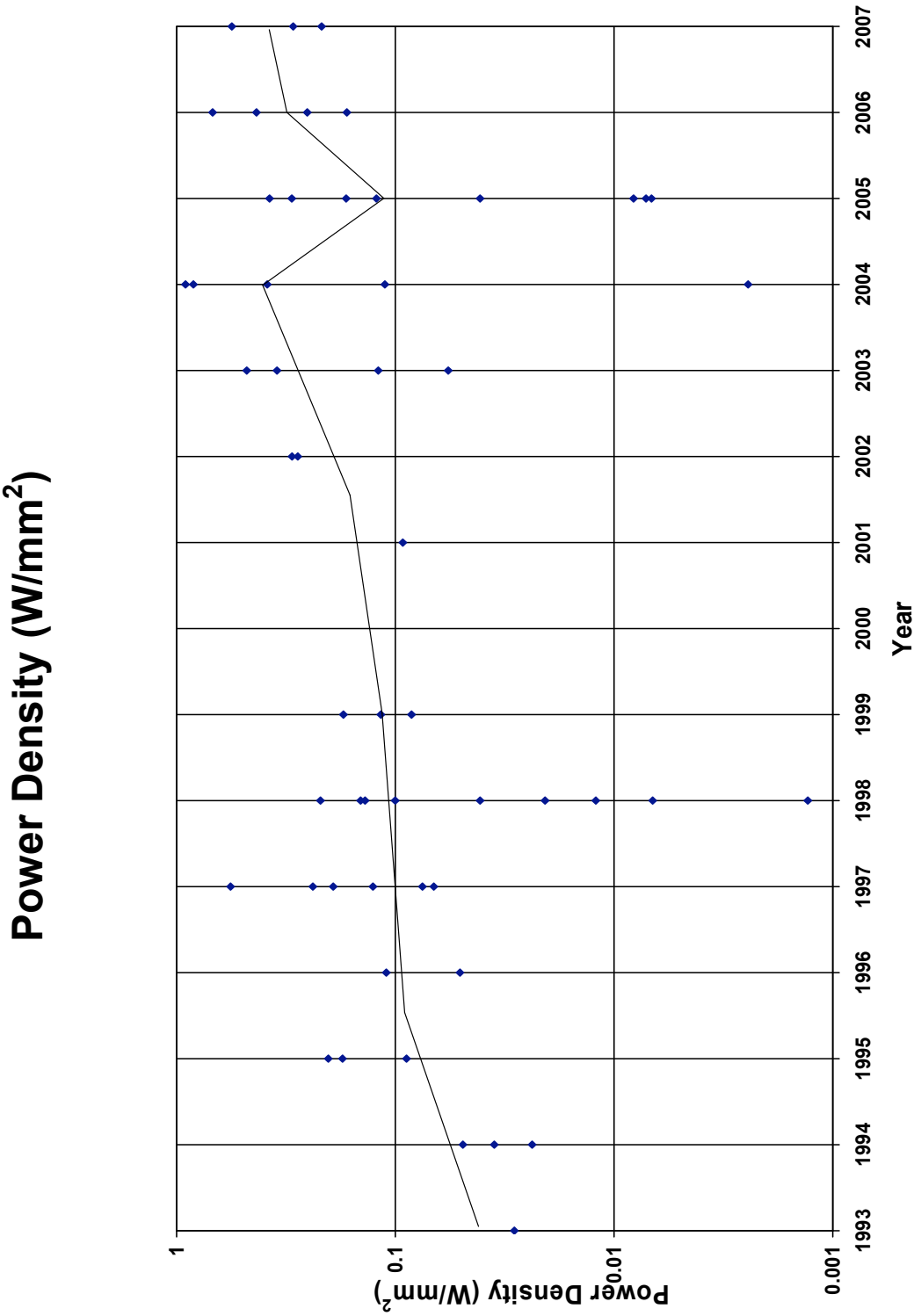
The first talk by **David Scott,** [TI], "Technology Challenges of Adaptive Techniques", will set the stage for the Forum by explaining the technology-scaling issues which have contributed to an ever-widening range of post-fabrication behaviors. **Ishibashi-san,** [Renesas], will then present "Adaptive Body-Bias Techniques for Low-Power SoCs". This talk will focus on various methods of static and dynamic body biasing, primarily applied to low-power designs. The next two talks discuss dynamically-adaptive techniques for high-end microprocessor-based systems. "Adaptive Control for High-End Processor Power Management" by **Thomas Pflüger,** [IBM], will address voltage versus frequency control mechanisms, as well as various fundamental architectural techniques to dynamically manage power. **Jim Dorsey,** [AMD] will follow with "Processor Support for Advanced Power and Thermal Management Techniques in Multi-Core Environments". This talk will address issues such as detailed thermal monitoring, clock domains, and the software control loop, all in the context of a multi-core environment. The fifth presentation, by **David Blaauw,** [U. Michigan], "Adaptive Architectural Techniques and the Hardware/Software Interface", comes in two parts: The first will review some of the most-useful architectural techniques that can be employed to manage power versus performance on a dynamic basis. The second part will address a specific method, known as "Razor", which dynamically corrects for timing-based errors on-chip. Finally, **Eric Fetzer,** [Intel], will discuss the challenges in testing, debugging, and practically-implementing, dynamically-adaptive systems, in his talk "The Challenges of Testing Adaptive Techniques".

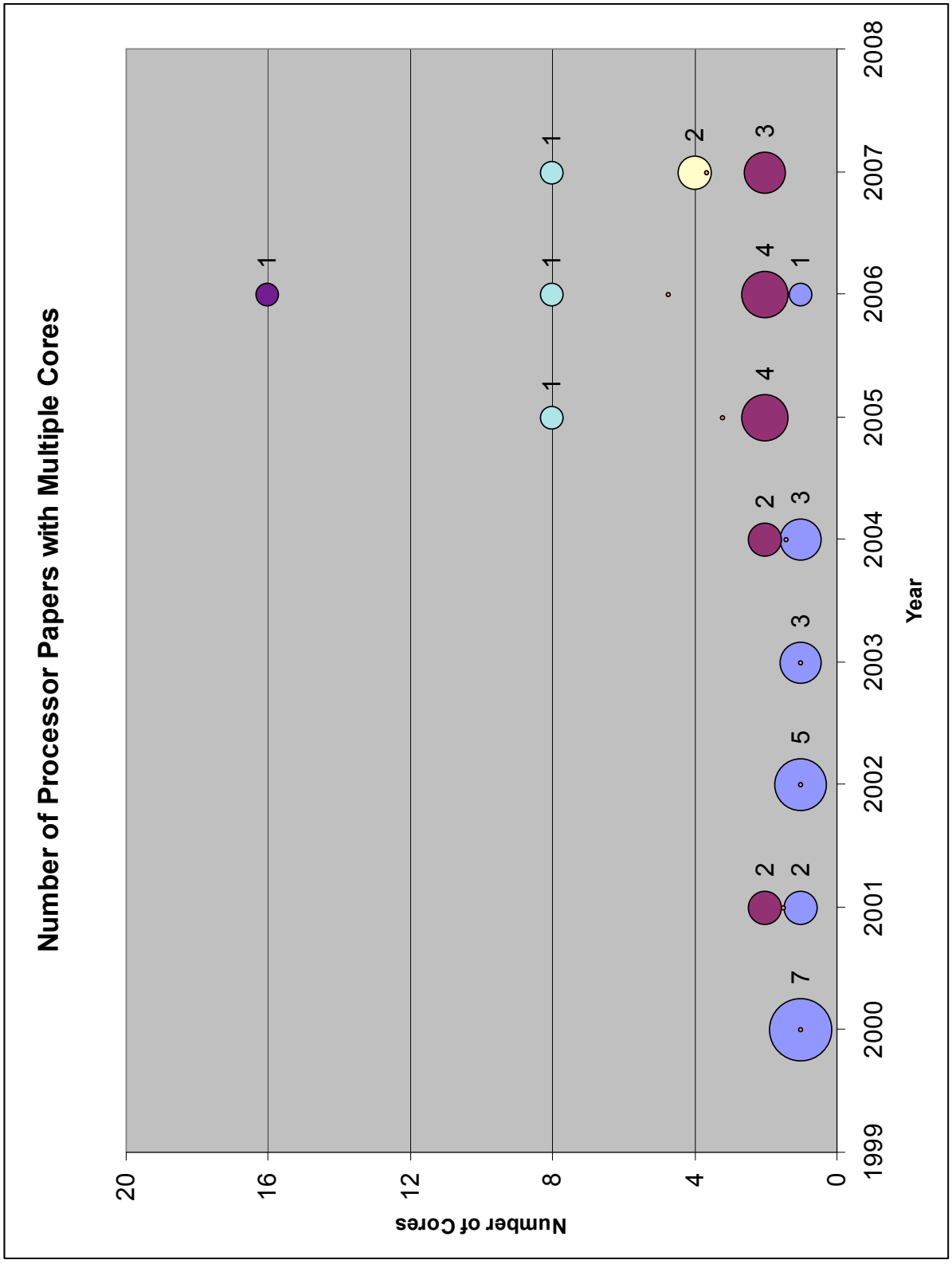
In wrapping up, all of the presenters will assemble in a panel format for an open and forthright discussion with the audience.

CHIP COMPLEXITY









IMAGERS, MEMS, MEDICAL AND DISPLAYS

- **Overview**
- **Featured Papers**
- **Special-Topic Sessions**
- **Tutorial**
- **Forum**
- **Trends**

ISSCC 2007 – IMMD

Subcommittee Chair: *R. Daniel McGrath, Eastman Kodak, Rochester, NY,*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- Low-Temperature-Polysilicon Active-Matrix OLED display with integrated 8b/color DAC and driver **[7.1]**
- Single component combining display and image-sensing enables touch-screen and biometrics **[7.2]**
- Retinal stimulator realized in 0.35µm HV CMOS providing 232 channels with programmability, testability, and safety features **[8.1]**
- Advances in power and noise figures for implantable deep-brain neural-recording implant **[8.6]**
- Single-chip micro-compass with industry-standard SPI serial readout **[21.2]**
- MEMS gyroscope achieves the highest-reported accuracy of 0.2° per hour **[21.4]**
- 8.1 Mpixel sensor with smallest commercially-available (1.75µm) pixel **[28.5]**
- Low noise enables high image-quality in high-definition camcorder **[28.6]**

APPLICATIONS AND ECONOMIC IMPACT

- Improved digital displays for mobile phones **[7.1]**
- Improved human-interface devices in mobile displays for smaller/smarter mobile phones **[7.2]**
- Closing in on providing rudimentary sight to significant numbers of patients **[8.1]**
- CMOS inplant enables cost-effective and compact neural recording systems **[8.5]**
- Deep-brain implant to enable feedback for treating neural degenerative diseases **[8.6]**
- Integration of compasses into hand-held applications such as cell phones and PDAs **[21.2]**
- High-precision low-power-dissipation sensor for automotive and hand-held GPS navigation systems **[21.4]**
- Lower-cost digital cameras with photographic performance **[28.5]**
- CMOS image sensors catch up with CCDs for HD camcorder applications requiring real-time image-processing **[28.6]**

SPECIAL-TOPIC SESSIONS

Implantable and Prosthetic Devices: Life-Changing Circuits [SE7]

TUTORIAL

Dynamic-Offset Cancellation Techniques in CMOS [T4]

FORUM

Noise in Imaging Systems [F4]

Display Electronics

An 8b Source Driver for 2.0 inch Full-Color Active-Matrix OLEDs Made with LTPS TFTs [7.1]

Samsung; Hanyang University

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Mobile displays using low-temperature polysilicon (LTPS) backplanes have been limited to 6bits of color depth. There is increasing demand for mobile displays with 16 Million colors. To do this with LTPS, requires improvements in the onboard drive electronics
- LTPS devices have poor tolerances and matching, even though they are superior to amorphous silicon.
- LTPS is being used in mobile displays because it offers smaller pixels, and allows some of the driver electronics to be integrated onboard, even though it is more expensive.
- There is limited space for the column-drive electronics embedded onto the backplane, so increasing the resolution of the drive DACs needs to be done with the minimum number of active components, which is very challenging.
- LTPS is preferred for implementing the current drive used for Active-Matrix Organic LEDs (AMOLEDs), so the natural extension is to incorporate the column driver and DAC to create a complete digital display.

NOVEL CONTRIBUTIONS

- The DAC is segmented twice, first into two sections, a 4b MSB sub-DAC and a 4b LSB sub-DAC, and then again segmented into an 8 x 2b resistor/switch DAC **[7.1]**
- First use of a pre-charge technique in LTPS to speed up response **[7.1]**

CURRENT AND PROJECTED SIGNIFICANCE

- Displays with greater color depth for mobile applications **[7.1]**
- Technique allows AMOLEDs to compete with LCD-TFTs on the basis of color depth **[7.1]**
- Competitor to Si TFT LCD backplanes with high-performance CMOS display-driver ICs **[7.5, 7.6]**

Display Electronics

A 2.6 inch VGA LCD with an Optical Input Function Using a 1-Transistor Active-Pixel Sensor [7.2]

Sharp Europe, Sharp Japan

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Mobile products are increasingly demanding the use of the screen as an extended part of the human-interface system.
- The industry-standard technique for adding touch-sensitive capability is to add a capacitive sensing layer and associated electronics. This has limited resolution (to a few dpi), and adds thickness and cost. Adding a layer onto the display in the optical path also degrades light transmission.
- To be cost-effectively implemented in the backplane, any function needs to use a minimum number of active components

NOVEL CONTRIBUTIONS

- Integration of an image sensor and the display-drive electronics on the same backplane **[7.2]**
- 300dpi resolution suited for more than touch-screen applications, such as stylus operation and fingerprint input **[7.2]**
- Operation of an active pixel with only 1 transistor and 1 capacitor including readout in low-temperature polysilicon (LTPS) technology to minimize cost and increase dpi. **[7.2]**

CURRENT AND PROJECTED SIGNIFICANCE

- Can provide a flexible human-interface device, for applications ranging from simple programmable buttons to stylus and biometric input at higher dpi **[7.2]**
- Potential to reduce cost and size so that every mobile display could also be a user interface device **[7.2]**
- Could replace current capacitive and pressure sensors on top of display **[7.2]**
- Another approach uses a companion readout device with an embedded passive pixel array on an Amorphous-Si TFT-display backplane, but it may not be competitive in cost and quality **[7.3]**

Retinal Prostheses

A 232-Channel Visual-Prosthesis ASIC with Production-Compliant Safety and Testability [8.1]

sci-worx; IIP Technologies

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Small number of stimulated sites
- Limited testability and safety features

NOVEL CONTRIBUTIONS

- Retinal stimulator realized in 0.35µm HV CMOS with 232 channels **[8.1]**
- Practrical programmability, testability, safety, features **[8.1]**

CURRENT AND PROJECTED SIGNIFICANCE

- Increased number of active electrodes and thus increased resolution **[8.1]**
- Human compatibility and safety **[8.1]**

Live Recording of Brain Neural Activity

256-Channel Neural Recording Microsystem with On-Chip 3D Electrodes [8.5]

University of Toronto

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Applications such as neural prostheses, animal studies, and high-throughput drug screening require neural recording from multiple sites within a volume of tissue
- As the bandwidth of neural systems can reach above 5kHz, recording several simultaneous channels can yield large amounts of data that cannot be directly stored, processed, or transmitted.
- Live tissue is extremely sensitive to local temperature increases caused by heat dissipation of electronics in contact with tissue.

NOVEL CONTRIBUTIONS

- The recording-channel area is 4 times less than previously reported results, and the power dissipation of 15μW/channel is 3 times less **[8.5]**
- First report of experimental in-vitro validation of integrated CMOS recording chip with electrode array **[8.5]**
- First report of two-dimensional neural-activity mapping “electronic video” (simultaneous frame capture) recording from on-chip 3D electrodes **[8.5]**
- A delta-read-out compression circuit offers the ability to trade recording accuracy for output data rate **[8.5]**

CURRENT AND PROJECTED SIGNIFICANCE

- Enable applications in neural prostheses, animal studies, and high-throughput drug screening **[8.5]**
- Enables cost-effective and compact neural recording systems **[8.5]**

Implantable Brain Neural Recording

A 2.2μW 94nV/√Hz Chopper-Stabilized Instrumentation Amplifier for EEG Detection in Chronic Implants [8.6]

Medtronic

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Noise and power dissipation limit the performance of EEG detection in chronic-care implants

NOVEL CONTRIBUTIONS

- Low-power chopper-stabilized instrumentation amplifier (2.2μW at 1.8V) **[8.6]**
- Low noise: 0.94μV_{rms} within 0.5Hz to 100Hz band **[8.6]**
- Rail-to-rail inputs and 105dB CMRR **[8.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- Low-power, low-noise solution for deep-brain implants **[8.6]**
- Long-term battery operation of implants **[8.6]**

Electronic Compass

A CMOS Single-Chip Electronic Compass with Microcontroller [21.2]

Melexis

PRESENT STATE OF THE ART *(THE PROBLEM)*

- No single-chip resolution of micro-compass need
- Hand-held and automotive systems need low-cost micro-compasses to aid in a variety of navigation devices, including GPS and gyroscopes

NOVEL CONTRIBUTIONS

- Single-chip micro-compass with a 3-axis Hall-based magnetic sensor and an integrated microcontroller with industry-standard SPI serial data readout **[21.2]**
- Low-voltage operation of 2.2V to 3.6V with a current of 5mA **[21.2]**
- The heading accuracy is better than ±2°, and the short-term heading precision is better than 0.5° **[21.2]**

CURRENT AND PROJECTED SIGNIFICANCE

- Compass chip will enable the integration of compasses into hand-held applications such as cell phones and PDAs. **[21.2]**
- Compass chip can also be used to periodically calibrate gyroscopes in hand-held and automotive navigation applications. **[21.2]**

MEMS Gyroscope

A 0.2°/hr Micro-Gyroscope with Automatic CMOS Mode-Matching [21.4]

Georgia Institute of Technology

PRESENT STATE OF THE ART *(THE PROBLEM)*

- High-precision optical gyroscopes are too large and expensive to be used for GPS-augmented navigation
- MEMS gyroscopes do not achieve the high accuracy necessary for inertial-measurement systems required for GPS-augmented navigation

NOVEL CONTRIBUTIONS

- The MEMS gyroscope achieves the highest-reported accuracy of 0.2° per hour **[21.4]**
- Sensor accuracy is more than two orders of magnitude better than low-cost commercially-available MEMS gyroscopes **[21.4]**
- Sensor uses a CMOS IC for dynamic tuning of the device, consuming only 6mW in 2.25mm^2 **[21.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- High precision and low power allow gyroscope to be used to augment automotive and hand-held GPS navigation systems **[21.4]**
- Gyroscope will increase position accuracy when satellite communications are interrupted for example, a car traveling at 100 kilometers per hour, that encounters a 10-minute GPS satellite interruption, will experience a maximum additional position error of 34 meters **[21.4]**

Image Sensors for Digital Still-Cameras

A 1/2.5 inch 8.1Mpixel CMOS Image Sensor for Digital Cameras [28.5]

Micron Technology

PRESENT STATE OF THE ART *(THE PROBLEM)*

- In consumer cameras, size matters, as the trend continues toward fitting more and more megapixels into a limited space to keep cost down
- Last year, the industry standard was 2.2µm pixel pitch

NOVEL CONTRIBUTIONS

- New 8.1Mpixel sensor fits into 1/2.5-inch optical format **[28.5]**
- Provides 1.75µm pixel pitch **[28.5]**

CURRENT AND PROJECTED SIGNIFICANCE

- Lower-cost digital cameras with photographic performance **[28.5]**
- 8.1Mpixel sensor replaces current 5Mpixel sensors in the same optical format **[28.5]**

Low-Cost and Low-Noise CMOS Image Sensors for HD Camcorder Applications

A 1 / 2.7-inch Low-Noise CMOS Image Sensor for Full-HD Camcorders **[28.6]**

Canon

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Need better image quality with reduced noise level
- Only 2/3-inch optical format sensor available in Camcorder applications, so far

NOVEL CONTRIBUTIONS

- New 1 /2.7-inch optical-format CMOS image sensor (CIS) for HD camcorders**[28.6]**
- Saturation level of 14 ke^- with small pixel size**[28.6]**
- Low noise level of 3.7e^-_{rms} random noise and 12.2e^-/s dark current**[28.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- CMOS image sensors (CIS) catches up with CCD even in the area of HD-camcorder applications, requiring real-time image processing **[28.6]**

SPECIAL-TOPIC SESSION

Implantable and Prosthetic Devices: Life-Changing Circuits

Organizer: ***Reid Harrison,*** *University of Utah, Salt Lake City, Utah*
Chair: ***Ken Wise,*** *University of Michigan, Ann Arbor, Michigan*

OVERVIEW

Advances in the miniaturization of electronics and increased understanding of neurophysiology during the twentieth century, have led to a rapid growth in neurological technologies – circuits that communicate directly with the human nervous system. Today, analog and mixed-signal integrated circuits form the heart of implantable devices that restore hearing to the profoundly deaf, and calm the tremors of Parkinson's disease. Technologies to stimulate paralyzed muscles and restore vision to the blind are becoming a reality, as well. Yet, circuits that must operate within the body, present enormous technical challenges. Power dissipation is extremely limited since excess heat can damage surrounding tissue, and power typically must be delivered wirelessly. The speakers in this Special-Topic session have backgrounds spanning technology and medicine, and bring a multidisciplinary perspective to this exciting field.

Tim Denison will provide an overview of pacemaker development and show how this well-established technology is leading to new circuits for "deep brain" stimulation intended to treat disorders such as Parkinson's or epilepsy. **Gerald Loeb** will describe small, implantable ASICs for neuromuscular stimulation. **Peter Seligman** will discuss cochlear implants – one of the most successful neural-interfaces developed in the past few decades – which restore hearing to tens of thousands of deaf persons worldwide. **Eberhart Zrenner** will describe microelectrode stimulation-arrays being developed to restore vision to patients who suffer from retinal degeneration. This Session will introduce attendees to the challenging field of biomedical microelectronics, one that promises to improve the quality of life for millions of people in the coming decades.

CONTENTS

Biological systems are embedded with complex, bio-electrical circuits. Heart attacks, seizures, and other problems, result when these biocircuits fail. Engineers can help "repair" damaged biocircuits with silicon alternatives, as shown by the proliferation of pacemakers and defibrillators.

A relatively new area for biocircuit troubleshooting is the field of "deep-brain" stimulation to treat disorders such as Parkinson's or epilepsy. These therapies place electrodes within the brain to focus treatment on a key neural circuit. Just as with pacemaker technology, deep-brain stimulation is becoming more sophisticated as our understanding of the underlying biological circuits grows.

This talk will provide an overview of the challenges engineers face when developing deep-brain stimulation devices. After providing a brief overview of key neural circuits, and setting the context for

the pacemaker evolution, the discussion will focus on the electro-mechano-chemical system constraints of deep-brain intervention, with a particular focus on low-power circuit-design challenges.

BIONic Neuromuscular Interfaces

Gerald Loeb, University of Southern California, Los Angeles, CA

Control of muscles and limb movements poses special challenges for neural prosthetics because the action is in the periphery, rather than in the mechanically-protected and physically-localized central nervous-system. Multiple widely-spaced devices must be implanted and controlled without encumbering the patient, and they must function for decades in an extremely hostile environment. The unusual form factor of an injectable hermetic package (BION = BIOnic Neuron) dictates the use of a single ASIC that supports bidirectional RF communication, low-noise signal detection, high-voltage stimulation, complex digital control, and low power consumption. Development and clinical testing of such disruptive, but highly regulated, technology in an academic research environment, has posed further challenges.

Cochlear-Implant Technology – The Bionic Ear

Peter Seligman, Cochlear, East Melbourne, Australia

Cochlear implants have become an established prosthetic device to help people who have lost all their useful hearing. Cochlear implants are distinct from hearing aids, which amplify sound for those for whom some conventional hearing remains . For those with absolutely no conventional hearing, the sensation of hearing is restored by electrical stimulation of the auditory nerve in the inner ear. The prosthesis consists of two parts: a surgically-implanted device in a hermetic capsule, and an externally-worn sound processor that includes a microphone and a battery. The sound processor communicates with the implant via a radio-frequency inductive link. The hearing sensation is produced by analyzing the sound into typically 16 to 22 frequency bands, and stimulating nerves approximately corresponding to these frequencies in normal hearing.

The Cochlear Implant is designed to last for the lifetime of the recipient, but upgrades to the external hardware are periodically available, with improvements in convenience and sound quality.

Subretinal Multielectrode Arrays: Therapy for Blindness?

Eberhart Zrenner, University Eye Hospital, Tübingen, Germany

A short survey of the high incidence of neurodegenerative retinal diseases that lead to serious visual impairment and blindness, indicates the high demand for rehabilitation by biological and technical devices. The rapid progress in electronic retinal prostheses during the last 12 years has opened a new field of visual rehabilitation for the blind, that is based on a number of developments discussed in the talk: Understanding of the retinal function, research in electrical stimulation of retinal neurons, development of novel micro-electronic chips with high spatial resolution, development of novel surgical techniques, progress in material sciences concerning electrode arrays for stimulation, new encapsulation developments for long-term stability and bio-compatibility of electronic implants, new methods of powering subretinal electronic devices. Ongoing clinical studies with such devices will be briefly discussed, including the limitations tor regaining vision, based on the physiological properties of the retina, and the technical limitations of neuroprosthetic devices.

Tutorial

Dynamic Offset-Cancellation Techniques in CMOS

Kofi A. A. Makinwa, Delft University of Technology, The Netherlands

OVERVIEW

In analog CMOS design, offset is a fact of life! Even in modern processes, device mismatch typically results in offset voltages of several millivolts. But many analog circuits, such as precision amplifiers, sensor interfaces, and ADCs, require much lower offset levels. Fortunately, by using dynamic offset-cancellation techniques, such as auto-zeroing and chopping, microvolt levels of offset can be routinely achieved in standard CMOS. Compared to the alternatives, such as the use of huge devices or trimming, the use of dynamic-offset-cancellation techniques, has the added advantage of also reducing 1/f noise and drift, thus making it possible to design circuits that are thermal-noise-limited. In this Tutorial, an introduction to the basic theory behind auto-zeroing and chopping will be given, the pros and cons of both techniques highlighted, and recent advances in the state-of-the-art reviewed. Examples will be given of the use of auto-zeroing and chopping in CMOS circuits and systems with residual offsets as low as 50nV.

SPEAKER BIOGRAPHY

Kofi A. A. Makinwa is an Associate Professor at Delft University of Technology, The Netherlands. He received the B.Sc. and M.Sc. degrees from Obafemi Awolowo University, Nigeria, in 1985 and 1988 respectively. In 1989, he received the M.E.E. degree from the Philips International Institute, The Netherlands, and then joined Philips Research Laboratories as a research scientist. In 2004, he received the Ph.D. degree from Delft University of Technology. He holds nine U.S. patents, has (co)-authored over 40 technical papers, and has given tutorials at the Eurosensors and the IEEE Sensors conferences. His main research interests are in the design of precision analog circuitry, delta-sigma modulators and sensor interfaces. He has served on the technical program committees of ISSCC, the International Solid-State Sensors and Actuators Conference (Transducers), and the IEEE Sensors Conference. In 2005, he received the Veni and Simon Stevin Gezel awards from the Dutch Technology Foundation (STW), and was a co-recipient of the ISSCC 2005 Jack Kilby award.

Forum

Noise in Imaging Systems

OVERVIEW:

Noise in Imaging Systems has much in common with noise in the classical world of analog electronics, but imaging adds some very specific noise issues to consider. In many cases, the electronic engineer refers only to temporal noise when discussing noise, but in an imaging system non-temporal noise sources also need to be taken into account. In addition, the perfect image sensor in a perfect camera still suffers from noise, because of the photon shot noise of the input signal.

This Forum is organized to contribute to a better understanding of noise issues in imaging systems, and to stimulate creativity in this field. The speakers at this Forum are world experts in this area.

Takao Kuroda (Matsushita) will introduce the topic to begin the Forum. The next talk, by **Boyd Fowler** (Fairchild Imaging), will discuss several noise mechanisms, starting with the most important one, kT/C noise. The kT/C noise sets a fundamental detection limit on capacitive sensors. Therefore, it is important to understand the factors that determine the kT/C noise and how this noise may be mitigated.

Bedrabata Pain (JPL) will speak on the topic of device-level noise. The pixels in imagers are becoming extremely small, and several noise sources can be distinguished within every pixel. Shrinking the CMOS technology will put constraints on the pixel's noise behavior.

A CMOS imager is usually a complex mixed analog-digital system-on-a-chip, and circuit noise often dominates the total noise of the image sensor. The circuit noise is observed as a fixed-pattern noise (FPN) or a temporal random noise. The former is originated by device mismatches and is cancelled in the analog and/or digital domains, while the latter is more problematic. **Shoji Kawahito** (Shizuoka University) will discuss noise at the circuit level.

One level higher than the circuit is the system level. Each of the system elements plays an important role in determining the overall noise of the system. The optics may introduce noise in the form of stray signals, such as flare and ghost images, both of which result from internal reflections. A system-level view must also consider factors such as the pixel spectral response, which affects noise amplification, as well as the noise originating from power-supply variation, timing jitter, and imperfect FPN-cancellation circuits. The speaker invited to talk about system-level noise is **Rick Baer** (Micron Technology).

Random noise and distortion added to an image signal only matters when it can be seen. Seeing it, however, does not necessarily mean that it will be considered as a defect. Visual artists learn to use the features of a technology that impart a distinctive look to the resulting image, to fulfill artistic goals. **Jim Larimer** (Image Metrics) will review the properties of the human visual system that allow viewers to see distortion and noise in the temporal, spatial, and intensity domains of the image, how the eye samples the signal, and how this process can "beat" with capture and reconstruction methods.

The last presentation of the Forum will highlight some algorithms used to cancel noise in images. **Aleksandra Pizurica** (Ghent University) will review some of the latest and best-available multiresolution methods for noise reduction. Attention will be given to the following topics: estimation of the noise statistics from the input image (or video); construction of spatially adaptive denoising methods; motion estimation/compensation and noise suppression, adapted to motion-estimation reliability. In addition, some application-specific topics, such as the use of "noise patterns" and camera reference frames for denoising digital-camera images, will be reviewed.

Although this Forum focuses on imaging systems, the issues and techniques dealt with are also applicable to other emerging fields.

TRENDS in BIOMEDICAL DEVICES and SYSTEMS

- *Restoring lost functionalities:* An aging population poses a significant challenge to the development of effective restoration of the functionalities of hearing and sight. New research advances in the field of retinal prostheses have produced a 232-channel-neural-stimulator implant, an important advancement in the field of sight restoration to the blind. Advances in auditory restoration have been realized through a digital hearing aid customized to individual variances in the human auditory canal.
- *Electronic neural tissue and bio-molecule interfaces:* Advances are seen in sensor chips for electronic DNA detection, as well as cell-tissue interfaces to record neural activity, and an integrated MRI device that can provide "inside" information at the level of single cells.
- *Prosthetic devices:* The possibility of interfacing electronic devices to our nervous system is essential for basic research leading to the development of therapies for neural degenerative diseases. These interfaces require high reliability, and must be able to work for a long time without additional intervention. New devices with wireless connectivity have been integrated with an increased number of neural signal-channels.

TRENDS IN SENSING

- Integrated-Circuit Sensors are continuously getting smaller, and finding increasing use in a wide variety of applications. Control signals and outputs are becoming almost exclusively digital. Advances in IC technologies are enabling higher levels of integration and signal processing.
- Although advanced IC technologies enable higher levels of integration, they also negatively impact the analog-sensor-interface design. This includes lower power-supply voltages, leaky MOS transistors, higher 1/f noise, higher device-to-device variation, and lower-accuracy device models.
- Sensors continue to penetrate the worlds of both biology and medicine. This includes implantable chips for prosthetic hearing, prosthetic vision, neural stimulation, neural amplification, and even laboratory-on-a-chip magnetic resonance imaging.
- Multi-axis high-performance low-cost inertial sensors, namely accelerometers and gyroscopes, are becoming ubiquitous in the marketplace. They are currently being used in mass-market portable electronics and gaming applications. The handheld market is starting to emerge for high-performance low-cost motion-sensing and navigation devices. The performance of these sensors is continually being improved, while cost is being reduced.

TRENDS in DISPLAY ELECTRONICS

The integrated-circuit (IC) market is continuing to be driven by two major forces: the consumer-electronics demand for the largest brightest most-cost-effective flat-screen technology; and by mobile devices that continually thrive on reduced power and cost, to achieve the highest resolution in the smallest form factor.

In large-size displays, TFT-LCDs are still the dominant technology, with the 8th-generation of TFT manufacturing technology being rolled out in 2006. The main driving factors for the electronics in these displays are high image quality (increasing gray levels, improving response times, and increasing frame rate), and cost reduction (increasing the number of output channels/chip, and reducing die size by shrinking the high-voltage (20V) CMOS technology to <0.18μm, and by improving pad/packaging techniques). As displays increase in size, and resolution increases, power-consumption and high-speed interfaces are becoming important subjects that need to be addressed.

In mobile displays, there is continued driver and panel development for TFT-LCD and OLED display technologies. The market is asking for high resolution (>200ppi), a large number of colors (>16M), high brightness, low power consumption, and, of course, low cost. However, in addition, there are developments to help systems integration, and increase the value-added of what is often the most expensive component in the mobile system. Display drivers and panels are integrating high-speed serial interfaces and adding smart functions (eg scanning, and backlight control using ambient-brightness sensing, touch sensing, and finger-print reading). There is a competition in system partitioning between CMOS display-driver ICs (DDI) working with an amorphous backplane, and low-temperature polysilicon (LTPS) integrating functions such as gate/source drivers, and power supplies onto an LTPS backplane, which now have feature sizes in the 2 micron region.

There are other technologies for both markets, for example, spatial light modulators within projection systems, are being used as a cost-effective technology for extremely large formats. LCOS and digital mirrors are good examples of CMOS-based silicon that compete well with amorphous or polysilicon TFT backplanes. It would be impossible to list, here, all the current display technologies (eg ePaper, field-emission display, …) that are being investigated to fulfill this multi-billion dollar market, as there is a huge research activity in any device that shows potential to radically change the nature and capability of displays. It seems as if the future for display-electronics designers is secure!

TRENDS in IMAGE SENSORS

The image-sensor area is now drawing lots of attention due to the explosive growth of imaging in the semiconductor industry, triggered by a huge camera-phone market (the camera adoption rate for mobile phones is expected to be around 50% by 2006, and over 60% for 2007), and substantially growing markets such as digital cameras, camcorders, automotive applications, and security.

As application areas diversify, requirements for image sensors also increase in terms of low power consumption, small chip size, along with low cost, high integration capability, and high data-transfer rate, all of which favor CMOS image sensors over their CCD competitors. As a matter of fact, CMOS image sensors have already surpassed CCDs in production volume, and have caught up in performance, enabling their penetration into digital-camera and camcorder applications, as well, and it is noticeable that traditional CCD makers in Japan are now shifting their equipment to the CMOS image-sensor area.

The major trends observed in the CMOS image-sensor area are miniaturization, increased frame rates, and increased level of function integration. CMOS image-sensor vendors targeting high-volume applications, such as mobile imaging, continue to offer smaller and smaller pixels to miniaturize the camera modules, and/or to enable increased image quality (resolution). The need for miniaturization has been tremendous due to the thin, light nature of mobile devices, and is a major driving force to attack the sub-2-micron pixel dimension. However, when moving to sub-2-micron pixel sizes, which is in the range of the diffraction limit, new challenges arise in uniformity, noise, etc. Therefore, special processing techniques are essential to compensate for such issues arising from the photodiode area in smaller pixels.

There is also a strong trend toward higher frame rate to accommodate the requirements from camcorders and machine-vision, etc. Higher frequency operation for data treatment in both for the analog and digital domains is a key to realizing real-time image processing for those applications.

Image-sensor-technology trends also include automatically detecting and segmenting fast-moving objects in the scene. This allows the readout of a fast-moving regions-of-interest with much higher frame rate than the rest of the image, which can be read out at typical video rates, (30 frames per second).

Other trends including infrared imaging, and fluorescence imaging, where the challenge is to extract interesting scene information from on top of a very large pedestal signal, are of possibly emerging importance.

NOTES

MEMORY

- **Overview**
- **Featured Papers**
- **Panel**
- **Tutorial**
- **Forum**

ISSCC 2007 – MEMORY

Subcommittee Chair: *Katsuyuki Sato, Qimonda Japan, Tokyo, Japan*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- Clock for 65nm SRAMs for CELL processor targets 6GHz **[18.1]**
- Ultra-low-leakage SRAMs in 65nm, with 2pA/b at retention voltage, using integrated leakage-reduction schemes **[18.2]**
- SRAMs penetrate subthreshold regime with 6T, 8T, and 10T architectures **[18.4, 18.5, 18.6]**
- PRAM breaks new records with 512Mb density, and 266MB/s throughput **[26.1]**
- First 1.8V 1G Multi-Level NOR Flash memory in 65nm, with fastest read and write throughput **[26.3]**
- Largest-capacity (2Mb) Spin-Transfer-Torque-RAM (SPRAM) with optimized performance **[26.5]**
- First high-performance 65nm embedded DRAM in SOI **[27.1]**
- Industry targets known-good-die concept for embedded SRAMs at 65nm **[27.2]**
- First GDDR4 designs press memory bandwidth over 4Gb/s/pin with single-ended interface **[27.4]**

APPLICATIONS AND ECONOMIC IMPACT

- High-frequency SRAM for CELL processor enables high-performance gaming applications **[18.1]**
- Ultra-low-leakage SRAMs for mobile applications with wide operating-voltage range **[18.2]**
- Subthreshold SRAM enables longer battery life for mobile consumer applications **[18.4, 18.5, 18.6]**
- Scalable universal memory (PRAM) with higher level of integration for high-speed non-volatile memory **[26.1]**
- PRAM advances rapidly in density, and performance, to become a viable candidate for high-volume technology **[26.1]**
- Reduction of cost/b for higher-data-rate non-volatile storage applications **[26.3]**
- High-density NOR Flash with fast read and write throughput meets the requirements of mobile applications for code and data storage **[26.3]**
- SPRAM improves write margin, getting closer to product readiness **[26.5]**
- Embedded SOI DRAM satisfies the growing cache requirements of multicore processor designs, and associated performance improvements, for high-performance microprocessors **[27.1]**
- Known-good-die concept reduces test cost in embedded SRAMs, and allows greater level of integration and complexity **[27.2]**
- GDDR4 enables higher-performance graphics while maintaining low-cost system implementation **[27.4]**

PANEL

Ultimate Limits of Integrated Electronics [E1]

This panel will address technology scaling and the future of transistor scaling.

TUTORIAL

Error-Correcting Codes for Memories [T5]

This tutorial will explain how to design a memory ECC to improve yield and resolve soft-error rates

FORUM

Non-Volatile-Memory Circuit Design and Technology [F1]

This Forum will discuss various NVM circuit-design techniques in detail

SRAM Applies Sub-Threshold Regime

A 65nm 8T Sub-V_t SRAM Employing Sense-Amplifier Redundancy [18.4]

MIT

A High-Density Subthreshold SRAM with Data-Independent Bitline Leakage and Virtual-Ground Replica Scheme [18.5]

University of Minnesota

A Sub-200mV 6T SRAM in 0.13µm CMOS [18.6]

University of Michigan

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Low-voltage SRAM operation limited to 600mV
- Process variations degrade minimum operating voltage
- Leakage is the critical factor for energy-scavenging applications

NOVEL CONTRIBUTIONS

- A 65nm 8T SRAM with new sense amplifier operating at 330mV **[18.4]**
- Removes data dependency of bit-line leakage **[18.5]**
- First-reported sub-200mV SRAM in 130nm **[18.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- 330mV SRAM enables low-power operation for consumer applications **[18.4]**
- Ultra-low-power operation for environmental and biomedical sensing applications **[18.6]**

Scalable Phase-Change Memory Advances Rapidly in Density and Performance

A 90nm 1.8V 512Mb Diode-Switch PRAM with 266MB/s Read Throughput. [26.1]

Samsung Electronics

PRESENT STATE OF THE ART *(THE PROBLEM)*

- 100nm is the most-advanced lithography for phase-change RAM (PRAM) reported
- 256Mb is the largest PRAM memory density reported
- 132MB/s fastest read throughput reported for PRAM memory

NOVEL CONTRIBUTIONS

- PRAM fabricated in 90nm process lithography **[26.1]**
- Diode-Switch Cell allows smallest-reported cell size of 0.0467um^2 **[26.1]**
- 266MB/s read throughput achieved **[26.1]**

CURRENT AND PROJECTED SIGNIFICANCE

- PRAM is rapidly advancing in memory size, technology-node reduction, and performance. It is confirmed to be a promising candidate technology for overcoming performance and scalability limits of currently-dominating Flash memories **[26.1]**

NOR-Flash Density and Performance Meets Mobile-Applications Needs

A 65nm 1Gb 2b/cell NOR Flash with 2.25MB/s Program Throughput and 400MB/s DDR interface [26.3]

ST Microelectronics

PRESENT STATE OF THE ART *(THE PROBLEM)*

- 90nm technology commercially available today for NOR Flash in large volumes
- 512Mb largest 1.8V NOR-Flash density reported
- 1.5MB/s fastest programming throughput reported for Flash-NOR
- 266MB/s fastest read throughput reported for Flash

NOVEL CONTRIBUTIONS

- Fabricated on 65nm process lithography **[26.3]**
- 1.8V 1Gb for high-performance mobile applications **[26.3]**
- 2.25MB/s program throughput achieved **[26.3]**
- 400MB/s read throughput through 16b DDR interface **[26.3]**

CURRENT AND PROJECTED SIGNIFICANCE

- Advanced lithography and 2b/cell allow high-performance 1Gb NOR Flash on a 52mm^2 chip significantly reducing cost of memory in most-demanding mobile applications **[26.3]**
- Large improvement in write and read performance keeps pace with application requirements for code and data storage in advanced mobile applications. **[26.3]**

Embedded DRAM Moves Aggressively to SOI

A 500MHz Random Cycle 1.5ns-Latency SOI eDRAM Macro Featuring a 3-Micro-Sense Amplifier [27.1]

IBM

PRESENT STATE OF THE ART *THE PROBLEM)*

- Embedded DRAM macros are limited to bulk CMOS technology
- State-of-the-art today is 3 to 4ns random cycle with 4 to 5ns latency
- Complementary 11-transistor cross-coupled sense amplifiers in use today

NOVEL CONTRIBUTIONS

- First-reported SOI embedded-DRAM macro **[27.1]**
- Fabrication in 65nm process lithography **[27.1]**
- 500MHz random cycle using novel 3-transistor micro-sense amplifiers **[27.1]**

CURRENT AND PROJECTED SIGNIFICANCE

- Advanced technologies such as SOI enable higher-performance and lower-power memory **[27.1]**
- Higher levels of integration not previously available for high-performance microprocessors **[27.1]**
- Increased cache size will simultaneously extend microprocessor performance and reduce power **[27.1]**

Graphics DRAM Presses Memory Bandwidth

An 80nm 4Gb/s/pin 32b 512Mb GDDR4 Graphic DRAM with Low-Power and Low-Noise Data-Bus Inversion [27.4]

Samsung Electronics

A 2.5Gb/s 512Mb GDDR3/GDDR4 SDRAM with Phase Tolerant Latency Control [27.5]

Micron Technology

PRESENT STATE OF THE ART *(THE PROBLEM)*

- 1.6Gb/s/pin is current GDDR specification
- Data-bus inversion is currently not used

NOVEL CONTRIBUTIONS

- Enhanced-Majority-Voter circuit used to trigger data-bus inversion **[27.4]**
- Innovative circuit techniques for latency control **[27.5]**

CURRENT AND PROJECTED SIGNIFICANCE

- Enhanced video-gaming performance **[27.4]**
- Higher data rates and improved system performance **[27.5]**

Panel

Ultimate Limits of Integrated Electronics

Organizer: ***Nicky Lu****, Etron Technology*
Co-Organizer: ***CK Wang****, National Taiwan,*
Co-Organizer/Moderator ***Philip Wong****, Stanford University,*
Co-Organizer: ***Sreedhar Natarajan****, Emerging Memory Technologies,*

OBJECTIVE

- To debate the existence and nature of limits of technology due to natural laws
- To investigate the limits of the current evolutionary approach, as predicted by Moore's or Huang's laws, and of revolutionary approaches involving hierarchical studies, ranging from circuits to devices, to materials, to fundamental limits and back to system requirements

CHALLENGE

- Huang's law predicts that the capacity of NAND Flash will double every year. Based on such continued technological progress (with 10nm demonstrated already), the industry will soon reach limits using today's evolutionary CMOS-scaling approach. We will need alternative solutions.
- With such business challenges and only obscure technological solutions ahead, can our IC industry thrive with sufficient profit margins, while enduring the need for huge capital investments and escalated design expense?
- How can the industry reach 2.5nm? Will it ever? For how long?

CONTROVERSY

- The limits of scaling are application-dependent: At which technology node will CMOS-scaling stop working for each targeted application?
- What are the largest obstacles and limitations of devices, and how can circuit design change in the face of these contingencies?
- How can system architecture extend the life of CMOS, and will multi-dimensional die-integrated system-chips (SC) help extend technological progress from IC toward SC?
- What applications (new or existing) will be the economic drivers, and what business models and industrial/academic infrastructures are most suitable for these applications to enable sufficient ROI?

Tutorial

Error-Correcting Codes Design for Memories

Takayuki Kawahara, Hitachi, Kokubunji, Tokyo, Japan

OVERVIEW

Today's memories are increasingly susceptible to cosmic-ray-induced ("soft") errors. In addition, lowering voltage can increase circuit errors by reducing noise margins. Error-Correcting Code (or Error-Checking and Correcting) (ECC) can help solve both these problems by adding redundancy that allows recovery from errors. The application of ECC to soft-error reduction is well known, but ECC has recently also been used for the additional purpose of improving margins. This Tutorial, starting from the basic Shannon's theorem, explores the need for ECC in nano-scale CMOS, soft errors in memory, and basic coding techniques such as Hamming code, cyclic code, and BCH code. It covers these topics in the context of modern memory, and their effects on the performance advancing memory. The techniques presented are also applicable for application to high-speed logic LSI.

SPEAKER BIOGRAPHY

Takayuki Kawahara is a chief researcher at the Central Research Laboratory, of Hitachi. Since joining the laboratory in 1985, he has made fundamental contributions in many areas in the field of low-power memories, including subthreshold-current reduction by using gate-source self-reverse biasing, an over-drive sense-amplifier scheme, and charge-recycling. Currently, his responsibility is to explore a new conceptual memory. He received the B.S. and M.S. degrees in physics in 1983 and 1985, and the Ph.D. degree in electronics in 1993 from Kyushu University, Fukuoka, Japan.

FORUM

Non-Volatile-Memory Circuit Design and Technology

Objective

This all-day Forum is dedicated to Non-Volatile-Memory (NVM) design and technology, addressing a broad range of issues and solutions for traditional and emerging memories. A technology overview of current electron-storage-type memory cells, and emerging non-electron-type non-volatile memories will lay down the foundation for discussion of the circuit-design challenges, issues, and solutions.

Audience

The targeted participants are circuit-design and test engineers working on advanced non-volatile memory, as well as others in the technical community having a circuit- or technology-based interest in understanding design techniques and technologies.

Scope

Solid-state non-volatile memories have seen explosive growth in the last few years in all electronics applications such as memory cards, cell phones, still and video cameras, digital music, video players, and other consumer-electronics devices. With the memory cost-per-bit reducing at very aggressive rates, the industry is seeing even more solid-state non-volatile memory applications emerging, such as disk caches, and solid-state disks for use in personal and portable computers. Application requirements for low-cost, low-power, high-performance non-volatile memory, and major challenges associated with aggressively-scaling process technologies have driven the industry to many new circuit-design, architecture, and technology innovations.

Many circuit-design and architectural innovations have been developed over the years to overcome scaling challenges and improve performance on established non-volatile memory technologies. In addition, new circuit and architecture developments are required to design a memory utilizing the new cell types and structures. Multi-level design, multi-bit design, and on-chip read/write buffer architectures, are just a few examples.

The Advanced-Circuits Forum on Non-Volatile Memory will first present an overview of floating-gate-type non-volatile memory cells and structures, along with recent advancements in possible extensions of electron storage with new material types, as well as non-electron storage type cells. Many of the circuit-design techniques for each memory type are unique to the memory technology. This Forum will describe the design challenges and issues and the corresponding circuit designs and architectures to implement the various non-volatile memory designs.

Program

The Forum will begin with an overview of non-volatile memory (NVM) technology, including cell structures and device-physics principles associated with reading, programming, and erasing the memory cell. **Al Fazio** (Intel) will cover electron-storage-type non-volatile memory technologies, such as NAND Flash, NOR Flash, and NROM. This will include state-of-the-art technologies, as well as new technologies to extend the scalability of electron-storage NVM. He will then go on to discuss emerging memory types and alternatives to electron-storage structures, such as PRAM, MRAM, and FeRAM, and their corresponding read, write, and erase operations. This talk will lay down the foundation for an extensive look at circuit and architecture design for each memory type.

Kerry Tedrow (Intel) will describe circuit design and chip architectures required to realize a NOR-Flash memory design. NOR-Flash memory is well-suited for applications that require fast random access for code execution as well as data storage. Many challenges will be discussed, those associated with sensing circuits used to achieve fast random access, along with multi-level-cell storage. Different chip architectures will be discussed that describe implementation of designs that achieve simultaneous read and program operations.

NAND-Flash memory design presents quite different design challenges when compared to NOR-Flash. NAND-Flash memory is typically used in applications needing high-density storage, high-performance read and program throughput times, at a low cost per bit. **Tomoharu Tanaka** (Micron) will present circuit-design challenges and techniques used to design NAND-Flash memory along with design and architectures needed to address scaling issues, as new NAND-Flash technologies are being developed for aggressive cell-size reduction at historic rates. Multi-level-cell design has further reduced the bit cost. Circuits, architectures, and challenges associated with more-complex multi-level-cell designs, will also be presented.

NAND and NOR Flash-type cell structures have been the workhorse of non-volatile memories for the past three decades. Other electron-storage devices utilize a different material type at the electron-storage node. **Yair Sofer** (Saifun Semiconductors) will present NROM circuit design. This technology uses a nitride material that stores electrons in two separate regions to achieve a novel 2-bit-per-cell design. Design techniques that achieve regular multi-level operation will be discussed. Combining the novel 2-bit-per-cell architecture with regular multi-level storage can achieve 4 bits per cell memory storage. These design techniques will also be discussed.

Flash memory is well-suited for system-on-a-chip with a process technology that can combine Flash technology with logic technology. **Hideto Hidaka** (Reneses) will present embedded-Flash memory design for applications that are well-suited for a monolithic chip that requires on-chip non-volatile memory for both code storage and data. Flash-memory design in these types of chip typically execute code directly out of the Flash memory requiring fast sensing schemes along with large bandwidth out of the memory array.

Shine Chung (TSMC) will discuss circuit-design techniques for emerging memory types, such as PRAM, MRAM, as well as other non-electron storage cells, such as FeRAM. For these memory types, the cell structure and operation is quite different than traditional electron-storage-type memories. This presents a new set of design challenges. Major differences in array architecture require different implementations of decode circuits, and sensing circuits compared to the traditional electron-storage type memory cells.

The various non-volatile memory types have attributes that make them suitable for different applications. NAND-Flash memory has been the memory of choice for mass-storage applications, such as MP3 players and digital cameras. NOR-flash memory, with fast random access is well suited for portable devices, like cellular phones and Personal Digital Assistants, due to the attribute of fast random access for Execute-in-Place code applications. Our final speaker, **Koji Suki** (Sony) will discuss various non-volatile memory applications available today, and potential new applications on the horizon. He will discuss how the emerging memory types will function in today's applications, or potentially drive new applications due to the memory's unique attributes.

NOTES

RF

- **Overview**
- **Featured Papers**
- **Special-Topic Session**
  (co-sponsored by Analog/Data Converters/RF)
- **Tutorial**
- **Forum**
  (co-sponsored by RF/Wireless)
- **Trend Chart**

ISSCC 2007 – RF

Subcommittee Chair: *John R. Long, Delft University of Technology, The Netherlands*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- High-efficiency digital-to-RF power amplifier concept **[4.1]**
- Closed-loop impedance-mismatch-protection circuit for CMOS power amplifiers **[4.2]**
- Feed-forward filtering technique to cancel interferers in a radio receiver **[4.4]**
- Millimeter-wavelength (60GHz) combined with milliwatt power consumption demonstrated by CMOS receiver front-ends [**10.1, 10.2]**
- CMOS on-chip voltage-controlled oscillators (VCOs) break the100GHz barrier, with the demonstration of a Colpitts oscillator **[10.7]**
- SiGe BiCMOS phased-array receiver capable of beamforming (with a phased-array antenna) at 60GHz **[10.8]**
- Novel broadband (10GHz bandwidth) beamforming technique reusing a delay-line, significantly reduces area and cost **[23.5]**
- Clever re-use of a delay-line significantly reduces size and cost of a steerable-beam antenna for radio imaging **[23.5]**
- Highly integrated silicon-based radar IC at 79GHz **[23.7]**

APPLICATIONS AND ECONOMIC IMPACT

- Near doubling of power-amplifier efficiency compared to today's technology for 64QAM OFDM signals **[4.1]**
- Ability to sustain a 20:1 load-standing-wave ratio (VSWR) at full output power in a CMOS power amplifier **[4.2]**
- Over 20dB of blocker suppression is a step toward the realization of a radio receiver without expensive off-chip passive filtering **[4.4]**
- Low-cost of CMOS technology opens the door to use of millimeter-wave frequency bands (e.g., in the 60GHz-band, worldwide) for gigabit-rate wireless in portable consumer electronic **[10.1, 10.2]**
- Phased-arrays used for high-gain steerable-beam antennas is an enabling technology for Gb/s wireless communication at frequencies above 20GHz **[10.8]**
- Low-cost CMOS solutions enable the use of high-frequency radio waves for imaging in applications such as tumor detection (medical) and weapon/explosives detection (homeland security) **[23.5]**
- Widespread adoption of automotive radars for collision detection and avoidance will save lives **[23.7]**

SPECIAL-TOPIC SESSION

(Co-sponsored by Analog/Data ConvertersRF)

Digitally-Enhanced Analog & RF [SE1]

Self-calibration of transceivers can dramatically improve performance and lower the costs and testing time of highly-integrated radio-frequency ICs. Self-Calibration is becoming essential for portable handsets integrating multiple applications with state-of-the-art performance.

TUTORIAL

CMOS Front-End-Circuit Design [T6]

CMOS technology dominates the high-volume and highly-integrated market for portable wireless devices. Receiver circuits in CMOS for RF applications will be described.

FORUM

(Co-sponsored with RF/ Wireless)

GIRAFE: Power-Amplifiers and Transmitter Architectures [F3]

Power amplifiers have resisted integration with other transceiver circuits in cellular mobile applications. This Forum will focus on the latest trends in power-amplifier and transmitter architectures, including design concepts amenable to integration in silicon technologies.

Radio-Frequency Circuits Enable Compact Low-Cost Feature-Rich Phones

A Digitally-Modulated Polar CMOS PA with a 20MHz Signal BW [4.1]

Stanford University

A 3W 55%-PAE CMOS PA with Closed-Loop 20:1 VSWR Protection [4.2]

University of Catania; STMicroelectronics

A Blocker-Filtering Technique for Wireless Receivers [4.4]

Broadcom

PRESENT STATE OF THE ART

- Modern digital-modulation formats demand linear power amplifiers in order to meet stringent spectral (FCC) regulations.
- Linear power amplifiers are difficult to operate with efficiencies above 20%.
- CMOS is usually not rugged enough to operate reliably under high output-mismatch conditions (e.g., antenna disconnection)
- Demand for higher data rates and seamless mobility raise the bar on receiver performance

NOVEL CONTRIBUTIONS

- Constant-envelope digital-to-RF power-amplifier (PA) concept **[4.1]**
- Closed-loop output-impedance-mismatch protection circuit **[4.2]**
- Feed-forward filtering technique to cancel interferers **[4.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- Near doubling in PA efficiency for 64QAM OFDM signals. **[4.1]**
- Ability to sustain a 20:1 load standing-wave ratio (VSWR) at full output power in a CMOS PA **[4.2]**
- Over 20dB of blocker suppression provides a step towards a receiver without off-chip passive filtering **[4.4]**

mm-Wave Transceivers and Building Blocks

A mm-Wave CMOS Heterodyne Receiver with On-Chip LO and Divider [10.1]

University of California at Los Angeles

A 23-to-29GHz Differentially-Tuned Varactorless VCO in 0.13μm CMOS [10.4]

Delft University of Technology

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Integration of RF front-ends in silicon CMOS is limited by device speed and design skill at frequencies above a few GHz. Development of deep sub-micron CMOS (below 130nm) has pushed device gain-bandwidth limits above 100GHz, opening the door to new design techniques for integrating very-high-frequency transceiver sub-systems in MOS.

NOVEL CONTRIBUTIONS

- First receiver circuits realized at 60GHz in digital CMOS **[10.1, 10.2, 10.8]**
- Unprecedented tunability above 24GHz for a VCO **[10.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- Enables low-cost short-range Gbit/s-data-rate communications for portable devices in millimetre-wave frequency bands (e.g., 57 to 62GHz) **[10.1, 10.2, 10.8]**
- Low-power high-performance local oscillator at extremely-high frequency (20+GHz) **[10.4]**

Low-Cost Radars Aimed at Cars and Security

A Monolithic 4-Channel UWB Beam-Former in 0.13µm CMOS Using a Path-Sharing True-Time-Delay Architecture [23.5]

University of Southern California

A 79GHz SiGe-Bipolar Spread-Spectrum TX for Automotive Radar [23.7]

Infineon; Vienna University of Technology

A 75GHz PLL in 90nm CMOS [23.8]

National Taiwan University

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Sub-systems are implemented using discrete components and ICs in technologies such as GaAs, with low levels of integration.
- High-cost of current technologies prohibit consumer applications.

NOVEL CONTRIBUTIONS

- Novel technique for beamforming re-uses a delay line to significantly reduce size and cost of a steerable-beam antenna **[23.5]**
- Highly integrated silicon-based demonstrators using production technologies **[23.5, 23.7, 23.8]**

CURRENT AND PROJECTED SIGNIFICANCE

- Low-cost CMOS solutions enable the use of high-frequency radio waves for imaging, in applications such as homeland security **[23.5]**
- Enables the widespread commercialization of automotive radars for collision detection and avoidance. Excellent accuracy is possible up to 100m distance when traveling at 100km/h **[23.7]**

SPECIAL-TOPIC SESSION

Digitally-Enhanced Analog & RF

Organizers: ***Kari Halonen,*** *Helsinki University of Technology, Espoo, Finland*
Stefan Heinen, *Infineon Technologies, Germany*
Chair: ***Robert Neff,*** *Agilent Technologies, Santa Clara, CA*

OVERVIEW

As CMOS chip technologies scale to finer line widths, smaller devices, and lower voltages, the job of the analog-circuit designer is getting harder every year. Analog-circuit targets are harder to achieve with larger device mismatch, non-ideal device characteristics, and less voltage available for design. At the same time, scaled technologies reduce power and area for digital circuits, and modern design tools make digital signal-processing and control lower in cost every year. The trends promise the displacement of high-linearity high-accuracy challenging-to-design analog circuits by lower-cost lower-performance analog, enhanced by digital signal-processing. The final achievement goal is better performance, at lower cost and lower design time.

CHALLENGE

- Where can digital assist analog?
- How can digital improve linearity and speed performance of analog-to-digital and digital-to-analog converters?
- How can digital improve linearity performance and yield for power amplifiers and direct-digital-synthesis systems?
- How does digital enhance widely-tunable multi-standard radios in cell-phone and Wi-Fi applications?

RECAP

Four experts with backgrounds in analog-circuit design, analog-to-digital converters, power amplifiers, and radio systems, will address the widening breadth of applications where digital signal-processing, control, and calibration, techniques enhance analog applications with performance, yield, and design-time improvements.

Tutorial

CMOS Frontend-Circuit Design

Marc Tiebout, Infineon Technologies, Villach, Austria

OVERVIEW

After a general introduction covering RF-communication-system aspects and relevant definitions, the Tutorial covers CMOS RFIC design of low-noise amplifiers (LNA), and downconversion mixers. First the modeling of CMOS devices, including noise sources, will be presented. Next, LNA and mixer design is presented from specifications to discussions of detailed topology including all relevant aspects, such as impedance matching, noise figure, gain, bandwidth, linearity and low voltage design, without forgetting the crucial and critical RF ESD-protection of LNAs. The circuits are illustrated through many measured testchip case studies aiming at RF standards from 1 to 20GHz.

SPEAKER BIOGRAPHY

Marc Tiebout received the M.S. degree in Electrical and Mechanical Engineering in 1992 from the Katholieke Universiteit, Leuven, (Belgium), and the Ph.D. degree in Electrical Engineering from the Technical University of Berlin, in 2004. In 1993, he joined Siemens Corporate Research and Development, Microelectronics, in Munich (Germany), designing analog integrated circuits in CMOS and BiCMOS technologies. In 1997, he started the design of radio-frequency devices and building blocks in sub-micron CMOS technologies. From 1999 to 2005, he was with Infineon Technologies, Munich, (Germany), where he worked on RFCMOS circuits and transceivers for cellular-wireless-communication products, and conducted highest frequency RFCMOS research for 17 and 24GHz applications. Since March 2006, he has been with Infineon Technologies, Villach, (Austria), acting as concept engineer for UWB analog & RF development. His main interest is low-power high-frequency circuits and systems in CMOS. Marc Tiebout serves as a member of the Technical Program Committees of ISSCC and of ESSCIRC. He has authored and coauthored more than 30 IEEE publications.

GIRAFE FORUM

Power Amplifiers and Transmitter Architectures

Objective

This all-day Forum will investigate and discuss new trends in power amplifiers and transmit architectures for wireless communications, and their dependency on the standards to be supported.

Attendance is limited, and pre-registration is required. This all-day Forum encourages open interchange.

Audience

The targeted participants are circuit designers and concept engineers working on wireless transmitters or power amplifiers, who want to learn about the latest developments in system and circuit design.

Scope

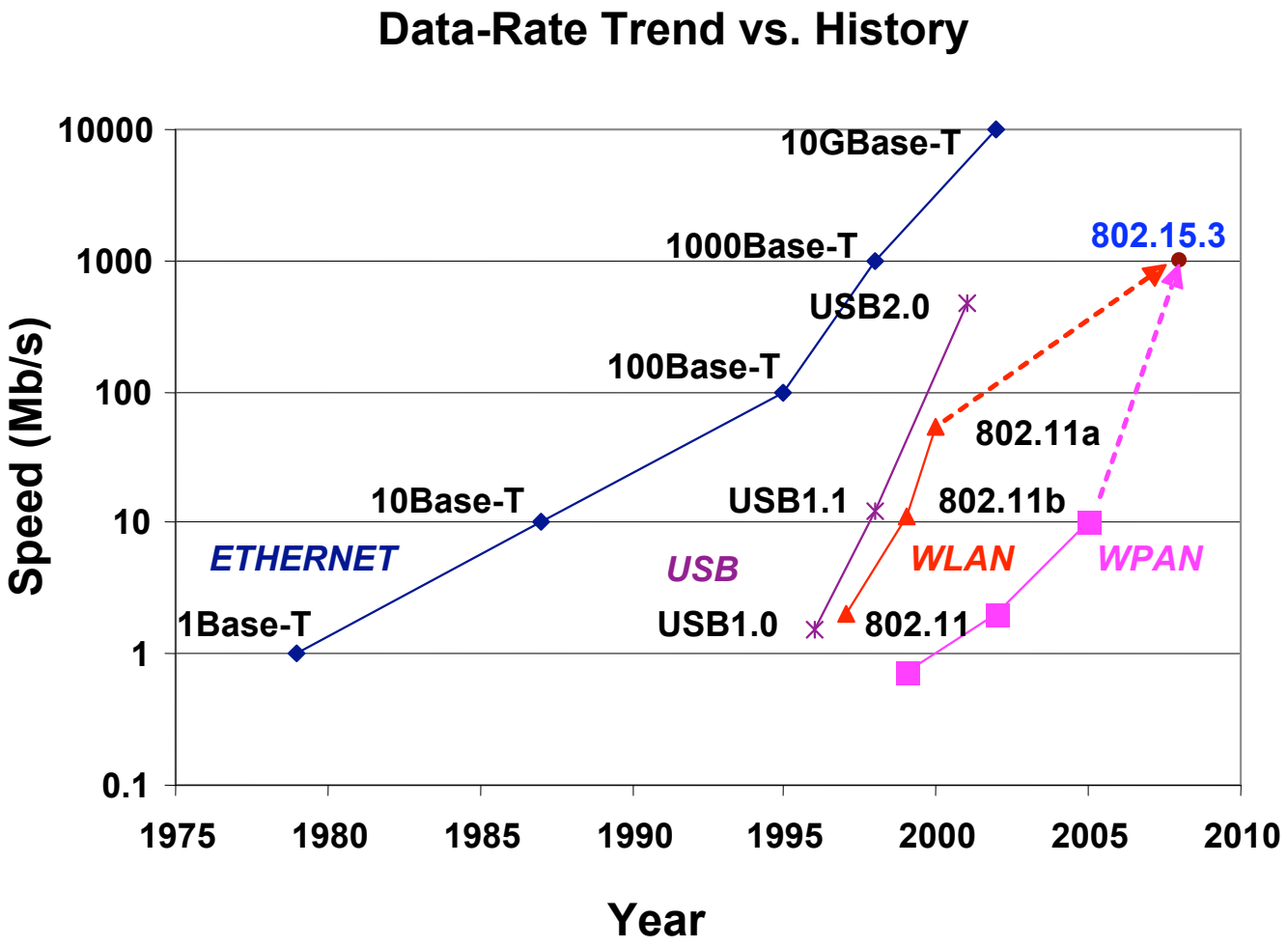
Mobile phones are evolving from single-standard voice phones to multi-standard multi-band multi-application mobile terminals. High integration levels plus re-configurability of the signal-processing chain are a must for those all-in-one-phones to minimize chip area and cost, but have so far only been demonstrated in transceivers. For entry-level phones single-chip transceiver and baseband integration is a reality, now. Power amplifiers, however, have so far been resisting this trend, at least in cellular applications. One PA per band and per standard will be too bulky and too expensive for future terminals. Future PAs must be reconfigurable to support several standards. Silicon integration is a requirement for "intelligent" Pas, and is promising cost reduction over 3/5 compound-constructed PAs, but can it handle the power levels and peak voltages of cellular phones? A variety of PA architectures promise high PAE under certain conditions. For power-effective concepts, it is, however, no longer sufficient to optimize the PA alone. Rather, co-development and common optimization of transmitter, PA, and power supply, is required. This Forum will highlight the latest trends in PA and transmitter design and architectures.

Program

The morning session begins with an introduction to the topic by **David Su (**Atheros Communications). The second speaker, **Earl McCune** (Panasonic), will discuss transmit architectures, their impact on the PA concept, and show practical results for various approaches. The third and last speaker of the morning session, **David Pehlke** (Silicon Labs), will look in detail into a variety of PA concepts and linearization techniques, and explain their tradeoffs.

The afternoon session will be opened by **Lawrence Larson** (UC San Diego), who will show how the various power-supply modulation schemes can be used to enhance PA efficiency. Special attention will be given to OFDM applications. The fifth speaker, **Gene Tkachenko** (Skyworks Solutions), will cover technology requirements and solutions for cellular PAs and frontend modules. The effects of critical system parameters on technology choice will be explained. Finally **Ali Hajimiri** (Cal Tech), will show novel circuit concepts enabling CMOS integration of power amplifiers, even for GSM.

The Forum will conclude with a panel discussion, where the attendees have the opportunity to ask questions and to share their views.



This data-rate Trend Chart projects the capabilities of wireless and wireline datacom technologies, using current standards. Millimeter-wave frequency bands (e.g., 60GHz) are a potential disruptive technology, enabling gigabit/s data rates over a short-range wireless link at speeds well over 1Gb/s.

NOTES

SIGNAL PROCESSING

- **Overview**
- **Featured Papers**
- **Special-Topic Session**
- **Tutorial**

ISSCC 2007 – SIGNAL PROCESSING

Subcommittee Chair: *Wanda Gass, Texas Instruments, Dallas, TX*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- GSM baseband radio integrates power-management circuits and memory with RF, digital, and analog baseband functions **[14.6]**
- First-reported 3x3 MIMO PHY/MAC processor **[14.7]**
- First implementation of a real-time 3D-display processor with a programmable 3D-graphics-rendering engine **[15.4]**

APPLICATIONS AND ECONOMIC IMPACT

- GSM baseband-radio development enables 3-chip cell-phone solution **[14.6]**
- Applications for GSM chip include low-cost basic cell-phones for emerging economies **[14.6]**
- 802.11n-compliant chip enables new applications via increased range and throughput (e.g., high-definition-multimedia-content streaming) **[14.7]**
- The synergic coupling of a 3D-display processor and a programmable rendering engine, which supports advanced functionalities, provides, viewers with true reality in real-time **[15.4]**

SPECIAL-TOPIC SESSION

Automotive Signal-Processing Technologies [SE4]

Automotive requirements will drive next-generation signal-processing technology

TUTORIAL

Vector Processing as an Enabler for Software-Defined Radio in Handsets [T7]

Software-Defined Radio enables the interoperability of multiple wireless standards

New Chip Enables Low-Cost Cell Phones

A GSM Baseband Radio in 0.13μm CMOS with Fully-Integrated Power Management [14.6]

Infineon Technologies

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Most cellular phones separate digital, analog, RF, and power-management functions into multiple chips.
- Multiple-chip solutions increase total system cost.
- Handset cost remains a barrier to subscriber growth in emerging economies.

NOVEL CONTRIBUTIONS

- Integrates power-management circuits and memory with RF, digital, and analog baseband functions. **[14.6]**
- Addresses electrical and thermal-coupling challenges of integrating power-management functions on-chip. **[14.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- Reduces cell phone to 3-chip solution. **[14.6]**
- Applications include low-cost basic cell phones for emerging economies. **[14.6]**

"n"-abling the Future of WLAN

An Integrated Draft 802.11n-Compliant MIMO Baseband and MAC Processor [14.7]

Atheros Communications

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Existing WLAN standards (802.11 a/b/g) have limited range and throughput which constrain their utility for next-generation applications (e.g., streaming high-definition multimedia content).
- Existing WLAN solutions utilize single data-stream and limited receiver-diversity.

NOVEL CONTRIBUTIONS

- First-reported 3x3 MIMO PHY/MAC processor. **[14.7]**
- Draft 802.11n-compliant.**[14.7]**
- Highest-reported WLAN data rate (300Mb/s). **[14.7]**
- Longest-reported WLAN range (700feet). **[14.7]**

CURRENT AND PROJECTED SIGNIFICANCE

- Represents the future of 802.11 WLAN technology. **[14.7]**
- Enables new applications via increased range and throughput (e.g., high-definition-multimedia-content streaming). **[14.7]**
- Dramatically improves the utility of WLAN in emerging markets with limited wired infrastructure. **[14.7]**

High-Resolution 3D-Display Processor

A 36-fp/s SXGA 3D-Display Processor with a Programmable 3D-Graphics Rendering Engine [15.4]

KAIST

PRESENT STATE OF THE ART *(THE PROBLEM)*

- 3D-graphics hardware for various multimedia devices has developed tremendously in recent years, but true 3D reality is not being provided to users due to insufficient computing power, and the lack of depth-perception of 2D displays.
- The technologies of 3D display are a probable next-generation development. However, only preprocessed static pictures and video data have been visualized since complex image-processing is required to synthesize required output images from two different view-images and a disparity-map.

NOVEL CONTRIBUTIONS

- The first implementation of a real-time 3D-display processor with a programmable 3D-graphics rendering engine **[15.4]**
- 3D-display processor synthesizes SXGA (1280x1024) output images at interactive rates of 36 frames/s **[15.4]**
- The synergetic coupling of the 3D-display processor and the rendering engine provides true reality in real-time interactive 3D applications such as games and GUI **[15.4]**
- The integrated 3D-rendering engine supports Pixel-Shader 3.0 and OpenGL ES 2.0. **[15.4]**

CURRENT AND PROJECTED SIGNIFICANCE

- The synergic coupling of the 3D-display processor and the programmable rendering engine, which supports advanced functionalities, provides viewers with true-reality in real-time. **[15.4]**

SPECIAL-TOPIC SESSION

Automotive Signal Processing Technologies

Organizer: **Toru Shimizu**, Renesas Technology, Tokyo, Japan
Chair: **Ram Krishnamurthy**, Intel, Hillsboro, OR

OVERVIEW

- The automobile has become much more than a means of traveling from point A to point B. Today's automobiles are complex signal-processing environments that bring together a wide variety of innovative systems including user-friendly interfaces, multimedia-content delivery, real-time sensing / control, and networking. This Special-Topic Session presents some of the exciting trends and emerging technologies for future automotive signal-processing systems.

OBJECTIVES

- To describe some of the emerging trends and semiconductor technologies for future automotive electronics.
- To present test methodologies for safety-critical automotive applications.
- To discuss signal-and-media-processing technologies for engine control and car-information systems.
- To review vision-processing architectures for advanced driver-assistance systems.

CHALLENGES

- What are some of the key trends and semiconductor technologies for future automotive electronics?
- How do we design efficient test methodologies for safety-critical automotive systems?
- What are some of the emerging signal-, media-, and vision-processing technologies for advanced automotive-information systems?

STRUCTURE

Masayuki Hattori, Toyota, will present "Future Semiconductor Technologies for Next-Generation Car Electronics".

Recent automotive systems require high-performance for control of the environment, the safety, the security, and the entertainment, of passengers. This presentation discussion will cover advanced electronics technologies for next-generation cars for which goals include perfect driver safety, low fuel consumption, and clean exhaust.

Hari Pendurty, Texas Instruments, will present "CPU Application Self-Test Using Logic BIST for Automotive Devices". Safety-critical automotive applications, such as anti-lock-brake controllers, require a self-test of CPU cores while the application is running. This presentation will discuss the Built-In Self-Test (BIST) technology applied to increase the dependability of automotive systems.

Toru Baji, Renesas Technology, will present "Micro-Brains and Muscles for Automotive Electronics".

MCUs and DSPs are used in a wide range of automotive applications. This presentation will focus on two application areas, namely engine control and car-information systems, where higher levels of signal-processing technologies are applied.

Kurt Sievers, NXP Semiconductors, will present "Vision Processing for Advanced Driver-Assistance Systems".

Advanced driver-assistance systems use radar and infra-red technologies. This presentation will discuss vision-processing architectures for applications such as lane-departure warning, traffic-sign recognition, and headlight-beam assist.

RECAP

This Session will provide ISSCC attendees with an introduction to, and overview of, some of the key trends and technologies for future automotive signal-processing systems.

Tutorial

Vector processing as an enabler for Software-Defined Radio in Handsets

Kees van Berkel, NXP Semiconductors, Eindhoven, The Neterlands

OVERVIEW

- Wireless-radio standards (for cellular, broadcast, connectivity, and positioning) are proliferating rapidly, and evolving continuously.
- Software-Defined Radio (SDR) promises multi-standard and multi-channel operation, and supports product differentiation and evolution.
- Vector DSPs offer the required flexibility and high GOPS for baseband processing, at acceptable power levels.
- Vector DSPs for SDR, ranging from existing products to research prototypes, will be reviewed.

SPEAKER BIOGRAPHY

Kees van Berkel is currently a **Fellow** at NXP Semiconductors in Eindhoven, The Netherlands. He is involved in the design of hardware-software architectures for applications in software-defined radio, focusing on low-power and programmability. He received his PhD degree in Computer Science from the Eindhoven University of Technology, Computer Science and Mathematics, located in Eindhoven, The Netherlands, in 1992.

NOTES

TECHNOLOGY DIRECTIONS

- **Overview**
- **Featured Papers**
- **Special-Topic Session**
- **Tutorial**
- **Forum**

ISSCC 2007 – TECHNOLOGY DIRECTIONS

Subcommittee Chair: *Anantha Chandrakasan, MIT, Cambridge, MA*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- First microsystem combining energy scavenging from thermal and RF sources **[3.1]**
- First closed-loop system tracking the minimum-energy operating voltage with embedded high-efficiency DC-to-DC converter **[3.2]**
- Complementary-type carbon nanotube transistors are demonstrated, enabling CMOS-like logic gates **[3.4]**
- The advantage of using carbon nanotubes rather than ultra-scaled CMOS transistors is quantified in terms of a maximum 2x better FO4-delay improvement and 30x better average energy-delay product (EDP) **[3.5]**
- An ultra-thin (< 300μm) e-paper display with high-speed response (< 0.2ms) is demonstrated **[3.7]**
- Lowest-power capacitive chip-to-chip interconnect, uses 0.08pJ/b **[20.1]**
- Lowest-power inductive chip-to-chip interconnect uses 0.14pJ/b **[20.2]**
- Adaptive Software-Defined Radios (SDRs) achieve up to 40% lower energy through run-time quality-of-service and energy management **[32.1]**
- See-through imaging camera using passive detection of millimeter and submillimeter waves, with amplifiers operating up to 300GHz **[32.3]**

APPLICATIONS AND ECONOMIC IMPACT

- Highly-energy-efficient circuits enable battery-less systems for ultra-low-power portable devices **[3.1, 3.2]**
- Carbon-nanotube devices offer better performance than 32nm CMOS transistors **[3.5]**
- Optimized carbon-nanotube circuits can compete in performance with ultra-scaled CMOS **[3.5]**
- Flexible electronic paper enables new and exciting application areas **[3.7]**
- Data links demonstrated to consume sufficiently less power, compete with ohmic-contact 3D technology **[20.1 and 20.2]**
- Lower cost through Software-Defined Radios (SDRs), and lower energy through continuous adaptation of the SDRs' quality-of-service and energy-management **[32.1]**
- Enabling chip-scale compact high-resolution millimeter and submillimeter camera for see-through-imaging applications **[32.3]**

SPECIAL-TOPIC SESSION

Circuit Design in the Year 2012 [SE2]
Highlights of IEDM 2006 [SE5]

TUTORIAL

Organic-Transistor Circuit Design [T8]

FORUM

Design of 3D-Chipstacks [F2]

Energy Harvesting and Minimum-Energy Tracking

Efficient Power-Management Circuit: Thermal Energy Harvesting to Above-IC Microbattery Energy Storage [3.1]

CEA LETI; CEA LITEN

Minimum-Energy Tracking Loop with an Embedded DC-to-DC Converter Delivering Voltages Down to 250mV in 65nm CMOS [3.2]

Massachusetts Institute of Technology

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Need for energy-autonomous devices operating with energy scavenged from the environment for use in wireless sensor networks, RFID tags, health-monitoring systems, and ambient-intelligence applications
- Minimizing energy consumption by dynamically tracking the optimum supply voltage of a digital circuit with changing workload and operating conditions

NOVEL CONTRIBUTIONS

- First microsystem combining energy scavenging from thermal and RF sources, together with a DC-to-DC converter, power-supply management, and charge/discharge monitoring of a microbattery integrated above the IC **[3.1]**
- First closed-loop system tracking the minimum-energy operating voltage of a 65nm digital circuit, and embedding a DC-to-DC converter for delivering voltages as needed, as low as 250mV, from a 1.2V supply, with a power efficiency better than 80% for a typical 1μW workload **[3.2]**

CURRENT AND PROJECTED SIGNIFICANCE

- Highly-energy-efficient circuits enable battery-less systems for ultra-low-power portable devices **[3.1, 3.2]**

First Circuits Based on Carbon Nanotubes

Gate-Work-Function Engineering for Nanotube-Based Circuits [3.4]

IBM

Carbon-Nanotube Transistor Circuits: Circuit-Level Performance Benchmarking and Design Options for Living with Imperfection [3.5]

Stanford University, University of Southern California

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Most state-of-the-art carbon-nanotube devices present ambipolar characteristics that make them difficult to use in practical circuit applications
- The circuit design community does not have a clear idea of how carbon nanotubes could improve circuit performance when compared with ultra-scaled CMOS transistors
- No circuits have yet been demonstrated using carbon nanotubes
- The impact on circuit performance of metallic carbon nanotubes, which are randomly mixed with semiconducting ones, is not yet clear

NOVEL CONTRIBUTIONS

- Complementary-type carbon-nanotube transistors are demonstrated, which enable CMOS-like logic gates. **[3.4]**
- The first 5-stage ring oscillator featuring CMOS-type carbon nanotubes is demonstrated. The circuit oscillates at 72MHz with a power supply of 1.04V. The oscillation frequency is limited by the presence of about 11fF of parasitic capacitances. **[3.4]**
- The advantages of using carbon nanotubes instead of ultra-scaled CMOS transistors are quantified in terms of a maximum 2x FO4-delay improvement and 30x better average energy-delay product (EDP) **[3.4, 3.5]**

CURRENT AND PROJECTED SIGNIFICANCE

- Carbon-nanotube devices offer better performance than 32nm CMOS transistors. **[3.5]**
- Optimized carbon-nanotube circuits can compete in performance with ultra-scaled CMOS **[3.5]**

Powder-in-Air Realizes Flexible e-Paper

Passive-Matrix Flexible Electronic Paper Using Quick-Response Liquid-Powder Display (QR-LPD) Technology and Custom Driver Circuits [3.7]

Kyushu University; Bridgestone

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Power consumption of conventional displays is relatively high.
- Conventional displays are heavy and rigid.
- Conventional e-paper is slow due to colored particles moving in a liquid.
- Active-matrix displays are relatively-high-cost.

NOVEL CONTRIBUTIONS

- An ultra-thin (< 300μm) e-paper display with high-speed response(< 0.2ms) is demonstrated **[3.7]**
- The display uses colored particles moving in air sandwiched between plastic films, which enable a passive-matrix addressing scheme **[3.7]**
- The display is physically flexible, thanks to its limited thickness and to thinned-down driving circuitry **[3.7]**

CURRENT AND PROJECTED SIGNIFICANCE

- Flexible electronic paper enables new and exciting application areas **[3.7]**
- Enables item-level identification tags with a vivid and informative display **[3.7]**
- Enables ultra-thin and lightweight ubiquitous graphic display, for portable-display applications **[3.7]**
- Enables electronic posters using e-paper, able to display motion pictures, which can change the way advertisements are presented **[3.7]**

Proximity Interconnect and Communication

3D Capacitive Interconnections with Mono- and Bi-Directional Capabilities [20.1]

ARCES- University of Bologna; STMicroelectronics, Fraunhofer IZM

A 0.14pJ/b Inductive-Coupling Inter-Chip Data Transceiver with Digitally-Controlled Precise Pulse-Shaping [20.2]

Keio University; University of Tokyo

PRESENT STATE OF THE ART *(THE PROBLEM)*

- 3D-integration technology promises to enable complex systems, but faces significant technological challenges
- Contactless (inductive and capacitive) communication between chips has reduced technological complexity
- Current contactless communication is power-hungry (with high energy/bit)

NOVEL CONTRIBUTIONS

- Lowest-power capacitive chip-to-chip interconnect, uses 0.08pJ/b **[20.1]**
- Lowest-power inductive chip-to-chip interconnect, uses 0.14pJ/b **[20.2]**

CURRENT AND PROJECTED SIGNIFICANCE

- New data links consume sufficiently less power, and compete with direct-contact 3D technology **[20.1, 20.2]**

Trends in Wireless Systems

Architectures and Circuits for Software-Defined Radios: Scaling and Scalability for Low-Cost and Low-Energy [32.1]

IMEC; KU Leuven

Advanced MMIC for Passive Millimeter and Submillimeter Wave Imaging [32.3]

Northrop Grumman

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Multitudes of wireless transceiver standards and modes exist for different applications, each requiring separate investment for development, deployment, and maintenance.
- Achieving energy efficiency of reconfigurable radios is an obstacle.
- Concealed-weapon identification and other see-through applications, require compact high-sensitivity millimeter-wave cameras.

NOVEL CONTRIBUTIONS

- Adaptive Software-Defined Radios (SDRs) achieve up to 40% lower energy through run-time quality-of-service and energy management. **[32.1]**
- Passive detection of millimeter and submillimeter waves for see-through imaging applications use amplifiers operating up to 300GHz. **[32.3]**

CURRENT AND PROJECTED SIGNIFICANCE

- Lower cost through Software-Defined Radios (SDRs) and lower energy through continuous adaptation of the SDRs' quality-of-service and energy management. **[32.1]**
- Enabling-chip-scale compact high-resolution millimeter- and submillimeter- wave cameras for see-through imaging applications **[32.3]**

SPECIAL-TOPIC SESSION

CIRCUIT DESIGN in the YEAR 2012

Co-Organizer: ***Anantha Chandrakasan****, Massachusetts Institute of Technology, Cambridge, MA*
Co-Organizer / Chair: ***Kerry Bernstein****, IBM TJ Watson Research Center, Yorktown Heights, NY*

OVERVIEW

This Special-Topic-Session will provide a thorough overview of special circuit-design considerations required to accommodate sub-32nm-device idiosyncrasies. While it is known that scaling effects will continue to profoundly impact high-speed logic and analog circuits designers rarely get a glimpse of the aggregate effect on the resources integrated into future high-performance processors. Four visionaries will share their insights into issues confronting the microprocessor-design teams of 2012, and offer solutions we can begin to develop today.

OBJECTIVE

- To prepare designers of high-performance analog and digital circuits for the challenges presented by the effects of scaling on specific-unit examples
- To introduce departures from conventional technology as asserted by emerging novel structures

CHALLENGE

- How can ISSCC incorporate intrinsic effects of device physics in a manner that is meaningful to the entry-level circuit designers or chip integrators, who rarely deal with fundamental device-properties?
- What can ISSCC contribute to the resolution of the known-looming crisis among analog designers who are struggling to deal with device impairments in a variety of CMOS circuits?

STRUCTURE

Impact of Future Technology-Scaling Options on Processor Design

David Frank, IBM TJ Watson Research

A variety of technology options are being actively considered for the 32nm generation and beyond, including high-k gate dielectrics, metal gates, higher-mobility channels, lower voltages, improved cooling technologies, and alternative FET geometries. In addition, some unwanted effects will continue to increase in importance for these generations, including random variability and quantum-mechanical effects such as band-to-band tunneling. These options and effects are summarized in this presentation. A power-constrained processor-oriented technology-optimization tool is used to analyze their impact on overall chip performance. Power and temperature constraints significantly limit the effectiveness of many options. It is shown that high-k gate dielectrics offer significant advantages for PDSOI, only if they are coupled with near-band-edge workfunction gates, and that

performance only increases by 1% or so for every 10% increase in mobility. Improved heatsink technology can, in principle, allow significant performance improvement, but requires nearly-exponential increases in power dissipation. Lower dielectric constants for wiring, and 3D integration, are also addressed.

Technology Scaling and Analog Circuits: Challenges and Solutions

Hae-Seung Lee, Massachusetts Institute of Technology

Technology scaling has a significant impact on analog-circuit design due to the reduced signal swing and decreased intrinsic device-gain. In addition, gate and subthreshold-leakage currents, higher flicker-noise corner frequency, and variations, pose additional complications. The difficulties imposed by technology scaling on analog circuits are examined, and possible solutions are proposed. In particular, a recent technique, the Comparator-Based Switched-Capacitor (CBSC) technique, has the potential to greatly outperform traditional analog circuits. Lack of explicit feedback and need for high device-gain, lower noise, and high power efficiency, make CBSC circuits more suitable in scaled technologies. Traditional and CBSC analog circuits are compared for resolution of issues that arise from scaling down to 45nm. For numerical comparison, analog-to-digital converters in traditional and CBSC styles are contrasted in terms of projected figures-of-merit and absolute performance limits. Finally, some of the challenges that designers may face in implementing high-performance CBSC are discussed.

Digital Circuit-Design Insights from Analog Experiences

Marcel Pelgrom, Philips Research Labs

The fundamental aspects of variability include phenomena such as threshold mismatch (often attributed to dopant fluctuation), and line-width variations. These local effects start to dominate well-known global variations. In analog design, a complete change in mitigation strategies has evolved: auto-zero comparators, data-weighted averaging, and digital calibration (up to I/Q mixers). Is this an inspiration for digital designers? Should the digital-design community go the analog way, and trade off area and extra transistors, for data redundancy, and system-level solutions? What will the role of future CAD tools be? Or do we wait for the FinFETs to solve the variability problems? We will review some of the problems in an analog/digital context, and discuss the merits of various solutions.

Will FinFETs Replace Planar CMOS by Year 2012?

Borivoje Nikolic, University of California, Berkeley

Vertical, double-gated fully-depleted SOI transistors (FinFETs) have intrinsically better electrostatics than planar CMOS devices, and present an opportunity for extended technology scaling. When competing with mainstream CMOS logic devices, FinFETs must overcome various integration challenges, such as body-thickness control, fin contacts, and mobility enhancement. On the other hand, planar CMOS 6T SRAM faces significant stability challenges in scaling to 32nm technology. The use of two independent gates allows for the design of stable 6T FinFET SRAMs in sub-32nm processes. A technology that efficiently integrates, in the same process, the double-gate SRAM with planar CMOS logic could emerge by 2012.

RECAP

The Technology-Directions Subcommittee is pleased to present a Special-Topic-Session-format overview of special circuit-design considerations that will accommodate sub-32nm device idiosyncrasies. While it is known that scaling effects will continue to profoundly impact high-speed logic, and analog, designers rarely get a glimpse of the aggregate effect on the resources integrated into future high-performance processors. Four forward-thinking experts will share their insights into issues confronting the microprocessor design teams of 2012, and offer solutions we can begin to develop today.

SPECIAL-TOPIC SESSION

HIGHLIGHTS OF IEDM 2006

Organizer: ***Albert Theuwissen*** *DALSA, Eindhoven*
Chair: ***Ernesto Perea*** *ST Microelectronics*

IEDM is the most important international forum for advances in solid-state devices and breakthrough in semiconductor technology, and is fully supported by the IEEE Electron Devices Society. Amongst the IEDM papers presented at IEDM2006, following a very rigorous selection process, four papers were invited to be presented at ISSCC this year.

It is the very first time that IEDM papers will be presented at the ISSCC. Having a session like "Highlights of IEDM" tries to bring the circuitry engineers closer to the forefront of device and technology developments. Both worlds of devices and circuits have so much in common that one cannot live without the other. This special evening session is a major ISSCC initiative to bring both worlds together, based on the following program:

Three Dimensionally Stacked NAND Flash Memory Technology Using Stacking Single Crystal Si Layers on ILD and TANOS Structure for Beyond 30nm Node,

Soon-Moon Jung, et al., Samsung Electronics

Three dimensionally stacked NAND flash memory cell arrays are formed on the ILD as well as on the bulk to double the memory density without increasing the chip size, by implementing S^3 technology. The feasibility of the technology was proven by the successful operations of 32 bit NAND flash memory cell strings with 63 nm dimensions, TANOS structures, and the novel SBT (Source-Body Tied) operational scheme.

Doubling or quadrupling MuGFET fin integration scheme with higher pattern fidelity, lower CD variation and higher layout efficiency,

R. Rooyackers, et al., IMEC

Multiple Gate Field Effect Transistors (MuGFET) with fin quadrupling by adding two operations to the fin doubling module are demonstrated. Due to the 50 nm fin pitch, selective epitaxial growth silicon (SEG-Si) will connect the fins outside the spacer region reducing the high parasitic source/drain-resistance (R_{SD}) and resulting in higher drive current per surface unit.

A Cost-Effective Low Power Platform for the 45-nm Technology Node,

Emmanuel Josse et al., ST Microelectronics

The paper presents a cost-effective 45 nm technology platform, primarily designed to serve the wireless multimedia and consumer electronics needs. This platform features low power transistors operating at a nominal voltage of 1.1 V, an ultra low k dielectric (k = 2.5) with up to 9 Cu metal layers and 0.25/0.3/0.37 μm^2 SRAM cells. This platform also features an optional third gate oxide for either higher speed or active power mitigation. This technology has been developed on the (100)-oriented substrate with a key focus on process simplicity. Transistor improvement relies on mask-free strain engineering techniques along with co-implanted halos and laser anneal. The impact of laser anneal on transistor reliability and mixed-signal capabilities are also examined. Drive current as high as 660/320 $\mu A/\mu m$ and 1.1 V are reported.

Ultra-Thin Phase-Change Bridge Memory Device Using GeSb,

Y.C. Chen et al., IBM Almaden Research Center

An ultra-thin phase-change bridge (PCB) memory cell, implemented with doped GeSb, is shown with < 100 μA RESET current. The device concept provides for simplified scaling to small cross-sectional area (60 nm^2) through ultra-thin (3 nm) films; the doped GeSb phase-change material offers the potential for both fast crystallization and good data retention.

TUTORIAL

Organic-transistor circuit design

Takayasu Sakurai, University of Tokyo, Japan

OVERVIEW

Organic transistors are expected to provide a way to build printable flexible large-area electronic systems, which may open up new applications. This Tutorial provides a comprehensive view of integrated-circuit design approaches based on organic transistors. The Tutorial covers organic IC examples such as e-skin, sheet-type scanners, and Braille displays with the following structure:

- Technology (material, process, structure, and encapsulation)
- Advantages and disadvantages
- Circuit design (modeling, and distinguishing characteristics relative to silicon)
- Coping with issues of low speed and reliability
- Applications and design examples
- Remaining issues and future directions

SPEAKER BIOGRAPHY

Takayasu Sakurai received the B.S., M.S. and Ph.D degrees in EE from the University of Tokyo. In 1981, he joined Toshiba, where he designed numerous VLSI products including memories and processors. From 1988 to 1990, he was a visiting researcher at the University of California, Berkeley. From 1996, he is now a Professor at the University of Tokyo, working on VLSI design and organic circuits. He has been a conference chair and a TPC member for a number of international conferences in the field of VLSI design, including ISSCC, VLSI Circuit Symposium, A-SSCC, CICC, ESSCIRC, and DAC. He is a recepient of the IEEE 2005 ICICDT award, the ISSCC 2004 Takuo Sugano Award, and the P&I 2005 patent-of-the-year award, and other awards. He is an IEEE Fellow, a STARC Fellow, an elected AdCom member of the IEEE SSCS, and an IEEE CAS and SSCS distinguished lecturer.

FORUM

DESIGN of 3D-CHIPSTACKS

OBJECTIVE

Many experts claim that 'Moore's Law' will gradually come to its end for cost reasons and be replaced by the consequences of innovations headlined by the term 'More Than Moore.' Amongst other things, this term comprises advanced multi-chip integration methods such as 3D System Integration. This technology promises to provide high-potential performance benefits in terms of geometry and speed, and has drawn major attention by a large number of research groups in the past few years. Numerous different process architectures have been developed, and the first cost-effective commercialized applications in the communications and memory fields, are expected to come to market soon. The objective of this Forum is to introduce the various process architectures, and present potential applications to be deployed in the coming years.

AUDIENCE

This Forum is intended for circuit and system designers and engineering students wishing to gain insight into this (3D) interface between circuit design, system design, and packaging, and how it may impact applications in the near future.

SCOPE

The Forum will provide an overview of 3D fabrication and of associated technological approaches. Digging deeper, the Forum will provide an understanding of potential memory and processor applications, giving performance and cost arguments.

PROGRAM

The Forum will begin with a technology overview by **Harry Hedler** (Qimonda) highlighting the different process architectures and their benefits and shortcomings. In the second presentation, **Mitsumasa Koyanagi** (Tohuku University) will present prototypes based on wafer-to-wafer stacking and chip-to-wafer stacking. He is one of the fathers of 3D integration who introduced wafer stacking 20 years ago. **Muhannad Bakir** (Georgia Institute of Technology) will then address the important topics of heat removal and power distribution in the chip-stacks. Finally the technology section of the Forum is concluded with a presentation by **Tadahiro Kuroda** (Keio University) who will address chip-to-chip data communication by inductive and capacitive coupling.

The applications section of the Forum starts with a presentation by **Dan Radack** (DARPA) who provides an overview of possible applications and their advantages and disadvantages. **Wilfried Haensch** (IBM) will then discuss processor applications, elaborating on alternative integration strategies. **Bryan Black** (Intel) will continue the discussion of processor applications, by discussing the design challenges of 3D integration. **Dong-Ho Lee** (Samsung) will contrast this with memory applications. The presentation by **Bert Gyselinckx** (IMEC) will highlight the opportunities presented by 3D integration for miniaturized wireless-sensor networks. Finally, **Hannu Tenhunen** (Royal Institute of Technology) will elaborate on the cost and performance trade-offs for 3D mixed-signal systems. The Forum concludes with a panel discussion which will provide the audience with the chance to engage in extended discussion with the presenters.

WIRELESS

- **Overview**
- **Featured Papers**
- **Panel**
- **Tutorial**
- **Forum**
  (co-sponsored by RF/Wireless)

ISSCC 2007 – WIRELESS COMMUNICATIONS

Subcommittee Chair: *Trudy Stetzler, Texas Instruments, Stafford, TX*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- The first 65nm CMOS WiMedia-compliant UWB transceiver **[6.1]**
- An all-digital 90nm CMOS ultra-low-energy (47pJ/Pulse) UWB transmitter **[6.4]**
- The first direct-conversion cable-TV tuner chip covering the entire 48 to 860MHz band, using no external filters **[11.1]**
- Single-chip transceivers for multi-class global RFID readers **[11.5, 11.6]**
- Direct-conversion linear-uplink WCDMA transmitters requiring no SAW filters **[19.1, 19.2]**
- A MEMS-enabled fully-reconfigurable Software-Defined-Radio transceiver in 130nm CMOS **[19.6]**
- The first Bluetooth EDR SoC implemented in 0.13µm CMOS **[31.1]**
- The first fully-integrated dual-band CMOS direct-conversion MIMO transceiver for 802.11n/EWC, capable of supporting > 270Mb/s PHY rate **[31.2]**

APPLICATIONS AND ECONOMIC IMPACT

- Complete integration of a WiMedia-compliant UWB transceiver **[6.1]**
- An all-digital pulse-based transmitter allowing for ultra-low energy per bit and low-standby power-consumption **[6.4]**
- A 48 to 860MHz direct-conversion cable-TV tuner enabling low-cost system implementations **[11.1]**
- Single-chip UHF RFID readers enabling low-cost extended-range fast-data-rate automatic identification **[11.5, 11.6]**
- Low-out-of-band-noise WCDMA transmitters allow the implementation of lower-cost more-compact higher-efficiency systems **[19.1, 19.2]**
- A chip that takes a significant step toward an energy-efficient software-defined radio **[19.6]**
- Low-cost fully-integrated Bluetooth SoC allows for higher-data-rate PAN communications at low cost **[31.1]**
- Fully integrated 802.11n-compliant transceiver opens the door for high-data-rate wireless multi-media applications **[31.2]**

PANEL

Digital RF – Fundamentally a New Technology or Just Marketing Hype? [E2]

To determine the future of analog and mixed-signal design if an all-digital communications channel can really be implemented.

TUTORIAL

Radio Design for MIMO Systems with an Emphasis on IEEE 802.11n [T9]

FORUM

(Co-sponsored by RF/Wireless)

Power Amplifiers and Transmitter Architectures [F3]

UWB and mm-Wave Communication Systems

A WiMedia-Compliant UWB Transceiver in 65nm CMOS [6.1]

NXP Semiconductors

A 47pJ/pulse 3.1-to-5GHz All-Digital UWB Transmitter in 90nm CMOS [6.4]

Massachusetts Institute of Technology

PRESENT STATE OF THE ART *(THE PROBLEM)*

• The state-of-the-art in UWB has evolved from a proof-of-concept technology to manufacturable SoCs.

• UWB solutions have several major application domains. One application is in high- speed communication systems where the emphasis is on the large data-throughput. Another application relates to the use of UWB in low-power but low-data-rate applications such as wireless sensor networks. A third area of application is for short-distance RADAR such as for automotive applications. Both domains require specific solutions and dedicated circuits.

• UWB, as its name implies, covers a very-wide frequency range (one band extends from 3.1GHz to 10.6GHz). The scarcity of available spectrum is overcome by transmitting at a very-low-power level and spreading information over a wide frequency-range. Interference that can arise when sharing a crowded frequency band is avoided by very quickly hopping to different frequencies. Current transceiver technology for applications such as cellular phones and WLAN is aimed at relatively-narrow-band applications. Therefore, radically-new wide-band receivers, transmitters, and frequency-synthesizer circuits are required.

• Spectrum is also available at 24GHz for high-data-rate communication and RADAR applications.

• To become commercially viable, UWB systems must be cost-effective. Cost effectiveness can only be guaranteed with CMOS technologies. Until now, this was not feasible for the highest-frequency bands. Furthermore, the complete system should be integrated on one die. Frequency synthesis and efficient transceiver design for 24GHz bands continues to be a challenge.

NOVEL CONTRIBUTIONS

- WiMedia-compliant UWB transceiver for MB-OFDM bands 1 and 3 in 65nm CMOS **[6.1]**
- Dual-band pulse-based transceiver supporting high data rates up to 800Mb/s **[6.2]**
- Ultra-low-power UWB receivers and transmitters for pulse-based UWB **[6.3, 6.4, 6.5, 6.6]**
- Phased-array transceiver for 24GHz band based on variable-phase ring oscillator and PLL architecture **[6.7]**
- DDFS-based frequency synthesis for 19GHz FMCW radar application **[6.8]**

CURRENT AND PROJECTED SIGNIFICANCE

- UWB hardware will ultimately allow the wireless connection of new high-definition audio/video equipment, including high-definition video that will make use of wires and cables for communications unnecessary. This will also allow for wireless transfer of Gigabytes of information in home and office environments **[6.1]**
- Ultra-low-power UWB will enable wireless sensor networks with very long battery lifetime **[6.4]**

TV Tuners and RFID Readers

A 48-to-860MHz CMOS Direct-Conversion TV Tuner [11.1]

Chrontel; University of California, San Diego

A 900MHz UHF RFID-Reader Transceiver IC [11.5]

Intel; Catena Wireless Electronics

A Single-Chip CMOS Transceiver for UHF Mobile RFID Reader [11.6]

Samsung; Kwangwoon University

PRESENT STATE OF THE ART *(THE PROBLEM)*

- We are in the early stages of a worldwide transition in television broadcasting from analog to digital. In a few places in the world, analog broadcasts have already been switched off; However, most of the world will still require support for legacy broadcasts through 2009, 2012, and even 2015. During the transition period, it is necessary to support both the legacy analog-TV standards, as well as the new digital-TV standards. Up until now, highly integrated silicon TV tuners have employed dual (up-down) conversion, low IF, and (in the case of some mobile-TV applications) even direct-conversion when the input frequency range was narrow enough to avoid harmonic mixing of large interferers. However, a direct-conversion solution without external filters, that can cover the full 48-to-860MHz TV band has only been a dream, until now.
- An RFID reader has to receive the weak signal transmitted by the passive tag in the presence of a large self-jammer from the transmitter. Until now, this RFID reader function was accomplished by separating the transmitter from the receiver, and using multiple antennas in the RFID reader to provide sufficient isolation between RX and TX.

NOVEL CONTRIBUTIONS

- First publication of a direct-conversion TV tuner that covers the full 48-to-860MHz TV bandwidth, and solves the harmonic-mixing problem. For this highly-integrated design, all necessary filtering is included on the 0.18µm CMOS chip; good image rejection is achieved; and power consumption is 750mW. **[11.1]**
- Single-chip integration of a UHF RFID reader transceiver has extended range and higher data rates compared to traditional lower-frequency RFIDs **[11.5, 11.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- Because of the transition from analog to digital TV, there will be a multi-year increase in the volume of units shipped, both for integrated digital TVs that incorporate digital and analog reception, and for converter boxes that accept a digital TV input and convert it to an analog TV output for display on a legacy analog TV. The technical challenges for receiving analog or digital TV broadcasts are different, and they increase when both must co-exist. In addition to the technical challenges, the cost of the solution must also be made very low for wide market adoption. Today, almost all TV sets and off-air set-top converter boxes still use surprisingly-low-cost tuner modules consisting of hundreds of discrete components and requiring manual tuning (frequency alignment). The first three papers in Session 11 present highly-integrated TV tuners to meet both the technical and commercial challenges of the digital-TV transition around the world. **[11.1, 11.2, 11.3]**
- Integration of the UHF RFID reader will reduce reader cost and make integration within mobile devices possible, ultimately bringing RFID to the consumer market. Broadening the availability of RFID readers increases the availability of RFID information and will ultimately result in new RFID applications, ranging from simple product identification in the supermarket, to all kinds of sensor monitoring. **[11.5, 11.6]**

Cellular and Multi-Mode Transceivers

Direct-Conversion WCDMA Transmitter with -163dBc/Hz Noise at 190MHz Offset [19.1]

Analog Devices

A Linear Uplink WCDMA Modulator with -156dBc/Hz Downlink SNR [19.2]

ACP; ETH

A WCDMA Transmitter in 0.13µm CMOS using a Direct-Digital RF Modulator [19.3]

Nokia

PRESENT STATE OF THE ART *(THE PROBLEM)*

- 3G cellular networks are finally being deployed in earnest. Data rates high enough to support painless mobile Internet access, video phones, and other data-enabled applications will dramatically change the user experience.
- Increasing demand for high-speed data, coupled with finite spectrum availability, force 3G standards to include very-stringent spectral-emissions limits.
- 3G handsets must simultaneously transmit high-power signals and receive low-power signals. Without either very-low-noise transmitters or off-chip SAW filters, the transmit noise can desensitize the receiver which is at 190MHz offset from the transmit signal. Current state-of-the-art WCDMA transmitters achieve transmit SNRs between 145 and 150dB/Hz, which dictates the inclusion of a SAW filter in the transmit path. But, SAW filters are relatively expensive and bulky. The inclusion of a SAW filter is especially problematic in handsets supporting multiple standards.
- While SoCs for 2G cellular systems have been demonstrated, SoCs for 3G systems have not.

NOVEL CONTRIBUTIONS

- Two WCDMA transmitters capable of meeting the spectral-emission limits without an external SAW filter are presented. Each TX uses a completely different approach to solve the problem. The first **[19.1]** uses a novel mixer topology that suppresses noise related to the local oscillator, and achieves 163dB/Hz SNR. The second **[19.2]** uses a new linearity-boosting technique, and achieve 156dB/Hz SNR **[19.1, 19.2]**
- A third WCDMA transmitter employs a direct-digital RF-modulator topology that is well-suited to CMOS SoC integration. **[19.3]**

CURRENT AND PROJECTED SIGNIFICANCE

- For 3G cellular phones to reach the level of acceptance that 2G phones have achieved, the cost and size of these phones must come down. These papers – either by eliminating bulky and expensive external components **[19.1, 19.2]** or by enabling SoC integration **[19.3]**. This, in turn, will enable much smaller and lower-cost 3G cellular phones than are currently possible. **[19.1, 19.2, 19.3]**
- With the cellular-phone market approaching one billion units per year, the commercial implications are enormous. But, much of the current market growth is driven by sales of low-end phones in the developing world. While this growth is impressive in terms of units sold, the low sales prices (and low profit margins) leave phone makers searching for more lucrative markets. Affordable 3G phones are just the ticket!
- The implications of the new services made possible by ubiquitous access to high-speed data are hard to predict. But today, it's also hard to imagine life without the Internet. Will it be just as hard to imagine life without mobile Internet, tomorrow?

WLAN/Bluetooth

A Single-Chip Bluetooth EDR Device in 0.13μm CMOS [31.1]

Broadcom

A Fully Integrated MIMO Multi-Band Direct-Conversion CMOS Transceiver for WLAN Application (802.11n) [31.2]

Broadcom; IQ Analog

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Wireless devices imply handheld and mobile operation. Such devices generally have limited battery capacity due to their small size. The users demand increasing time between charging, or longer battery life, for handheld devices.
- Current WLAN data throughput has been viewed to be inferior compared with wireline solutions, and it cannot support the high-data-rates required for video distribution.

NOVEL CONTRIBUTIONS

- Low-power-consumption Enhanced-Data-Rate (EDR) Bluetooth SoC for handheld applications **[31.1]**
- A single-chip 2x2 MIMO transceiver implemented in 0.18μm CMOS technology. **[31.2]**

CURRENT AND PROJECTED SIGNIFICANCE

- For consumer mass-markets, low-cost and small-form-factor are the keys to success. As the battery cost/technology does not scale as fast as the silicon technology, innovations in circuit and system design, to reduce the overall power consumption, are greatly needed. A successful implementation of ultra-low-power wireless devices will be widely accepted by the mass market. **[31.1]**
- A robust MIMO-system implementation will soon be adopted by consumers and gain popularity. The market will then be looking for lower-cost and lower-power devices that can achieve similar data rates in order to explore other market opportunities. **[31.2]**

Panel

Digital RF –A Fundamentally-New Technology, or Just Marketing Hype?

Organizers: ***Jacques C. Rudell****, Intel, Santa Clara, CA*
Qiuting Huang*, ETH Zurich, Zurich, Switzerland*
Moderator: ***Thomas H. Lee****, Stanford University, Stanford, CA*

OBJECTIVE

- To discuss the true impact of recent publications describing all-digital radio front-ends.
- To explore whether digital-RF is really a new concept, or just much hype about what has always been known for decades — the more digital, the better!
- To determine the future of analog and mixed-signal design, if an all-digital communications channel can really be implemented.

CHALLENGE

- "Digital-RF" seeks to replace traditional design-intensive analog-RF and mixed-signal blocks with extremely-scalable and highly-programmable wireless channels.
- Wireless applications, particularly cellular, tend to provide the most challenging mixed-signal implementations from a performance perspective. At first sight, more digital noise and coupling would degrade performance.
- Although challenging to implement an all-digital radio channel, implementations potentially provide many benefits: Replacing analog blocks with digital circuits holds the promise of highly-scalable and extremely-low-power radio front-ends, while minimizing the overall die area as compared with more traditional solutions.

CONTROVERSY

- Are the concepts of all-digital radio, as recently described in publications, truly innovative ideas that will revolutionize analog and mixed-signal design, as we know it? Or, is this more hype by marketers?
- Is radio performance to be compromised for the sake of replacing traditional analog functions with an all-digital implementation?
- Does an all-digital solution for a communications channel really help reduce design complexity, or does it create more problems than it solves?

Tutorial

Radio Design for MIMO Systems with an Emphasis on IEEE 802.11n

Arya Behzad, Broadcom Corporation, San Diego, CA

OVERVIEW

With the great success and vast deployment of legacy single-input, single-output (SISO) WLAN systems in the world, the industry has begun to release next-generation systems based on multi-input, multi-output (MIMO) technology. Essential to the overall system design, is the radio design. This Tutorial will begin by providing a brief introduction to the legacy 802.11 a/b/g systems. This will be followed by a discussion of the history of multiple-antenna systems, and the conventional analog-based techniques such as antenna-diversity and analog maximum-ratio combining (MRC). A general introduction to the 802.11n standard will then follow. This includes the channelization and modulation types, the definition and description of the concepts behind the multiple spatial streams (M x N), and additional PHY and MAC techniques allowing higher rates and/or longer reach. Such features include the use of short guard-interval (GI), implicit and explicit beam-forming, space-time block codes (STBC), the use of Greenfield mode, and aggregation techniques. The requirements of the 802.11n standard, such as sensitivity and EVM, and their relation to analog impairments such as phase noise, quadrature imbalances, linearity, and cross-talk, will also be discussed. Some specific circuit examples will be presented, and some unique circuit-implementation challenges of MIMO radios will be discussed. Several actual measured-performance numbers (range and throughput) will be presented, and interoperability and legacy-mode support, will be examined. The Tutorial will wrap up with a discussion of the future trends in MIMO-radio implementation.

SPEAKER BIOGRAPHY

Arya Behzad worked at MicroUnity Systems Engineering from 1994 to 1996 as a Senior Analog and System Engineer implementing RF and analog front-ends for set-top boxes and cable modems. From 1996 to 1998, he worked at Maxim Integrated Products implementing high-precision analog components, infra-red receivers, and cellular-phone ICs. Since 1998, he has been with Broadcom Corporation, working on integrated tuners, gigabit Ethernet, and wireless LAN systems, and ICs. He is currently a Director of Engineering in charge of radios for current- and future-generation wireless products, and Product-Line Manager for all Wireless-LAN Radio products.

He has over 70 patents issued and pending, as well as several publications in the areas of precision analog circuits, cellular transceivers, integrated tuners, gigabit Ethernet, and wireless LANs. He has taught courses, and presented technical seminars, at various conferences, and at several universities.

He is in his fifth year as a member of the ISSCC Wireless Technical Committee. He has served as a Guest Editor of JSSC and is currently an Associate Editor for the SSC Journal.

Arya Behzad obtained his M.S. in EE from UC Berkeley in 1994 after completing his thesis on the Infopad Project.

GIRAFE FORUM

Power Amplifiers and Transmitter Architectures

Objective

This all-day Forum will investigate and discuss new trends in power amplifiers and transmit architectures for wireless communications, and their dependency on the standards to be supported.

Attendance is limited, and pre-registration is required. This Forum encourages open interchange.

Audience

The targeted participants are circuit designers and concept engineers working on wireless transmitters or power amplifiers, who want to learn about the latest developments in system and circuit design.

Scope

Mobile phones are evolving from simple single-standard voice phones to multi-standard multi-band multi-application mobile terminals. High integration levels plus re-configurability of the signal-processing chain are a must for those all-in-one-phones to minimize chip area and cost, but have so far only been demonstrated in transceivers. Now, for entry-level phones, single-chip transceiver and baseband integration is a reality. Power amplifiers, however, have so far been resisting this trend, at least in cellular applications. One PA per band and per standard will be too bulky and too expensive for future terminals. Future PAs must be reconfigurable to support several standards. Silicon integration is a requirement for “intelligent” PAs, and is promising cost reduction over 3/5-compound PAs; But can it handle the power levels and peak voltages of cellular phones? A variety of PA architectures promises high PAE under certain conditions. For power effectiveness, it is, however, no longer sufficient to optimize the PA, alone. Rather, co-development and common optimization of transmitter, PA, and power supply, is required. This Forum will highlight the latest trends in PA and transmitter design, and architectures.

Program

The morning session begins with an introduction to the topic by **David Su** (Atheros Communications). The second speaker, **Earl McCune** (Panasonic), will discuss transmit architectures, their impact on the PA concept, and show practical results for various approaches. The third and last speaker of the morning session, **David Pehlke** (Silicon Labs), will look in detail into a variety of PA concepts and linearization techniques, and explain their tradeoffs.

The afternoon session will be opened by **Lawrence Larson** (UC San Diego), who will show how various power-supply-modulation schemes can be used to enhance PA efficiency. Special attention will be given to OFDM applications. The fifth speaker, **Gene Tkachenko** (Skyworks Solutions), will cover technology requirements and solutions for cellular PAs, and frontend modules. The effects of critical system parameters on technology choice will be explained. Finally, **Ali Hajimiri** (Cal Tech) will show novel circuit concepts enabling CMOS integration of power amplifiers, even for GSM.

The Forum will conclude with a panel discussion, where the attendees have an opportunity to ask questions and to share their views.

WIRELINE

- **Overview**
- **Featured Papers**
- **Special-Topic Session**
- **Tutorial**
- **Forum**
- **Trends**

ISSCC 2007 – WIRELINE

Subcommittee Chair: *Franz Dielacher, Infineon Technologies, Villach, Austria*

OVERVIEW

MOST-SIGNIFICANT RESULTS

- A fully-integrated 4x10Gb/s DWDM optoelectronic transceiver in standard 0.13µm CMOS SOI **[2.1]**
- A fractional-N PLL for SONET-quality clock-synthesis applications **[2.9]**
- A 72mW 0.03mm^2 inductorless 40Gb/s CDR in 65nm SOI CMOS **[12.3]**
- A 7Gb/s 9.3mW 2-tap current-integrating DFE receiver **[12.5]**
- A 12.5Gb/s SerDes in 65nm CMOS using a baud-rate ADC with digital receiver equalization and clock recovery **[24.1]**
- A 14mW 6.25Gb/s transceiver in 90nm CMOS for serial chip-to-chip communication **[24.3]**
- A 16Gb/s Source-Series-Terminated Transmitter in 65nm CMOS SOI **[24.6]**
- Performance variability of a 90GHz static CML frequency divider in 65nm CMOS SOI **[30.3]**

APPLICATIONS AND ECONOMIC IMPACT

- The integration of photonic and transceiver functions in silicon will be a key driver for further development in the area of high-speed data communications. A fully-integrated 40-Gb/s throughput optoelectronic transceiver is successfully demonstrated **[2.1]**
- Fractional-N-based clock generators are being used to replace costly reference and voltage-controlled crystal oscillators in mature 130nm CMOS technologies for demanding 10-Gb/s SONET applications **[2.9]**
- Many contributions in 65nm CMOS show very promising results for further reduction of the power dissipation of high-speed serial links, while targeting even-higher data rates that require deeper understanding of the issues related to technology variability **[12.3, 24.1, 24.6, 30.3]**
- Major efforts are underway to increase the power efficiency and to reduce the cost of 6 to 7 Gb/s serial chip-to-chip communication links with innovative implementations in 90nm CMOS technology **[12.5, 24.3]**

SPECIAL-TOPIC SESSION

Last-Mile Access-Options: PON/DSL/Cable/Wireless [SE 3]

To understand what new silicon functions are needed to keep cable, DSL and wireless competitive, as legacy networks respond to the challenge of new Passive Optical Networks.

TUTORIAL

Fundamentals of Electronic Dispersion Compensation [T10]

Electronic dispersion compensation (EDC) has emerged as the technology enabling the migration of metro and long-haul optical fiber, and backplane and I/O links, to 10-to-40Gb/s rates. The design of an OC-192 EDC chip-set will be presented as a case-study.

FORUM

ATAC: Automotive Bus Systems [F5]

Dedicated to automotive bus systems, this Forum gives an overview, from the physical layers, up to the system perspective and implementation issues, for a representative car platform.

OPTICAL COMMUNICATIONS

A Fully-Integrated 4x10Gb/s DWDM Optoelectronic Transceiver in Standard 0.13µm CMOS SOI [2.1]

Luxtera

A Fractional-N PLL for SONET-Quality Clock-Synthesis Applications [2.9]

Silicon Laboratories

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Difficult to integrate multiple-channel 10Gb/s optical devices in silicon
- Challenging to achieve low-cost high-performance clocking for 10Gb/s

NOVEL CONTRIBUTIONS

- Integration of silicon optical interleaver with 4-channel Mach-Zender-interferometer drivers and receivers on a single chip for 40Gb/s DWDM throughput in 0.13µm CMOS SOI **[2.1]**
- Clocking solution based on low-cost crystal delivering sub-picosecond jitter performance acceptable for 10Gb/s SONET applications **[2.9]**

CURRENT AND PROJECTED SIGNIFICANCE

- Low-power low-cost optoelectronic integration in CMOS with aggregate 40Gb/s throughput **[2.1]**
- Low-cost high-performance clocking for SONET OC-192 applications **[2.9]**

Gigabit CDRs and Equalizers

A 72mW 0.03mm^2 Inductorless 40Gb/s CDR Circuit in 65nm SOI CMOS [12.3]

IBM

A 7 Gb/s 9.3mW 2-Tap Current-Integrating DFE Receiver [12.5]

MIT; IBM

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Power consumption of DFEs limits their use in many applications.
- CMOS CDRs limited to 25Gb/s
- Inductors are required to achieve high performance in CMOS CDRs.

NOVEL CONTRIBUTIONS

- Amazingly-low power-consumption and area in the fastest CMOS CDR published to date. **[12.3]**
- Disruptive technology for enabling the use of DFE receivers in low-power applications. **[12.5]**

CURRENT AND PROJECTED SIGNIFICANCE

- 40Gb/s CDRs proven practical in CMOS. **[12.3]**
- Low power and area enable the deployment of dense arrays of high-speed links.**[12.3,12.5]**
- Link density in low-power systems can now be increased by employing DFE to provide equalization without crosstalk enhancement. **[12.5]**

Multi-Gb/s Transceivers

A 12.5Gb/s SerDes in 65nm CMOS Using a Baud-Rate ADC with Digital RX Equalization and Clock Recovery [24.1]

Texas Instruments

A 14mW 6.25Gb/s Transceiver in 90nm CMOS for Serial Chip-to-Chip Communication [24.3]

Rambus

A 16Gb/s Source-Series-Terminated Transmitter in 65nm CMOS SOI [24.6]

IBM

PRESENT STATE OF THE ART *(THE PROBLEM)*

- Very high power required for high-speed links (tradeoff between power, and speed)
- State-of-the-art : 20mW/Gb/s for backplane, 10mW/Gb/s for on-board interface
- DFE is required for low BER. Analog operation of DFE is difficult with <90nm CMOS devices

NOVEL CONTRIBUTIONS

- Two interleaved 6.25GS/s (baud-rate) 4.5b ADCs support 12.5Gb/s all-digital DFE and FFE **[24.1]**
- 2.2mW/Gb/s for short-length on-board transceiver using low-swing voltage-mode driver **[24.3]**
- Source synchronous (push-pull) transmitter for low power and flexible termination voltage(0V to VDD) **[24.6]**

CURRENT AND PROJECTED SIGNIFICANCE

- All-digital approach used with <90nm CMOS enables inexpensive, low-power, high-speed communications **[24.1, 24.3, 24.6]**
- More design effort directed toward 20Gb/s CMOS chip-to-chip communication **[24.1, 24.3, 24.6]**

Building Blocks for High-Speed Transceivers

40GHz Wide-Locking-Range Regenerative Frequency Divider and Low-Phase-Noise Balanced VCO in 0.18µm CMOS [30.4]

National Taiwan University

A Self-Calibrated On-Chip Phase-Noise-Measurement Circuit with -75dBc Single-Tone Sensitivity at 100kHz Offset [30.5]

Intel; Arizona State University

PRESENT STATE OF THE ART *(THE PROBLEM)*

- The fastest clock divider in 0.18µm CMOS reported is at 30GHz (JSSC 2005).
- On-chip jitter-measurement methods have been reported in the last few years.

NOVEL CONTRIBUTIONS

- Clever use of series- and shunt-peaking inductors within a regenerative divider topology allows higher-frequency operation and greater frequency range. **[30.4]**
- On-chip measurement of signal purity allows better characterization of on-chip broadband communication system. Frequency-domain measurement of signal purity (i.e., phase noise) is performed rather than time-domain measurement (i.e., jitter). **[30.5]**

CURRENT AND PROJECTED SIGNIFICANCE

- The high-speed clock divider is often the most difficult and delicate circuit block in a transceiver. Design techniques are presented that improve the performance and robustness of such a circuit in a given technology. **[30.4]**
- Measurement of phase noise is seen to provide more information about the effect of noise from the circuit components on clock purity than does measurement of jitter. **[30.5]**

SPECIAL-TOPIC SESSION

Last-Mile Access Options: PON/DSL/Cable/Wireless

Organizer: ***Yusuke Ohtomo****, NTT*
Chair: ***Larry DeVito****, Analog Devices*

OVERVIEW

Passive Optical Networks (PONs) are the next step in the evolution of the access network. The opportunity, now, is to offer a "triple-play" — high-speed Internet, Voice over IP (VOIP), and multi-channel television (TV) — to your home. In particular, rapid growth in high-definition TV, needing six times more bandwidth than the standard-definition TV, is one driver of the movement to increase bandwidth of home-access networks. Passive Optical Networks (PONs), and wireless-access networks (WANs) are now offering an alternative to familiar Cable and DSL networks. Over 2.5 million PONs are installed in Japan, and deployment now begins in North America. The worldwide market is projected to be hundreds of millions of households; naturally, such a huge opportunity creates fierce competition. Advances in silicon LSI for each LAST-MILE ACCESS OPTION, is surely the key to survival. This presentation session introduces the major options for current and future broadband-access networks. The speakers in this Special-Topic education session come from various areas of applications: **Thomas Quigley** (Broadcom) will present the cable market and technology; **Denis Khotimsky** (Motorola) and **Jun-ichi Nakagawa** (Mitsubishi Electric), will introduce PONs for the US and the Far East; **Cyrus Namaji** (Conexant Systems), and **Jörg Hauptmann** (Infineon), will explain DSL from the viewoint of market analysis and technology; and **Krishnamurthy Soumyanath** (Intel), will introduce the impact and technical challenges of low-cost wireless access. This comprehensive overview of access solutions will introduce attendees to the practical systems and associated LSI technologies along with market implications, with the goal of stimulating new advances from silicon providers.

OBJECTIVE

- This Special-Topic Session introduces the major options for current and future broadband-access networks.
- The comprehensive coverage of access solutions introduces attendees to practical systems and associated LSI solutions, and to the expanding market with the goal of stimulating advances from silicon providers.

CHALLENGE

- How will cable, DSL and wireless respond to the challenge of new Passive Optical Networks?
- What new silicon functions are needed to keep cable, DSL and wireless competitive?

SPEAKERS

Thomas Quigley, Broadcom, *will present*
"Cable Continues to Dominate High-Speed Access in the Next Five Years"

Despite significant challenges from other high-speed access methods, including VDSL2, PON, Wireless, and their variants, Cable's DOCSIS communications standard will continue to dominate the high-speed data market in North America. The new DOCSIS 3.0 specifications provide extensive new tools to provide high-speed access with extensive QoS support, enhancing Voice-over-IP, Video-over-IP, higher-speed data access, and regular standard and high-definition broadcast and PPV video. DOCSIS 3.0 sets the stage for operators to move all their digital-data transmission onto a common IP-based communications platform, and speed up their transition to an all-digital pipe to the home. This presentation will look at some of the key features of the 3.0 specification, including downstream and upstream channel bonding, statistical multiplexing gain, IPV6 support, and enhanced security.

Denis A. Khotimsky, Motorola, *will present*
"Progress and Perspectives of PONs for Residential Broadband Access"

In North America, all major carriers are in various stages of implementing FTTP/FTTN projects. Verizon is rolling out the FiOS FTTP service, and plans to add 3 million homes each year for the next few years, to the 6 million homes already passed, by the end of 2006. AT&T is pursuing an FTTN strategy, having deployed fiber in the Dallas, TX, area. The technology of choice is FSAN/ITU's Broadband PONs with subsequent migration to Gigabit PON. This choice is due to the support of the carrier-class quality standards that the legacy carriers have always adhered to. This presentation will cover the early history and the evolution of the technology, the standardization efforts, the service evolution to fully-fledged "triple-play" and RBOCs' massive move into the video business, as well as technological advances and perspectives for the future.

Jun-ichi Nakagawa, Mitsubishi Electric, *will present*
"Optical and Circuit Design Challenges for High-Speed PON Systems"

The rapid growth of IP traffic has spurred the development of low-cost and convenient broadband access services. GE-PON (Gigabit Ethernet Passive Optical Network) has recently attracted a great deal of attention as a way of exceeding 1Gb/s for Fiber-to-the-Home (FttH) systems. The standardization of GE-PON was completed by the IEEE802.3ah committee in 2004, and GE-PON systems are being now introduced into commercial networks in Japan. In the PON-based network architecture, multiple optical-network units, (ONUs) located at the subscribers' premises are connected with an optical line terminal (OLT) through a single optical fiber and a tree network, based on a 1:N passive star coupler; Thus, the PON system is the most promising solution for reducing installation and operating costs, by sharing fibers and OLT equipment. This presentation will review the optical- and circuit-design challenges in GE-PON and high-speed next-generation PON systems.

Cyrus K. Namazi, Conexant Systems, *will present*
"A View into the Future of the DSL Broadband Access Market; Why the Market Analysts are Wrong"

Worldwide DSL market penetration has surpassed all other forms of broadband-access technologies combined. But, many market analysts have been predicting a decline in the rate of DSL penetration growth rates for some time. Yet, less than 5% of the world's phone lines are connected to DSL networks. With over 150 million, DSL subscribers, as of June 2006, the majority of the world remains "unconnected". The DSL broadband-access market is undergoing a fundamental shift related to its market drivers, a shift which is creating a different set of dynamics in demand for semiconductors, systems, and services. This presentation focuses on the forces driving these changes, and their impact on the future of broadband in general, and of DSL, in particular.

Jörg Hauptmann, Infineon Technologies, *will present*
"Ongoing Innovation in DSL: The Enabler for 'Triple-Play' over the Last Mile"

Datarate requirements to and from the home are steadily increasing due to new service offerings like 'triple-play' (data, voice, video). Multitudes of different access technologies have been deployed, and standardized. While PON is used in new access networks offering very high bandwidth, DSL is reusing the billions of available twisted pairs of the classical plain-old-telephone-service (POTS). Many innovative steps have been taken to bring the overall system costs continuously down, while the offered bandwidth was increased at the same time. Today, VDSL2 with 30MHz bandwidth can offer 100Mb/s symmetrical data rate, and enables real 'triple-play'. This talk will highlight the diversity of different DSL technologies and applications, where major themes are cost-per-port, maximum flexible bandwidth, and high bitrates with reasonably-low power. The latest design challenges for Linedrivers, analog frontends, DSPs, and externals, will be presented.

Krishnamurthy Soumyanath, Intel, *will present*
"Low-Cost Wireless as an Alternative for Last-Mile Access"

Wireless links are emerging as significant contenders in the battle for last-mile access. The importance of wireless as an alternative link is being driven by the rapid adoption of new standards (like Wimax), the emergence of new standards, activities in the mm-wave space, and the dramatic improvement in cost/performance of CMOS wireless ICs. In many emerging economies, wireless access removes the need for expensive infrastructure upgrades/installations, making it a very attractive choice for broad-band connectivity. This is particularly true of markets that are outside of the relatively well-developed metro areas. In this presentation, we will outline the challenges and opportunities for a significant wireless presence in the last mile. We will discus strategies for achieving high performance in various frequency bands, and discuss the complementary-digital processing technologies that will allow low-cost broadband-system realizations.

RECAP

- Our goal is to understand what new silicon functions are needed to keep cable, DSL, and wireless, competitive as legacy networks respond to the challenge of new Passive Optical Network (PON) systems.

Tutorial

Fundamentals of Electronic Dispersion Compensation

Naresh Shanbhag, University of Illinois at Urbana-Champaign, Urbana, IL.

ABSTRACT

Electronic dispersion compensation (EDC) has emerged as the technology enabling the migration of metro and long-haul optical fiber, and backplane and I/O links, from 10Gb/s to 40Gb/s rates. Both long and short links suffer from various forms of dispersion or intersymbol interference (ISI), and noise. Fiber links also exhibit non-linearities originating in fiber amplifiers and photo-detector. The stringent power and throughput requirements have forced transmitter and receiver ICs to be predominantly mixed-signal, and the modulation to be binary. Meeting the challenges of designing next-generation high-data-rate systems within a tight power budget requires the designer to understand the very basis of information transfer, and go beyond the waveform-shaping aspect exemplified by the 'eye-opening' techniques prevalent today. This Tutorial will provide an overview of efficient transmit-and-receive techniques for both linear (back-plane) and non-linear (fiber) channels, such as matched filtering, linear decision-feedback, transmit techniques (pre-emphasis and partial-response coding), maximum-likelihood detector ('Viterbi equalizer'), and their implications on mixed-signal design. The design of an OC-192 EDC chip-set will be presented as a case-study. Finally, the Tutorial will conclude with a discussion of advanced topics and future directions.

BIOGRAPHY

Naresh Shanbhag is currently a Professor in the Department of Electrical and Computer Engineering, and the Coordinated Science Laboratory, at the University of Illinois at Urbana-Champaign, Urbana, IL. His research interests are in the area of low-power high-performance integrated circuits and systems for DSP and communications. He is also a co-founder and Chief Technology Officer of Intersymbol Communications, Inc., (a wholly-owned subsidiary of Kodeos Communications), since March 2006, Champaign, IL, which was founded in 2000, and where he provides strategic direction in the development of EDC-based mixed-signal receivers for next-generation optical-fiber links. He received his Ph.D. in EE from the University of Minnesota, Minneapolis, MN, in 1993. From 1993, Dr. Shanbhag worked at AT&T Bell Laboratories, where he lead the development of its 51.84 Mb/s VDSL chip-sets, before joining the University of Illinois in 1995. Dr. Shanbhag is a Fellow of the IEEE, and has received numerous awards including the 2001 IEEE Transactions-on-VLSI Best-Paper Award, the 1999 IEEE Leon K. Kirchmayer Best-Paper Award, the National Science Foundation CAREER Award in 1996, the 1994 Darlington Best-Paper Award, and has served as an Associate Editor for the IEEE Transactions on Circuits and Systems: Part II (1997 to 1999), and the IEEE Transactions on VLSI (1999 to 2002).

FORUM, (ATAC)

Automotive Bus Systems

Objective

This all-day Forum is dedicated to automotive bus systems, giving an overview from the physical layers up to the system perspective, along with implementation issues, in a representative car platform.

Audience

The target participants are designers and users of chips for highly-dependable bus systems, especially targeting the automotive field. Chip designers, as well as software engineers involved in the development of the interface and electronic-control units, will benefit from this circuit Forum.

Scope

This Forum covers the physical layers as well as the higher levels of implementation (processors, protocols, and system aspects) of automotive bus systems. Electrical and system-design issues will be discussed, as well as the important field of EMC and other aspects of the harsh automotive environment. Processors and protocols will be presented, as well as overall system aspects, which have to be taken into account when choosing the bus systems for a car platform.

Program

This Forum will begin with an overview of different bus systems used in automotive applications by **Herman Casier** (AMI Semiconductor). In the next presentation, **Martin Peteratzinger** (BMW) will discuss the criteria for bus-system selection and optimization, based on the development experience with a recent car platform. The following two presentations focus on physical-layer aspects: **Geert Vandensande** (AMI Semiconductor) and **Harald Gall** (austriamicrosystems) will discuss the LIN & CAN bus and Flexray, respectively. They will emphasize the bus-characteristics and design considerations needed to cope with low-cost and harsh-automotive-environment requirements. The next talk will concentrate on processors and protocols for bus systems. **Shunichi Ko** (Fujitsu) will use Flexray as an example for the discussion of this topic. **Dave Knapp** (SMSC) will focus on the MOST network as a backbone for the multimedia-enabled car in the next presentation. Safety and dependability is the topic of the concluding presentation: From a system perspective, **Stefan Poledna** (TTTech) will highlight the needs and state-of-the-art of automotive buses in time- and safety-critical applications.

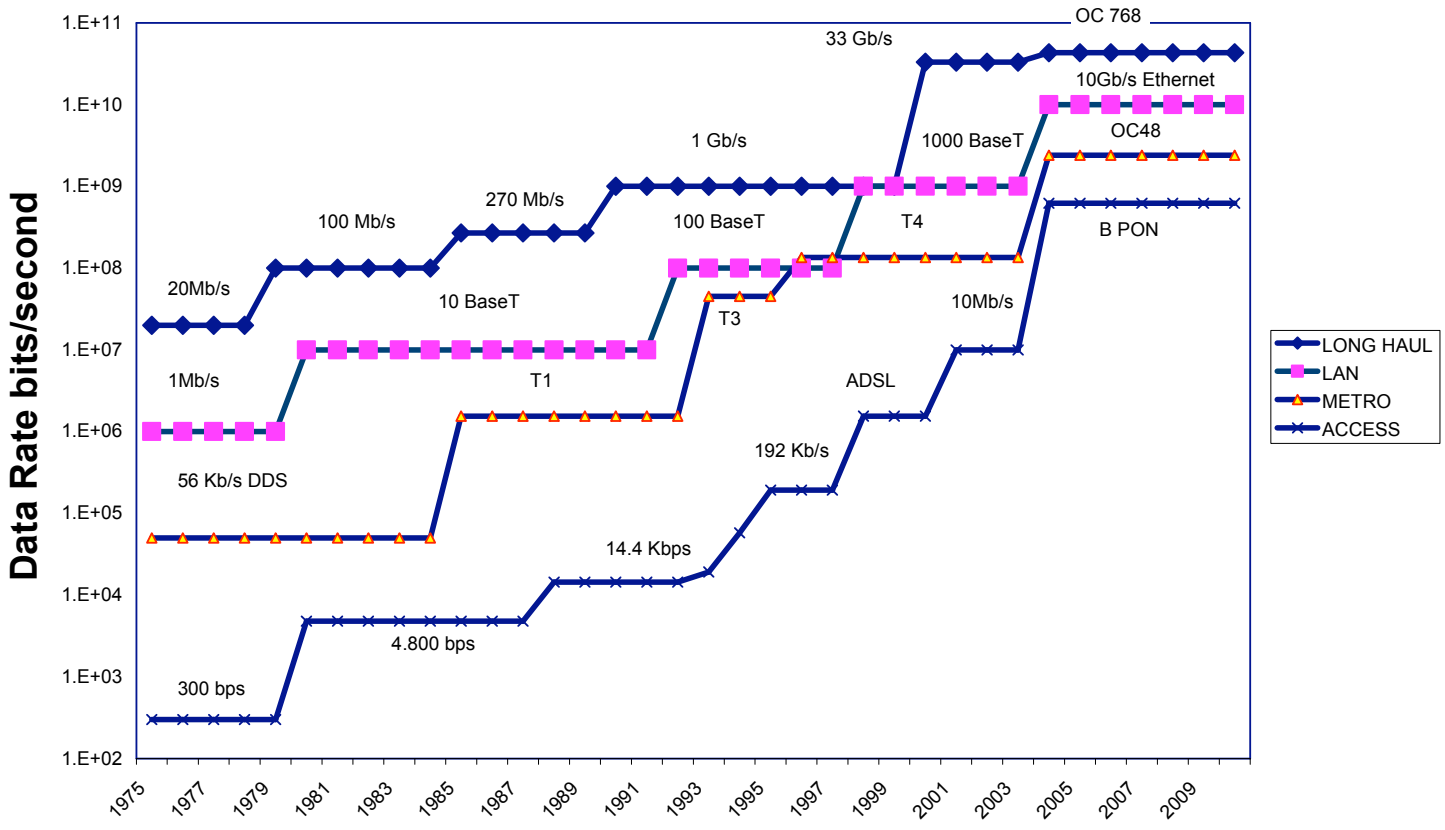
At the end of the afternoon, all speakers will assemble in a panel format for an open discussion, with the audience, on the challenges in all aspects of automotive bus systems.

This all-day Forum encourages an open interchange in a closed environment. Attendance is limited, and pre-registration is required. Coffee breaks and a lunch break will be provided to allow participants to mingle and discuss issues of mutual interest.

TRENDS IN WIRELINE COMMUNICATIONS

- Wireline technologies continue to be driven by two forces, namely CMOS features-size scaling to 65nm and below, and the emergence of new applications techniques, such as passive optical networks (PONs), targeting home connections. The Sessions at the 2007 International Solid-State Circuits Conference will present papers reflecting these trends:
- Network requirements are being enhanced to support consumer demand for "triple-play" (voice, video, and data). These requirements are resulting in the emergence of fiber technologies in access networks such as PON which provide data rates up to 1 Gb/s. PON achieves low-cost by sharing of fiber among multiple customers. But, this sharing also presents new challenges, such as burst-mode operation. We expect continuing innovation in this area for the foreseeable future.
- The re-emergence of 40 Gb/s data rates for long-haul fiber-optic links, can be seen as Internet traffic threatens to exceed network capacity. This year's ISSCC highlights 40 Gb/s amplifiers and clock-data-recovery circuits in advanced CMOS.
- Expectation of the introduction of significant amounts of signal processing to achieve such high data rates over low-quality legacy fiber, requiring continued use of these advanced process technologies.
- Legacy backplanes are continuing a renaissance that began several years ago with the use of low-cost electronics to boost data rates, instead of replacing the chassis.
- The emergences of digital signal-processing and software-based techniques replace building blocks which previously have been analog. This trend is enabled by the migration to 90nm and 65nm technologies that puts inter-chip communications on the same growth path as digital functions.

DATA RATE TRENDS



NOTES

ISSCC 2007

SESSION OVERVIEWS
Press-Release Material

- **Conditions of Publication**
- **Session Overviews**

CONDITIONS OF PUBLICATION

PREAMBLE

- **The Session Overviews to follow serve to capture the context, highlights, and potential impact, of the papers to be presented in each Session at ISSCC 2007 in February in San Francisco.**
- **OBTAINING COPYRIGHT to ISSCC press material is EASY !**
  - You are welcome to use this material, copyright- and royalty-free, with the following understanding:
    - That you will maintain at least one reference to ISSCC 2007 in the body of your text, ideally retaining the date and location. For detail, see the FOOTNOTE below.
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FOOTNOTE

- **From ISSCC's point of view, the phraseology included in the box below captures what we at ISSCC would like your readership to know about this, the 54nd appearance of ISSCC, on February 11th to 15th, in San Francisco.**

This and other related topics will be discussed at length at ISSCC 2007, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 11-15, 2007, at the San Francisco Marriott Hotel.

Optical Communications

Chair: *Sung Min Park, Ewha Womans University, Seoul, Korea*
Associate Chair: *Yuriy Greshishchev, Nortel, Ottawa, Canada*

Competitive future of optical communications entirely depends upon the development of low-cost optoelectronic solutions and low-cost high-performance clocking systems. One of the promising and effective ways to reduce cost is the integration of electronics and optical devices in a single chip. Paper 2.1 from Luxtera describes an integrated solution based upon recent advances in SOI photonics. Last year, an optical modulator and a WDM MUX/DEMUX were introduced by the same authors. This year, they introduced an optical interleaver that allows the integration of 4-channel optoelectronic devices. This dramatically reduces the cost of optoelectronics for DWDM applications. Paper 2.9 from Silicon Lab describes a fractional-N PLL in 0.13µm CMOS. It offers a low-cost solution for SONET clock generation with 0.3ps dynamic jitter in OC-192 band. The PLL uses a low-frequency crystal oscillator and a DSP-based loop filter and hence, it does not require any expensive VCXO.

Another way of reducing cost is the use of arrays of VCSEL optical devices. Paper 2.2 from Stanford and Columbia U introduces an optical transceiver exploiting a 4-tap FIR filter transmitter and an integrating/double-sampling receiver in order to remove the front-end transimpedance amplifier (TIA). Compared to Paper 2.1, this work implemented in 90nm CMOS includes a SERDES function with 5:1 MUX/DEMUX ratio.

PON systems currently operate at 1.25Gb/s. The frontier research presented in this session goes far beyond this speed and provides a potential solution even for 20Gb/s and 33.8Gb/s. The areas of interest are burst-mode fast-acquisition CDR circuits and also front-end transimpedance and limiting amplifiers.

Papers 2.3 and 2.4, both from National Taiwan U, describe burst-mode CDRs in 90nm CMOS. The former, based upon injection-locking scheme, operates at 20Gb/s with the acquisition time of 1UI. It also employs 2 gated-VCOs in series for improved jitter performance. The latter introduces a 33.8Gb/s burst-mode CDR, exploiting a new LC gated VCO, a phase selector, and transformer-based circuit solutions to improve input matching and bandwidth.

The next three presentations demonstrate the design of high-performance TIAs. Paper 2.5 from ETRI and ICU describes a burst-mode TIA in 0.18µm CMOS. It incorporates selective internal reset to simplify the burst-mode receiver design for 1.25Gb/s EPON systems. A 3Gb/s TIA is described in Paper 2.6 from National Chiao-Tung U and ITRI, focusing on the bandwidth and gain improvement with the combination of the self-compensated topology with the negative-impedance compensation technique. Paper 2.7 from National Taiwan U and NTU introduces a 40Gb/s transimpedance-AGC amplifier in 90nm CMOS, exploiting reversed triple-resonance networks and negative feedback in a common-gate configuration.

The authors of Paper 2.8 from Yonsei U and Ewha Womans U present a 2.5Gb/s limiting amplifier in 0.18µm CMOS, which employs the negative-impedance compensation technique for gain and bandwidth improvement. Operating with 1.2V power supply, it demonstrates 5.2mW power dissipation.

TD: Emerging Devices and Circuits

Chair: *Eugenio Cantatore, Philips Research, Eindhoven, The Netherlands*
Associate Chair: *Shuichi Tahara, NEC, Tsukuba, Japan*

The trend to provide increasingly complex electronic applications, to both support and improve one's life, compels the electronics industry to provide more and more processing power in portable and miniaturized, ubiquitous platforms.

The form factor of portable electronics is nowadays determined by the limited energy density offered by batteries. To overcome this limitation, circuit designers need to invent systems with unprecedented power efficiency. The design community is also investigating alternative methods to power circuits, in a continuing effort to improve portability and enable truly pervasive electronics.

On the other hand, novel applications often necessitate the use of novel technologies. Consumer electronics needs inexpensive and power-efficient interfaces and sensors to communicate effectively with users, while the quest for smaller, cheaper and higher performance solid-state devices fuels and ensures growth to the electronics industry.

The seven papers in this session offer a broad and exciting perspective on the latest achievements in these fields.

In the first part of the session, devoted to the efficient use of energy, Paper 3.1 from CEA LETI/LITEN presents an important milestone towards truly energy-autonomous microsystems: in the proposed solution, energy scavenged from a thermal source or from electromagnetic radiation is conditioned on-board and used to recharge an above-IC integrated battery. Paper 3.2 from MIT demonstrates a system able to automatically tune the power supply to reach minimum energy operation in a digital circuit. All active components of the control loop, i.e., the energy sensor, the controller and the DC-DC converter used to adapt the supply voltage (featuring >80% efficiency at more than 1μW from a 1.2V primary supply) are integrated in a 65nm technology. Paper 3.3 from U Tokyo and NEC presents an alternative method to achieve energy efficiency, based on the choice of a locally asynchronous, globally synchronous architecture where the power supply is regulated to the minimum value needed to achieve a pre-defined speed performance.

The second part of the session, focusing on novel solid-state devices, begins with two papers presenting the ultimate challenge in terms of device miniaturization: transistors and circuits based on carbon nanotubes. While Paper 3.4 from IBM describes advancements in device and circuit technology enabling complementary carbon nanotube logic, Paper 3.5 from Stanford and USC discusses the performance improvements that circuit designers can expect using carbon nanotubes, instead of ultra-scaled Si CMOS transistors. The session completes with innovative interface devices: Paper 3.6 from MIT and Columbia U discusses a flexible, large-area image sensor based on co-integration of organic semiconductor-based sensors and TFTs and Paper 3.7 from Kyushu U and Bridgestone presents a new, fast e-paper, enabling flexible, bi-stable passive matrix displays, together with its driving circuitry.

RF Building Blocks

Chair: *Nikolaus Klemmer, Ericsson Mobile Platforms, Research Triangle Park, NC*
Associate Chair: *Satoshi Tanaka, Hitachi, Tokyo, Japan*

Over the past decade, wireless-enabled devices have evolved from single-purpose, single-band, and single-modulation novelties to highly powerful, ubiquitously available, and ever more lifestyle changing information exchange devices with multi-band and multi-standard modulation capabilities. Growing popularity and per-user capacity requirements from mobile voice and data traffic, multi-purpose wireless information managers and entertainment devices, makes RF link capacity the driver for wireless technology development. To deliver on the wireless promise, regulatory bodies and network operators continue to open new frequency bands to accommodate more bandwidth and make use of higher-order modulation formats to increase bandwidth efficiencies. These introduce new challenges in the design of RF transceivers.

For mobile transmitters, design challenges arise from the need for high-linearity power amplifiers while simultaneously maintaining high power efficiency and low complexity. In addition, the interference environment for receivers is becoming more hostile, with a wider range of interfering bands and a wider range of interfering modulation formats, front-end linearity enhancement and circuit impairment cancellation methods are becoming more crucial. The higher number and a wider spread of allocated frequency bands globally pose stringent requirements on the frequency tuning range and noise performance of on-chip oscillators.

The focus of this session is on building blocks for RF transceivers that provide novel contributions to the design of linear high-efficiency transmitters, receiver front-ends that are able to cope with the presence of strong blockers and modulated interferers, as well as low-noise and high-tuning-range oscillators. Most notably, increased use of digital signal processing and calibration techniques in traditionally analog-only circuit blocks helps to achieve the presented performance increases.

The first three papers of this session describe transmitter building blocks. Paper 4.1 from Stanford shows an implementation of a digital-to-RF converter for use as an OFDM PA. Oversampling and interpolation of the digital amplitude information at RF helps to cope with aliasing artifacts. Paper 4.2 from U Catania and STMicroelectronics describes a 3W CMOS PA with a novel implementation of a closed-loop output load mismatch protection and Paper 4.3 from Arizona State U demonstrates increased power efficiency for polar-modulation PAs via the use of a combination switched-mode and linear power supply regulator system.

Paper 4.4 from Broadcom describes the use of a translational loop around a receiver LNA to cancel blocker signals at the input to the down-conversion mixer, while Paper 4.5 from U Erlangen-Nuremberg and Infineon demonstrates a continuously-on digital LMS-based background calibration scheme for cancellation of down-converter second-order nonlinearity effects. Paper 4.6 from Alfaplus Semiconductor and National Taiwan U makes use of scalable time-to-digital conversion techniques to reduce the SNR requirement, chip area, and power consumption of GFSK demodulators for Bluetooth receivers.

The last two papers focus on low-noise and high-tuning-range oscillators. Paper 4.7 from Epoch Microelectronics and Renesas Technology shows a current re-use technique that allows for low bias-current noise without adding extra bias-generator supply current. Finally, Paper 4.8 from U Pavia and STMicroelectronics shows the beneficial use of tunable current ratios in the windings of a transformer-capacitor resonator to increase oscillator tuning range to over an octave.

Microprocessors

Chair: *Stefan Rusu, Intel, Santa Clara, CA*
Associate Chair: *Jim Warnock, IBM, Yorktown Heights, NY*

This year's microprocessor session highlights the accelerating trend towards multi-core integration on a single chip, setting new records for the number of threads supported. This year, most of the chips presented feature at least 4 cores, a marked increase in integration from last year. Cache sizes continue to increase, with typically 2MB to 4MB L2/L3 integrated on-die. These advances in integration are enabled by ever increasing numbers of interconnect layers, with two papers describing the use of 11 interconnect layers, and also the progression to 65nm technology. Power continues to be a critical concern, as all papers describe special active power and leakage reduction techniques. Most of the designs focus on low-voltage operation, presenting circuit techniques for minimum supply-voltage reduction, and two papers describe independent dynamic frequency control of individual cores. Even as the industry shifts towards multi-core, power-constrained designs, frequency improvements are still possible, with a new record being reported this year for microprocessor operating frequency.

The session starts with Paper 5.1 from IBM describing the dual-core POWER6™ design, operating at frequencies up to 5GHz. The 341mm^2 die contains over 700M transistors and is fabricated in 65nm SOI technology with 10 levels of interconnect. Paper 5.2 from Intel is also a high-frequency design, describing a network-on-chip architecture that contains 80 tiles including floating-point cores and packet-switched routers, all operating at 4GHz. The 100M transistor die, implemented in 65nm technology, achieves 1TFLOP peak performance using a variety of circuit techniques to keep power dissipation under 100W. The third paper, 5.3, from Renesas, Hitachi, and Waseda U describes a quad-core SoC implemented in 90nm triple-V_T CMOS technology with 8 levels of metal. This chip also employs advanced techniques to reduce average operating power with the capability of operating each processor core dynamically at a different frequency. With a die size of less than 100mm^2 this chip achieves a performance 4320MIPs and a floating-point performance of 16.8GFLOPS.

In the second half of the session, all four papers describe multi-core microprocessors implemented in 65nm CMOS technology. The first quad-core Opteron™ processor is presented by AMD in Paper 5.4. Similar to the previous paper, this design allows independent dynamic frequency control of each core. The 450M transistor chip is built in 65nm SOI technology with 11 interconnect levels. Each core includes 512kB of L2 cache, with a 2MB L3 cache shared by all cores. Paper 5.5 from PA Semi describes a power-efficient SoC integrating two 2GHz Power™ cores with shared 2MB L2 cache, coherent crossbar interconnect, and memory and I/O subsystem. The 115mm^2 die is implemented in a 65nm 8-layer metal technology. Paper 5.6 from Intel describes the dual-core, and quad-core (on MCM) implementations of the Core™ architecture. The 143mm^2 die has 291M transistors in an 8-layer metal 65nm process. The shared 4MB L2 cache uses PMOS power gating to minimize leakage. The processor has a wide operating range, from 0.85V to 1.325V, at frequencies from 1 to 3GHz. Finally, Paper 5.7 from Sun Microsystems presents the 8-core, 64-thread second generation Niagara SPARC™ SoC, doubling the number of threads from the previous design. The chip integrates 4MB L2 cache, one x8 PCI-express, two 10G Ethernet ports, and 8 FBDIMM ports. The 500M transistor chip, with a die size of 342mm^2, is implemented in an 11-metal 65nm triple-V_T CMOS process.

UWB & mm-Wave Communications Systems

Chair: *Sang-Gug Lee, ICU, Daejeon, Korea*
Associate Chair: *Ranjit Gharpurey, University of Texas at Austin, Austin, TX*

Ultra wideband (UWB) systems promise a revolution in radio technology with the ability to support data rates 1Gb/s. Transceivers exemplifying two different system approaches, namely, multi-band OFDM and pulse-based schemes, continue to make significant strides in performance compared to prior years. In addition to high data-rate applications, these systems can provide highly efficient communications in terms of data-rate per unit power. The UWB approach is thus suited for wireless sensors, where the data rate is relatively modest, but battery lifetime is of critical importance. Another emerging application for UWB systems is in the area of vehicular radar. Transceivers and synthesizers for the above applications are discussed in this session.

A WiMedia-compliant UWB transceiver is discussed in Paper 6.1 by Philips and NXP Semiconductors. Implemented in a 65nm CMOS process, the highly linear transceiver supports communications in MB-OFDM band groups 1 and 3. The chip consumes 114mW by drawing 95mA from a 1.2V supply.

Paper 6.2 from Singapore Institute of Microelectronics describes a dual-band transceiver for a high-data-rate pulse-based UWB approach. The transceiver is implemented in a 0.18µm CMOS process and consumes 138.8mW in the receive mode and 99mW in the transmit mode. It supports data rates of up to 800Mb/s.

An energy-efficient receiver for wireless sensor networks is presented in Paper 6.3 by MIT. Implemented in 90nm CMOS, the radio can support data rates of up to 16Mb/s, utilizing the 3-to-5GHz UWB band with an energy requirement of 2.5nJ/b.

In Paper 6.4 from MIT, a fully digital UWB transmitter that is implemented in a 90nm CMOS process and generates PPM pulses in the 3-to-5GHz band is presented. The transmitter has a low energy requirement of 47pJ/b, and generates output pulses without using an RF oscillator.

Paper 6.5 from IMEC and Vrije U Brussel describes a low-power UWB transmitter that supports the IEEE 802.15.4a standard. It utilizes a digitally controlled oscillator to generate RF carriers for all bands between 3 and 10GHz, and a digital modulator to generate BPSK symbols at the required 500MHz chip rate.

A baseband lowpass filter for the WiMedia UWB system is presented in Paper 6.6 by TKK Helsinki. The chip uses a 5^{th}-order g_m-C lowpass topology and includes 13 to 48dB of gain control.

Paper 6.7 from USC describes a phased-array transceiver for 24GHz applications including communications and radar. The transceiver is implemented in a 0.13µm CMOS technology and uses beam-forming techniques to achieve a transmit EIRP of greater than 23.8dBm and a receiver gain that exceeds 42dB.

Finally, in Paper 6.8 from Arizona State U and TI, a 19GHz frequency-modulated continuous-wave transmitter based on a bandpass ΔΣ DDFS-driven RF frequency synthesizer is described. The transmitter is implemented in a 0.25µm BiCMOS process and can provide an output power of -5dBm while drawing 63mA from a 2.5V supply.

Display Electronics

Chair: Hiroyuki Hirashima, *Sharp Corporation, Nara, Japan*
Associate Chair: Oh-Kyong Kwon, *Hanyang University, Seoul, Korea*

Flat-panel displays are being used in many new applications. These applications require that all sizes of displays continue to improve display quality, as well as reducing power and cost. For large displays, cost is a very important consideration because of the expanding market size and increasing competition. For small- and medium-sized displays, on the other hand, the applications require integrating more features into the displays. For example, displays may include fingerprint recognition, touch screens, ambient brightness sensing and backlight control, or other smart functions.

In this session, five papers describe work to extend the performance, add more functionality to, and reduce the power dissipation of mobile displays. Two papers describe efforts to improve the performance and reduce the cost of large displays, and one paper describes a DC-DC converter for active-matrix OLED mobile displays.

The authors of Paper 7.1 from Samsung and Hanyang U, present a design that achieves greater color depth using LTPS system-on-glass TFTs for QVGA active-matrix OLEDs. This display uses a new 8b DAC architecture that reduces the source driver size by 40% and achieves a maximum DNL of less than 1LSB.

Paper 7.2, from Sharp, describes a 2.6 inch VGA active-matrix LCD that has an integrated optical input function. This function enables touch input or fingerprint recognition applications and uses a 1-transistor active-pixel sensor integrated into each display pixel to achieve an aperture ratio of 40%. The 300dpi sensor image is output with a 30Hz frame rate. In Paper 7.3, from Samsung, the authors present an integrated LVDS display interface (LDI) that includes a readout function for displays that have embedded touch sensors.

In Paper 7.4 the authors, from KAIST and JDA Technology, describe a DC-DC switching converter for active-matrix OLED mobile display panels. The dual-output step-up converter uses only one inductor.

Paper 7.5, from Hanyang U and Samsung, describes a 10b driver IC for laser projection full-HDTV applications. The driver uses a 7b resistor-string DAC and a unity-gain buffer with a 3b DAC. It has 546 output channels and a maximum settling time of 2.4μs for a 1080-pixel spatial optical modulator with 40pF capacitive loads.

The authors of Paper 7.6, from Samsung, present a one-chip 16.7M-color VGA display driver IC featuring partial graphic RAM and a 500Mb/s/ch high-speed serial interface. This driver pairs with a 1.98 inch mobile VGA amorphous-silicon TFT-LCD panel with 400 pixels per inch. The driver is fabricated in a 0.18μm triple-well CMOS process.

Paper 7.7, from KAIST, Siliconworks and LG.Philips LCD, focuses on the column driver design as a means to reduce chip size and power consumption. The authors present a column driver using push-pull buffer amplifiers operated in a transient mode.

Biomedical Devices

Chair: Roland Thewes, *Qimonda, Neubiberg, Germany*
Associate Chair: Dennis Polla, *DARPA, Arlington, VA*

CMOS ICs for biomedical applications have attracted a great deal of interest in recent years. The signal processing and computing capabilities available in small devices with low power consumption open up new horizons in biomedical interfacing. While some of these CMOS-based techniques are still in their infancy, others have already provided commercial solutions. In this session, recent advances are presented concerning prosthetic and implantable devices, in-vitro neural recording, and amplifiers for bio-electrical signals, magnetism-based cell imaging and bio-molecule detection techniques.

Paper 8.1, from sci-worx and IIP Technologies, reports on a retinal implant with a total of 232 channels, where 116 of these can be independently operated – the highest number of channels reported to date. Moreover, special emphasis is put on programmability, testability and safety.

The authors of Paper 8.2, from KAIST, present a hearing aid chip custom tailored to the individual's auditory canal. Key innovations in this chip include the implementation of a pre-fitting verification algorithm that implements both coarse and fine amplifier gain adjustments. A significant amount of electronics was integrated with the hearing aid to implement this new algorithm.

Paper 8.3, from UC Santa Cruz, reports on the use of a PSK receiver using bandpass sampling for potential neural implant stimulation applications. This approach eliminates the need for phase-locked loops in recovery circuits and implements an attractive approach for realizing transcutaneous inductively-coupled telemetry to support high-data-rate neural implants such as 1000-electrode arrays to be used in future retinal prosthesis systems.

CMOS chips are highlighted for in-vitro recording and stimulation of neural tissue. Paper 8.4, from ETH Zurich, NewLogic and Miromico, describes a CMOS microelectrode array with 126 channels. By selecting target sites within an array of 11k electrodes by means of a switching matrix, a spatial resolution of 18µm is achieved, allowing one to focus the available recording and stimulation capability on regions of interest within neural tissue slices. An alternate neural interface in Paper 8.5, from U Toronto and Toronto Western Hospital, uses a 2D CMOS chip with 256 channels combined with noble metal needles to form a 3D interfacing system. High recording accuracy and data compression are obtained by using a SC-based delta read-out approach.

Two amplifiers are presented for bio-electrical signal detection and processing. Paper 8.6, from Medtronic, describe an ultra low-power, low-noise chopper-stabilized instrumentation amplifier for "deep brain" human implants. A current-sensitive amplifier is presented in Paper 8.7 by Politecnico di Milano uses a specifically developed design technique to provide ultra-high resistance active resistors up to 300GΩ. These are operated in the feedback path of a transimpedance amplifier interfacing with extremely low signal currents.

The authors of Paper 8.8, from National Tsing Hua U report on their work integrating MEMS gradient- and RF-coils with CMOS circuitry for a new compact approach to 3D cellular imaging. Miniaturization and integration methods are described for future high-resolution magnetic resonance imaging (MRI) microsystems.

Finally, Paper 8.9, from Stanford and Stanford Genome Technology Center, expounds on the circuit design issues addressed by the first CMOS-based magnetoresistive DNA microarray. Based on a 0.25µm BiCMOS technology, the sensor-site circuitry provides input-referred noise levels below 55nV/√Hz. Drifts induced by chemical and biochemical reactions are removed using AC techniques; readout is realized by means of combined frequency-division and time-division multiplexing.

Clocking

Chair: Thucydides Xanthopoulos*, Cavium Networks, Marlboro, MA*
Associate Chair: Atila Alvandpour*, Linköping University, Linköping, Sweden*

The job of the clock designer in a large digital chip is increasingly challenging. The designer is faced with the competing requirements of increasing clock frequency and clock distribution area, reducing skew, jitter, and power dissipation, all while adding testability and reliability features. Furthermore, recent design trends in digital chips use variable supply voltages and operating frequencies to achieve multiple power/performance envelopes to enable products that simultaneously address different market segments. These requirements place additional burdens on the clocking system, especially on the clock generation mechanism.

Although traditional analog PLLs have very good jitter performance, they are not versatile enough for these applications in terms of power supply and tuning range. Moreover, migration to more advanced process nodes with higher-leakage devices requires challenging and time-consuming redesign of analog circuits. Going all-digital addresses the issues of process migration, supply voltage versatility and wide dynamic range. But can an all-digital clock generator ever approach the jitter performance of an analog one? Can we build an all-digital clock generator that reaches 40GHz? There are three papers in this session that provide concrete answers to these questions.

Despite their problems and limitations, traditional balanced-tree-based clock distributions are not going away any time soon since they are robust and well-understood. Over the past few years, this conference has presented alternative distribution methods based on traveling rotary waves, standing waves and LC resonance. Although the feasibility of such distribution schemes for a large digital chip is yet unproven, their benefits are hard to ignore. The benefits include lower power dissipation from energy recycling, reduced jitter due to LC filtering, and limited buffering and limited skew due to the predictability of electromagnetic wave properties. Two papers in this session advance the state-of-the-art in LC techniques. Finally, two papers present interesting digital phase-locking techniques with a wide application range.

Paper 9.1 from IBM presents an all-digital PLL (ADPLL) with a 0.5V-to-1.3V supply range and 500MHz-to-8GHz output frequency range. The ADPLL uses an inverter-array structure as a VCO, which has a wide and linear tuning curve. The achieved period jitter is 0.7ps rms, good enough for very demanding digital applications. The design follows the trend of multiple power/performance operating points dissipating 8mW/GHz at 1.2V and 1.6mW/GHz at 0.5V. Clock multiplying DLLs are a well-known technique for delay-line-based clock generation. Paper 9.4 from NTU takes this concept to the next level by using this structure to generate a 40GHz output clock in 90nm CMOS. The authors solve the coarse delay resolution problem by phase locking the delay line to multiple clock periods and using equivalent phases from different periods to feed an LC-tank based oscillator. Paper 9.2 from NEC is also a clock-multiplying DLL using a multiplexer-based edge interleaver as the clock multiplier. The edge interleaver, along with dithering techniques, enables high resolution control of both rising and falling edges that makes this system appropriate for testing timing margins.

Paper 9.5 from Hiroshima U and Elpida presents a standing-wave clock oscillator that solves the issue of diminishing clock amplitude along the length of the transmission line by using inductive loading. Multiple such oscillators are synchronized and form an entire distribution scheme by magnetic coupling. Paper 9.6 from UCLA presents an LC-based clock distribution that trades off input versus clock buffer jitter. This adaptive scheme achieves power reduction while maintaining low jitter by adaptively adjusting the ratio between the LC-resonant buffer and the injection-locked oscillator.

Paper 9.3 from IBM describes a digital technique for static phase offset reduction in a PLL. It can be used in applications where a small offset between reference and output clock is desired, and as an added benefit the reference spur is reduced. Paper 9.7 from Korea U and Hynix presents an interesting open loop DLL based on replica delays. It has a fast lock time, wide dynamic range and includes duty-cycle correction.

mm-Wave Transceivers and Building Blocks

Chair: Ali Niknejad, *University of California, Berkeley, CA*
Associate Chair: Hiroyuki Sakai, *Matsushita Electric Industrial, Osaka, Japan*

Technology scaling and Moore's law have paved the way for ever faster transistors, with device unity gain frequency (f_t) exceeding 100GHz for today's 90nm CMOS technology. The realization of functional circuits operating at or above the device f_t is a challenging task, and the subject of much of this session, with demonstrations of circuits operating above the f_t and close to the device f_{max}. The main advantages of Si-based technologies are the promise of high levels of integration and low manufacturing cost. In fact, in this session we see several highly integrated CMOS and SiGe front-end receivers and frequency synthesizers integrated into a single chip operating in the mm-wave frequency range.

Operation of high frequencies has several interesting and important applications. The 60GHz band offers a wide unlicensed spectrum allowing extremely high data rate multi-Gb/s communication systems. Traditionally 60 GHz radios were built as modules with expensive III-V technologies. The realization of low-cost integrated circuit solutions will allow widespread commercial deployment of multi-Gb/s communication devices, allowing short range personal area networks for downloading multi-media (video) to mobile devices, Gb/s wireless LAN for an untethered connection to the network, and high data rate point-to-point communication and indoor video transmission. The key technology challenges to compete in this market are low-noise operation, high output power capability, and low phase-noise voltage-controlled oscillators.

Moving beyond 60GHz opens the door to new potential applications such as automotive radar, medical imaging, and security. Due to the high cost of mm-wave electronics, today only high-end automobiles are equipped with radar for automatic cruise control and safety. Implementation of such systems in Si integrated circuits can reduce the cost by an order of magnitude, enabling ubiquitous adoption of radar, increasing the safety and security of transportation. Other potential applications include mm-wave medical imaging as a low-cost non-ionizing alternative to x-rays.

The session begins with the three of the first reported highly integrated CMOS mm-wave transceivers. Paper 10.1 from UCLA demonstrates a 50GHz CMOS heterodyne receiver in 90nm technology. The chip includes the LNA, mixer, LO and divider. Paper 10.2 from UC Berkeley and SiBEAM presents a 60GHz highly integrated receiver in 0.13µm technology, including the LNA, mixer, LO, and frequency doubler. Paper 10.3 from National Taiwan U describes a fully integrated 60GHz 0.13µm CMOS six-port transceiver which includes transmit and receive amplifiers, RF switch, transmit VCO and modulator, and a six-port power detector. This paper demonstrates successful demodulation of data up to 4 Gb/s using BPSK modulation. All three papers represent the state-of-the-art in integration of CMOS mm-wave circuits into a single chip.

Paper 10.4 from TU Delft and IBM presents a varacterless VCO in 0.13µm CMOS that operates from 23 to 29GHz using a coupled-inductor tuning scheme. In Paper 10.5 by National Taiwan U, the first 60GHz synthesizer realized in 90nm CMOS technology is presented with record levels of integration and phase noise for CMOS mm-wave applications. Paper 10.6 from Bochum Rohr-U describes a divider with record speed performance as fast as 90GHz that is realized with an injection-locked topology in a 65nm CMOS process.

Paper 10.7 from UC Berkeley includes the world's fastest CMOS tuned amplifier, working up to 104GHz in a 90nm CMOS process. This paper also demonstrates record power performance for a 60GHz amplifier, and a high output power 104GHz oscillator. The final paper of the session, Paper 10.8 by Caltech, describes a highly integrated bidirectional SiGe phase shifter for RF-combining phased-array applications.

TV Tuner/RFID

Chair: David Su, *Atheros Communications, Santa Clara, CA*
Associate Chair: Bud Taddiken, *Microtune, Plano, TX*

We are in the early stages of a worldwide transition in television broadcasting from analog to digital. In a few places in the world, analog broadcasts have already been switched off; however, most of the world will still require support for legacy broadcasts through 2009, 2012, and even 2015. During this transition period, it is necessary to support both the legacy analog TV standards – NTSC, PAL, and SECAM – as well as the new digital TV standards – DVB-T, ISDB-T, and ATSC. Because of this transition, there will be a multi-year increase in the unit volume shipments both for digital TVs that incorporate both digital and analog reception and also for converter boxes that accept a digital TV input and convert it to an analog TV output for display on a legacy analog TV. The technical challenges for receiving analog or digital TV broadcasts are different, and the challenges increase when both must co-exist. In addition to the technical challenges, the cost of the solution must also be made very low for wide market adoption. Today, almost all TV sets and off-air set-top converter boxes still use surprisingly low-cost tuner modules consisting of hundreds of discrete components and requiring manual tuning (frequency alignment). The first three papers in this session present highly integrated TV tuners to meet both the technical and commercial challenges of the digital TV transition around the world.

Up until now, highly integrated silicon TV tuners have employed dual (up-down) conversion, low IF, and – in the case of some mobile TV applications – even direct conversion when the input frequency range was narrow enough to avoid harmonic mixing of large interferers. Paper 11.1 from Chrontel and UCSD is the first publication of a direct-conversion TV tuner that covers the full 48-to-860MHz TV bandwidth and solves the harmonic mixing problem. For this highly integrated design, all necessary filtering is included on the 0.18µm CMOS chip: good image rejection is achieved and power consumption is 750mW. A SiP solution that also covers the full 48-to-860MHz TV bandwidth is presented in Paper 11.2 by NXP Semiconductors. The SiP uses a low-IF approach with discrete LC tracking filters. The 0.25µm BiCMOS die inside the SiP has smaller die area than either Paper 11.1 or 11.3. Power consumption is 750mW, and good image rejection is achieved with an auto-calibration technique. Paper 11.3 from Microtune employs a dual-conversion architecture with external filters that not only covers the full 48-to-860MHz TV bandwidth but also extends the range to a full 1GHz for compatibility with next generation CATV systems. The 0.35µm SiGe BiCMOS die is slightly larger than that of Paper 11.2 and consumes 1.5W. It achieves excellent image rejection, adjacent channel rejection, and fully loaded cable performance.

An RF tuner plus baseband demodulator chipset for ISDB-T mobile TV reception is presented in Paper 11.4 by Sharp. The RF tuner covers the 470-770MHz UHF bandwidth. Nominal power consumption for the chipset is a mere 105mW and compsumption as low as 77mW is demonstrated in the absence of strong interferers using an adaptive power control technique. The tuner uses 0.5µm BiCMOS while the baseband demodulator uses 0.13µm CMOS.

The use of near-field radio frequency identification (RFID) systems based on inductive coupling is gaining momentum in a wide variety of applications such as supply-chain management, anti-fraud solutions, and object tracking systems. UHF RFID systems operating at 900MHz has extended range and higher data rates compared to traditional lower frequency RFIDs at 125kHz and 13.56MHz. The main challenge in the design of RFID reader is to receive weak signals while transmitting a 20 to 30dBm CW signal to power the passive RFID tags. This session includes three highly integrated UHF RFID papers that can receive weak signals in the presence of large CW blocker without requiring highly selective off-chip filters. A UHF RFID transceiver implemented in 0.18µm BiCMOS technology is described in Paper 11.5 by Intel and Catena. This transceiver features a 20dBm power amplifier and an I/Q receiver with -83dBm sensitivity in the presence of a 0dBm blocker. A 0.18µm CMOS UHF RFID transceiver is presented in Paper 11.6 by Samsung and Kwangwoon U. This transceiver has a die size of 23.8mm^2, 18.5dBm IIP3, and 4dBm transmit power. Finally, in Paper 11.7 from UC Irvine, a novel receiver topology that can handle a large CW jammer is presented. This design employs two parallel paths, an LNA, and a limiter, to receive an incoming signal. The CW jammer is extracted by the limiter and then removed from the LNA output.

Gigabit CDRs and Receivers

Chair: John T. Stonick, *Synopsys, Hillsboro, OR*
Associate Chair: Jri Lee, *National Taiwan University, Taipei, Taiwan*

Two critical technologies for the design of robust Gb/s communication links are clock and data recovery (CDR) circuits and equalizers. As communication links operate at higher speeds, the symbol intervals are becoming extremely short. At 40Gb/s the entire bit interval is only 25ps! Two papers in this session provide innovative solutions to the problem of operating CDR circuits in CMOS at such speeds. An additional challenge of realizing CDR circuits in shrinking technologies is coping with performance degradation of analog circuit elements. One paper in this session overcomes this challenge with an all-digital CDR. Of course, for a CDR to operate properly; it often requires an equalizer to improve the input signal quality. However, applications and channel degradation vary widely and thus require a broad range of equalizers optimized differently for complexity and power consumption. In this session, 3 equalizer solutions are presented. Finally, while CDR circuits are critical to the performance of most digital communication systems, the session concludes with an interesting study of the power/performance tradeoffs of utilizing transparent mode repeaters in memory interfaces.

The first paper from Seoul U focuses on overcoming the difficulty of realizing CDRs in shrinking process technologies by presenting a purely digital approach to clock and data recovery. The resulting circuit is small in area ($0.13mm^2$) and achieves 7.2 ps_{rms} jitter when operating at 2.8Gb/s from a sub-1V supply. A key aspect of the design is its 10b DCO which does not utilize any analog circuits.

The pursuit of low-power 40Gb/s CDRs in CMOS is a difficult and compelling problem. In the next 2 papers, two different solutions are presented. In Paper 12.2 from Fujitsu, an oversampling CDR utilizes a 24-phase clock to retime and demultiplex the input into 16 channels. The circuit consumes less than 1W and conforms to the ITU G.8251 jitter tolerance mask. In Paper 12.3 from IBM, a quarter-rate CDR incorporating a phase-programmable clock consumes only 72mW while operating at rates in excess of 40Gb/s. Fabricated in 65nm CMOS technology, it uses no inductors and occupies only $0.03mm^2$.

At this point the focus of the session switches from CDRs to the circuits that make them possible to achieve their performance, equalizers. The most challenging channels require DFEs to compensate for ISI impairments without enhancing crosstalk and noise. It is well known that one of the most challenging issues of a DFE is the timing of the loop from the sampler, through the decision circuit and back to the equalizer. In this paper, the concept of loop unrolling or partial response is extended from the first tap to the second tap. An additional innovation is the use of spectrally gated adaptation to prevent the tap drift that can occur during long periods of spectrally non-white data.

A second major hurdle in the deployment of DFEs is their power dissipation. In Paper 12.5 from MIT and IBM, a summing stage based on clocked integrators is adopted to save power. The result is a power consumption of only 9.3mW for 7Gb/s operation. Yes, that is not a typo 9.3mW at 7Gb/s.

In Paper 12.6 from Texas A&M, a 1Gb/s 5-tap T/2 fractionally-spaced transversal equalizer constructed from 3^{rd}-order linear-phase cells is presented. This paper presents an excellent solution to the problem of designing delay cells which have constant group delay and magnitude response over the data bandwidth. An additional key innovation is to improve the bandwidth of the summing circuit by utilizing a transimpedance load. The result is an increase in bandwidth by a factor of 3.6 over a conventional resistive load.

Finally, the session which was initially focused on CDR circuits ends with a twist. Paper 12.7 from Qimonda makes a convincing case for using transparent mode repeaters (no CDR) instead of resampling mode repeaters in point-to-point daisy-chained memory interface operating up to 5.3Gb/s. Operating the repeaters in transparent mode consumes 40% less power and has 80% less latency!

ΔΣ ADCs and Converter Techniques

Chair: Zhongyuan Chang, *IDT-Newave Technology, Shanghai, China*
Associate Chair: Tatsuji Matsuura, *Renesas Technology, Tokyo, Japan*

The ever-increasing data rates in multi-standard wireless communication systems demands for wireless receivers with higher dynamic range and wider bandwidth. Further, the power consumption of the receiver building blocks should be kept at minimum. Reconfigurable ΔΣ modulators are the promising ADC topologies to cope with multi-standard challenges due to their power efficiency and high SNR. This session highlights the advances in ΔΣ modulators and other converter techniques that enhance the dynamic range and power consumption of ADCs.

In Paper 13.1 from NXP Semiconductors, a quadrature ΔΣ modulator with 77dB dynamic range and 20MHz bandwidth for near-zero-IF wideband receivers is presented. The quadradure modulator employs a cascade of 2 continuous-time modultors with a digital quadrature noise-cancellation filter. Implemented in 90nm CMOS, the modulator achieves 71dB SNR in 20MHz bandwidth.

In the next 3 papers, the authors report the implementation of ΔΣ modulators that are targeting multi-band wireless applications. Paper 13.2 from Advanced Circuit Pursuit and ETH describes a 0.13μm tri-mode (EDGE/UMTS/WLAN) ΔΣ ADC with -92dB THD. The modulator employs a 2-2 cascaded feedforward topology with reduced integrator swing for 1.2V operation. Low power and reconfigurability are achieved by programming optimal oversampling frequency and opamp biasing. In Paper 13.3 from NXP Semiconductors, the implementation of a reconfigurable continuous-time 5^{th}-order single-bit ΔΣ modulator in 90nm CMOS is presented. The modulator consists of a continuous-time feedforward loop filter combined with switched-capacitor feedback DAC to minimize the effect of clock jitter. The extensive reconfigurability of 121 modes with dynamic-range/bandwidth of 85dB/100kHz to 52dB/10MHz is demonstrated covering the whole range of GSM to WLAN/WiMAX applications. The next paper, 13.4 from NXP Semiconductors, reports on a 5^{th}-order ΔΣ modulator embedded in an EDGE/CDMA/UMTS receiver in 65nm CMOS. By combining a front-end continuous-time integrator with discrete-time 2^{nd}- to 5^{th}-stage integrators, low power and accurate transfer function are achieved. An open-loop switched-capacitor OTA is used for the discrete-time integrator allowing fast settling with low power consumption resulting in an FOM as low as 0.25pJ/conversion-step.

Low-power and high-speed SAR converter techniques are demonstrated in the next 2 papers that push the performance limit of conventional SAR ADCs. A charge-sharing SAR ADC in Paper 13.5 from IMEC reports an FOM of 65fJ/conversion-step by using the passive charge-sharing techniques, dynamic offset calibration, and an asynchronous controller. Paper 13.6 from Infineon reports a 14b 2× time-interleaved SAR ADC operating at 480MHz with redundancy pushing the conversion rate up to 40MS/s with 66mW in 0.13μm CMOS, which surpasses previously achieved performance by pipelined ADCs.

The last paper, 13.7 from Infineion, reports a 13b 25mW 200MS/s DAC in 0.13μm CMOS operating at 1.5V. Two novel background calibration techniques are proposed: the nested background calibration trims all segments without the use of current splitters, and randomized period calibration converts spurious tones into wideband noise resulting in 87.3dB SFDR.

Baseband Signal Processing

Chair: Steffen Paul, *Infineon, Neubiberg, Germany*
Associate Chair: Tzi-Dar Chiueh, *National Taiwan University, Taipei, Taiwan*

The computational demand of today's wireless standards has reached a level that requires a high degree of CMOS integration. In this session, different aspects of such implementations are discussed at the block, architectural, and system level. Clock recovery as an important module in a design is discussed. Decoding at high data rates expands the application of wireless communications. In the emerging market of multi-standard terminals, new architectural proposals are an active area of investigation. Among such proposals is Network-on-Chip as an interconnect technology between processing elements. Base station signal processing for WCDMA/HSPA demands high integration and high performance while on the terminal side, ultra low-cost platforms attract market share. MIMO as a transmission technology enables high data rates and more efficient use of spectrum.

Paper 14.1 from MediaTek presents the first RTL cell-based clock recovery circuit for optical disc drives. The clock recovery circuit can be easily migrated to other technologies because it is synthesizable.

In Paper 14.2, from Intel, an on-die special purpose channel decoding accelerator for high-performance processors is shown. It reaches a data rate of 1.9Gb/s and is reconfigurable.

Network-on-Chip (NoC) for communication among 20 processing nodes for use in telecommunications applications is presented in Paper 14.3 by CEA-LETI, France Telecom, Mitsubitshi, STMicroelectronics. This chip explores an architecture for future multi-mode wireless terminals.

Different goals of integration for cellular wireless chips are presented in the next three papers of this session. In Paper 14.4 from ETH, ACP, Miromico, a power and area-efficient baseband ASIC realization is described. The design contains a multi-mode front-end suited for EDGE, WCDMA, and WLAN modes. Furthermore, the baseband processing for WCDMA and HSDPA is added as hardware accelerators.

The integration of 3 DSP cores and support of WCDMA/HSPA+ base station signal processing on a single chip is reported in Paper 14.5 from TI. This allows for a reduction in the cost of base stations.

Paper 14.6 from Infineon describes the full integration of the power management unit into a GSM compliant baseband radio GSM chip, helping to accelerate the arrival of ultra low-cost terminals.

A PHY and MAC processor for draft 802.11n, featuring a 3x3 MIMO system, is presented in Paper 14.7 from Atheros Communications. The system transmits data at a maximum rate of 300Mb/s or at a maximum range of 700ft.

Multimedia and Parallel Signal Processors

Chair: Michel Harrand*, CEA,Gif-sur-Yvette, France*
Associate Chair: Liang-Gee Chen*, National Taiwan University, Taipei, Taiwan*

Consumer electronics equipment such as game consoles, mobile handsets, home entertainment, or automotive security systems have become a major driver for high-performance yet low-power signal processing circuits. The diversity of new emergent standards adds a requirement for flexibility as an increasingly important feature of these systems. The trade-off between flexibility, performance and power consumption is addressed through a wide range of architectures mixing programmable and dedicated blocks.

On one extremity of this scale are massively parallel processing systems for applications such as video scene analysis like those presented in the first half of this session. On the other side of this scale are dedicated circuits for 3D graphics or video encoding/decoding still supporting several standards and offering programmable trade-offs between performance and power consumption. Examples of such circuits are presented in the second part of the session.

The first two papers present completely different massively parallel processing architectures:

Paper 15.1 from Philips and NXP presents a single-instruction multiple-data (SIMD) processor well-suited to the frame-iterative algorithms required by video scene analysis applications. It features 320 processing elements providing 107GOPS for a power consumption of 600mW, and 10M on-chip memory able to store up to 4 VGA images interconnected through a 1.3Tb/s network. An innovative internal feedback path is provided to have a low-cost look-up table for the vector data.

Paper 15.2 from Stream Processors and Stanford presents a stream processor based on a VLIW architecture. The chip features 80 parallel ALUs organized into 16 data-parallel lanes running at 800MHz, and 2 CPU cores. It provides 512 8b GOPS at a power consumption of 0.082mW/MMAC (16b).

Paper 15.3 from Renesas, NTT DoCoMo, Fujitsu, Mitsubishi and Sharp presents a chip integrating a dual-mode WCDMA-HSDPA/GSM-EDGE baseband with multimedia functions such as MPEG4 and /H264 video codecs, 3D graphics, and GPS. It includes 3 processor cores running up to 390MHz and dedicated hardware accelerators. In order to optimize static power consumption, the chip is split into 23 power islands, and a retention mode is implemented on its cache memories. Dynamic power consumption reduction is addressed through a dynamic bus-clock stop scheme. Bandwidth with the external SDRAM is minimized through a specific on-chip interconnection buffer.

The next two papers in this session demonstrate novel designs for 3D graphics processing:

Paper 15.4 from KAIST presents a 36 frames/s SXGA 3D display processor with a programmable 3D graphics rendering engine. This is the first implementation of a real-time 3D display processor. The integrated rendering engine supports Pixel Shader 3.0 and OpenGL ES 2.0, which supports advanced functionalities that provides users with a realistic experience in real-time interactive 3D applications like games and GUI.

Paper 15.5 from KAIST presents a 52.4mW 3D graphics processor with 141Mvertices/s vertex shader and 3 power domains of dynamic voltage and frequency scaling. This graphic processor is 17.5% faster, consumes 50.5% less power and takes 35.4% less area than previous designs. It presents the first unification of floating-point vector, transcendental and matrix operations in a single arithmetic platform. The chip also improves its power efficiency by using 3 power domains of dynamic voltage and frequency scaling.

Paper 15.6 from National Chung-Cheng U and National Yun-Lin UST presents the first dynamic quality-scalable H.264 video encoder chip suitable for power-adaptive video applications. With 0.13µm CMOS technology, the chip consumes 7mW~183mW in encoding CIF~HD720 videos at the cost of 470kgates and 13.3kB SRAM. Compared to the state-of-the-art design for real-time HD720 video encoding, it presents a reduction of 49% in gate count and 61% in internal memory.

The final paper, Paper 15.7 in this session from National Chung-Cheng U and Feng-Chia U introduces a 71mW 252kgates Multi-Standard Multi-Channel Video Decoder for High Definition Video Applications. This design provides decoding functionalities for JPEG/MPEG-1/2/4/H.264 image/video standards. Through a 70% reduction in external memory bandwidth and 60% reduction in computational complexity, the proposed chip reduces gate count by 72% and power consumption by 87% as compared to the state-of-the-art design in 0.13µm CMOS technology.

Power Distribution and Management

Chair: Alice Wang, *Texas Instruments, Dallas, Texas*
Associate Chair: Jos Huisken, *Silicon Hive, Eindhoven, The Netherlands*

There is an extreme range of power constraints in today's electronic applications, ranging from high-performance servers to low-power personal-health-care products. Traditionally, chips in these domains have been designed with a fixed power-supply-voltage and frequency. With the explosion in variability in today's nanoscale circuits, fixed operating points with large process variations require wide design margins, incurring a cost in power consumption or performance. Squeezing the most out of these designs involves optimizing the power distribution and management methods. To do this, two independent technologies are needed: the ability to measure accurately the chip behavior and the ability to use this information to control system parameters such as frequency and voltage.

The seven papers in the session present techniques allowing designers to take advantage of adaptive systems to reduce design margins and either improve performance or reduce power dissipation. For the coming years, this kind of adaptive control will be essential for maintaining growth in performance and improving battery life in the face of increasingly unpredictable circuits and environments.

Paper 16.1 from Intel and HaoKai describes an active on-die damping circuit to suppress resonance in the power distribution between the die and the power delivery network. Reducing peak-to-peak noise allows for increased operating frequency, robustness against hold time failures and improved chip lifetimes by reducing gate oxide stress.

The next two papers highlight on-die supply-noise sensors to provide valuable insight into supply-noise characteristics for diagnosis and for real-time operation. Paper 16.2 from Kobe U and Renesas employs two different types of sensors. Built-in probing circuits that measure power and ground voltages at 120 fine-grain locations across a device, as well as higher accuracy sampling monitor circuits measuring at a higher precision at 26 locations. Paper 16.3 from Fujitsu and A-R-Tec performs real-time monitoring by using histograms and counters to focus on the worst noise events while the chip is in normal operation.

Adaptive voltage supply and body-bias techniques are used to optimize power-performance trade-offs and lifetime effects. Paper 16.4 from Intel, Tyfone and Oregon State U selectively maximizes average performance or improves energy-efficiency by adapting frequency, supply voltage and body bias to react to changes in supply noise, temperature and transistor aging. Paper 16.5 from National Chung Cheng U highlights an ultra-low-power RISC core using aggressive voltage and body-bias scaling to run down to an astonishingly low 230mV, while significantly improving operating speeds. Paper 16.6 from Hitachi and Renesas describes an active resource manager controlling the core frequencies and data bandwidth while monitoring on-die thermal changes.

Paper 16.7 from IBM gives for the first time, cycle-by-cycle supply noise traces of split- and connected-core power supplies with various combinations of active and inactive cores. These results give designers insight into noise interaction between cores and enable power grid optimizations for the class of increasingly heterogeneous chips with multiple power domains.

Analog Techniques and PLLs

Chair: Vadim Gutnik, *Impinj, Newport Beach, CA*
Associate Chair: Stefan Heinen, *Infineon Technologies, Duisburg, Germany*

Phase-locked loops (PLLs) are ubiquitous and critical blocks in solid-state electronic systems. The stability of clock signals affects the performance and power (and, hence, battery-life) of microprocessors, data converters, radios and cell phones. The first six papers in this session present several PLLs and DLLs that incorporate techniques to overcome various limitations of highly scaled CMOS technologies when used for analog circuits.

The first two papers deal with fractional-N PLLs for wireless applications. Paper 17.1 From UC San Diego demonstrates a 730kHz bandwidth using a 12MHz reference clock, which enables SoC applications such as Bluetooth. The key for achieving the high bandwidth and associated 35µs settling time is an adaptive phase-noise cancellation technique. The next paper, 17.2 from Columbia U, describes a fully integrated 2.5GHz fractional-N PLL in a 90nm CMOS technology operating at 0.65V. The measured performance of this synthesizer complies with Bluetooth requirements.

Using a technique previously limited to data converters, the DLL in Paper 17.3, from Pohang U and Samsung, achieves a wide locking rang of 40 to 800MHz with a very small phase step error of less than 17ps and low jitter ($12ps_{pp}$ and $1.6ps_{rms}$).

In Paper 17.4 from PA Semi, a dual-supply ring-oscillator PLL in 65nm uses a novel ping-pong counter approach and multiple device types to achieve very low jitter (1.5ps) while using only 15mW of power. It has a 50% duty-cycle output and a short critical path, which are both essential for low-noise clock generation. The PLL in Paper 17.5 from Samsung achieves very low power and area via a simple solution; a replica of the oscillator control current is used in the loop filter to ensure that the bandwidth tracks with the update rate. Paper 17.6 from IBM shows off a 65nm partially-depleted SOI process with a fast clock generator that has sufficient tuning range to have excellent yield when fabricated.

The next two papers deal with high-speed comparators focusing on low power and low voltage. Paper 17.7 from U Twente describes a high-speed comparator with a large common-mode input range achieved by a folded latch structure. A benchmark for low-voltage and high-speed operation of CMOS comparators is given in Paper 17.8 from TU Vienna. The circuit presented in that paper achieves 600MHz operating speed with a 0.5V supply.

The last paper in the session, Paper 17.9 from Helsinki U and U Turku, shifts the scope to low-power sensor interfaces by demonstrating a 3-axis accelerometer in a 0.13µm CMOS technology.

SRAM

Chair: Kevin Zhang*, Intel, Hillsboro, OR*
Associate Chair: Hiroyuki Yamauchi, *Fukuoka Institute of Technology, Fukuoka, Japan*

The ever-growing demand on high-performance multimedia processors continues to drive the performance of embedded SRAM to meet the bandwidth requirement of multiple processing engines in a single die. Meanwhile, low-power consumption in SRAM has also become increasingly important for a wide range of applications in mobile and hand-held devices where extending the battery-life is essential. The low-power requirement can be even more stringent in emerging applications such as environmental and biomedical sensors where the operating voltage has to be scaled down into the subthreshold regime to meet the power constraints. On the technology front, Moore's law continues to drive the scaling of CMOS technology, which brings constant improvement in SRAM density and performance. But the shrinking transistor dimensions also make the memory cell vulnerable to device mismatch due to various sources, including both process variations and fundamental device physics. It is becoming more and more challenging to achieve reliable low-voltage operation and meet both read stability and write margin requirements.

The six papers in this session provide a broad perspective in addressing many challenges facing today's SRAM designers. These papers reveal the latest advancements in some of the key technical areas, including high-frequency scaling for high-end processors, balanced power-performance design for handheld applications, cell-stability enhancement, and SRAM design for ultra-low voltage operation.

Paper 18.1 from IBM, Toshiba and Sony describes the implementation of an L1 cache design for the CELL® Broadband Engine in a 65nm SOI technology. It adopts a large-signal ripple-domino sensing scheme to achieve up to 6GHz operation at 1.3V to meet the processor core requirement. The SRAM design employs a dual-power supply to achieve voltage scalability while maintaining cell stability.

Low leakage power during standby mode is critical to having long-battery life in mobile applications. The SRAM designs in this segment trade off performance for low-power. Paper 18.2 from Intel reports a 65nm SRAM design for this application. A co-optimization between transistor technology and advanced circuit techniques helps achieve 2pA/cell leakage at retention voltage and 1.1 GHz performance at nominal voltage.

Techniques for SRAM cell-stability enhancement have been reported before but many of them lose their benefits in manufacturing environments due to process, voltage, and temperature (PVT) variations. Paper 18.3 from Renesas and Matsushita introduces a design to improve the tracking of PVT variations. The benefits are demonstrated using 45nm SRAM cells with a cell size of $0.245\mu m^2$.

The remaining three papers from this session address the emerging applications of ultra-low-voltage operations. Three different SRAM cell topologies ranging from 6T to 10T are explored, reliably operating down to the subthreshold regime. A variety of design techniques in the peripheral circuits assist the ultra-low voltage operation while further reducing the SRAM leakage power. Paper 18.4 from MIT presents bitline leakage gating and built-in redundancy in data sensing. Paper 18.5 from U Minnesota presents data-independent bitline leakage and data-sensing enhancements. Paper 18.6 from U Michigan presents dynamic voltage scaling for read and write margin improvement. The silicon results of these three papers demonstrate the functionality of these designs well below 350mV.

Cellular and Multi-Mode Transceivers

Chair: Tony Montalvo, *Analog Devices, Raleigh, NC*
Associate Chair: Aarno Pärssinen, *Nokia, Helsinki, Finland*

After a slow ramp up, 3G cellular networks are beginning to be deployed in earnest. With data rates high enough to support painless mobile internet access, video phones, and other high-speed-data-enabled applications, the user experience is on the verge of a dramatic change. The increasing demand for wireless data places an unprecedented premium on spectral efficiency so that 3G standards include very stringent spectral emissions requirements. Further, as with any consumer application, low cost is essential. Meanwhile, 2G and 2.5G handsets sales continue to be robust with sales approaching 1 billion units per year and with growing markets in the third world cost pressures are unceasing. Still further, consumers demand continuous connectivity though sometimes incompatible networks, so the demand for multi-mode transceivers is growing. These challenges, and more, are addressed by the papers in this session.

Our first two papers address the problem of achieving high spectral purity *and* low cost. Since WCDMA phones need to simultaneously transmit high power signals and receive very low-power signals, it is necessary to suppress the transmitter's noise such that it is well below the receiver's noise in order to prevent desensitizing the receiver. To date, a typical WCDMA transmitter's SNR is between 145 and 150dBc/Hz in the receive channel at 190MHz offset. This level of noise dictates the inclusion of a SAW filter in the transmit path. Papers 19.1 by Analog Devices and 19.2 by ACP Zurich and ETHZ use completely different techniques to produce unprecedented spectral purity with SNRs of 163dBc/Hz in the case of Paper 19.1 and 156cdB/Hz in the case of 19.2. These transmitters enable the elimination of the TX SAW filters for further cost reduction and miniaturization.

Paper 19.3 from Nokia addresses the challenge of cost reduction by employing an architecture that is amenable to integration in digital CMOS. A direct-digital RF modulator is particularly challenging for WCDMA applications because of the very large power control range requirement.

Coexistence with 1st-generation analog cellular systems in the US makes CDMA2000 a particularly difficult 3G standard – especially with respect to receiver linearity and local oscillator phase noise. Paper 19.4 from Danube IC Engineering and Infineon is the first published highly integrated transceiver for this standard.

Paper 19.5 from Comlent, Orange Coast Semiconductor, and U Florida is the first paper describing a transceiver for TD-SCDMA – a Chinese cellular standard that is a TDD version of WCDMA.

The extremely difficult challenge of software-defined radio is addressed in Paper 19.6 by IMEC, Samsung, and U Lecce. The authors use external MEMS switches to enable band-select filters thus reducing the linearity and power dissipation requirements in the transceiver.

Cost reduction for GSM/EDGE handsets is a never-ending goal. Paper 19.7 from Hitachi and Renesas describes a polar-loop transmitter for EDGE with the power amplifier controller integrated. The transceiver includes integrated ADCs and DACs enabling a completely digital baseband processor IC.

The linearity required of a WCDMA transmitter results in relatively low power amplifier efficiency. Paper 19.8 from Sony describes an analog-domain pre-distortion technique that enables lower power amplifier backoff and thus better efficiency.

Our final paper, Paper 19.9 by U Michigan, describes a PLL-based modulator with a novel digital phase detector without the inverter-delay resolution limit of previously published efforts**.** This wideband modulator is well suited to multi-mode and low-power transmitters.

TD: Proximity Data and Power Transmission

Chair: Chris Van Hoof, *IMEC, Leuven, Belgium*
Associate Chair: Philippe Royannez, *Texas Instruments, Villeneuve Loubet, France*

To allow for increasingly complex system functionalities, electronic systems are also becoming more-and-more heterogeneous in their technology buildup. Specific technologies (e.g., logic, memory, analog, mixed-signal, RF, MEMS) need to be integrated in a very small footprint. 3D integration is a key technology to achieve this heterogeneous integration as well as dramatic size reduction.

A new class of 3D-integrated systems is emerging that relies on contactless coupling between dice in close proximity. Such an approach puts fewer constraints on the integration technology. This coupling can be achieved by inductive as well as by capacitive coupling. While continuous progress is being made, size of proximity interconnects and power consumption overhead still are critical factors.

This session presents significant advances in terms of size and power reduction of inductive and capacitive coupling (Papers 20.1, 20.2, 20.3 and 20.7). Capacitive coupling with an energy consumption of 0.08pJ/b and a throughput of more than 22Mb/s/μm^2 is demonstrated in an array of 104 8x8μm^2 electrodes, in Paper 20.1 from ARCES, STMicroelectronics and Fraunhofer IZM. Inductive coupling at 1Gb/s/channel with energy consumption of 0.14pJ/b is demonstrated in Paper 20.2 from Keio U and U Tokyo. Paper 20.3 from Keio U and Renesas presents how this technology can be applied effectively to achieve proximity probing of logic circuits at a distance of 1.2mm and a maximum data rate of 20Mb/s. Paper 20.7 from Sun Microsystems presents a capacitively-coupled I/O link with 144 channels that operates at 1.8Gb/s/channel.

Apart from data transmission, power can also be provided. Paper 20.4 from U Tokyo and Kobe U presents advances in a contactless power delivery sheet with 50% power transmission efficiency as an enabler for wireless sensor networks and ambient intelligence. A key advance is an organic level-shifter from 5V to 40V so digital LSI logic can drive the organic FETs.

The next two papers of the session concentrate on ultra-low-power communication in a Body-Area Network environment. In Paper 20.5, from National Chiao-Tung U, an ultra-low-power wireless sensor node consuming 21μW and a central processing node consuming 566.4μW is demonstrated in a 10 sensor node configuration and is based on Multi-Tone CDMA with front-end calibration. By designing a scalable body-coupled transceiver in 0.18μm CMOS, Paper 20.6, from KAIST, achieves communication at up to 10Mb/s over the shared body channel at a reception bit-energy of the transceiver of 0.19nJ/b.

Sensors and MEMs

Chair: Euisik Yoon, *University of Minnesota, Minneapolis, MN*
Associate Chair: Farrokh Ayazi, *Georgia Institute of Technology, Atlanta, GA*

A major challenge in integrated sensors and MEMS has been to enhance performance by integrating signal processing and conditioning circuitry with the sensor or MEMS in CMOS technology. The availability of submicron CMOS processes allows a significant amount of customized circuitry and DSP to be packaged with or embedded in sensors and MEMS. In addition, wireless links can be implemented for supplying power and transmitting data.

The eight papers in this session illustrate recent advances in microsensors and MEMS technologies that yield higher integration with CMOS circuitry for improved performance, smaller form factors, and lower cost implementations. Advanced micromachined devices are interfaced with CMOS electronics to achieve state-of-the-art performance and wireless data transfer. Novel CMOS-integrated circuit techniques are implemented for precision sensing of strain, angular velocity, magnetic field, mass change and single photons. The closed-loop control of MEMS resonators provides precision detection of changing mass and angular motion. A magnetic concentrator integrated on a CMOS chip paves the way to implementing a micro-compass on a chip.

The first paper of the session, 21.1 from Case Western Reserve U, presents a wireless sensing microsystem powered by an external RF power source for precision sensing of strain and temperature. The system can resolve sub-micro strain over a 10kHz bandwidth and simultaneously transmit strain and temperature data to an external receiver base. Paper 21.2 from Melexis describes a single-chip CMOS micro-compass with integrated DSP. The Hall-based microsensor uses a post-processed metal layer as a magnetic field concentrator to implement a three-axis magnetic field transducer. The micro-compass provides heading resolution of better than 0.5 degrees in a die area of $2.3\times2.8mm^2$. Paper 21.3 from CEA and Ecole Centrale presents a low-noise servo-controlled micro-fluxgate magnetometer with a programmable ASIC that makes the sensor adaptable for various applications.

Today, affordable MEMS gyroscopes do not have the resolution required for GPS-augmented navigation. Paper 21.4 from Georgia Tech describes a solution to this problem; a silicon-based tuning-fork gyroscope interfaced with a CMOS ASIC for dynamic tuning and control of the device achieves sub-deg/hr precision and accuracy. When combined with precision micro-accelerometers, these devices can assemble into micro inertial measurement units (micro-IMU) for short-range navigation in consumer products.

Paper 21.5 from Space Research Institute, Fraunhofer Institute, and European Research and Technology Centre presents a high dynamic range ΔΣ modulator interface for read-out of fluxgate sensors. The chip can resolve magnetic fields with a resolution of 10pT and shows radiation hardness for space applications. The authors of Paper 21.6 from U Pavia, STMicroelectronics, CNR-IMM, and U Lecce present another CMOS integrated micro-system for detecting the earth's magnetic field. An integrated micro-fluxgate sensor with a sputtered ferromagnetic core is interfaced with a CMOS ASIC to achieve 4° accuracy on measured angles while providing a digital output.

Paper 21.7 from TU Munich, Infineon Technologies, Siemens, and Qimonda presents an FBAR-based gravimetric sensing array for operation in liquids. The resonant FBAR array is flip-chip bonded to CMOS circuits to create high-frequency oscillator arrays with picogram mass sensitivity. Finally, Paper 21.8 from EPFL presents a CMOS single-photon avalanche diode (SPAD) detector array with high-speed readout functionality for molecular imaging applications.

Digital Circuit Innovations

Chair: David Blaauw, *University of Michigan*
Associate Chair: *G*eorgios Konstadinidis, *Sun Microsystems, Sunnyvale, CA*

Last year at ISSCC, a panel hotly debated the question “is the digital designer is dead?” Counter to some of the voiced opinions at this panel, this session demonstrates vibrant innovation in the area of digital circuits. These innovations address a number of challenges that have emerged in 65nm technology that are stressing existing circuit design practices. For instance, the analysis and control of process variation has come to the forefront of digital design. Device performance has become increasingly unpredictable due to process variations, sensitivity to temperature and supply voltage, and life-time wear-out mechanisms, such as oxide breakdown and negative-bias temperature instability (NBTI). To address this looming challenge, four papers in this session propose techniques that measure and adjust to variations. While these papers resist the consequences of variation, two other papers actually exploit variation to create random numbers for security applications.

In addition to the increase in variation, dynamic and static power consumption are concerns that must be addressed by today’s circuit designers. The slowdown of supply-voltage reduction in the nanometer era, combined with continuing scaling has resulted in tight power-constraints for digital circuit designs. A significant component of the total power consumption resides in global wires. Hence, the final two papers in this session present approaches for high-speed on-chip communication with substantially reduced power consumption.

In Paper 22.1, IBM introduces a delay-measurement sensor to monitor the critical path delays, which can be used to optimize the performance across voltage, process and in the face of life-time wearout. Results are reported for a commercial 65nm POWER6 processor. Paper 22.2 from IBM and Purdue U addresses the need for characterizing process variations in advanced processes. An integrated array of sense amplifiers allows efficient statistical characterization of random dopant fluctuations for different types of devices. A self-adjusting circuit that addresses variations and chip wear-out is presented in Paper 22.3 from NEC. The method employs in-situ delay monitoring latches for the critical paths and proactively reconfigures the circuit to avoid impending failures.

Papers 22.4 from U Michigan and Paper 22.5 from U Washington both present different methods for random number generation for security applications. The method in Paper 22.4 uses meta-stability to generate and grade the quality of a continuous stream of true random numbers. In Paper 22.5 introduces a new method that produces a random but fixed string of bits for chip ID applications.

Paper 22.6 from Korea U and Hynix addresses variation by introducing an output driver that uses on-die delay measurement to control slew rates and dynamically compensate for noise and process variations.

Paper 22.7 from Sun Microsystems discusses a state-of-the-art TLB design for the Niagra-2 processor, addressing the design challenges in 65nm process and in multi-core and multi-threaded processing.

The final two papers in the session, Paper 22.8 from Sun Microsystems and Paper 22.9 from U Twente, introduce a new method for high speed on-chip interconnects. Both methods use a capacitively-coupled driver which produces both pre-emphasis and small signal swings, leading to significant interconnect power reduction.

Broadband RF and Radar

Chair: *Tom Schiltz, Linear Technology, Colorado Springs, CO*
Associate Chair: *Kari Halonen, Technical University of Helsinki, Espoo, Finland*

RF and microwave integrated circuit development is rapidly expanding into the millimeter-wave frequency range. Once the domain of exotic III-V semiconductor technologies, standard CMOS and BiCMOS are now well-suited for these applications. Significant factors driving RFIC development at these high frequencies are the availability of wideband unlicensed spectrum at 60GHz and the impressive speed capability of modern CMOS devices. New consumer applications include automotive radar at 79GHz and ultra-wideband (UWB) communication in the 3-to-10GHz band. These new consumer applications all require low-cost solutions, and modern CMOS and BiCMOS technologies are prepared to serve these new markets.

The eight papers in this session highlight several significant advances in broadband RFIC development. Paper 23.1 from NXP Semiconductors describes a broadband, 2-to-8GHz UWB receiver front-end realized in 65nm CMOS. This front-end IC incorporates a transformer-feedback LNA and a passive down-converting mixer to deliver high dynamic range with only 51mW of power consumption. Paper 23.2 U Padova and Infineon also addresses UWB applications with a 3-to-5GHz LNA that includes an integrated notch filter to mitigate WLAN blockers. The LNA is implemented in 0.13µm CMOS and delivers 19dB of gain with 44dB of attenuation at the notch frequency.

Papers 23.3 and 23.4 present impressive wideband, inductor-less LNAs, each with 17dB of gain and sub-3dB noise figures. In Paper 23.3 by IMEC, DC-to-6GHz bandwidth with 2.8dB NF is achieved using a shunt-shunt feedback topology. This wideband LNA occupies an area of only 50x35µm^2. In Paper 23.4 by Linköping U, a differential LNA with current re-use has 7GHz of bandwidth and 2.4dB NF at 3GHz. Both of these LNA designs show significantly wider bandwidth than traditional source-degenerated designs, and occupy considerably less chip area since inductors are not required.

Following the break, the presentations include two papers that address radar and phased-array applications. Paper 23.5 from USC describes a 4-channel beam-forming receiver front-end for UWB applications in 0.13µm CMOS. The novel aspect of this beam-forming receiver is a path-sharing technique that reduces the die size. Paper 23.7 from Infineon and TU Vienna presents a 79GHz spread-spectrum transmitter for automotive radar applications implemented in BiCMOS. The RF output is BPSK-modulated at 1.235Gb/s and the output power is -1dBm.

Essential building blocks for millimeter-wave frequency synthesis are presented in Papers 23.6 and 23.8. Paper 23.6 from UCLA discusses frequency synthesis using the heterodyne phase locking technique. A series connection of mixers is used to generate various divide ratios with a lock range of 64 to 70GHz. The session concludes with Paper 23.8 by National Taiwan U, which presents a 75GHz PLL in 90nm CMOS. This PLL includes an integrated 75GHz VCO based on integrated transmission line resonators, with total power consumption of 88mW from a 1.45V supply.

Multi-Gb/s Transceivers

Chair: Robert Payne, *Texas Instruments, Dallas TX*
Associate Chair: Muneo Fukaishi, *NEC, Kawasaki, Japan*

Once isolated to optical communication systems, multi-Gb/s serial transceiver technology continues to be deployed in broader applications. The capability to create, consume, and process massive quantities of data in industrial and consumer applications likewise increases the bandwidth requirements for system-to-system, chip-to-chip, and even system-in-a-package (SiP) communications.

An optimized high-speed transceiver technology is required for each of these distinct applications. The tradeoffs between power consumption, data rate, port density, and signal integrity must be examined for each application. For example, in backplane communications, channel count may be limited but robust operation often must be guaranteed in legacy systems which were never intended to carry such high data-rate signals. In contrast, chip-to-chip communications often occur over shorter channels with relatively high signal integrity but a premium is placed on low power consumption.

In backplanes, both linear and decision-feedback varieties of analog equalization have been employed to address the poor signal integrity. Paper 24.1 from TI describes a digital approach to both equalization and clock recovery using a front-end A/D converter operating at 12.5Gs/s and backend digital signal processing. A BER<10^{-15} is achieved in a system with 24dB loss at the Nyquist frequency.

The next three papers describe different approaches to transceivers in 90nm CMOS technology. In Paper 24.2 from Sony and Mixed Signal Systems, 10GHz clocks are driven directly from an LC oscillator to the receiver to avoid the additional power and jitter contributions of clock buffers, resulting under 1ps of recovered clock jitter.

Low power is the focus of Paper 24.3 from Rambus, where a combination of techniques including circuit sharing, resonant clock distribution, and low-swing signaling achieves a power efficiency of 2.2mW/Gb/s in a 6.25Gb/s chip-to-chip transceiver.

The authors of Paper 24.4 from Fujitsu describe an equalizer adaptation technique for a 3.1/10.3Gb/s transceiver that minimizes convergence variations for highly periodic 8B/10B encoded data.

New approaches to >16Gb/s transmitters are presented in Papers 24.5 from National Taiwan U and 24.6 from IBM. The former presents an approach to channel characterization and transmit equalizer configuration using the data channel as part of a voltage-controlled oscillator. The latter presents a voltage-mode approach to a 16Gb/s transmitter that addresses equalization and process tuning and supports DC termination from 0V to V_{DD}.

In Paper 24.7 from UCLA and SST Communications, two techniques for 10Gb/s interconnect are presented for 3D chip integration for SiP applications. The measured performance of both impulse and RF techniques are compared.

Nyquist ADC Techniques

Chair: Dieter Draxelmayr, *Infineon Technologies, Villach, Austria*
Associate Chair: Venu Gopinathan, *Texas Instruments, Bangalore, India*

Many applications like video data conversion, fast communication services, and direct IF conversion require medium resolution A/D converters, sampling in the range of a few 100MHz. The pipelined-converter technique offers an attractive implementation possibility. Consequently, in this session there are 6 examples demonstrating the current state-of-the-art in this category. Advances are characterized mostly in getting highly power-optimized solutions. Most designs are implemented in state-of-the-art 90nm technologies. While this helps to get good performance it also poses the challenge of low power supplies.

Obviously, another direction of advancing the state-of-the-art is to go for extreme performance. In this session there will be two examples: A 50GS/s T/H amplifier, which can be used for direct conversion of a 40Gb/s signal from an optical link including even slight oversampling. This can be used to boost the performance of such a link in enabling advanced equalization techniques. The second example is a cryogenic ADC which can operate at the temperature of liquid helium, which is a major step forward in low-temperature readout electronics.

The nine presentations of this session are grouped as follows: the first 7 papers demonstrate the current capabilities in medium-resolution high-speed low-power applications. The last 2 papers demonstrate benchmark performance.

The converter in Paper 25.1 from Fujitsu demonstrates very low power consumption at a supply voltage of only 0.8V. The regulation of the gate overdrive voltage for optimizing the available voltage headroom is introduced as an enabling technique. The next paper, 25.2 from UCLA, attempts to perform the same precision of data conversion at twice the speed but using a sub-ranging architecture, operating at 1V. The converters proposed in Papers 25.3 from ETRI and 25.4 from ETRI and LG Electronics use 3b pipeline stages to achieve 10b precision at 30MS/s and 205MS/s sampling rate, respectively. The faster one needs a S/H in front of the converter.

The authors of Paper 25.5 from MIT present an 8b 200MS/s pipelined converter implemented in a just recently invented circuit technology which does not need active amplifiers. This promises another boost in power saving since opamps usually are the most power-hungry parts in an ADC. Papers 25.6 from Nordic Semiconductor and 25.7 from Realtek and UCLA improve the performance in using foreground and background calibration. Foreground calibration is used for a fast power-up, and after that, background calibration ensures adequate performance over time.

The authors of Paper 25.8 from Lucent present a 50GS/s T/H amplifier in SiGe technology. This benchmark in speed is achieved using a distributed topology, a technique well known in high-speed amplifiers, here applied to track-and-holds.

Finally, Paper 25.9 from IMEC and KU Leuven discusses a SAR ADC that can work from room temperature down to 4.2K. The specifics in this paper are that at 4.2K the transistors work differently than what we are used to. Therefore, specific circuit techniques had to be adopted to cope with this challenge.

Non-Volatile Memories

Chair: Hideto Hidaka, *Renesas Technology, Itami, Japan*
Associate Chair: Yair Sofer, *Saifun Semiconductors, Netanya, Israel*

A wide range of applications is emerging to take advantage of diverse non-volatile memory technologies. From stringent automotive applications demanding reliability in high temperatures to ultra-low-power computing in handheld consumer devices, the forefront of non-volatile memory is advancing in density, speed and a variety of features. RFID-tag applications require ultra-low-power non-volatile memory and a very small form factor. To meet the expanding needs of application requirements, this sessions presents advancements in phase-change RAM (PRAM), magnetic MRAM, NOR type flash memories and an electron-beam-written ROM.

Paper 26.1 from Samsung starts the session with a breakthrough, reporting the first published 512Mb PRAM using a diode-switch storage cell in 90nm technology and featuring 266MB/s read and throughput.

Paper 26.2 from Hitachi and Renesas describes a different implementation of PRAM for embedded applications. Using with a 100µA write-current cell structure, this ultra-low-power design operates with a 1.5V supply, and opens a new era for easy-to-use logic-compatible applications.

In the NOR flash memory arena, Paper 26.3 from STM introduces the first gigabit-level integration in 65nm technology with 2 bits per cell. This first implementation of a DDR interface for NOR flash provides 400MB/s read throughput. Innovative solutions in the programming algorithm and circuitry produce the fastest reported 2.25MB/s programming throughput, making the device well-suited for portable code and data applications.

NOR flash technology also comes into the stringent automotive applications at the 0.13µm technology node. Paper 26.4 from Infineon presents a high-bandwidth embedded NOR flash module intended for upgradeable code storage in a -40C to 150C automotive environment. A fast random access time of 23.5ns, including ECC overhead, provides 2GB/s read throughput.

Paper 26.5 from Hitachi and Tohoku U presents a new type of MRAM technology using the spin-torque switching mechanism and sees the first megabit-level integration. This spin-tranfer torque MRAM (SPRAM) addresses the scaling problem of the high-intesity magnetic-field needed for writing in previous MRAM cells. With a reduced switching current of 200µA, this 2Mb device represents a significant improvement in MRAM design.

The final paper from Hitachi and Renesas reports a very small 0.05 x 0.05 mm^2 chip intended for RFID-tag applications. The chip features a scalable electron-beam-written ROM for ID storage. By realizing an order-of-magnitude reduction in the chip area, this work promises to increase the convenience of electronic tagging.

DRAM and eRAM

Chair: Martin Brox, *Qimonda, Neubiberg, Germany*
Associate Chair: Kazuhiko Kajigaya, *Elpida Memory, Sagamihara, Japan*

Demand growth for electronic systems has been driven by new consumer and computing applications. The most popular examples are the next-generation, high-resolution game-consoles. These systems heavily leverage the performance of today's memories and processors. Yet, these applications are still unable to create a life-like experience due to the limitations of the on- and off-chip memory bandwidth available to the processing functions. Careful optimization of the memory hierarchy bandwidth is necessary to improve system performance. High-speed embedded-DRAM (eDRAM) has evolved as a serious contender to embedded-SRAM (eSRAM), while external data-rates continue their rapid rise. However, speed improvements cannot stand on their own as system costs must be kept reasonable. To this end, good test and repair solutions reduce cost and facilitate higher levels of integration. The presentations in this session report recent advances that address these challenges.

Paper 27.1 by IBM introduces an innovative sense-amplifier for use in an eDRAM macro operating at a random-cycle frequency of 500MHz. This macro, which occupies only 32% of an equivalent eSRAM-macro in the same technology, enables higher-density cache implementations improving system level performance.

Cost, test strategy and system integration are the focus of the next two presentations. Paper 27.2 by Renesas and Shikino explores strategies needed for known-good-die (KGD) applications with the example of an eSRAM-macro. KGD is a pre-tested die that guarantees the full-spec operation, which is indispensable for cost-effective multi-chip package (MCP) applications. MCPs are implemented in almost all new cell phones and will be widely implemented in the consumer applications soon. Paper 27.3 by Renesas describes a DDR2-memory-interface for consumer applications. This interface uses an I/O loop-back measurement technique which is fully integrated into the DDR2-clocking system.

Continuing from last year's ISSCC, graphics devices continue to increase external bandwidth. Paper 27.4 by Samsung establishes the new benchmark by demonstrating a data-rate of 4Gb/s/pin with the recently finalized GDDR4 standard. Implementation details of the high-speed single-ended interface are presented. Paper 27.5 by Micron presents a second GDDR4 device that conquers the battle of deterministic clock-domain management necessary to achieve a data-rate of 2.5Gb/s/pin in a double-data-rate interface. This device implements GDDR3 and GDDR4 operating modes on the same chip, providing flexibility for the consumer market. The last paper of the session by KAIST and Samsung demonstrates a jitter-resistant DLL architecture capable of 1GHz clock-frequency required for a 2Gb/s/pin data-rate and details a solution to reduce DLL jitter in a noisy, on-chip memory environment.

Image Sensors

Chair: Johannes Solhusvik, *Micron Technology, Oslo, Norway*
Associate Chair: Hirofumi Sumi, *Sony Corporation, Tokyo, Japan*

CMOS image sensors are now the undisputed technology of choice for most consumer imaging applications including camcorders and digital still cameras (DSCs). CMOS image sensors offer lower cost, lower size and lower power than CCDs without compromising on performance.

The constant drive for improved image quality and target extraction leads to continued innovation in multiple-resolution image sensors in both the spatial and temporal domains for both infrared and fluorescence imaging. Innovations are presented in the area of on-chip processing, both inside and outside the pixel array.

The push for lower cost motivates both innovations in pixel design to reduce die size and advanced optics to compensate for non-uniformities and color shading artifacts. These artifacts are associated with small-pixel image sensors and optics with wide angles of incidence.

Paper 28.1 from ARC Seibersdorf Research describes the first line sensor to combine an asynchronous, data-driven pixel circuit with on-chip sub-microsecond time-stamping and a synchronous bus-arbiter. The asynchronous operation reduces the data output rate by orders of magnitude.

The authors of Paper 28.2 from U Minnesota, Pixelplus, and KAIST describe an image sensor capable of automatically detecting fast moving objects in the scene. The region-of-interest associated with the object can then be read out at up to 960 frames per second. This rate is much higher than the rest of the image, which is typically read out at 30 frames per second.

In certain imaging applications, such as infrared imaging and fluorescence imaging, the challenge is to extract the scene contrast in the presence of a very large background signal level. Paper 28.3 from Stanford presents an excellent technique for subtracting the background signal in such situations.

Image sensors designed for high-speed readout often use one ADC per column, with the ADCs operating in parallel to achieve the desired frame rate. Paper 28.4 from TU Delft and DALSA describes a CMOS image sensor that uses a column-parallel ADC with a new multiple-ramp single-slope architecture. It achieves a 3.3× reduction in ADC conversion time compared to classical single-slope ADCs with only a 24% increase in power consumption.

Paper 28.5 from Micron Technology presents the first 8.1Mpixel CMOS image sensor product that features 1.75×1.75μm^2 pixels intended for consumer applications such as DSCs and cell phones using the 1/2.5 inch optical format. This format typically uses 3Mpixel and 5Mpixel sensors today. The sensor yields 63.8dB dynamic range and an impressively low noise floor of 3.8e^-_{rms}.

Paper 28.6 from Canon describes a 1/2.7 inch high-definition (HD) CMOS image sensor. This sensor uses low-noise readout circuitry and optimized pixel design to achieve an impressive 3.7e^-_{rms} noise floor and 12.2e^-/s dark current at 60°C.

The authors of Paper 28.7 from Grass Valley and Thomson Silicon Components conclude the session by presenting a 2/3 inch HD CMOS image sensor. It offers a wide selection of readout modes, such as progressive/interlaced, from 1080p/i and 540p/i down to 270p/i, and additionally has readout modes with high dynamic range based on multiple-exposure techniques yielding up to 122dB DR in 1080p.

Analog and Power Management Techniques

Chair: Doug Smith, *SMSC, Phoenix, AZ*
Associate Chair: JoAnn Close, *Analog Devices, San Jose, CA*

Power management appears as a central theme among the nine papers in this session, which reflect a wide range of applications. Advances in the two amplifier designs reflect a combination of linear and switching techniques. Power efficiency and minimizing the use, size and cost of external components continue to be of paramount importance in switching converters.

Switching DC-DC converters, a staple of electronic systems for decades, were first constructed with discrete transistors and recently as standalone ICs. Now we see that that these key high-efficiency circuits are being embedded in larger SoCs to manage the multiple supply voltages and accuracy requirements of modern ICs. One of the main impediments to integrating these converters has always been the inductor required. Inductors are often bulky and expensive, and one external inductor is typically required for each output voltage. This challenge is being met with both an increase in switching speed while maintaining acceptable efficiency, and the generation of multiple outputs using just a single inductor.

Polar modulation schemes have significant potential for power savings in wireless transmitters, but place very stringent demands on the supply regulation systems. Paper 29.1 from KAIST and MagnaChip Semiconductor shows that the combination of linear and switching techniques that once was reserved for amplifiers in the audio range can be applied to deliver the control bandwidth required for EDGE modulation while keeping the efficiency high. In this design, the performance of the output stage of the linear amplifier, which modulates the PA supply, remains important as it must correct for the ripple of the switching amplifier.

Paper 29.2 from Georgia Tech and Paper 29.3 from U Brescia present advances in LDO and charge pump designs that highlight the fact that the control of power continues to be an important and active area in analog IC design.

Paper 29.4 from KU Leuven continues the theme in that a combination of linear and switching techniques is used to produce an ADSL central office line driver with low power dissipation. This paper advance previous work by increasing the sophistication of the feedback loop around the switching stage while maintaining the previously reported high supply voltage using low-voltage CMOS devices.

Paper 29.5 from U Pavia and austriamicrosystems, and Paper 29.9 from KAIST, KEC, and JDA Technology demonstrate various advances in control schemes in addition to the use of a single inductor. Paper 29.6 from Stanford and National Semiconductor describes a buck converter optimized to improve efficiency for light loads. The authors of Paper 29.7 from U Pisa describe a converter whose output changes in such a way that it makes the performance of the sub-threshold MOS circuits it drives less sensitive to process variations and temperature.

Paper 29.8 from U British Columbia realizes an embedded 3GHz DC-DC converter with fully integrated inductor, delivering higher overall system efficiency by combining the converter and the system clock tree, and recycling clock charge and delivering it to the load instead of ground.

Building Blocks for High-Speed Transceivers

Chair: Michael M. Green, *University of California, Irvine, CA*
Associate Chair: Thomas Burger, *ETH Zurich, Zurich, Switzerland*

Not long ago, the feasibility of realizing multi-Gb/s transceivers in standard CMOS seemed questionable. However, the rapid decrease in CMOS feature sizes and major advances in analog high-speed design techniques in recent years have made such high-speed performance a reality. Currently, bit rates of 10Gb/s and higher are commonplace even in standard CMOS processes. This session highlights papers exploiting both of these improvements. Two of the papers show extraordinary circuit speeds (70GHz and higher) using a 65nm SOI CMOS process. Five of the papers show very high-speed performance blocks using mature ($\geq$ 0.13µm) CMOS or BiCMOS technologies. Finally, two other papers show how high-performance analog circuit design can allow further integration of systems on a chip.

Two papers demonstrate how a 65nm SOI CMOS process can achieve very high-speed analog circuit blocks. The design presented in Paper 30.3 from MIT and IBM breaks a speed record for a CMOS clock divider that operates up to 100GHz input frequency. Paper 30.2 from IBM and Yale describes an LC-VCO that oscillates at a center frequency near 70GHz with a tuning range of over 6GHz. Both papers demonstrate the feasibility of volume production over process variations.

The next three papers demonstrate that innovation in circuit design can still yield considerable performance improvements. Papers 30.1 and 30.6 demonstrate amplifiers using standard CMOS that operate near 40GHz: in Paper 30.1 from National Taiwan U, cascaded gain stages in a 0.18µm CMOS are used to maximize the gain-bandwidth product; in Paper 30.6 from U Waterloo, loss compensation using active negative resistance in a 0.13µm CMOS process allows flattening of the frequency response. Paper 30.4 from National Taiwan U cleverly uses series- and shunt-peaking inductors to achieve a wide-range 40GHz clock divider and low-phase-noise VCO using a 0.18µm CMOS process.

Two papers describe the use of circuit design techniques in BiCMOS to greatly enhance performance of broadband ICs. In Paper 30.8 from TU Denmark, Intel, and IPtronics, an active-load circuit replaces the conventional 50Ω back-termination resistor, allowing nearly 50% decrease in the power dissipation of a laser driver. In Paper 30.9 from TU Vienna, the exponential characteristic of a BJT is used to achieve 112dB dynamic range in a TIA for an optical receiver while maintaining 240MHz bandwidth.

Paper 30.5 from Intel and ASU demonstrates a new on-chip phase-noise measurement technique that achieves -75dBc sensitivity at a 100kHz offset frequency for carrier frequencies up to 2GHz. Paper 30.7 from TU Munich, Stanford, and Infineon shows that effective ESD protection can co-exist with high-speed I/Os: 2kV protection is achieved on an input pad in a 90nm CMOS process while still exhibiting a bandwidth of over 10GHz.

WLAN/Bluetooth

Chair: George Chien, *Marvell Semiconductor, Santa Clara, CA*
Associate Chair: Mototsugu Hamada, *Toshiba, Kawasaki, Japan*

The proliferation of wireless communication devices in recent years has driven their adoption into consumer electronics. The wide range of applications in the consumer markets demands lowest power (handheld devices), highest data rate (video distribution), highest level of integration (small form factor), and lowest cost (low component count). These requirements have been applied to the popular WLAN and Bluetooth devices in the previous years. In this session, a collection of current state-of-the-art devices that attempt to address each one of these requirements will be presented. These include an enhanced-data-rate (EDR) Bluetooth SoC that achieves Receiver/Transmitter (RX/TX) power of 38/48mW for low power, a multi-band MIMO transceiver IC that achieves >270Mb/s PHY rate for high throughput, an 802.11a/b/g SoC in 0.13µm CMOS, and an 802.11g SoC with integrated power amplifier implemented in 0.18µm CMOS for low cost.

In the area of low power consumption, Paper 31.1 from Broadcom describes a single-chip Bluetooth EDR device implemented in a 0.13µm CMOS technology. This transceiver integrates includes all the Bluetooth system building blocks, plus CPU, RAM/ROM and host interfaces. For low-voltage operation, an integrated low drop-out (LDO) voltage regulator is also included. This device achieves a low RX sensitivity of -84dBm for 3Mb/s while consuming only 38/48mW (in RX/TX mode) of power from a 1.5V supply.

In the high data rate area, the authors of Paper 31.2 from Broadcom and IQ Analog present a fully integrated multi-band MIMO transceiver for Draft-802.11n implemented in 0.18µm CMOS technology. This 2x2 MIMO transceiver integrates 2 complete transceivers on the same die with a single common LO. The paper addresses some of the key performance parameters for MIMO operation, such as I/Q imbalance, LO phase noise, and 40MHz operation. The measured phase noise at 100kHz offset is -108dBm/Hz while achieving the TX EVM of better than -40dB at -2dBm of output power. The paper concludes with a real-life demonstration of data throughput at the host interface level that reaches up to 200Mb/s while running at 270Mb/s PHY data rate.

For high integration, the authors of Paper 31.3 from Infineon and U Erlangen-Nuremburg describe an 802.11a/b/g SoC implemented in a 0.13µm CMOS technology. The RX achieves a sensitivity of -77/-74dBm for 2.4/5GHz bands and the TX outputs -2dBm with EVM better than -30dB. The die area for the RF transceiver is 6.7mm^2.

In the area of low component count/cost, the authors of Paper 31.4 from Atheros Communication and Stanford extend the integration level of an 802.11g SoC to include an RF front-end complete with a power amplifier (PA), low-noise amplifier (LNA), and a TX/RX switch all in a 0.18µm CMOS technology. This allows the possibility of connecting this SoC device directly to the antenna port to create a low-cost solution. The paper describes the circuit configuration that allows the sharing of RF ports between LNA and PA. The PA achieves +20dBm at 6Mb/s rate and an overall RX NF of 5.8dB.

TD: Trends in Wireless Systems

Chair: Donhee Ham, *Harvard University, Cambridge, MA*
Associate Chair: Siva Narendra, *Tyfone, Portland, OR*

Amid a plethora of wireless systems and applications that have become indispensable in our daily lives, there still continues to emerge burgeoning efforts to develop new wireless applications and systems.

Eight presentations comprising this session are designed to share some of these exciting applications and systems. Three papers discuss RF oscillators built with hybrid approaches that combine standard silicon integrated circuits with bulk acoustic wave resonators on the top or side of the IC, or with an optical system (modelocked laser). These hybrid approaches improve short- and long-term frequency stability beyond what silicon-only approaches can achieve. The other five papers are concerned with new integrated circuit or architecture designs in emerging wireless markets, including software defined radios, passive millimeter and submillimeter wave imaging, RF identification tags, and cognitive radios.

The authors of Paper 32.1, from IMEC and KU Leuven, report a Software Defined Radio that constantly estimates the required quality of service and opportunistically modulates its power usage to attain low energy operation. A Software Defined Radio approach combined with adaptive energy scaling enables both low-cost and low-energy.

In Paper 32.2, from Luxtera, OEwaves and Forza Silicon, the optoelectronic oscillator concept is realized by integrating, for the first time, the electronics in a CMOS integrated circuit, which leads to excellent phase noise performance. To attain the same goal of lowering phase noise, the authors of Papers 32.5 at U Washington and 32.7 at STMicroelectronics and IEMN/ISEN combine a bulk-acoustic-wave resonator with a standard silicon integrated circuit. The former also advances the state of the art by presenting the first such hybrid circuit with a quadrature topology.

Paper 32.3 from Northrop Grumman reviews passive millimeter wave and submillimeter wave imaging applications and reports amplifiers in the frequency range from 100GHz to 300GHz. These amplifiers are built with state-of-the-art InP high electron mobility transistors (HEMTs). The amplifiers may be used in the front end of the passive imaging cameras.

In Papers 32.4 and 32.8, UHF RFID tags are reported. In 32.4, from the Semiconductor Energy Laboratory and TDK, the RFID is implemented on a flexible substrate, with an effort to maximize the computation capability by including a central processing unit. The flexible substrate has the potential to enable ubiquitous application of such devices. The RFID tag reported in Paper 32.8 from TI conforms to the EPC Gen 2 standard and introduces an anti-collision architecture necessary for deployment of this technology.

Paper 32.6, from National Taiwan U, reports the first discrete wavelet multi-tone-based cognitive radio baseband receiver. This achieves 153.6 Mb/s data rate while consuming 165mW from a 1.8V supply.

NOTES

ISSCC 2007

Press-Release Material

- **Conditions of Publication**
- **Press Copy**

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This and other related topics will be discussed at length at ISSCC 2007, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 11-15, 2007, at the San Francisco Marriott Hotel.

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PRESS COPY

ADVANCES IN CMOS FOR OPTICAL APPLICATIONS

Communication using light signals and optical fiber holds great promise to lower costs for all data transport over both short and long distances. The huge bandwidth and favorable physical characteristics of optical fiber beg to be exploited : In telecom networks, transmitting high-data-rate signals over long distances becomes practical; In computer systems, high-capacity interconnect, free from electromagnetic interference and awkward bulky copper cables, is enabled by parallel optics. But, of course, practical details limit cost-effective commercial solutions.

At ISSCC 2007, in February, several advances in the practical art of sending and receiving of optical signals will be presented. Inevitably, such advances will lead to exciting new const-effective telecom services, and to higher-performance computer systems.

A CMOS SOI solution will be presented by Luxtera, Carlsbad, CA (in **Paper 2.1**). It dramatically reduces the cost of optical interconnects by monolithically integrating both photonic and electronic components, in a standard SOI CMOS process, for 4-channel 10Gb/s DWDM applications. Existing optical transmitters and receivers are expensive modules built from separate optical and electronic components. In a standard process used for ordinary manufacture of microprocessors, this technology integrates all of the pieces needed to transmit and receive optical signals. Since everything is on one piece of silicon, there is no mechanical assembly needed (in assembly of modules), and this leads to lower cost. But combining optical and electrical components creates new design challenges. Last year, at ISSCC 2006, an optical modulator and a WDM multiplexor/demultiplexor were introduced by the same authors. This year, the integration of a new optical interleaver allows the 4-channel optoelectronic devices to be combined on one die.

While the basic idea of fractional-N PLLs is simple, the key to a successful implementation of a frequency synthesizer is in managing jitter and spurious performance. At ISSCC 2007, a low-cost clocking chip for the SONET OC-192 standard will be described by Silicon Labs, Austin, TX (in **Paper 2.9**). This new circuit allows the use of low-cost low-frequency quartz crystals, rather than expensive VCXOs.

On another front, the impact of 90nm CMOS can be seen in further increases of data rate, and power reduction for some traditional circuits, including CDR circuits, and transimpedance and limiting amplifiers. At ISSCC 2007, research from National Taiwan University will present a burst-mode CDR circuit and a transimpedance amplifier that reach up to 40Gb/s. And so the Information Age progresses, with data moving ever-faster and faster, at ever-decreasing cost!

This and other related topics will be discussed at length at ISSCC 2007, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 11-15, 2007, at the San Francisco Marriott Hotel.

PRESS COPY

FREE BUT FRUGAL

With the price of energy continuously going up, it is now time to find new solutions for exploiting the energy that is available (still!) for free in our environment. This energy can then be used to operate ultra-low-power and miniaturized electronics devices, for example RFID tags, or sensors on the body for health monitoring. Energy can be scavenged, for example, from the thermal energy emanating from the human body, or from the ubiquitous electro-magnetic energy always available in our urban environments. Since such sources can provide only very little power, they need highly-energy-efficient circuits to convert this energy into a voltage that is sufficiently high to power an end-use circuit. This energy can also be accumulated on a microbattery for deferred (burst) use at a later time. In order to create highly-miniaturized systems, the microbattery can be fabricated on top of the IC, saving space and reducing wiring.

At ISSCC 2007, in San Francisco, CEA-LETI (France) (in **Paper 3.1**) will report on the development of all components required to build such a microsystem. These components include a micro-thermogenerator exploiting the Seebeck Effect, and delivering a 1V outputfor a 60ºC temperature difference. This generator drives a DC-to-DC converter delivering a maximum voltage of 4.3V and consuming 70µW when operating from a 1V supply. A Lithium microbattery is fabricated on top of the IC, and is monitored by a charge/discharge circuit consuming only 5nW. If the battery voltage is checked for one second every hour, the microbattery charge can last for about one year for the envisaged low-duty-cycle applications.

Energy should not only be efficiently harvested, but also wisely spent. This is particularly true when powering electronic digital devices from a battery. It is well-known that digital circuits integrated in leaky ultra-deep-submicron technologies (such as 65nm CMOS), show an optimum supply voltage that minimizes the total energy consumed for a given workload, and operating temperature. This optimum operating voltage actually balances the switching and leakage energy spent in the circuit. Since the workload changes with time, the optimum operating voltage must be tracked in real-time in order to achieve a maximum energy efficiency.

As will be reported at ISSCC 2007, researchers at the Massachusetts Institute of Technology (in **Paper 3.2**) have developed the first minimum-energy tracking system for digital circuits. This includes on-chip energy-sensor circuits that are used in a closed-loop system to track the minimum-energy operating voltage in real-time, depending on the workload and the temperature. The key building block includes a DC-to-DC converter delivering voltages down to 250mV from a 1.2V supply, with a power efficiency better than 80% for a typical load of 1µW.

The two new developments to be reported at ISSCC 2007, providing novel circuits and techniques, for energy capture and management, open the door to true energy-scavenging, and optimum energy management for all kinds of ultra-low-power applications, such distributed wireless-sensor networks, RFID tags, wireless body-borne health monitoring, and ambient intelligence.

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WHAT MOORE CAN BE EXPECTED AFTER CMOS?

While Moore's Law continues, as predicted, to the integration of over one billion CMOS transistors onto a single integrated circuit, manufacturing realities will soon make it necessary to look for technologies beyond CMOS, if this phenomenal integration pace is to continue. Expected new device structures will allow CMOS transistors to scale toward 10-nanometer effective channel-lengths, while operating much as they do today, but, ultimately, we will reach the point where we can count the number of atoms in a channel. At that point, we will no longer be able to scale those structures any further using lithography and in associated manufacturing processes. Even before that physical limit is reached, however, power-density limits might preclude us from increasing the number of devices integrated in a small area, simply due to the increased energy that would be expended per unit area, with these super-small ultra-fast transistors. Apparently, for future progress, the decree is clear: we must learn to create circuits from atomic-size particles, and components that can reliably perform circuit operations at acceptable power-density levels.

Fortunately, this CMOS limit is not news to many researchers, and much work has been ongoing to discover a replacement for the CMOS transistor. Optimistically, this task is perhaps no more daunting than what we faced merely a few decades ago, when the Internet was non-existent, and simple electronic functions, such as machine-based addition and multiplication, required an entire room of electronic components. At that time, only our greatest visionaries were able to see the future possibilities that integrating CMOS transistors would bring. But, soon, at ISSCC 2007, we all will be able to take a peek at the future when we listen to researchers describing their work with Carbon-Nanotube Transistors (CNTs), the most promising of all potential post-CMOS technologies.

Researchers from IBM (in **Paper 3.4**) will present the world's first ring-oscillator circuit that is comprised solely of single-strand CNTs with nanometer-scale cross-sections. The design, manufacture, and measurement, of this historic first circuit will be described in detail by a recognized authority on CNTs. It should be noted, however, that much work remains to be done before such circuits can realistically replace CMOS. CNTs are not printed like CMOS transistors, but, rather, are rather grown, or transferred onto silicon substrates. One fundamental limitation with this process is controlling the CNTs' location and behavior. Further, while a grown or transferred nanotube might behave like a transistor, some fraction of the CNTs will have, instead, the characteristics of a metal wire; Unfortunately, determination of the CNT's conduction state is subject to the whim of mother nature!

To explore circuit configurations that can utilize the powerful benefits of nanotubes while tolerating their uncertainty, researchers from Stanford University (in **Paper 3.5**) postulate how groups of nanotubes might be used to form logic gates that can accommodate either of their conduction states. Unlike traditional logic circuits, these CNT-based logic gates can be constructed to include built-in fault-tolerance. This first-of-a-kind speculative logic-gate design facilitates a direct comparison with logic implemented in scaled CMOS, and allows us to consider what the future might bring. Together, these two presentations at ISSCC 2007, form a first step toward what might be much Moore to come!

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POWDER-IN-AIR REALIZES A FLEXABLE E-PAPER

How about a vivid and informative electronic commodity-tag in a supermarket? How about posters on a wall displaying motion, or an ultra-thin and light-weight portable electronic book? Clearly, we need a very-low-power physically-flexible low-cost display to enable these applications.

Tiny colored-particles confined in air between two thin plastic plates, moved by an electric field, realize this kind of display. The technology is called “Quick-Response Liquid-Powder Display” (QR-LPD). Since the particles move so smoothly, the technique is called “liquid-powder” although the particles are moving in air. Once data is written, the display does not need power to maintain the image. Thus, the technology provides an ultra-low-power paper-like display. The QR-LPD does not need transistors within each pixel, in contrast to the existing active-matrix e-paper technology, therefore reducing the manufacturing cost of the display.

This year, at ISSCC 2007, researchers from Kyushu University and Bridgestone Corporation (in **Paper 3.7**) will discuss their new low-power high-voltage physically-flexible driver circuits designed for the QR-LPD display. The novel circuit effectively reduces power consumption and chip area. One of the supply voltages is as high as 70V, but the use of high-voltage transistors and a new circuit design, accommodate the high voltage without reliability problems. The flexible driver chip is 2.3mm × 21.4mm in size with 160 output pins. Since it is milled as thin as 35μm, the silicon chip, which is attached to the display, can be bent sufficiently to achieve the physical flexibility of the rest of the display.

Come to hear more about flexible circuits for flexible electronic paper of the future!

This and other related topics will be discussed at length at ISSCC 2007, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 11-15, 2007, at the San Francisco Marriott Hotel.

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ADVANCED RADIO-FREQUENCY BUILDING BLOCKS ENABLE COMPACT LOW-COST FEATURE-RICH PHONES

Today's cellphone user insists on data-intensive features such as wireless e-mail, Web browsing, and even television reception, in a tiny portable device. This, in turn, demands efficient highly-integrated low-cost radio-frequency circuits, manufactured using inexpensive CMOS integrated-circuit processes.

High-efficiency-radio power-amplifiers are critical to the success of the next generation of high-bandwidth radio systems. Power-amplifier (PA) efficiency is the primary determinant of mobile handset talk-time. Modern digital-modulation formats also require linear power amplifiers in order to meet stringent regulations on spectral use. However, linear power amplifiers are difficult to operate above 20% efficiency!

But, this year, at ISSCC 2007 in San Francisco, three presentations (in Session 4) by researches from Stanford, Università di Catania and ST Microelectronics, and Arizona State University will demonstrate improved efficiency for power amplifiers in low-cost CMOS.

This same push toward higher data-rates, and seamless mobility from one system to another, also raises the bar for receiver performance. New circuit-tuning and digital-self-calibration techniques will also be presented at ISSCC 2007. These innovations from Broadcom, promise unprecedented radio-receiver performance in CMOS, thereby allowing simplified designs with fewer components and improved manufacturability. The development of highly-integrated multi-band multi-standard 3G and future-generation portable handsets, with long battery life and top performance, depends on such innovations. Even more critically, at the moment, they are being commercialized very rapidly.

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INCREASED INTEGRATION AND FREQUENCY DRIVE MICROPROCESSOR PERFORMANCE

Microprocessor designers continue their drive for higher performance, either by integrating more execution units on a chip or operating at higher frequencies. At ISSCC 2007, the microprocessor session will highlight the accelerating trend toward multi-core integration on a single chip, with most processors featuring at least four cores, a marked increase from last year. This advance in integration is enabled by the progression to 65nm technology, and an ever-increasing number of metal interconnect layers, with two papers describing the use of 11 interconnect layers. Power continues to be a critical concern, especially as the level of integration increases. All papers describe special active power- and leakage-reduction techniques, and two papers describe independent frequency control of individual cores. Even as the industry shifts toward multi-core power-constrained designs, frequency improvements are still possible, with a new record being reported this year for microprocessor operating frequency.

In this session, an aggressive dual-core processor is introduced, which operates at frequencies up to 5GHz, and contains about 700 million transistors. Two other papers also highlight the high level of integration achieved in modern processors, with a network-on-chip architecture containing 80 tiles operating at 4GHz, and an 8-core System-on-Chip capable of running 64 simultaneous program threads. Two multi-core processor chips support dynamic frequency control of each individual core, a novel feature providing increased flexibility for average-power reduction. Power-reduction techniques are also emphasized in the other multi-core processors presented in this session, including PMOS power gates that minimize leakage in a 4MB cache.

It is clear from the innovation and diversity present in these technical disclosures that progress in both computing capability and efficiency will continue for the foreseeable future. The processors to be described provide substantial improvements both in peak performance and in parallelism, both of which make for much-faster computation.

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UWB COMES OF AGE

Over the last couple of years, a century-old paradigm for implementing radios underwent a fundamental transformation, from narrowband systems to a broadband approach that has led to over a ten-fold improvement in the communication data rate. The emergence of this technology, broadly termed Ultra-Wideband (UWB), has enabled short-range links capable of supporting applications such as wireless video. With the demonstration of highly-integrated silicon integrated circuits, suitable for mass manufacture, such systems will see a prolific growth in the near future. The high bandwidth of these systems also enables other exciting applications, such as RADAR for automotive applications, and communication for wireless sensor-network monitoring systems.

Wireless sensors are generating significant market interest. Sensor networks can be used in a large range of applications such as monitoring environmental conditions, and for security. These applications do not need very-high data rates, but have a requirement of extremely low power, in order to maximize battery lifetime. UWB systems can also be effectively used for such applications, as UWB allows for very low power consumption for a given data rate.

This year, at ISSCC 2007, presentations by Philips, NXP Semiconductors, and Institute of Microelectronics, will address all of the issues introduced above. Complete RF transceivers for MB-OFDM type UWB (in **Paper 6.1**), and pulse-based high-data-rate UWB (in **Paper 6.2**) are capable of supporting data rates of hundreds of Megabits per second. Ultra-low-energy requirements in the 10^{-12} to 10^{-9} Joules/bit range are also demonstrated in CMOS IC transmitter and receiver implementations (in **Paper 6.4**) by researchers from MIT at ISSCC 2007.

Overall, the work presented here is expected to impact a broad range of applications. Clearly UWB techniques, allowing very-low-power wireless data transmission at data rates, from low to very high, are potentially set to change our world: Transfers of gigabits of data, without wires, in home and office settings, is expected to become commonplace over the next few years. High-bandwidth transceivers, such as those to be presented at ISSCC 2007, will be used in various consumer-electronics applications, such as digital cameras and HDTV. On the other hand, low-power implementations, will allow for large-scale deployment of wireless sensor networks for environmental and security applications.

Watch as Wild Wideband Wireless Wends its Way to everyone's Wish list!

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MULTI-GHZ CLOCKING BREAKTHROUGHS WITH ALL-DIGITAL PLLS

The relentless pursuit of performance continues to drive clock-frequency requirements into the multi-GHz range. This greatly challenges designers, as the need for speed is in direct conflict with the need to keep power and thermal dissipation within system bounds. In response, designers are inventing increasingly-innovative techniques for delivery of high-performance clocks at low power levels. As process technologies shrink and voltages scale, full digital solutions to "super-speed" clock generation which are tolerant to process variations are gaining traction over analog techniques.

At ISSCC 2007 in February in San Francisco, several papers will present details and technical disclosures on these exciting new developments. A PLL with wide voltage and frequency range will be presented which dissipates merely 8mW/GHz at 1.2V whilst delivering up to 8GHz clock frequency. At 0.5V, this same design dissipates merely 1.6mW/GHz! Clocking networks which harness inductively-coupled resonant networks, will also be presented. These enable very-high-frequency clock generation and distribution at very low power, whilst also providing low jitter, by virtue of the in-phase property of a standing-wave. In response to the need to reduce power dissipation, numerous solutions employ robust fully-static digital logic techniques in their implementation. Furthermore, such techniques enable these designs to scale rapidly and easily into future technology generations, improving time-to-market and providing a competitive edge.

This and other related topics will be discussed at length at ISSCC 2007, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 11-15, 2007, at the San Francisco Marriott Hotel.

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WIRELESS COMMUNICATIONS HEADS TOWARD GIGABIT DATA RATES

The 7GHz of unlicensed bandwidth, centered around 60GHz, holds the promise of wireless communications at several giga-bits per second, in the near future, making the design of 60GHz transceivers a red-hot research topic. In particular, the adoption of standard cheap CMOS processes is viewed as the most-attractive way for commercialization of high-data-rate radios. Short-range networks for downloading multi-media (video) to mobile devices, Gb/s wireless LANs for untethered connection to the network, and high-data-rate point-to-point inter-building communication, are just a few application examples.

Several exciting advances in the art of millimeter-wave radio design will be presented at the forthcoming IEEE International Solid-State Circuits Conference (ISSCC) in February, 2007.

Researchers from UCLA and SiBeam/UC Berkeley (in **Papers 10.1, 10.2**) will describe 60GHz receivers featuring the highest levels of integration to date. Implemented in 90nm and 130nm standard CMOS processes, these circuits work close to the frequency limit set by the technology, and yet consume less than one-tenth of a Watt! Researchers from the National University of Taiwan, (in **Paper 10.3**), demonstrate successful communication at 4Gb per second while consuming 100mW DC power (in a 130nm CMOS process), by adapting traditional mm-wave circuits to monolithic integration in silicon.

The circuit techniques to be proposed at ISSCC 2007 constitute substantial progress toward commercialization of fully-integrated low-cost radios, operating in the 60GHz band at Gbit/s data rates. Commercialization of these innovations awaits standardization of modulation formats, and protocols for mm-wave wireless systems. Nevertheless, these first technology demonstrations may lead to commercial products within the next 5 years.

This and other related topics will be discussed at length at ISSCC 2007, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 11-15, 2007, at the San Francisco Marriott Hotel.

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INTEGRATED TV TUNERS AND RFID READERS

Television has been entertaining us for decades. We might wonder what can still be new in this area. And yet, the evolution is far from over. In fact, we are in the early stages of a worldwide transition in television broadcasting, from analog to digital. In a few places in the world, analog broadcasts have already been switched off; However, most of the world will still require support for legacy analog broadcasts. During the transition period, wherever it occurs, it is necessary to support both legacy analog TV and new digital TV standards. Today, almost all TV sets and over-the-air set-top converter boxes still use surprisingly-low-integration tuner modules, consisting of hundreds of discrete components and requiring manual tuning for frequency alignment.

At ISSCC 2007, in San Francisco, presentations from Chrontel, UC San Deigo, and Microtune, will describe highly integrated TV tuners which meet both the technical and commercial challenges of the digital-TV transition around the world. The systems to be presented come as either SoCs (in **Papers 11.1, 11.3**) or SiPs (in **Paper 11.2**), with significant cost improvement. The new TV-tuner chips will cover all existing standards used throughout the world, including digital broadcast and cable, all in a single integrated circuit.

The use of near-field radio-frequency identification (RFID) systems, based on inductive coupling, is gaining momentum in a wide variety of applications, such as supply-chain management, anti-fraud systems, and object-tracking systems. The small, low-cost RFID tags contain information on the product, replacing the traditional bar code. But, as well as, an extension, they can be equipped with sensors to provide information on the environment, such sensors, when very small, can be thought of as 'smart dust'. Since an RFID tag does not have its own power source, it relies on power being transmitted from the RFID reader. The main challenge in the design of RFID readers is to receive weak signals while transmitting a 20 to 30dBm CW signal to power the passive tag. At ISSCC 2007, three highly-integrated UHF RFID readers that solve this problem, will be presented by Intel, Catena Wireless Electronics, Samsung, Kwangwoon University, UC Irvine and Broadcom. In particular, they can receive weak signals in the presence of a large CW blocker, without requiring highly-selective off-chip filters. Of additional significance is that, UHF RFID systems operating at 900MHz have extended range and higher data rates compared with traditional lower-frequency RFIDs that operate at 125kHz or 13.56MHz. The complete UHF RFID reader transceiver can be integrated onto a single BiCMOS (in **Paper 11.5**) or CMOS (in **Paper 11.6**) IC, to enable significant cost reduction and integration-level improvement within the RFID reader.

The consequences of these developments are potentially revolutionary: Incorporating these high-data-rate RFID readers in portable devices, such as cellphones, will connect RFID tags to wide-area networks, potentially enabling *Personal-Area Awareness,* including personal-property tracking (of car keys, laptop computers, children, wallets, pets, etc) and automatic bill-paying at restaurants. In short, low-cost UHF RFID readers are poised to solve a large number of the world's petty problems!

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LOW-POWER HIGH-SPEED LINKS A REALITY AT LAST

At present, the density of high-speed inter-system and intra-system links is limited by several factors: First, inductor-based high-speed CDRs consume significant die area and power in order to realize their performance. Second, to resolve similar power and area concerns, systems have not been able to take advantage of decision-feedback equalization to provide inter-symbol-interference cancellation without crosstalk enhancement.

But, in a nearly-inconceivable turn-of-events, technological breakthroughs, which smash down both of these barriers, will be presented this year at ISSCC 2007. Researchers at IBM (in **Paper 12.3**) have been able to remove the need for area-hogging inductors, while simultaneously increasing the operating speed of CMOS CDRs by 60 percent (to 40Gb/s) using less than 100mW. At the same time, researchers working jointly at MIT and IBM (in **Paper 12.5**) have destroyed the belief that DFEs are area- and power-hungry, with the introduction of a tiny DFE that consumes less than 1.4mW per Gb/s.

This and other related topics will be discussed at length at ISSCC 2007, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 11-15, 2007, at the San Francisco Marriott Hotel.

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DATA CONVERTERS LEAP-FROG TO 90NM CMOS AND BELOW

Analog circuit designers have traditionally considered 0.18μm CMOS to be the 'sweet spot' for the implementation of analog-to-digital conversion circuitry. This process node offers transistors with good analog performance; The 1.8V supply allowed both ADC techniques developed over the past two decades to be used, while at the same time the MOSFETs are fast enough both for high-speed analog circuits and efficient digital processing. Until now, the industry has largely resisted the move to finer geometry CMOS technologies for data conversion.

This year, papers at ISSCC 2007 bear witness to a sea-change in design philosophy. More than half of the papers on analog-to-digital converters will describe devices implemented in 90nm CMOS or below. Startlingly, industry has leap-frogged from 0.18μm CMOS to 90nm CMOS! Based on these developments we believe that 90nm will be the new standard process for analog-to-digital converter design. New techniques are demonstrated that allow the converter to run off the low power supply voltage in these processes. The energy efficiency of analog-to-digital converters continues to improve defying skeptics.

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MUTLI-MODE CONTINUOS-TIME CONVERTERS ENABLE MULTI-MODE CELLULAR HANDSETS

Cellular phones, now, must operate with several communication standards, ranging from narrowband 2G cellular to wideband 4G cellular and WiMax. Although multi-mode analog-to-digital converters have covered the traditional 2G and 2.5G cellular standards, separate converter circuits were required for broadband communication over WLAN or 4G standards. New converters announced at ISSCC 2007 meet both the requirements of narrow band and broad band communication. These reconfigurable converters operate at optimum efficiency in several modes of operation.

The new converters work well in nanometer digital CMOS processes. Continuous-time techniques allow these devices to work well in large system ICs that contain tens of millions of gates of digital logic. A key advantage of the continuous-time technique is that it is relatively insensitive to the switching noise of digital logic on the same IC. Continuous-time converters, incorporate filtering, simplifying system design. This year, at ISSCC 2007, a tutorial features the continuous-time technique.

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NEW CHIP ENABLES LOW-COST CELL PHONES

Low-cost cellular telephony has the potential to dramatically improve quality-of-life in today's emerging economies. Despite rapid annual subscriber growth in developing countries, less than 10% of the people in India and sub-Saharan Africa have their own mobile phone. Handset cost remains a significant barrier to wider adoption. A single-chip cell-phone solution could enable basic voice connectivity for pennies. Over the past several years, steady progress has been made toward achieving this goal, by integrating more and more functions onto a low-cost IC.

At ISSCC 2007, in San Francisco, developers from Infineon (in **Paper 14.6**) will present the next evolutionary step toward a single-chip GSM phone, by showcasing a system-on-chip which includes audio, radio frequency (RF), digital, memory, and power-management circuits, all on the same die. The embedded power-management circuits support a 5.5V supply input so that the chip can be powered directly from low-cost nickel-metal hydride (NiMH) and nickel-cadmium (NiCd) batteries, as well as from the lithium-ion cells typically used in today's cell phones.

In addition to delivering power to the circuits on the chip, power-management circuits supply power for external components connected to the chip, such as the loudspeaker, display backlight, and the subscriber-identity module (SIM). Careful placement of the circuit blocks on the chip, and optimization of the chip package, allow integration of the power circuits without degrading the performance of sensitive analog and RF blocks. This innovative system-on-chip requires only an external Flash memory, a power amplifier, and peripherals, to create a fully-functional basic GSM phone. The ultra-low-cost mobile phones enabled by this and future single-chip solutions, will continue to drive worldwide subscriber growth, and the integration of the global economy over the next five years.

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"N"-ABLING THE FUTURE OF WLAN

It turns out that your parents were wrong! In fact, everyone speaking at the same time can be a good thing! In fact, the upcoming WLAN 802.11n standard advocates sending multiple data streams simultaneously via several antennas, as a means of doubling, or even quadrupling the speed of future wireless networks. The resulting Multiple-Input/Multiple-Output (MIMO)-based technology, coupled with the widespread penetration of WLAN (nearly 90% of all notebooks now ship with built-in WLAN capabilities!), will enable new applications for wireless networking, such as high-definition audio/visual-content streaming. MIMO-based WLAN technology will enable ubiquitous connectivity in both existing and emerging markets, where the wired infrastructure doesn't currently exist. This will foster the creation of a truly-global network, allowing the rapid development of knowledge-based economies across the world.

At ISSCC 2007, in San Francisco, researchers from Atheros Communications (in **Paper 14.7**) will feature a pioneering effort in the next era of wireless networking. They will report on the first fully-integrated 3x3 MIMO-baseband processor that utilizes multiple data streams and advanced signal-processing techniques to deliver, in the next two years, unprecedented throughput (300Mb/s) and range, for 802.11 WLAN systems. Their work is a harbinger of the coming era of computing, one will which further advance the dream of global connectivity.

This and other related topics will be discussed at length at ISSCC 2007, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 11-15, 2007, at the San Francisco Marriott Hotel.

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TRUE REALITY IN GAMES AND GUI !

Although 3D-graphics hardware for various multimedia devices has developed tremendously in recent years, true-reality is not being provided to users, due to insufficient computing power, and the lack of depth-perception available with 2D displays. The technologies of 3D-display, a probable target for next-generation display, realizes stereoscopy, and makes a viewer feel realistic 3D effects. However, now, only preprocessed static picture and video data have been visualized in existing 3D displays, because complex image-processing is required to synthesize output images from two different view-images (the left- and right-eye view-images) and a disparity-map.

At ISSCC 2007, in San Francisco, researches from KAIST (in **Paper 15.4**), will present an SXGA (1280x1024) 3D-display processor with a programmable 3D-graphics-rendering engine which can synthesize output images at an interactive rate, namely 36 frames/s. The synergetic coupling of a 3D-display processor and a rendering engine enables users to experience true-reality in real-time interactive 3D applications such as games and GUI.

And so, we see the future — in 3D!

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LOW POWER OR HIGH PERFORMANCE?

In today's electronic world, products ranging from high-performance servers down to low-power personal health-care monitors, illustrate the extreme range of power-constrained devices that must be designed for ultimate performance within the available power budget. Getting the most performance out of a design involves optimizing the power-distribution and management methods. Two independent technologies are needed – one to measure accurately the chip behavior and one to control frequency, voltage, etc. on the chip, using this information. Traditionally, chips are designed with fixed voltage and frequency settings, but given the explosion in variability in today's nanoscale circuits, fixed operating points with large process variations imply large design margins and lost performance capacity. This year, at ISSCC 2007 in San Francisco, designers will show how to take advantage of adaptive systems to reduce design margins and use them to provide either higher performance or lower power dissipation.

For the coming years, this kind of adaptive control approach will be essential for maintaining the expected growth in performance and battery life in the face of the appearance of increasingly unpredictable circuits and environments. As illustrated in three papers [16.1, 16.4, 16.6] adaptive techniques can control all parameters of a chip to maximize performance. Other papers apply similar techniques to reduce power dissipation.

In the past, power was secondary to performance importance, but that is no longer the case. Now, it is clear that dynamically optimizing power consumption is the key to achieving both lower power and higher performance, simultaneously.

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THE CLOCKS GO FORWARD

Timing circuits are a key part of personal electronic products ranging from personal computers, to cell phones, to PDAs to next-generation DVD players. More precise clocks give you improved computer performance, better cell-phone reception, and cooler electronic toys. Papers to be presented at this years ISSCC will show jumps in clocking performance in all of these directions, and much much more…

Although microprocessor manufacturers are putting multiple cores in a single processor chip, there is still a push for higher clock rates. Today's processors are running at a lowly 4 GHz clock speed, but microprocessors in the future will run at 6 times that speed! A paper in Session 17 at ISSCC 2007 will demonstrate a 24 GHz clock generator in a manufacturing process available today. Imagine never waiting for your computer again: with these advances, that day is closer than you think!

The magic of cellular phones is that so many can talk at the same time, in the same place. This is possible because each phone operates at a very precise frequency. Then, the equipment at the cell-phone tower can distinguish one from the next, just like the human ear can distinguish an oboe from a flute in an orchestra. But, imperfections in the circuits that make up the frequency (yes, the clock circuits!) turn this music into "noise", an orchestra out of tune. Calls get dropped; voice quality gets worse, and cell-phone batteries run out faster. Presentations at ISSCC 2007 will show timing generators with 10 times less off-key power!

Come to the Conference and be amazed!

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CELLULAR TRANSCEIVERS AND THE INTERNET

Remember life before the Internet? No email, no Google, no YouTube. There's little doubt that the Internet has changed our lives. Unfortunately, today, we generally only have Internet access while sitting at a desk. But, new developments to be presented at ISSCC 2007, in February 2007, will help make painless mobile Internet-access a reality.

Today's mobile Internet access relies on very-slow 2G and 2.5G cellular networks. It works for checking stock quotes, sports scores, and text messaging, but not much more. But, 3G networks are coming, and the mobile Internet experience will soon resemble the Internet you enjoy at home. But high-speed data capability, alone, won't solve the problem. Multimedia applications require space, and consume power: Thus, smaller and lower-power 3G radios must not only provide the raw data, but create space for the sexy new multimedia features.

But, with the capabilities of 3G handsets comes increasing complexity; 3G handsets have been, to-date, bulkier and more expensive than their 2G and 2.5G predecessors. At ISSCC 2007, in San Francisco, three presentations from Analog Devices (in Paper 19.1), ETH Zurich (in **Paper 19.2**), and Nokia (in **Paper 19.3**) will all describe cost- and size-reduction breakthroughs in the especially-difficult transmit path of these handsets.

So why do we care about all of this? Size does matter! Adding features is only appealing in a sleek package. If you can't carry it, it's not really mobile!

Stuck in traffic on Super-Bowl Sunday? No problem! Watch the game on your phone. But you would be wise to pull over, first!

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GOING 3D WITH WIRELESS INTER-CHIP COMUNCICATIONS

3D stacking of IC chips has been a research topic for 20 years. But only recently, has the interest in this topic become widespread, with researchers world-wide starting to look thoroughly into the practical aspects of this technology. This trend is largely fostered by the requirements of portable electronic devices that must become smaller and lighter, while, at the same time, consume less power. Increasingly, 3D integration of chips appears to be the obvious method to reach such goals. Various architectures for chip integration are contesting: Should one use galvanic, capacitive, or inductive, interconnects? Their technical features can be compared in terms of:

- Data rate
- Area
- Integration effort

Here the latter two items refer to the necessary technology changes to the existing CMOS platforms, In this context, such changes must be kept to a minimum.

This year at ISSCC 2007, there will be almost an entire session (Session 20) devoted to wireless-communication architectures for 3D integration. Data rates, area penalties, and integration effort, required for capacitively- and inductively-coupled inter-chip communication, will be described.

A presentation by ARCES- University of Bologna, ST Microelectronics, Fraunhofer IZM (in **Paper 20.1**) will show a capacitively-coupled device with a high data rate of 22Mb/s/μm^2, in an area of 8x8 μm^2 with an energy consumption of 0.08pJ/b. Researchers from Keio University, and University of Tokyo (in **Paper 20.2**) will present an inductively-coupled device that allows larger separation between the chips, and provides data transmission consuming 0.14pJ/b, while providing a data rate of 1Gb/s.

Cleary, these results show that wireless 3D integration is a new “big thing” on our pathway to “More than Moore” technologies, one which will provide new applications in the small-form-factor high-performance domain.

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DIGITAL CIRCUIT INNOVATION

Last year, at ISSCC 2006, a panel hotly debated the question “Is the Digital Designer Dead?”. Contrary to some of the opinions voiced at this event, this year, ISSCC 2007 again demonstrates vibrant innovation in the digital-circuits arena. These innovations address a number of key challenges that have emerged as the IC industry moved to smaller-feature-size integration, with 65nm technology. The first such issue is the increased uncertainty in the performance characteristics of the transistors in manufactured chips. Hence, several new methods proposed in the Conference, address the challenge of producing reliable designs using such unpredictable transistors. Aspects of this uncertainty are addressed using on-chip monitoring structures that characterize the shift in the transistor performance on individual chips. In addition, a number of “adaptive silicon” approaches are proposed, where failing transistors are dynamically swapped for new ones, are “tuned-up” during the operation of the chip. This exciting new direction in digital design allows for more robust designs that continue to work, even when the underlying individual transistors are becoming less predictable and more prone to failure.

In addition to the increase in variation, dynamic and static power consumption is an ever-more-dominant concern that must be addressed by today’s circuit designers. In the nanometer-process-technology era, supply-voltage reduction has come to a halt. This has resulted in the threat of significant power increase as designers continue to pack more transistors onto a die. Interestingly, significant component of the total power consumption resides in the wires that are used for communication within a chip. Hence, several of the proposals this year at ISSCC, present novel approaches for reducing this power consumption with a reported power reduction of ten times, compared to conventional approaches! And so, the digital designer soldiers on producing ever-more-effective, higher-density faster ICs for ever-cost-reducing products.

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LOW-COST RADARS AIMED AT TRANSPORTATION AND SECURITY

Up to now, radar has been restricted to military and law-enforcement applications, because of the costs involved in producing devices and systems that work at extremely-high frequencies. However, automotive radars operating at 77 to 79GHz, have demonstrated improved safety and reliability in passenger-car operation. Collision-detection and collision-avoidance radars, pre-emptive brake boosting, low-visibility driving aids, self-parking, and autonomous cruise-control radars are already available in high-end cars. Silicon IC technology can enable widespread adoption of this technology to all types of vehicles, by dramatically lowering costs.

The breakthrough required for opening up these markets is, as was also the case in previous consumer applications, the replacement of expensive modules based on discrete components, in expensive technologies, by cheap integrated solutions in silicon. At ISSCC 2007, (in **Papers 23.7** and **23.8**) from Infineon, Vienna University of Technology and National Taiwan University, respectfully, will describe solutions that enable integration of all components required for an automotive radar in one single silicon chip that can be mass-manufactured at very-low cost. Commercial products are expected to appear on the market within the next 1 to 2 years.

Another, less-known application for radar is imaging. Besides the well-know videos made with normal (optical) cameras, phased-array radar-imaging system, using microwave frequencies, enable vision in the dark or under foggy conditions. Home surveillance, airport security, night vision, and medical imaging (replacing X-rays), are just a few potential applications for this technology. At ISSCC2007, (in **Paper 23.5**) researchers from University of Southern California will present a new technique that may enable the integration of these systems into a significantly smaller silicon IC, thereby bringing us closer to commercialization of low-cost radar-imaging technology within this decade.

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Breaking Bandwidth Barriers

The generation and consumption of massive amounts of data has become commonplace in today's industrial and consumer environments. As the availability of broadband wired and wireless networks grows and access costs decrease, data communications bottlenecks emerge within and between chips and systems. At ISSCC 2007 in San Francisco, the presentations to be made at the Multi-Gb/s Transceivers session will describe approaches to overcoming these barriers.

Texas Instruments (in **Paper 24.1**) will present an outreach of their analog and digital signal-processing (DSP) expertise to address the limited bandwidth capacity within systems, such as in Ethernet routers. This is the first-reported application of DSP to system backplanes; It has the potential to reduce the cost of scaling-up bandwidth, by enabling continued use of legacy chassis backplanes.

Rambus (in **Paper 24.3**) will describe a new ultra-low-power chip-to-chip transceiver that will bridge the bandwidth gap between chips within a system. This compact and low-power solution promotes widespread and low-cost adoption of extremely-high-data-rate local communications.

Finally, IBM (in **Paper 24.6**) will report on a new technique for reducing the power, area, and complexity, of the transmitters that are required in all high-data-rate communications systems. This robust design promotes easier interoperability of systems, a strategy which pushes high-speed transceivers further into the mainstream, and reduces complexity.

And so, the bottlenecks in intra- and inter-chip, and intra- and inter-system sub-level communications are gradually cleared. But, of course, only temporarily, in preparation for the next challenge as another floodgate of processor performance is opened once again!

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SCALABLE PHASE-CHANGE MEMORY ADVANCES RAPIDLY IN DENSITY AND PERFORMANCE

Various non-volatile memories have been proposed in the past, with phase-change memory (PRAM) being one. Currently, it is well on the way to becoming a viable option, as more process issues are resolved. Earlier, such issues made PRAM difficult to scale. The amount of memory each SoC is increasing with technology scaling, and, hence, various higher-density memory solutions are required. As well, high-density memory solutions are becoming more predominant in the market due to silicon cost. As a consequence, this year at ISSCC 2007, in San Francisco, researchers from Samsung will present the first very-high-density Phase change RAM (PRAM).

This PRAM represents a significant advancement over previously-reported memories of this (PRAM) kind. While PRAM has been highlighted as one of the promising candidate technologies for overcoming performance and scalability limits of currently-dominating Flash memories, scalability had not been really demonstrated until now. The Samsung PRAM uses a Diode-Switch type of cell, allowing cell-size reduction without loss of current-driving capability, and disturbance-free operation. The design incorporates several circuit innovations which result in 266MB/s read throughput with even-faster write throughput.

Details of these developments will be revealed at ISSCC 2007, at the San Francisco Marriot Hotel, in February.

This and other related topics will be discussed at length at ISSCC 2007, the foremost global forum for new developments in the integrated-circuit industry. ISSCC, the International Solid-State Circuits Conference, will be held on February 11-15, 2007, at the San Francisco Marriott Hotel.

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AGGRESSIVE NOR FLASH SATISFIES MOBILE MARKETS

Flash is increasingly important in the electronics industry as consumer-market demand increases for more “smarts” in all products. Due to the increasing demand, a lot of companies in the industry are forced to evaluate Flash as a key driver for some of their high-performance mobile applications. At ISSCC 2007, researchers from ST Microelectronics (in **Paper 26.3**) will address this trend and present a 1.8V 1Gb NOR Flash for high-performance mobile applications.

Designed in an advanced 65nm technology, and using a 2bit/cell architecture, the chip measures only 52mm^2. A fast read path, large internal parallelism, and a 16b DDR I/O interface, allow the memory to acheive a 400MB/s read throughput. The introduction of a double write buffer and pipelined synchronous programming circuitry produces the fastest-reported programming throughput for a NOR Flash (2.25MB/s). The high-density and fast read and write throughput (400MB/s read) of this 1Gb NOR Flash memory meets the most demanding requirements of mobile applications, for code and data storage.

Details of these developments will be revealed at ISSCC 2007 at the San Francisco Marriot Hotel, in February.

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BREAKTHROUGH IN EMBEDDED DRAM

At ISSCC 2007, in San Francisco, IBM will present (in **Paper 27.1**) the first-published embedded trench DRAM using a (1T1 cell) SOI technology.

Silicon-on-Insulator (SOI) technology has been under development for over 20 years. In this exploration, there have been many variations and combinations investigated of memory and SOI technology, all trying to achieve high performance and low power. At ISSCC 2007, IBM will report on achieving a 2ns random cycle and impressive 1.5ns latency.

Novel circuit-design techniques, such as a micro-sense amplifier, help achieve the outstanding performance that the industry has been struggling to achieve over the years. The 3-transistor micro-sense amplifier allows the design to utilize a short-bit-line architecture without the area overhead associated with conventional cross-coupled sense amplifiers. Overall, this design provides a new direction for satisfying the growing cache requirements of multi-core processor designs, and associated performance improvements in high-performance microprocessors.

Details of the implementation of this new scheme will be revealed at ISSCC 2007 at the San Francisco Marriott Hotel, in February, 2007.

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ADSL GOES GREEN

Most Internet users outside the United States receive their service over their existing telephone lines via an ADSL modem which is based on a widely known technology standard. Each of these modems ultimately connects to the service provider's central office which contains racks of ADSL drivers, each dissipating large amounts of power due to the need to supply high voltage signals as necessitated by the stringent ADSL requirement. In fact, in some cases, the long-term cost of the air conditioning to cool the equipment can exceed the cost of the equipment itself!

At the International Solid-State Circuits Conference (ISSCC) in February, 2007, reduction of power consumption in integrated-ground-based systems will be a "hot topic", so to speak. In particular, the power hungry terminals at the other end of your Internet connection have received attention from researchers in Belgium. At ISSCC 2007 in February, Paper 29.4 entitled "A 237mW ADSL2+ Central-Office Line Driver in Standard 1.2V 0.13µm CMOS" describes a radically different power-amplifier structure which delivers precise signals to the line while minimizing wasted current. These new design techniques have been used to allow full driver integration, which, potentially, could reduce the cost of your modem while increasing system efficiency, reducing hardware cost and dramatically lowering the power consumed, while you surf the Net!

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100GHZ CMOS CLOCK DIVIDER

Yet another speed barrier has been broken by state-of-the-art CMOS technology. As the highest-frequency digital component in a system, a clock divider is a circuit that simply gives an output that is exactly half the frequency of its input. However, though its function can be simply described, its design cannot! The intricacies of the operation of such a circuit, operating at very-high frequencies, are far from straightforward. Indeed, it is often the clock divider that limits the speed of on-chip broadband transceivers. At ISSCC 2007, chip designers from MIT and IBM [30.3] will present a clock-divider, using a 65nm Silicon-on-Insulator (SOI) CMOS technology, that operates nominally at 90GHz, but in fact has been measured to operate at frequencies as high as 100GHz!

Think of it! Imagine anything happening 100 billion times in one second! This circuit, designed using standard current-mode logic (CML) techniques, dissipates only 52.4mW. Moreover, the designers will also demonstrate the robustness of their design by characterizing the performance of the chip for variations of many parameters.

An SOI process combines the low-power and high-integration capabilities of standard CMOS gates with a highly-insulated substrate that exhibits vanishingly-low parasitic device-capacitances, allowing much higher maximum speeds at lower power levels.

Most-importantly, the design techniques exhibited in this benchmark chip are of even greater impact on future design. In particular, they will make possible the design of next-generation broadband Systems-on-a-Chip at lower cost than for current systems that require niche technologies that do not lend themselves to high levels of integration, and are, corresponding, much more expensive.

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200MB/S WIRELESS CONNECTION

With the penetration of the high-speed Internet-access, the data rate required for wireless communication is increasing. Moreover, a data rate of 20 to 30Mb/s is required for real-time transmission of HD-TV. However, the data rate in wireless communication is limited by the frequency bandwidth of its channel. This year, at ISSCC 2007, in San Francisco, we will see a breakthrough, in the form of a transceiver that utilizes multi-input multi-output (MIMO) technology to alleviate the data-rate problem. MIMO utilizes a single channel with multiple streams, arranged so that the data rate per channel is increased by a factor of n. The MIMO transceiver to be described, achieves up to 200Mb/s throughput, enabling a multiple real-time wireless transmission of HD-TV streams. This has been impossible with a legacy 802.11a or 11g device. But now, you can watch an HD-football game in your bedroom, while your family enjoys an HD-movie in the living room.

At ISSCC 2007, at the San Francisco Marriott, in February, researchers from Broadcom and IQ Analog (in **Paper 31.2**), will present a fully-integrated multi-band MIMO transceiver for Draft-802.11n, implemented in 0.18µm CMOS technology. This transceiver integrates 2 receivers, 2 transmitters and a single common local-oscillator. This work to be reported, addresses some key issues in MIMO operation, such as I/Q imbalance, LO phase noise, and a problem, which is called "channel-bonding." The transceiver achieves -108dBc/Hz phase noise at 100kHz offset, with TX EVM of better than -40dB at -2dBm output power. The presentation will conclude with a real-life demonstration of data throughput at the host-interface level that reaches up to 200Mb/s, while running at 270Mb/s PHY rate.

Following the current integration path of 802.11abg and Bluetooth, a robust MIMO-system implementation will soon be available in an SoC form factor, while consuming the same or less power than the current generation of WLAN/Bluetooth solutions. These new MIMO-powered devices will enable the market to explore applications that are not physically possible on handheld devices, today.

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WIRELESS ACCESS: ANY-WHERE, ANY-TIME, USING ANY SYSTEM

Wireless-access nowadays is a necessity. People feel they must be equipped with various services, such as cellular telephones, WiFi, WiMax, etc, in order to be connected, anywhere, anytime. But, further problems occur when traveling, because of different communication modes such as GSM, CDMA, etc, and different-frequency bands, of operation in different countries.

A single universal device that can be used for all wireless accesses, using various modes and various frequencies in various countries, would be the ultimate approach, if it were battery-energy-efficient. Fortunately, a solution is at hand: Newly-emerging SDRs (Software-Defined Radios) are wireless-communication devices that can be instantaneously-tuned via software to any requirement when the mode/frequency must be changed. Also, for SDRs, energy utilization can be very efficient for different modes, bands, and applications, since power can be optimized flexibly.

But a consolidation of legacy services provided by various systems, is a challenging problem. But, new approach to the integration of software-hardware co-design for energy-efficient reconfigurations is on the horizon:

At ISSCC 2007, in San Francisco, researchers from IMEC and KU Leuven will present (in **Paper 32.1**) energy-scalable architectures and circuits for Software-Defined Radios. Both a reconfigurable RF frontend and, a heterogeneous-multi-processor SoC for the baseband platform are proposed. A performance-energy manager exploits energy scalability to compensate for the dynamics of application requirements and propagation environments to realize low-power operation. As well, they describe a transmitter that offers energy-scalability, ultimately providing a 40% improvement in average system-level energy efficiency.

And so, more obstacles are removed in the path to the Software-Defined-Radio era.

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THE REAL "TOTAL-RECALL" TECHNOLOGY

At ISSCC in February, researchers in millimeter-wave technology at Northrop-Grumman Space Technology (in **Paper 32.3**) will describe advances that many people will recognize as closely resembling the scanner technology profiled in the movie "Total Recall". In the movie, passengers are screened electronically, through their clothing, for weapons and other contraband. High-frequency electronics operating at very-low power levels, allows small-size cameras to peer through inert material to provide gray-scale images with which, to detect weapons, etc. As well, it can be used to see through heavy clouds, in order to perform aerial surveillance on days with inclement weather.

The technical details of this technology, known as PMMW or Passive MilliMeter-Wave, involve very-high-frequency (to 300GHz) amplifiers and detectors capable of sensing and processing picoWatt (10^{-12} Watt) power levels. At ISSCC 2007, the researchers from Grumman will describe, amongst other things, the achieving of a 2.5dB gain at 300GHz, the highest-frequency active integrated circuits ever reported. Operating at these frequencies requires the use of Indium-Phosphide (InP) technology with 70 and 35 nanometer feature sizes as well as lenses and detectors capable of processing millimeter-wavelength radiation.

The significance of the somewhat-fuzzy grayscale images to be presented is quite clear! Inevitably, such technologies will allow one to identify weapons carried beneath clothing. This technology presages an era of concentration on airport security, with technical meetings (such as ISSCC) at which recent science-fiction will be reported to be tomorrow's daily reality.

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NOTES

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