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Monte Carlo Simulation of Device Variations and Mismatch in Analog Integrated Circuits

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Abstract

Device mismatches, the small random variations in the characteristics of identically designed devices, occur during the manufacturing of integrated circuits. These mismatches result in behavioral variations of analog and digital integrated circuits. Except for very small circuits, it is difficult to analytically predict the behavior of a circuit due to the combination of the mismatch errors of individual devices. The impact of these random parameter variations on circuit behavior can be studied with Monte Carlo simulation by analyzing a large set of circuit instantiations with randomly varied devices.

In this paper, a set of Perl programs that automate the Monte Carlo simulation of circuits is presented. The tool generates a user specified number of modified netlists with randomly varied device characteristics. Each circuit device is modified according to a mismatch model for the device type. A user supplied parameters file controls the magnitude of variation for each device type and the tool automatically adjusts the parameter distributions of different device types and sizes. All netlists are simulated and their results are aggregated. These results reflect the tolerance of a circuit to device mismatch errors. Currently, the programs are optimized for the Spectre simulator from Cadence Systems, but the proposed approach can be adapted for other types of circuit simulators.

The use of this tool is illustrated with the Monte Carlo analyses for the DC accuracy of a cascode current mirror, the random variation of the delays of a pair of inverter strings under transient operation, the matching of the oscillation frequencies of a set of ring oscillators, and the variation of the transfer characteristics of a fifth order elliptic low pass active filter including its common-mode rejection.

Keyword: Circuit Analysis, CMOS Analog Integrated Circuits, Matching, Mismatch, Monte Carlo Simulation, MOSFET

1. Introduction

Small random variations occur during the manufacturing of circuit devices, resulting in behavioral differences between identically designed devices. These variations, or device mismatches, are often dismissed as an unimportant or difficult aspect of analog circuit design. This is not surprising because it is difficult to analytically predict the behavior of any non-trivial circuit due to the accumulation of the mismatch errors from individual devices. However, the physical aspects of device mismatch are well understood and quantitative models that accurately predict the device mismatch of individual devices exist[1,2,3]. Monte Carlo simulation can be used to investigate how the individual device mismatches of a circuit may accumulate and affect the circuit as a whole. This is achieved by analyzing a large set of circuit instantiations, whose circuit devices have each been individually randomized in accordance to the mismatch model of the particular device type. Section 2 of this paper explains the different approaches and device mismatch models that are used. As circuit designers have trouble properly assessing the effects of device mismatch, the main goal of this paper is to demonstrate a flexible tool that can not only simulate and analyze data, but also allow others to further research into device mismatch.

This paper presents a software package that simplifies the Monte Carlo simulation of analog circuits. The programs automate the process of generating a user specified number of netlists, recording simulation data from the

circuit simulator, and aggregating the data into a usable format. These results can be used to analyze the tolerance the circuit has to mismatch errors. The netlist randomization process is fully controlled by a user-supplied file containing the various parameters required by the device mismatch models. Currently, the software supports DC, AC, and transient circuit simulation modes and is optimized for the Spectre simulator from Cadence Systems. Section 3 of this paper steps through the Monte Carlo analyses of the DC accuracy of a cascode current mirror, the random variation of the delays of a pair of inverter strings under transient operation, the matching of the oscillation frequencies of a ring oscillator, and the variation of the transfer characteristics of a fifth order elliptic low pass active filter, including its common-mode rejection.

2. Methodology

Device mismatches are a result of manufacturing variations and can be observed lot to lot, wafer to wafer, die to die and device to device. Variations can be characterized in many different ways[1,2,3]. This paper introduces tools that apply specific mismatch modeling approaches to different device types. The tools allow for the introduction of both systematic and random variations. The discussion and examples within this paper mainly focus on random variations, i.e. the differences between two identically designed, closely spaced devices.

2.1. resistors, inductors, and capacitors

In this paper, basic two-terminal circuit elements such as resistors, capacitors, and inductors are characterized with two types of variation: systematic shift and random variation. The former assumes all types of elements are created with equal error and therefore, shifts the distribution of element values by a fixed amount. The latter assumes each individual element varies under a Gaussian distribution. In Figure 1, the variation and mismatch of two matched resistors are simulated by adding a random component to each resistor. This random component for each resistor is computed based on a user specified distribution, which depends on the size of the resistor. Similar approaches are followed for the capacitors and inductors in the circuit.

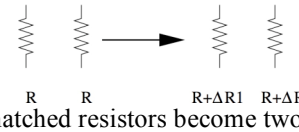

Figure 1. Two matched resistors become two simulated resistors

2.2 transistors

Modeling the variation of MOSFET devices is more difficult due to their nonlinear and multi-terminal nature. MOSFET devices have multiple parameters that vary, a dependence on bias for the current and voltage errors, and an area dependence for their variations, which cannot be modeled by a simple substitution of device values. There has been extensive research done on modeling the mismatch behavior of MOSFETs[1,2,3].

Pelgrom's model uses W, the gate-width, L, the gate-length, and A_β and A_{Vt}, technology-dependent constants of proportionalities, and derives (1) and (2)[1,2]. It is assumed that the dominating effects in random variations of a transistor are two independent variables: current factor differences $\Delta\beta$ ($\beta=\mu C_{ox}W/L$) and threshold voltage differences ΔVt. Using the Square Law current-voltage MOS equation in (3), small variations δV_t and $\delta\beta$ are added to simulate mismatch (4) for each device[3] with $\Delta\beta=\delta\beta_1-\delta\beta_2$ and $\Delta V_t=\delta V_{t1}-\delta V_{t2}$.

$$\left(\frac{\sigma(\Delta\beta)}{\beta}\right)^2=\frac{A^2_\beta}{W\cdot L} \tag{1}$$

$$\sigma^2(\Delta V_t)=\frac{A^2_{Vt}}{W\cdot L} \tag{2}$$

$$I_{DS}=\frac{\beta}{2}(V_{GS}-V_t)^2 \tag{3}$$

$$I_{DS}=\frac{\beta+\delta\beta}{2}(V_{GS}-V_t-\delta V_t)^2 \tag{4}$$

$$I_{DS} \cong \frac{\beta}{2}\left((V_{GS} - \delta V_t) - V_t\right)^2 + \frac{\delta\beta}{\beta} I_{DS} + \text{(higher order terms)} \quad (5)$$

Simplifying (4) leads to (5), which ignores higher order terms. It can been seen that as far as the effect on DC operation goes, the random variations can be expressed as a change in V_{GS} and an addition of a current proportional to I_{DS}; therefore, matched MOS transistors are replaced by a subcircuit containing an ideal voltage source δV_t in series with the gate and a current controlled current source with a gain of $\delta\beta / \beta$ in parallel with the drain source. The circuit shown in Figure 2 implements (5).

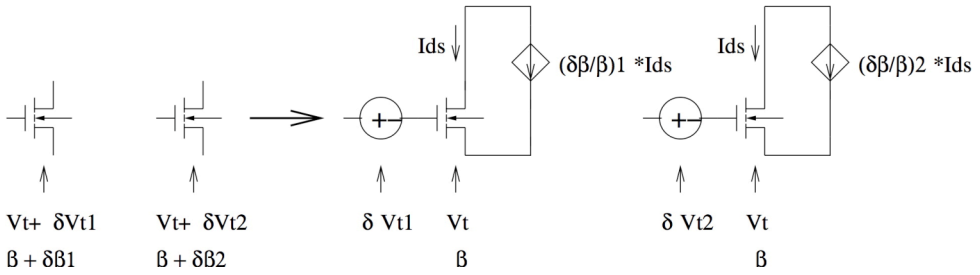

Figure 2. Two matched transistors are simulated using subcircuits

For each transistor in the netlist, the appropriate random variations are computed based on its W and L and user provided values for A_{Vt} and $A_{ß}$, and the transistor is replaced with the subcircuit shown in Figure 2. Transistors often include a multiplicity value signifying the number of equivalent transistors connected together in parallel. Even though these transistors are laid out on the same piece of bulk material, each device is subject to individual mismatch error. In order to simulate this, each line of code calling a transistor is "flattened" into the equivalent number of transistors so that each transistor's parameters can be randomized separately.

This model is accurate for DC analyses but has some shortcomings with parasitic capacitances in AC and transient analyses. The I_{ds} current measured at the drain terminal of the transistor also contains capacitive currents related to the drain-bulk and gate-drain capacitors; these currents are also multiplied in the voltage dependent current source modeling the current factor mismatch. In many cases, this limitation is not too significant. For some applications, a mismatch model different from Figure 2 might have to be implemented based on randomized model cards per transistor or using additional transistor calling parameters allowed in some circuit simulators.

2.3 additional considerations

2.3.1 subcircuit processing

Subcircuits are reusable blocks of circuit elements. They are defined once and can be used multiple times anywhere in the netlist, including from within other subcircuits. Special attention must be given to subcircuits because of their reusability. The randomization of a subcircuit definition is insufficient because the subcircuit may be used multiple times within the netlist, and each instance of a subcircuit must be uniquely randomized. This requirement, coupled with the fact that subcircuits may reference one another, means that a recursive parser is needed to properly interpret the netlist. Such a parser is used, thus allowing for the recursive generation of unique subcircuit instances. Every subcircuit reference, whether in the body of the netlist or within another netlist, is replaced by a reference to a uniquely randomized copy of the subcircuit.

2.3.2 Gaussian random number generator

All randomization within this project are generated with a normal Gaussian distribution. The random numbers are generated using the polar form of the Box Muller Transformation[4] (6). Given two independent and uniformly distributed variables x_1 and x_2, Gaussian distributions z_1 and z_2 (7-8) are created:

$$y = x_1^2 + x_2^2, y \forall (0,1] \tag{6}$$

$$z_1 = x_1 \cdot \sqrt{\frac{-2\ln(y)}{y}} \tag{7}$$

$$z_2 = x_2 \cdot \sqrt{\frac{-2\ln(y)}{y}} \tag{8}$$

2.4. tool usage

2.4.1 randomization process summary

The four steps of performing a Monte Carlo simulation using the presented software package are illustrated in Figure 3. The first step requires a tool-specific parameter file and a standard netlist, as shown in Figure 3(a). The parameter file controls the entire randomization process, and contains the entire mismatch model parameters mentioned in sections 2.1 and 2.2, as well as the list of nodes and currents, which are to be saved. From the input netlist and the parameter file, the randomizer program automatically generates a user specified number of randomized output netlists (Fig 3(b)). Next, a second program automates the simulation of the randomized netlists through the Cadence Spectre circuit simulator. The results from the simulations are stored in the nutascii file format (Figure 3(c)). Finally, the data aggregator reorganizes simulation results from being stored in a one file per simulation run format into the more useful one file per each saved node or current format (Figure 3(d)). Within an aggregated data file, each column represents the results for that node or current from a different simulation. The aggregated result files are suitable for any statistic analysis and graphing that is desired.

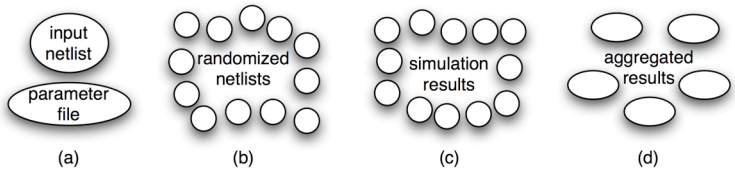

Figure 3. File types used during the simulation process
(a) user input files (b) generated input files (c) temporary output files (d) final output files

2.4.2 netlist randomization example

A portion of a Spectre netlist and the resulting randomized netlist code are shown in Table 1. The original netlist consists of a single call to a subcircuit containing a resistor and a transistor. The randomization process encapsulates the transistor within a subcircuit and implements flattening of the multiplicity factor, *m*. Hence, the original transistor line, which has multiplicity factor of two, is replaced by two individually randomized calls to the automatically generated transistor subcircuit.

Table 1. sample netlist segment and the randomized output netlist

Code Type	**Code Sample**
Original Netlist	I0 (net1 net2 0 0) testsubckt subckt testsubckt I G S GND R0 (I D) resistor r=4K M0 (D G GND GND) nch w=5u l=180.00n m=2 ad=1.4496e-13 as=1.4496e-13 pd=1.296u ps=1.296u ends testsubckt
Output Netlist	I0 (net1 net2 0 0) testsubckt_0 subckt testsubckt_0 I G S GND R0 (I D) resistor r=4.01707262342201K

```
  IM0_0 (D G GND GND) Mnch l=180.00n w=5u Vt=-0.00341901210509275 gain=0.00517345889556538
  IM0_1 (D G GND GND) Mnch l=180.00n w=5u Vt=-0.000837016763201703 gain=-0.0056403538044037
ends testsubckt_0

subckt Mnch d g s b
  parameters w=1u l=1u ad=1p as=1p pd=1u ps=1u Vt=0 gain=0
  vsub (g gp) vsource dc=Vt
  vtest (d dp) vsource dc=0
  Mnch (dp gp s b) nch w=w l=l ad=ad as=as pd=pd ps=ps
  F0 (d s) cccs gain=gain probe=vtest
ends Mnch
```

3. Examples

The following examples were simulated using 0.18 micron CMOS technology in Cadence Spectre 5.0. As stated before, the focus of this paper is on random variation, and thus, the systematic error was set to zero. All resistors, inductors and capacitors had a mean of the given value and a standard deviation of 1.5% of the given value.

3.1. cascode current mirror

The measurement setup is shown in Figure 4. For this simulation, the parameters for NMOS were W/L = 5µm/0.180µm, A_{Vt}=0.5 mV µm and $A_{ß}$=10.4% µm. Running a DC Operations Point analysis, an ideal current is sent through two MOSFETs, and a histogram of the percent difference between the input and output currents for 1000 simulations is graphed. The standard deviation of these simulations was 6.06%.

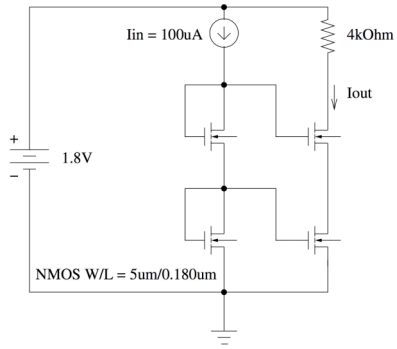

Figure 4. Cascode current mirror figure

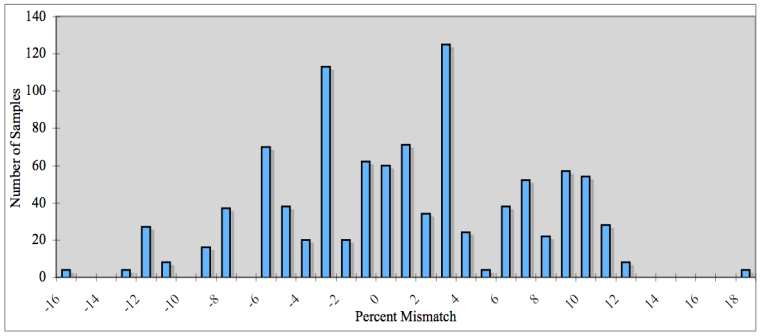

Figure 5. Number of samples versus percent mismatch between the currents of a cascode current mirror

3.2 Fifth order elliptical low pass active filter

The measurement setup is shown in Figure 6. In this example, a fifth order elliptical low pass active filter composed of ideal operational amplifiers and non-ideal resistors and capacitors are simulated using AC analysis. In Figure 7, differential input to differential output gain and differential input to common mode output gain are plotted against frequency (99 trials). For an ideal circuit without circuit variations, the differential input to common mode output gain is zero. Figure 8 is a histogram of the Common Mode Rejection Ratio (CMRR) in dB. The CMRR is defined as the ratio between the differential input to differential output gain over the differential input to common mode output gain. An ideal circuit without variations has an infinite CMRR.

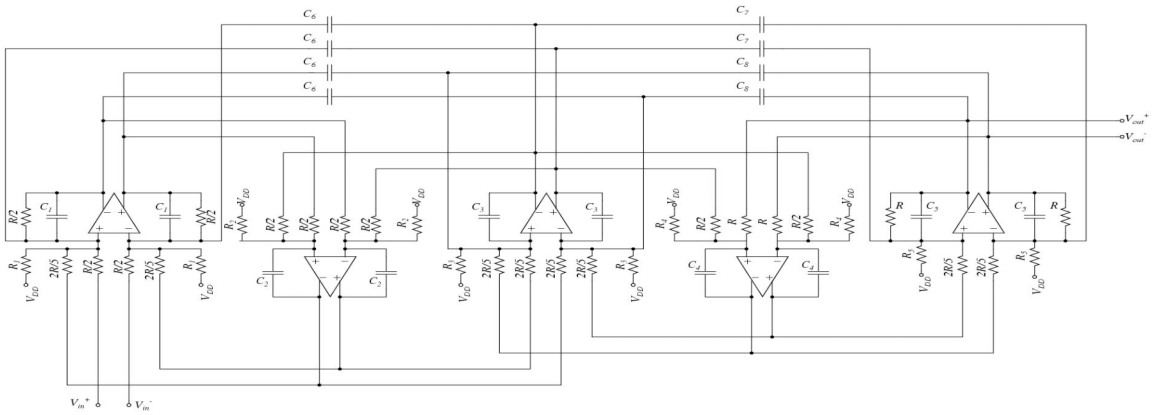

Figure 6. Fifth order elliptical low pass active filter circuit diagram

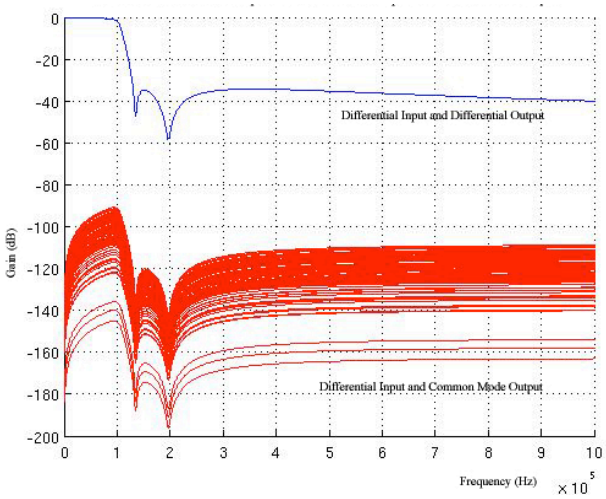

Figure 7. Gain versus differential input and differential output / common mode output

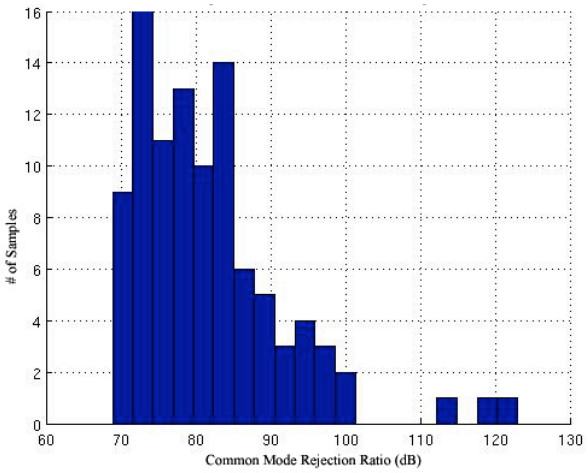

Figure 8. Number of samples versus common mode rejection ratio

3.3 inverter strings

The measurement setup is shown in Figure 9. For this simulation, the parameters for NMOS and PMOS were W/L = 240nm/180nm, A_{Vt}=0.5 mV µm and $A_{ß}$=10.4% µm. Running a transient analysis, a voltage is sent through each pair of inverter strings. The standard deviation of the two 8-stage inverter strings for 100 simulations was 0.146 ns.

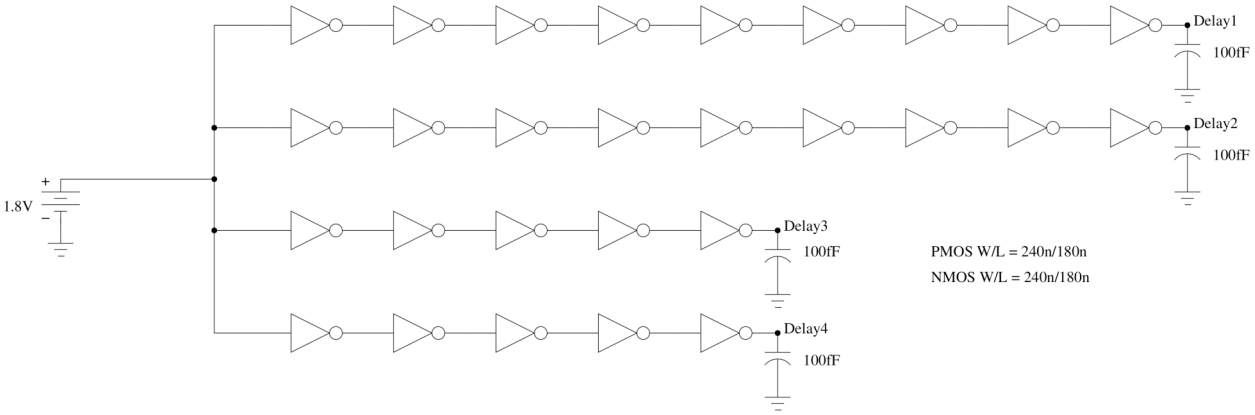

Figure 9. Circuit diagram of a pair of inverter strings with an 8-stage delay and a pair of strings with a 4-stage delay

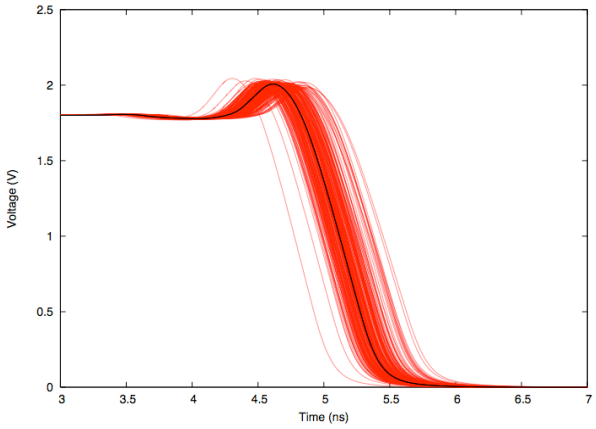

Figure 10. Graph of the output voltage versus time of the last inverters in the 8-stage inverter strings

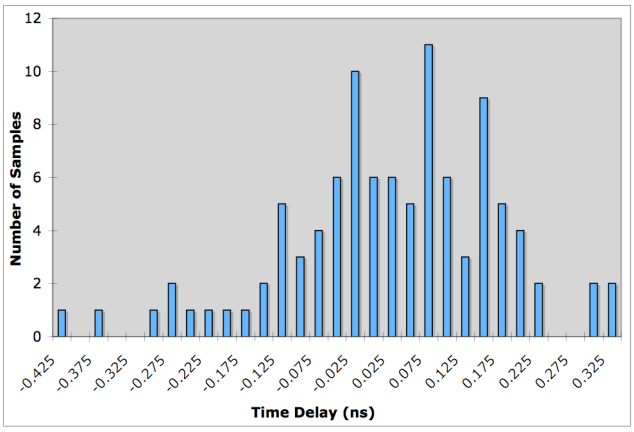

Figure 11. Histogram of the difference in time delay of the last inverters in the 8-stage inverter strings

3.4 ring oscillator

The simulated circuit is shown in Figure 12. For this simulation, the PMOS dimensions were W/L = 2µm/0.180µm, the NMOS dimensions were W/L = 0.5µm/0.180µm, and the mismatch parameters were A_{Vt}=0.5 mV µm and A_{β}=10.4% µm. Running a transient analysis, a voltage is applied to V_{out} in order to start the oscillation. Figure 13 is a histogram of frequency variation in percent, and has a standard deviation of 0.79%. Figure 14 is a histogram of average power variation in percent, and has a standard deviation of 2.58%. Both graphs were generated from the same 100 simulations.

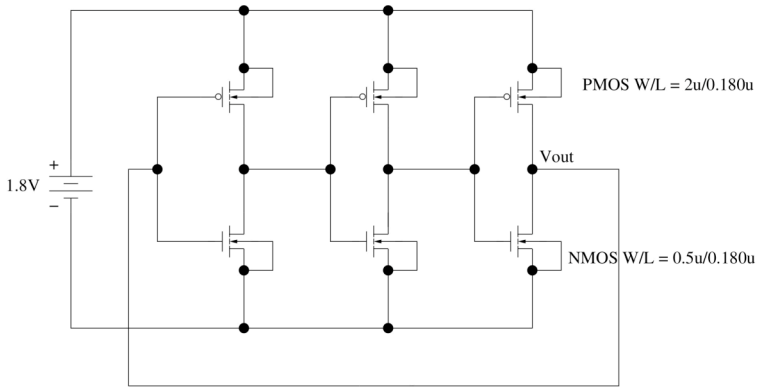

Figure 12. Ring oscillator circuit diagram

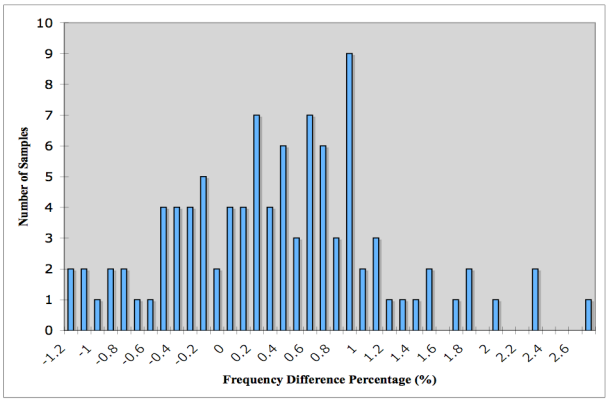

Figure 13. Histogram of frequency variation of ring oscillators (in percent)

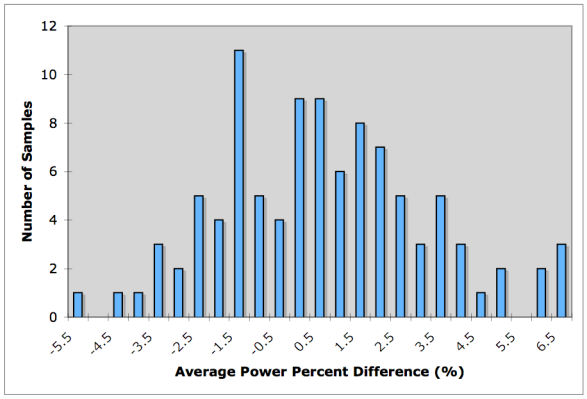

Figure 14. Histogram of average power variation of ring oscillators (in percent)

4. Conclusion

The presented tool reduces the difficulty of performing Monte Carlo analysis on analog circuits by automating the generation of many randomized netlists, their simulation, and the extraction of statistics from the collection of simulation data. Circuit components are randomized according to various mismatch models. Linear circuit components are varied using a Gaussian distribution for the component value based on user specified parameters. For MOSFETs, the dominating factors considered are threshold voltage and current factor mismatches. These transistors are randomized by adding an ideal voltage source in series with the gate to represent threshold voltage mismatches and a current controlled current source in parallel with the drain and source to represent current factor mismatches. Simulation results of four different circuits are presented along with a discussion of the advantages and limitations of the presented techniques.

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6. References

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