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1. An Ultra-Low Voltage, Low-Noise, High Linearity 900-MHz Receiver With Digitally Calibrated In-Band Feed-Forward Interferer Cancellation in 65-nm CMOS

Balankutty, A. Kinget, P.R.

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2. Digitally Assisted IIP2 Calibration for CMOS Direct-Conversion Receivers

Yiping Feng Takemura, G. Kawaguchi, S. Itoh, N.

Kinget, P.R.

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3. A Fast Phase Tracking ADPLL for Video Pixel Clock Generation in 65 nm CMOS Technology

Ching-Che Chung Chiun-Yao Ko

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4. A Miniature 2 mW 4 bit 1.2 GS/s Delay-Line-Based ADC in 65 nm CMOS

Tousi, Y.M. Afshari, E. Page(s): 2312 - 2325

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5. A 12-bit, 45-MS/s, 3-mW Redundant Successive-Approximation-Register Analog-to-Digital Converter With Digital Calibration

Wenbo Liu Pingli Huang Yun Chiu

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6. A 0.6-V 82-dB 28.6- μ W Continuous-Time Audio Delta-Sigma Modulator

Jinghua Zhang Yong Lian Libin Yao Bo Shi

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7. Design Techniques for Fully Integrated Switched-Capacitor DC-DC Converters Hanh-Phuc Le Sanders, S.R. Alon, E.

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8. A 2.4- $V_{\rm PP}$ 60-Gb/s CMOS Driver With Digitally Variable Amplitude and Pre-Emphasis Control at Multiple Peaking Frequencies

Aroca, R.A. Schvan, P. Voinigescu, S.P.

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9. Design and Analysis of a Self-Oscillating Class D Audio Amplifier Employing a Hysteretic Comparator

Jingxue Lu Gharpurey, R.

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10. Zero-Crossing Detector Based Reconfigurable Analog System

Lajevardi, P. Chandrakasan, A. P. Lee, H.-S.

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11. MOS operational amplifier design-a tutorial overview

Gray, P.R. Meyer, R.G.

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12. A 0.8-mW 5-bit 250-MS/s Time-Interleaved Asynchronous Digital Slope ADC

Harpe, P.J.A. Cui Zhou Philips, K. de Groot, H.

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13. A SAR-Assisted Two-Stage Pipeline ADC

Lee, C.C. Flynn, M.P.

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14. An Ultra-Wideband Impulse-Radio Transceiver Chipset Using Synchronized-OOK Modulation

Crepaldi, M. Chen Li Fernandes, J.R. Kinget, P.R.

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15. Low-OSR Over-Ranging Hybrid ADC Incorporating Noise-Shaped Two-Step Quantizer

Rajaee, O. Takeuchi, S. Aniya, M. Hamashita, K. Moon, U.

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16. Ultrahigh-Speed Low-Power DACs Using InP HBTs for Beyond-100-Gb/s/ch Optical Transmission Systems

Nagatani, M. Nosaka, H. Yamanaka, S. Sano, K.

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17. InP HBT IC Technology for Terahertz Frequencies: Fundamental Oscillators Up to 0.57

Munkyo Seo Urteaga, M. Hacker, J. Young, A. Griffith, Z. Jain, V. Pierson, R. Rowell, P. Skalare, A. Peralta, A. Lin, R. Pukala, D. Rodwell, M.

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18. A 20-MHz Bandwidth Continuous-Time Sigma-Delta Modulator With Jitter Immunity Improved Full Clock Period SCR (FSCR) DAC and High-Speed DWA

Jun-Gi Jo Jinho Noh Changsik Yoo

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19. Fully Integrated Switch-LNA Front-End IC Design in CMOS: A Systematic Approach for WLAN

Madan, A. McPartlin, M.J. Zhan-Feng Zhou Huang, C.-W.P. Masse, C. Cressler, J.D.

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20. A 90-nm CMOS Threshold-Compensated RF Energy Harvester

Papotto, G. Carrara, F. Palmisano, G.

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21. A 1.5-V, 1.5-GHz CMOS low noise amplifier

Shaeffer, D.K. Lee, T.H.

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22. A Single-Trim CMOS Bandgap Reference With a 3σ Inaccuracy of \pm 0.15% From 40 $_{\circ}$ C to 125 $_{\circ}$ C

Ge, G. Zhang, C. Hoogzaad, G. Makinwa, K. A. A.

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23. Transmitter Linearization by Beamforming

ChuanKang Liang Razavi, B.

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24. A Distributed Oscillator Based All-Digital PLL With a 32-Phase Embedded Phase-to-Digital Converter

Takinami, K. Strandberg, R. Liang, P. C. P. Le Grand de Mercey, G. Wong, T. Hassibi, M.

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25. A CMOS bandgap reference circuit with sub-1-V operation

Banba, H. Shiga, H. Umezawa, A. Miyaba, T. Tanzawa, T. Atsumi, S. Sakui, K.

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