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Solid-State Circuits, IEEE Journal of



1. A Wideband Receiver for Multi-Gbit/s Communications in 65 nm CMOS

Vecchi, F. Bozzola, S. Temporiti, E. Guermandi, D. Pozzoni, M. Repossi, M. Cusmai, M. Decanis, U. Mazzanti, A. Svelto, F. Page(s): 551 - 561

Digital Object Identifier: 10.1109/JSSC.2010.2100251

2. A 1-V Process-Insensitive Current-Scalable Two-Stage Opamp With Enhanced DC Gain and Settling Behavior in 65-nm Digital CMOS

Taherzadeh-Sani, M. Hamoui, A.A.

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3. A 300-GHz Fundamental Oscillator in 65-nm CMOS Technology

Razavi, B.

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4. A Continuous Time Multi-Bit $\Delta\Sigma$ ADC Using Time Domain Quantizer and Feedback Element

Dhanasekaran, V. Gambhir, M. Elsayed, M.M. Sánchez-Sinencio, E. Silva-Martinez, J. Mishra, C. Lei Chen Pankratz, E.J.

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5. A Wideband 3.6 GHz Digital $\Delta\Sigma$ Fractional-N PLL With Phase Interpolation Divider and Digital Spur Cancellation

Zanuso, M. Levantino, S. Samori, C. Lacaita, A.L.

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6. A SAR-Assisted Two-Stage Pipeline ADC

Lee, C. C. Flynn, M. P. Page(s): 859 - 869

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7. A 21 fJ/Conversion-Step 100 kS/s 10-bit ADC With a Low-Noise Time-Domain Comparator for Low-Power Sensor Interface

Seon-Kyoo Lee Seung-Jin Park Hong-June Park Jae-Yoon Sim

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8. A Quad-Band GSM/GPRS/EDGE SoC in 65 nm CMOS

Darabi, H. Chang, P. Jensen, H. Zolfaghari, A. Lettieri, P. Leete, J. C. Mohammadi, B. Chiu, J. Li, Q. Chen, S. Zhou, Z. Vadipour, M. Chen, C. Chang, Y. Mirzaei, A. Yazdi, A. Nariman, M. Hadji-Abdolhamid, A. Chang, E. Zhao, B. Juan, K. Suri, P. Guan, C. Serrano, L. Leung, J. Shin, J. Kim, J. Tran, H. Kilcoyne, P. Vinh, H. Raith, E. Koscal, M. Hukkoo, A. Hayek, C. Rakhshani, V. Wilcoxson, C. Rofougaran, M. Rofougaran, A.

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9. A Low-IF/Zero-IF Reconfigurable Analog Baseband IC With an I/Q Imbalance Cancellation Scheme

Kitsunezuka, M. Tokairin, T. Maeda, T. Fukaishi, M.

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10. High Power Terahertz and Millimeter-Wave Oscillator Design: A Systematic Approach

Momeni, O. Afshari, E.

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11. A 65 nm CMOS Quad-Band SAW-Less Receiver SoC for GSM/GPRS/EDGE

Mirzaei, A. Darabi, H. Yazdi, A. Zhou, Z. Chang, E. Suri, P.

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12. A Sensing Noise Compensation Bit Line Sense Amplifier for Low Voltage Applications

Myoung Jin Lee

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13. A 2.4 GHz Wideband Open-Loop GFSK Transmitter With Phase Quantization Noise Cancellation

Pin-En Su Pamarti, S.

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Tanabe, A. Hijioka, K. Nagase, H. Hayashi, Y.

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15. A 12-GS/s 81-mW 5-bit Time-Interleaved Flash ADC With Background Timing Skew Calibration

El-Chammas, M. Murmann, B.

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16. A CMOS 6-Bit 16-GS/s Time-Interleaved ADC Using Digital Background Calibration Techniques

Huang, C.-C. Wang, C.-Y. Wu, J.-T.

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17. An X- and Ku-Band Wideband Recursive Receiver MMIC With Gain-Reuse

Desheng Ma Dai, F.F. Jaeger, R.C. Irwin, J.D.

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18. Impedance Adapting Compensation for Low-Power Multistage Amplifiers

Xiaohong Peng Sansen, W. Ligang Hou Jinhui Wang

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19. A 2.6 nW, 0.45 V Temperature-Compensated Subthreshold CMOS Voltage Reference

Magnelli, L. Crupi, F. Corsonello, P. Pace, C.

Iannaccone, G.

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20. A Single-Chip 125-MHz to 32-GHz Signal Source in 0.18- \rlap/μ m SiGe BiCMOS

Shih-An Yu Baeyens, Y. Weiner, J. Koc, U.-V.

Rambaud, M. Fang-Ren Liao Young-Kai Chen Kinget, P.R.

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21. MOS operational amplifier design-a tutorial overview

Gray, P.R. Meyer, R.G.

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22. A 250 mV, 352 $\ensuremath{\mu}$ W GPS Receiver RF Front-End in 130 nm CMOS

Heiberg, A. C. Brown, T. W. Fiez, T. S. Mayaram, K.

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23. Dual Active-Capacitive-Feedback Compensation for Low-Power Large-Capacitive-Load Three-Stage Amplifiers

Song Guo Hoi Lee

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24. A Synthesis-Based Bandwidth Enhancement Technique for CMOS Amplifiers: Theory and Design

Deyi Pi Byung-Kwan Chun Heydari, P.

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25. Microwatt Embedded Processor Platform for

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Sridhara, S. R. DiRenzo, M. Lingam, S. Lee, S.-J.

Blazquez, R. Maxey, J. Ghanem, S. Lee, Y.-H. Abdallah, R. Singh, P. Goel, M.

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