


[Top Documents Accessed](#)
[BROWSE](#)
[SEARCH](#)
[IEEE XPLORE GUIDE](#)
[SUPPORT](#)

IEEE JOURNAL OF SOLID STATE CIRCUITS

Top Documents Accessed: May 2009

Display Format: ☒ Citation ☐ Citation & Abstract

Article Information

- Design of a High Performance 2-GHz Direct-Conversion Front-End With a Single-Ended RF Input in 0.13 μm CMOS**
 Yiping Feng; Takemura, G.; Kawaguchi, S.; Kinget, P.
 Solid-State Circuits, IEEE Journal of
 Volume 44, Issue 5, Date: May 2009, Pages: 1380-1390
 Digital Object Identifier 10.1109/JSSC.2009.2015824
[Abstract](#) | Full Text: [PDF](#) (1266 KB) (1266 KB)
- A 1 GHz Bandwidth Low-Pass $\Delta\Sigma$ ADC With 20–50 GHz Adjustable Sampling Rate**
 Hart, A.; Voinigesu, S.P.
 Solid-State Circuits, IEEE Journal of
 Volume 44, Issue 5, Date: May 2009, Pages: 1401-1414
 Digital Object Identifier 10.1109/JSSC.2009.2015852
[Abstract](#) | Full Text: [PDF](#) (1613 KB) (1613 KB)
- Measurements and Analysis of Process Variability in 90 nm CMOS**
 Liang-Teck Pang; Nikolic, B.
 Solid-State Circuits, IEEE Journal of
 Volume 44, Issue 5, Date: May 2009, Pages: 1655-1663
 Digital Object Identifier 10.1109/JSSC.2009.2015789
[Abstract](#) | Full Text: [PDF](#) (1995 KB) (1995 KB)
- A Fully Integrated 0.13- μm CMOS 40-Gb/s Serial Link Transceiver**
 Jeong-Kyoum Kim; Jaeha Kim; Gyudong Kim; Deog-Kyoon Jeong
 Solid-State Circuits, IEEE Journal of
 Volume 44, Issue 5, Date: May 2009, Pages: 1510-1521
 Digital Object Identifier 10.1109/JSSC.2009.2017973
[Abstract](#) | Full Text: [PDF](#) (3547 KB) (3547 KB)
- A 0.13 μm CMOS Quad-Band GSM/GPRS/EDGE RF Transceiver Using a Low-Noise Fractional-N Frequency Synthesizer and Direct-Conversion Architecture**
 Pei-Wei Chen; Tser-Yu Lin; Ling-Wei Ke; Rickey Yu; Ming-Da Tsai; Chih-Wei Yeh; Yi-Bin Lee; Bosen Tzeng; Yen-Horng Chen; Sheng-Jui Huang; Yu-Hsin Lin; Guang-Kaai Dehng
 Solid-State Circuits, IEEE Journal of
 Volume 44, Issue 5, Date: May 2009, Pages: 1454-1463
 Digital Object Identifier 10.1109/JSSC.2009.2015797
[Abstract](#) | Full Text: [PDF](#) (1867 KB) (1867 KB)
- Study of Subharmonically Injection-Locked PLLs**
 Jri Lee; Huaide Wang
 Solid-State Circuits, IEEE Journal of
 Volume 44, Issue 5, Date: May 2009, Pages: 1539-1553
 Digital Object Identifier 10.1109/JSSC.2009.2016701

[Abstract](#) | Full Text: [PDF](#) (3266 KB) (3266 KB)

7. **A 65 nm CMOS 30 dBm Class-E RF Power Amplifier With 60% PAE and 40% PAE at 16 dB Back-Off**

Apostolidou, M.; van der Heijden, M.P.; Leenaerts, D.M.W.; Sonsky, J.; Heringa, A.; Volokhine, I.

Solid-State Circuits, IEEE Journal of

Volume 44, Issue 5, Date: May 2009, Pages: 1372-1379

Digital Object Identifier 10.1109/JSSC.2009.2020680

[Abstract](#) | Full Text: [PDF](#) (2134 KB) (2134 KB)

8. **A Low Jitter Programmable Clock Multiplier Based on a Pulse Injection-Locked Oscillator With a Highly-Digital Tuning Loop**

Helal, B.M.; Chun-Ming Hsu; Johnson, K.; Perrott, M.H.

Solid-State Circuits, IEEE Journal of

Volume 44, Issue 5, Date: May 2009, Pages: 1391-1400

Digital Object Identifier 10.1109/JSSC.2009.2015816

[Abstract](#) | Full Text: [PDF](#) (1505 KB) (1505 KB)

9. **A DLL With Jitter Reduction Techniques and Quadrature Phase Generation for DRAM Interfaces**

Byung-Guk Kim; Lee-Sup Kim; Kwang-Il Park; Young-Hyun Jun; Soo-In Cho

Solid-State Circuits, IEEE Journal of

Volume 44, Issue 5, Date: May 2009, Pages: 1522-1530

Digital Object Identifier 10.1109/JSSC.2009.2016993

[Abstract](#) | Full Text: [PDF](#) (1298 KB) (1298 KB)

10. **A Fully Integrated Ultra-Low Insertion Loss T/R Switch for 802.11b/g/n Application in 90 nm CMOS Process**

Kidwai, A.A.; Chang-Tsung Fu; Jensen, J.C.; Taylor, S.S.

Solid-State Circuits, IEEE Journal of

Volume 44, Issue 5, Date: May 2009, Pages: 1352-1360

Digital Object Identifier 10.1109/JSSC.2009.2015813

[Abstract](#) | Full Text: [PDF](#) (1622 KB) (1622 KB)

[Back to top](#)

[Help](#) [Contact Us](#) [Privacy & Security](#) [IEEE.org](#)

© Copyright 2009 IEEE – All Rights Reserved

