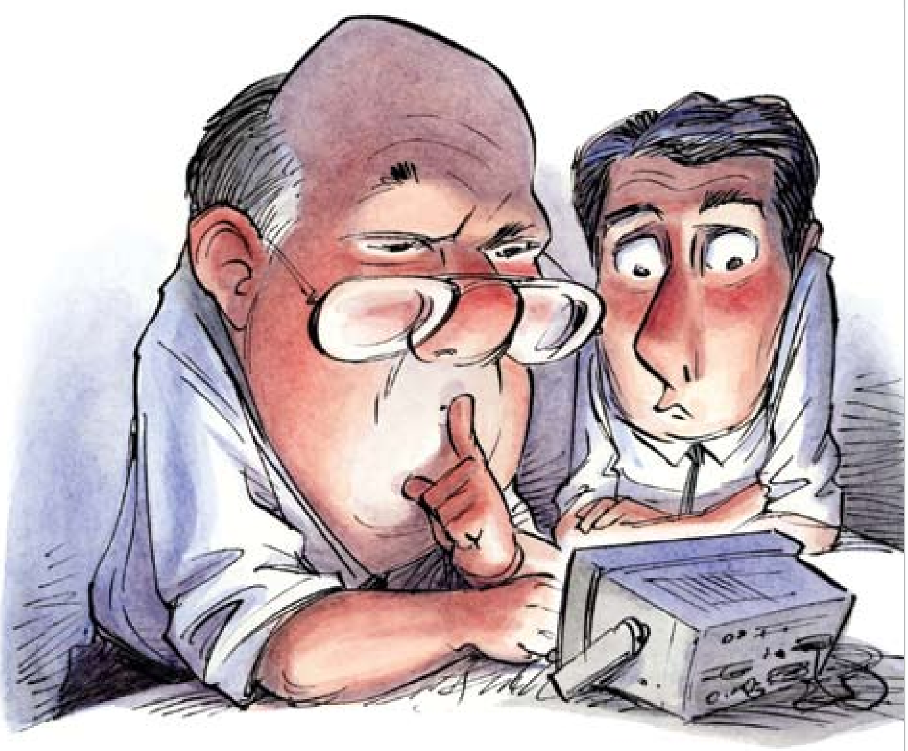
BY JIM DELMONICO • GENERAL ELECTRIC

All analog, all the time



DANIEL VASCONCELLOS

I was a rookie engineer fresh out of college in the late '80s. I had enjoyed long hours building analog-electronic projects as a hobby and thought that the digital world would be so much easier than analog electronics. After all, computer signals were all ones and zeros.

My first assignment was to write diagnostic software for a new RISC workstation. I relished the freedom from pesky analog signals as I rolled out diagnostic programs for the system. The project's hardware guru designed the SDRAM-interface ASIC and helped out with an optional cache-RAM module. He assigned me the cache-RAM diagnostic.

I did my best to write a bulletproof diagnostic. The optional cache-RAM module attached to the motherboard in a piggyback style using four dense, low-profile, high-speed connectors. The module's designer had allocated a good number of the connector pins to ground and power to feed the power-hungry synchronous-static-RAM chips. The diagnostic found all manufacturing-yield problems, and I was proud of myself.

Soon, though, some systems with the cache-RAM modules installed would fail intermittently when the system was running a real operating system. These infrequent failures were impossible to track down with a logic analyzer because the cache's 128-bit-wide data bus had 24 bits of address and several clocks. I didn't have the equipment to instrument that much cache capacity.

I humbly requested advice from the guru. He asked whether I had looked at any of the signals with an oscilloscope. Then, he smiled and led me to the lab. He probed a few data and address lines at the CPU and cache RAMs and left the scope on infinite-persistence mode as he booted the system several times. He showed me some odd outliers in the scope's eye patterns. Then, he told me to repeat the boot but to hold one scope probe on any cache RAM's ground pin.

The ground potential on the cache module intermittently differed from ground on the motherboard. He then lectured me on how everything, even digital circuitry, is analog.

He instructed me to add a diagnostic test that alternated writing and then reading back all ones and all zeros to sequential cache locations.

A significant amount of current was alternately flowing into the cache module from the power supply when the data bus was charging to logic one and then returning through ground when discharging the data bus to logic zero. The cache RAM's drivers were exhausting the local power-decoupling capacitance on the cache-RAM module when charging the wide cache-data bus. In addition, the ground path between the cache module and the motherboard had too much impedance to handle the current flow between the boards. This situation intermittently caused the logic levels at the CPU to miss the specified voltage specification for logic low, logic high, or both, causing data corruption.

The guru said that the module suffered from ground bounce. I was dumbfounded. He added more decoupling and bulk capacitance to the cache module and directed the designer to add a dedicated ground plane on the cache-RAM module's PCB (printed-circuit board) to reduce ground impedance. These changes fixed the problem.

I learned a lot on that day and have had the opportunity to give the same lesson to many young engineers, who were equally shocked when they, too, learned that everything is analog.EDN

Jim Delmonico is an engineer at General Electric (Skaneateles, NY). You can reach him at jim.delmonico@ge.com.

⊞ www.edn.com/tales