Outlook 2010: It's a mixed signal world

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Digital devices in an analogue world are driving the need for mixed signal IC design. The challenges are great, but solutions are emerging.

From mobile phones in third world villages to GPS units in luxury cars, the digital revolution is bringing electronics into people's lives everywhere. But digital devices must connect to the real world – and the real world is analogue.

Mixed signal design is the art of taking analogue information from the real world – such as sound, light, touch, vibration, or temperature – and bringing it into the digital 'cyber' world for processing. Virtually all digital devices have analogue interfaces and communication between digital components and devices is inherently analogue.

As new and innovative visions emerge for connecting the virtual digital world to the everyday analogue world, IC design teams are increasingly challenged by the ongoing convergence of more functionality into single devices. To meet consumer demands, chip designers must master the new levels of complexity that are required by mixed signal design as chips grow larger and more complex.

In 2010, the trend towards convergence will continue. Time and again, consumers have demonstrated a willingness to spend money on multifunction products with multiple connectivity options. Engineers are now faced with the challenge of bringing diverse functionality together in a small form factor with both cost and power efficiency constraints, while meeting stringent time to market demands. To keep pace with these escalating challenges, design teams are going to need to evolve their practices or fall victim to the combination of shortened schedules and rising complexity.

As an example, wireless platforms are being produced at a rate of more than 1billion devices per year, driven by the consumer's call for the convergence of audio, video, computation and wireless connectivity. In automobiles, mixed signal sensors and local processing units are being aggregated into central digital control systems. The medical device marketplace is another area where complex mixed signal design is helping to drive breakthrough innovations.

Market data from research firm International Business Strategies indicates that two thirds of the non memory integrated circuit market today is mixed signal in nature. That will grow to nearly three quarters by 2012. Mixed signal growth is driven by a shift towards more DSP centric designs for specialised data crunching from the real world and RF centric designs for more communication between virtual islands.

From a macro perspective, this means that chip design teams who previously identified themselves as 'analogue' or 'digital' will be thrust into the worlds of their counterparts. What will happen when the two worlds collide?

The focus of chip design is shifting towards systems on chip (SoCs) that include one or more processors, memory and various silicon intellectual property (IP) blocks. Since SoCs must interface with the real world through sensors, interfaces, antennas or other means, virtually all SoCs include analogue IP blocks and are thus mixed signal. To be successful, SoC design teams must orchestrate chip planning, reuse, verification and physical implementation into an effective mixed signal SoC realisation methodology.

Industry estimates show that 50% of silicon respins are due to mixed signal design issues. This means that mixed signal design teams must get more aggressive with advanced verification methodologies that thoroughly verify the interfaces between the analogue and digital domains. Many types of errors can contribute to chip failure. Miscommunication on control pin polarity and connection to an improper power grid are two common mistakes. Other, more vexing, design errors are prevalent and require more rigorous application of advanced verification technologies and methodologies.

For most designs today, verification is the biggest cost. Mixed signal designs are no exception. Customers are seeing, simultaneously, the growth in verification cost and the increasing

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complexity of analogue/digital domain interactions as more analogue intellectual property (IP) blocks are integrated into SoCs. It's getting more difficult to complete full chip simulations. New classes of failures are occurring, while old causes are being exacerbated.

Digital designers have some automated methods for generating the testbenches that provide stimulus for simulation and they often use coverage metrics to gauge the effectiveness of verification. Bringing these concepts to the world of analogue/RF verification is challenging, but is needed to help improve designer productivity.

Balancing runtime versus accuracy is critical, especially when considering system validation. The use of characterised models is essential for maintaining accuracy. When taping out a design, designers need to have confidence that they have accounted for parasitics and noise in their final simulations.

Mixed signal SoCs pose two verification challenges – making sure intent is specified correctly and ensuring that intent is retained through the implementation process. The first challenge is where simulation and advanced verification methodologies come into play. Applying the discipline of the metrics driven verification methodology that Cadence provides enables design teams to have specific coverage goals and strategies to measure verification progress.

The second challenge, ensuring that original intent is retained during implementation, calls for a hybrid of static (formal) and dynamic (simulation) technologies. Formal equivalence checking for digital circuitry has been in use for a long time now. Unfortunately, for analogue design, there is no complementary static technique available. The interfaces between analogue and digital circuitry do, however, provide the opportunity for further static checking.

The demand for reduced power consumption and energy efficiency impacts most IC designs today and mixed signal SoCs are no exception. Low power design is tough enough for digital designs. Mixed signal designs introduce even more complexity. To help designers capture and verify digital power intent, Cadence developed the Common Power Format (CPF), an open format currently available through the Silicon Integration Initiative. The Cadence Virtuoso AMS Designer Simulator can leverage CPF to understand what happens when power is shut off in mixed signal designs.

Mixed signal implementation also requires a detailed knowledge of the physical constraints and assumptions that were made while designing block level silicon IP. Combining analogue and digital circuitry can result in noise that degrades performance, limits yield or, worse yet, requires another design pass. Noise issues can be avoided by developing a constraint-driven physical design. This requires a design system that can capture and verify both physical and electrical constraints, such as the Cadence Virtuoso custom IC design platform.

Automating physical implementation with captured constraints provides a much needed boost to productivity. Since RF/analogue and digital designers have typically worked in separate domains, enabling them to be productive in their own environments with common data and constraints is critical for their success. For this reason, Cadence provides a common constraint mechanism across Virtuoso and the Cadence Encounter Digital Implementation System.

Top down floorplanning provides a high level layout of IP blocks and can reduce the parasitic impact of top level interconnect. But many designers don't want to start a floorplan before analogue and digital IP is well defined, for fear it will radically change the floorplan. However if they wait until it is fully defined, they consume precious time to market. A better solution is a flow that allows concurrent top level floorplanning and IP design and uses an open database solution, such as the OpenAccess database donated to the industry by Cadence, to make it easier to update IP sizes and pin locations later in the design process.

Having by far and away the largest user base in analogue design and an industry leading automated digital implementation solution – both available on the OpenAccess database – Cadence is prepared to help designers meet the mixed signal challenges of 2010 and beyond. We are committed to ensuring that mixed signal design is not mixed up!

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Author
Steve Carlson, vice president of marketing, low power and mixed signal solutions, Cadence Design Systems

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