Conference Coverage

CICC panelists: yes, analog designers can scale

By Richard Goering

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San Jose, Calif. -- Analog designers are not hopeless at scaling, according to panelists at the Custom Integrated Circuits Conference (CICC) here Sept. 17. But scaling involves more than just porting existing circuits to the next process node, several panelists said.

The panel was provocatively titled, "Are analog designers hopeless at scaling? Will digital designers eat their lunch at 45 nm and below?" The panel's stated premise was that analog circuit implementations have not been as successful as digital implementations in exploiting scaling for performance and density gains.

But panelists, who were mostly drawn from the analog design world, didn't necessarily agree. Among them was Boris Murmann, assistant professor of electrical engineering at Stanford University. He cited research showing that analog-to-digital converters (ADCs) have shown a 35-fold improvement in power dissipation over the past 10 years.

"If you say analog hasn't scaled, where have you been for the last decade?" Murmann asked. "Flash ADCs have scaled slightly better than microprocessors. Those guys stopped scaling clock speed some time ago and we kept going. That's one metric we're winning."

Murmann observed that there are "scaling studs" who think that going to 45 nm and below produces only benefits, and "scaling crybabies" who complain every time supply voltage drops. Neither view, he suggested, is accurate. The "crybabies," he said, will have to try some new things. These include getting rid of op-amps, which he said make inefficient use of energy; leveraging digital processing techniques; doing more work with oversampling; and rethinking signal-to-noise ratios.

The real challenge, Murmann said, is systems engineering. "We can no longer blindly port analog to new technology nodes," he said. "We must rethink and improve system partitioning to take advantage of nanometer technology."

Peter Kinget, associate professor of electronic engineering at Columbia University, was among several panelists who referred to Murmann's ADC study. Scaling, he noted, brings with it the need to deal with lower supply voltages. Digital designers like low Vdd because it reduces dynamic energy, but analog designers don't like it because it reduces signal swing and raises worries about not meeting performance goals, he said.

Nevertheless, Kinget said, "at this point there are no fundamental roadblocks to analog scaling." Moreover, he said, FinFETs – field effect transistors with fin-like channels -- will have very good scaling properties if they ever come into widespread use.

Kinget also observed that digital designers these days are so concerned about variability and power density that they are embedding analog circuits in digital gates so they can monitor what's going on, and are thus on "analog life support." He concluded that "we'd better keep analog scaling going. Otherwise, the digital designers won't have any lunch to eat."

Bogdan Staszewski, member of technical staff at Texas Instruments, warned that "scaling will not be achieved by porting the same circuit design to the next process node. Architectural redesign will be required." He noted that challenges like low-voltage operation will make signal-to-noise ratio much worse. Solutions at the architectural level will be needed, he said, such as letting digital logic do more work than it's done in the past.

Staszewski said that TI has "benefited tremendously" from analog scaling. He noted TI's usage of interdigitated metal capacitors at 130 nm, low drop-out (LDO) regulators at 90 nm, and switching regulators at 65 nm. Today, he noted, TI is under development with its 45 nm analog process.

Staszewski refuted three "myths" about analog scaling: that high-performance CMOS is getting worse for analog RF applications, that component matching is getting worse, and that high voltage cannot be supported by nanoscale CMOS. He noted, however, that development costs for systems-on-chip with digital and analog/RF circuitry are "higher than average" and that such chips make sense only for mass-produced products.

Things will get better for analog designers, said Bernhard Boser, professor of electrical engineering and computer science at the University of California at Berkeley, because Vdd has almost reached its minimum.

"This is good for analog and very bad for digital," he said. "Digital designers don't profit from scaling as much as they used to."

A somewhat gloomy, albeit tongue-in-cheek, view of analog scaling came from Marcel Pelgrom, member of technical staff at NXP Semiconductor. He showed several slides of scaling a chip design over a period of several years, with the overall chip design shrinking in size except for an ADC that stayed constant. "Indeed, we mess up scaling, but people who mess things up, like lawyers, often make more money than people who solve things," he said.

Pelgrom said, however, that the real question is not one of analog versus digital designers, but one of who will use statistics and how. Scaling makes statistics important, he said, because of random variations. Analog designers have been doing statistical design since 1985, he noted, using techniques such as dynamic element matching and Monte Carlo analysis.

And their digital counterparts? "The digital guys woke up around the turn of the century," Pelgrom said. Today, in 2007, there are "only meager attempts" to use statistical analysis in digital design, he said, in such areas as leakage distribution and timing. "Will digital designers eat our lunch? No, but if both [digital and analog designers] learn to master statistics we can have not only a free lunch but a free dinner," he said.

Ian Young, senior director and fellow at Intel, brought a digital background to the panel. Stating that the "world is going hybrid," he suggested the term "digilogic" to describe the merging of analog and digital design.

"Hybrid technology is the way of the future to overcome the challenges of analog circuits under technology scaling," Young said. This will happen, he suggested, through "digital assisted analog," in which circuits will quantize analog signals into digital as soon as possible, and the device will do as much processing in digital circuitry as possible.

In a question-and-answer session, several panelists suggested that the divide between digital and analog designers is easing. "I think digital designers are becoming EEs [electrical engineers] again," said Pelgrom. "They need to know about devices. They need to know statistics, and for statistics you have to go between the ones and zeros. The EEs have taken over again but the computer science is still there. We need all the skills from both worlds to make it work."