

Solid State Transformers:

architecture, control and simulation results.

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This document presents a preliminary analysis of Solid State Transformers (SSTs), aiming to provide a comprehensive introduction to the technology. The study proposes a potential layout for hardware architectures and control strategies, supported by Simscape modeling and simulation results. Furthermore, the document evaluates the capabilities of the Simscape models implemented for this investigation.

1 Introduction

Solid State Transformers (SSTs) are advanced power electronic devices designed to replace traditional low-frequency transformers in modern power distribution systems. By operating at high frequency and using fully controllable conversion stages, SSTs achieve a more compact size, improved energy efficiency, and enhanced functionality compared to conventional transformers. Beyond simple voltage transformation, they provide additional services such as bidirectional power flow, voltage and reactive power regulation, and seamless integration of distributed energy resources including renewables, electric vehicles, and energy storage.

A key difference from traditional transformers is the behavior of SSTs during fault conditions. Due to their electronic nature and active current limiting, SSTs inherently restrict short-circuit currents. This prevents downstream systems from relying on conventional overcurrent-based protection schemes, which depend on high fault currents for detection. As a result, new protection strategies based on advanced sensing, high-speed control, and intelligent fault identification must be implemented. This shift in protection philosophy presents both challenges and significant opportunities for the development of more flexible, reliable, and smart power networks.

2 Global Architecture

In this chapter few general architectures for SST solutions are proposed and investigated; the SST device is intended to operate between two different grids:

- a low voltage DC grid source where many contributors can be assumed are connected e.g. energy storage, photovoltaic installations, car chargers and others;
- a three phase medium voltage AC grid source;

Figure 1 shows a single phase architecture, which basically is made by a cascade of single phase inverters. Each single phase inverter is supplied by a galvanically isolated DC/DC converter.

From control point of view we could assume the following control strategy

- DC/DC power supply control can be assumed monolithic and independent;
- three phase active front end (AFE) control architecture can be assumed as follows
 - each single phase inverter is equipped by a single phase PLL (master and slaves);
 - an inverter current control (master);
 - a voltage controlled source mode (slaves).

Figure 2 a case scenario of global three phase architecture with a common communication bus which performs a global distributed control.

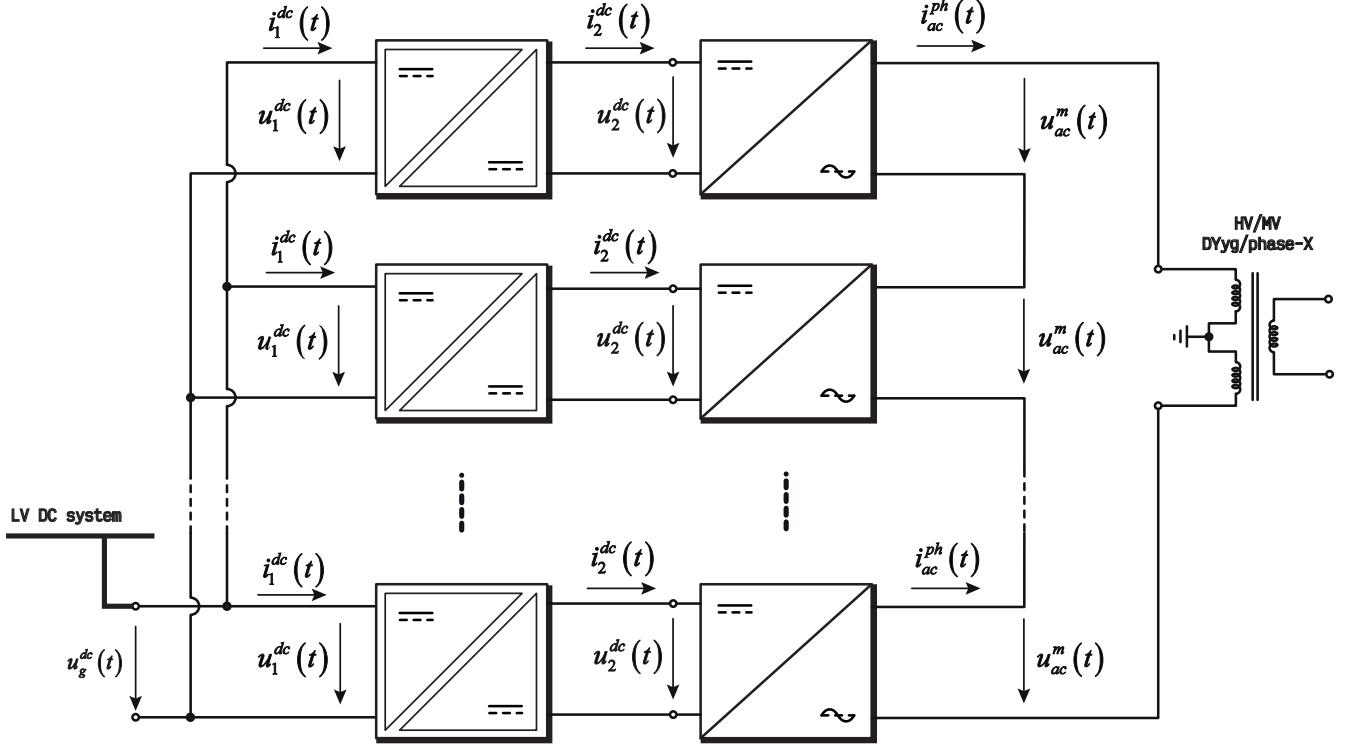


Figure 1: Single phase architecture based on galvanically isolated single phase inverter cascade.

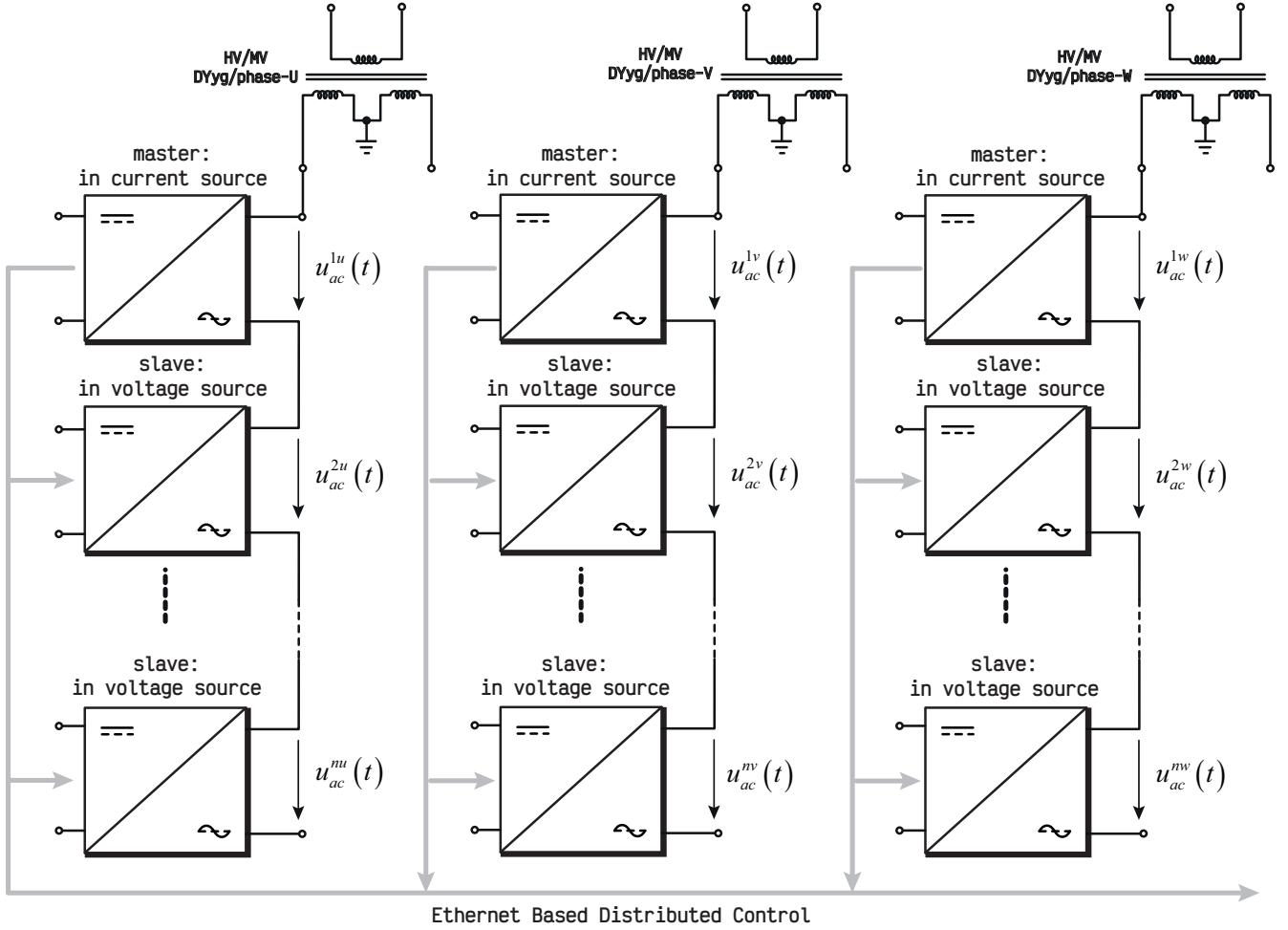


Figure 2: Global architecture for three phase system where a cascade of master/slaves single phase inverter implements the the single phase MV.

Single phase inverter will be here assumed made by a three levels NPC as shown in Figure 3. This solution permits to extend the nominal voltage of the single phase inverter and be able to operate with a dclink voltage around 1.5 kV.

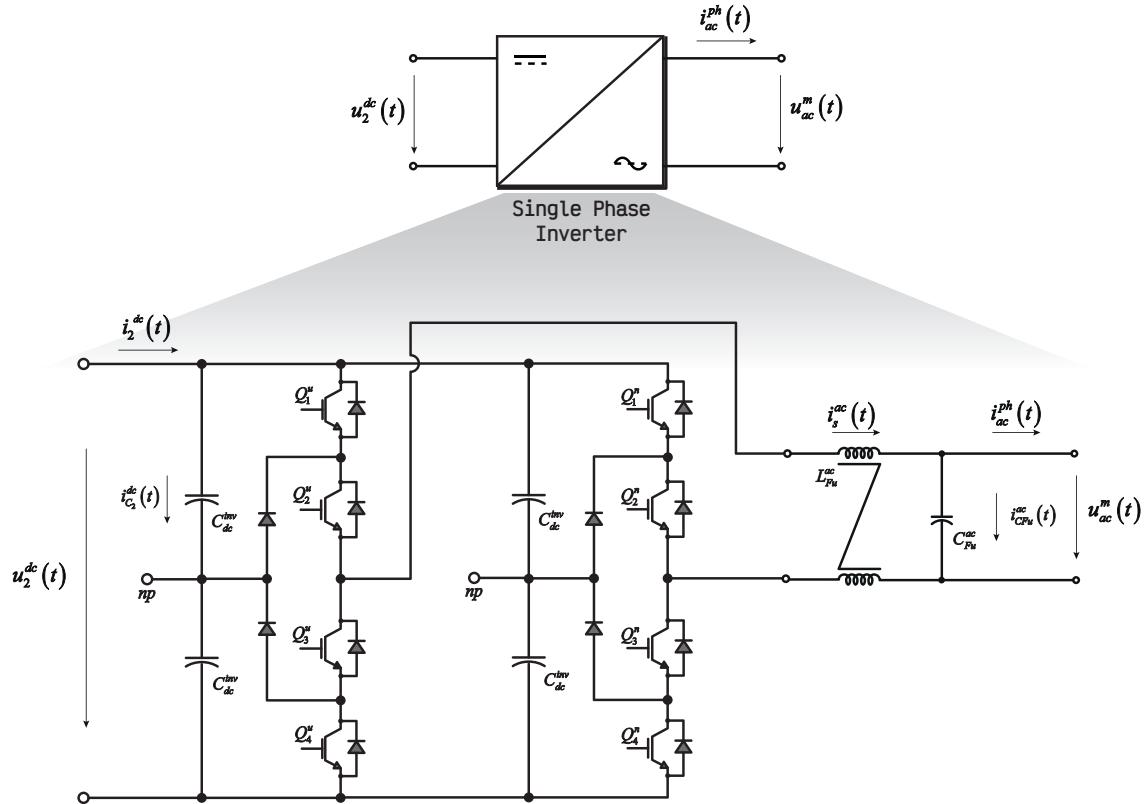


Figure 3: Single phase inverter stage: based on three level NPC.

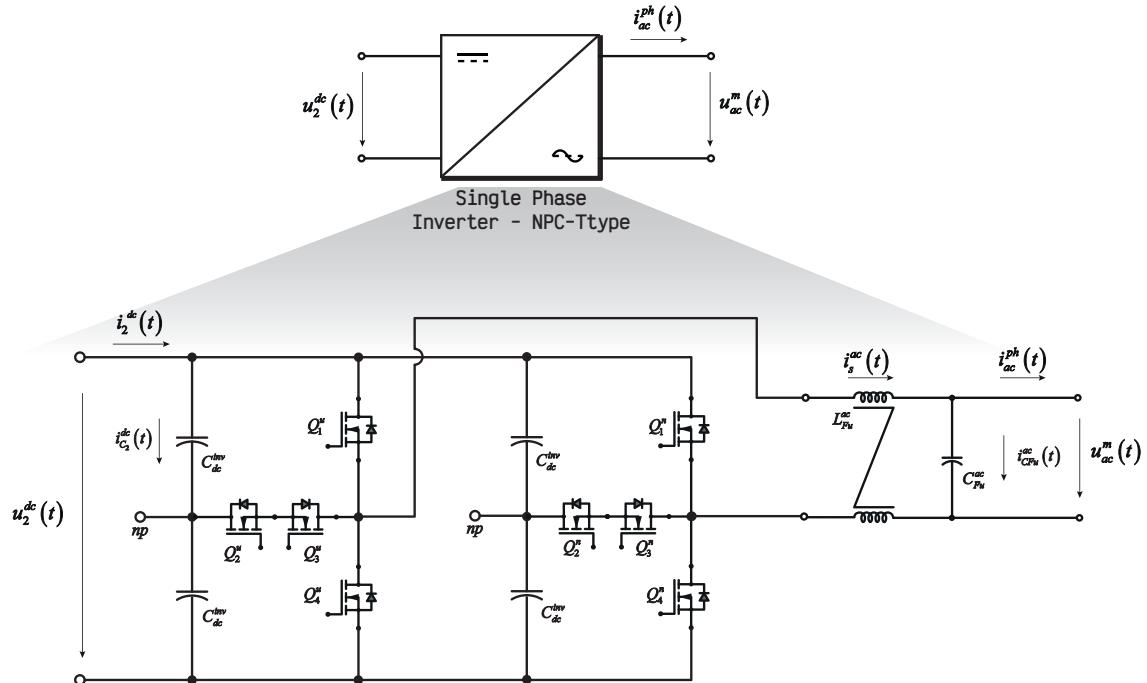


Figure 4: Single phase inverter stage: based on three level TNPC.

In SST applications, the galvanically isolated DC-DC power supply plays a fundamental role in terms of global efficiency and performance. In this document three different DC/DC architectures will be

investigated:

- three phase DAB;
- single phase bidirectional CLLC;
- single phase DAB;

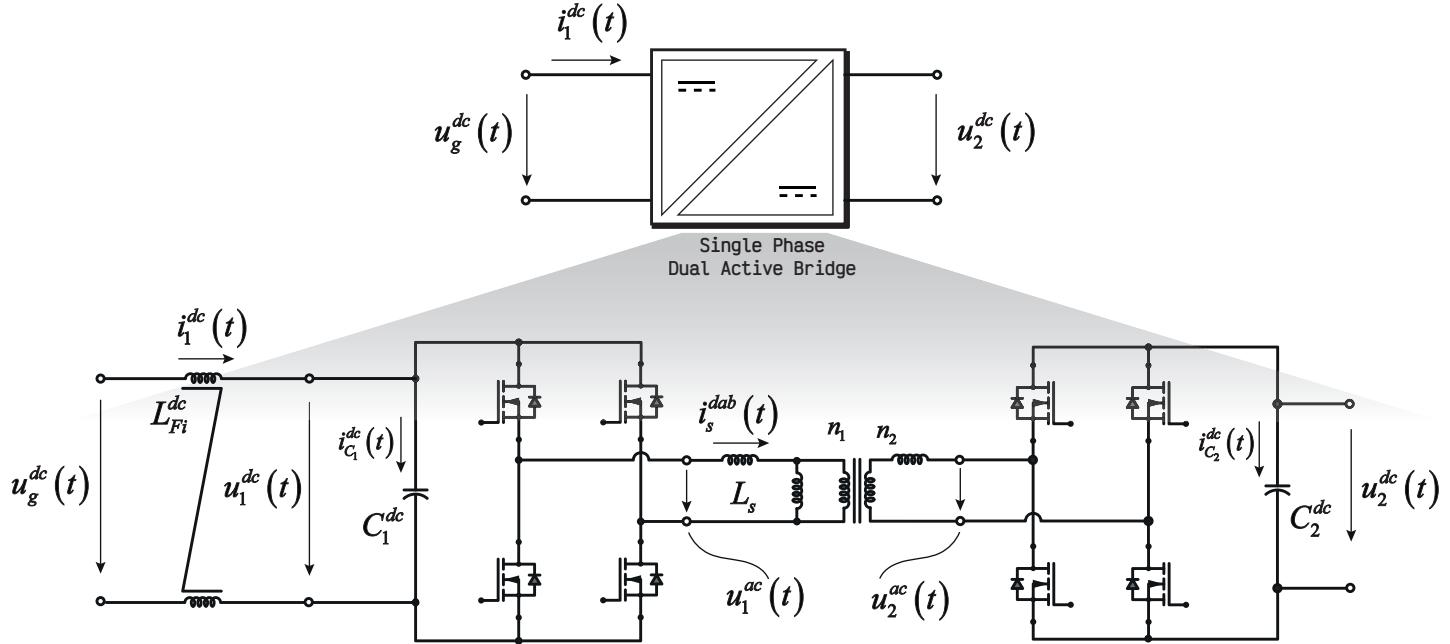


Figure 5: Single phase DAB.

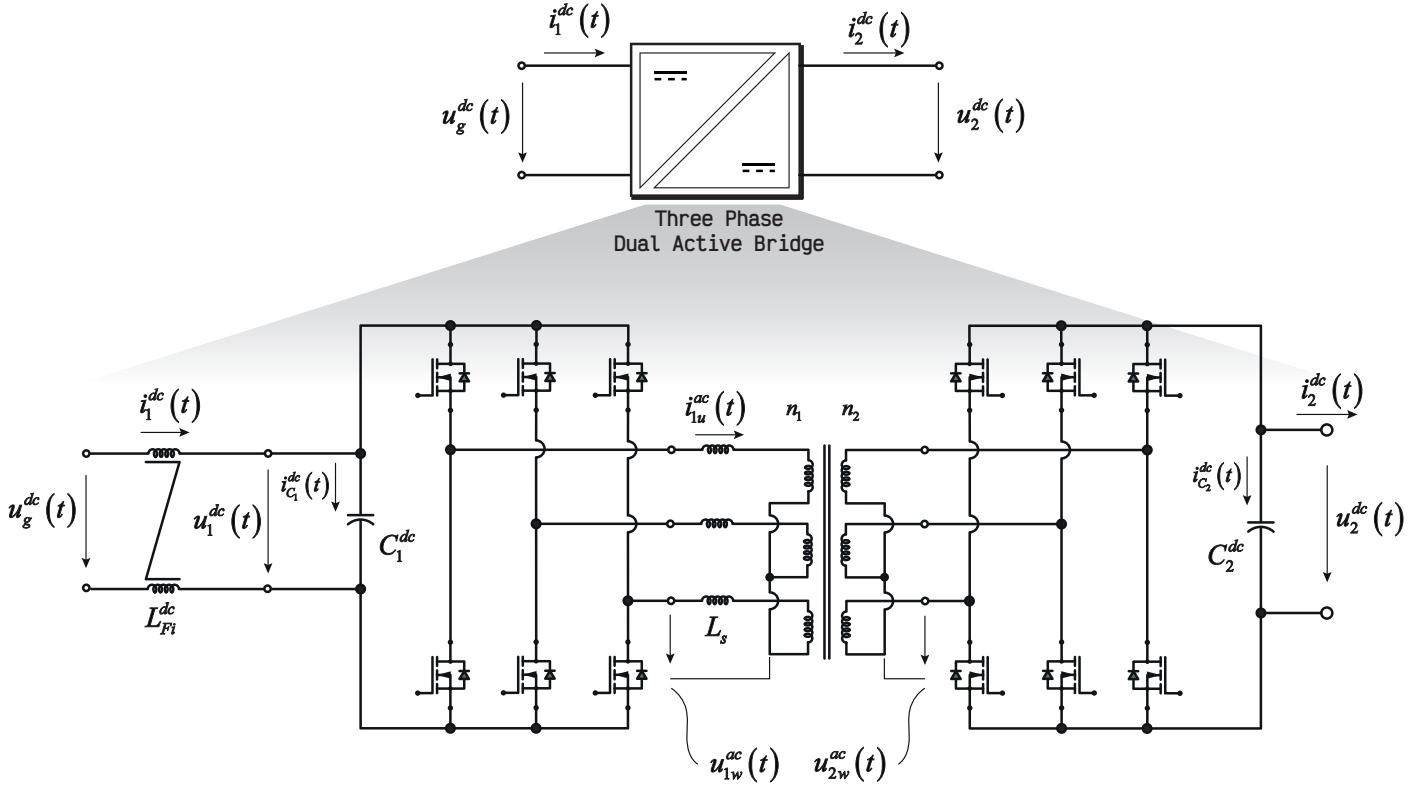


Figure 6: Three phase DAB.

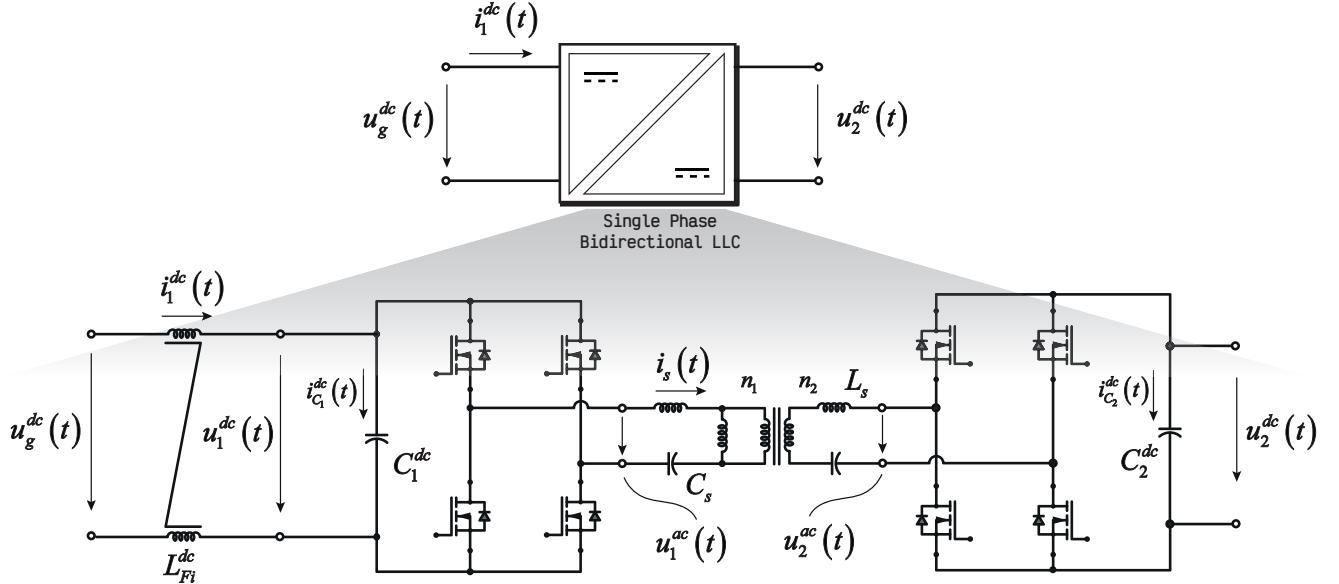


Figure 7: Single phase bidirectional CLLC.

3 Control Architecture

In the control concept here proposed the aim of the DC/DC power supply is to provide a controlled DClink voltage, $u_2^{dc}(t) = u_2^{dc}|_{ref}$, while the AFE will drive a current reference to the AC grid according to the status of the DC grid, Figure 8 shows a possible control principle.

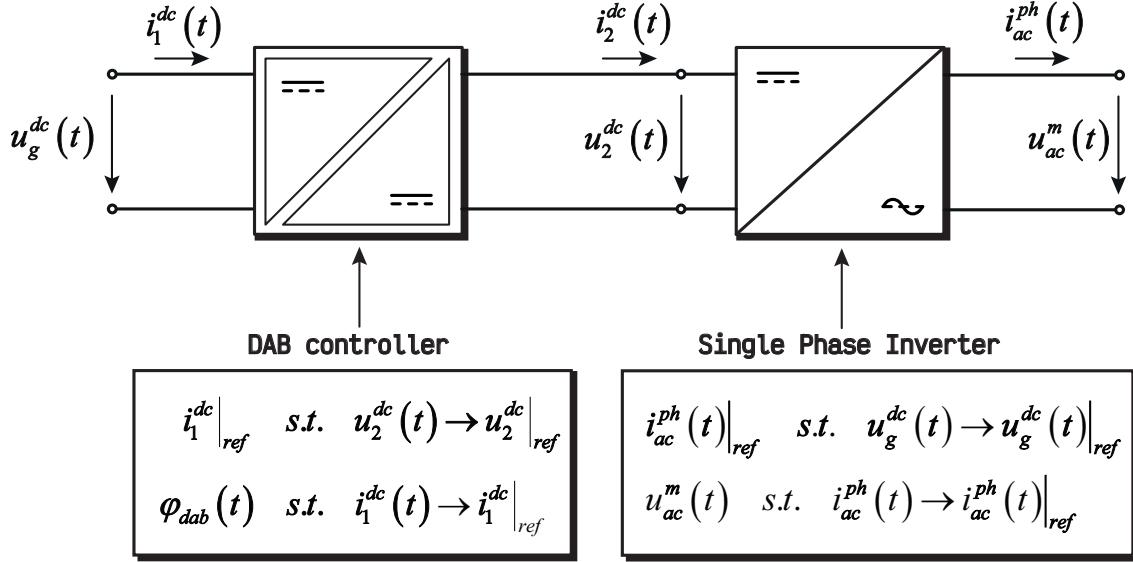


Figure 8: Fundamental control strategies of the isolated single phase inverter.

3.1 DC/DC Control Loops

DC/DC control is basically constructed by a cascade of PI-control with an outer voltage loop control followed by an inner current control loop;

Remark - ZVS condition, for the single phase DAB, is achieved with a dead-time of $t_{dt} = 400$ ns.

Remark - ZVC condition, for the CLLC, is achieved forcing DCM.

3.2 Single Phase Lock Loop

Single phase inverter uses a single phase lock loop as shown in Figure 9

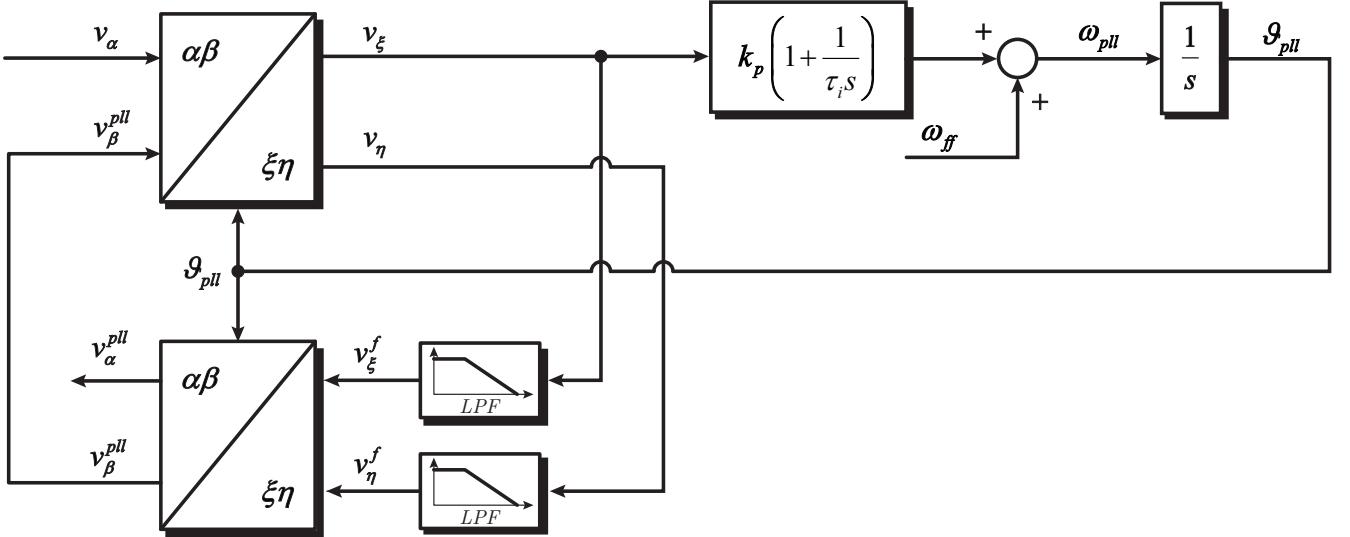


Figure 9: Single phase lock loop for grid phase estimation.

3.3 Single Phase Inverter Control Layouts

Single phase inverter has been simulated with resonant PI as well as with virtual vector control as shown in Figure 10

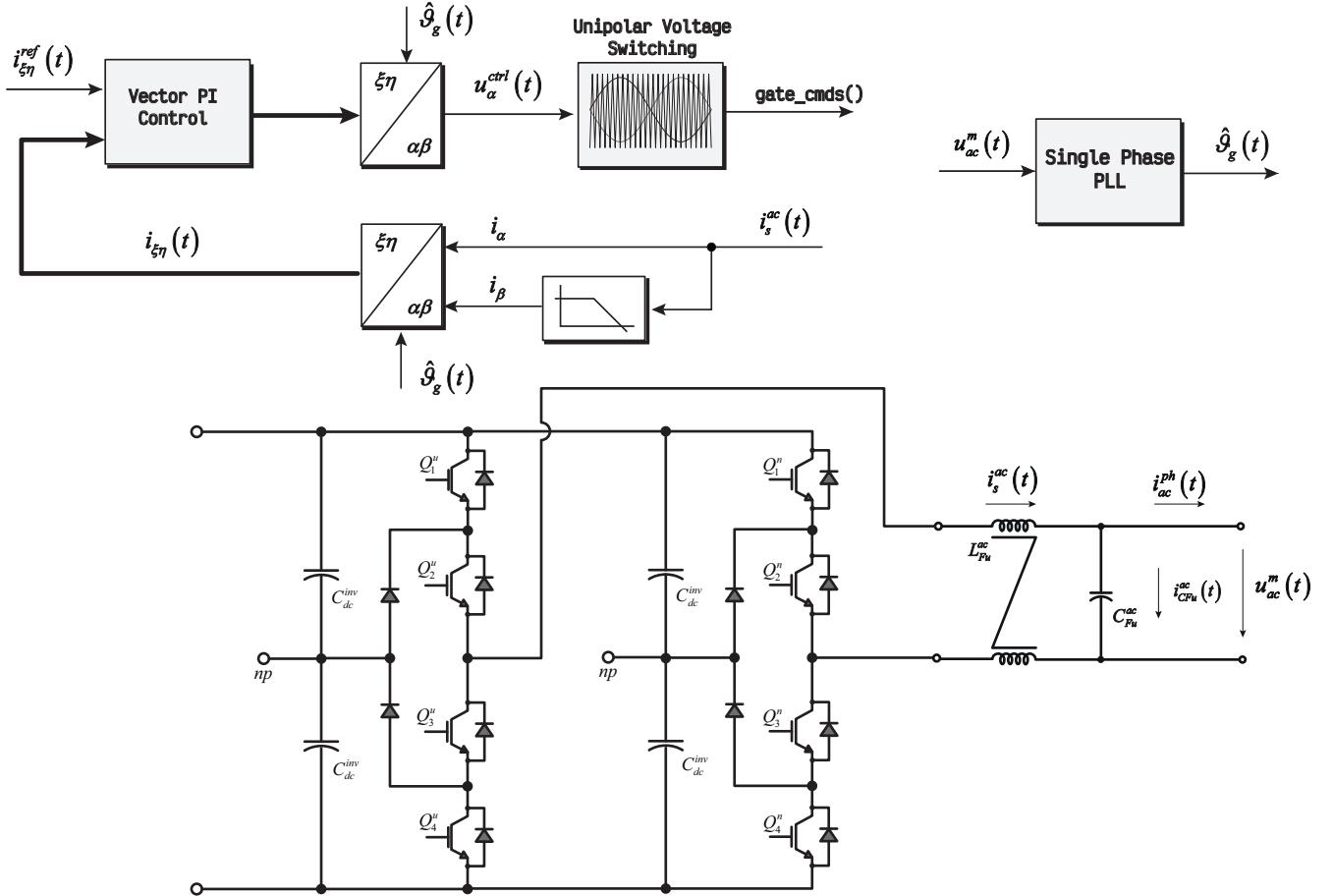


Figure 10: Control layout of the single phase inverter.

4 Simulation results

In this section simulation results of the architecture based on three phase DAB is shown, in particular the following operative conditions have been accounted:

- three phase DAB works at fundamental frequency of $f_{dab} = 4 \text{ kHz}$;
- single phase CLLC works at fundamental frequency of $f_{llc} = 9.6 \text{ kHz}$;
- single phase DAB works at fundamental frequency of $f_{spdab} = 10 \text{ kHz}$;
- single phase inverter operates at the switching frequency of $f_{inv}^{pwm} = 4 \text{ kHz}$.

The three phase DAB switching devices are based on SiC MOSFET, while Si based IGBT for the three level single phase inverter, as follows

- Danfoss **SKM1700MB20R4S2I4** for the DC/DCs;
- Wolfspeed **CAB760M12HM3** for the NPC;

4 Simulation results

According to Figure 7 and Figure 3, the following components shall be accounted:

- $L_{Fi}^{dc} = 400 \mu\text{H}$ - input DAB inductance with nominal current of $I_{LFu}^{nom} = 300 \text{ A}$;
- $C_1^{dc} = 3.6 \text{ mF}$ - input DAB capacitor with nominal voltage of $U_{C1dc}^{nom} = 1.5 \text{ kV}$;
- $L_s = 60 \mu\text{H}$ - DAB inductance (this value takes into account also the leakage inductance of the transformer) with nominal current of $I_{Ls}^{nom} = 250 \text{ A}$;
- $C_2^{dc} = 3.6 \text{ mF}$ - output DAB capacitor with nominal voltage of $U_{C1dc}^{nom} = 1.5 \text{ kV}$;
- $C_{dc}^{inv} = 3.6 \text{ mF}$ - output DAB capacitor with nominal voltage of $U_{C1dc}^{nom} = 1.5 \text{ kV}$;
- $L_{Fu}^{ac} = 500 \mu\text{H}$ - output single phase inverter of $I_{LFu}^{nom} = 300 \text{ A}$;

Figure 10 show the control architecture of the single phase inverter.

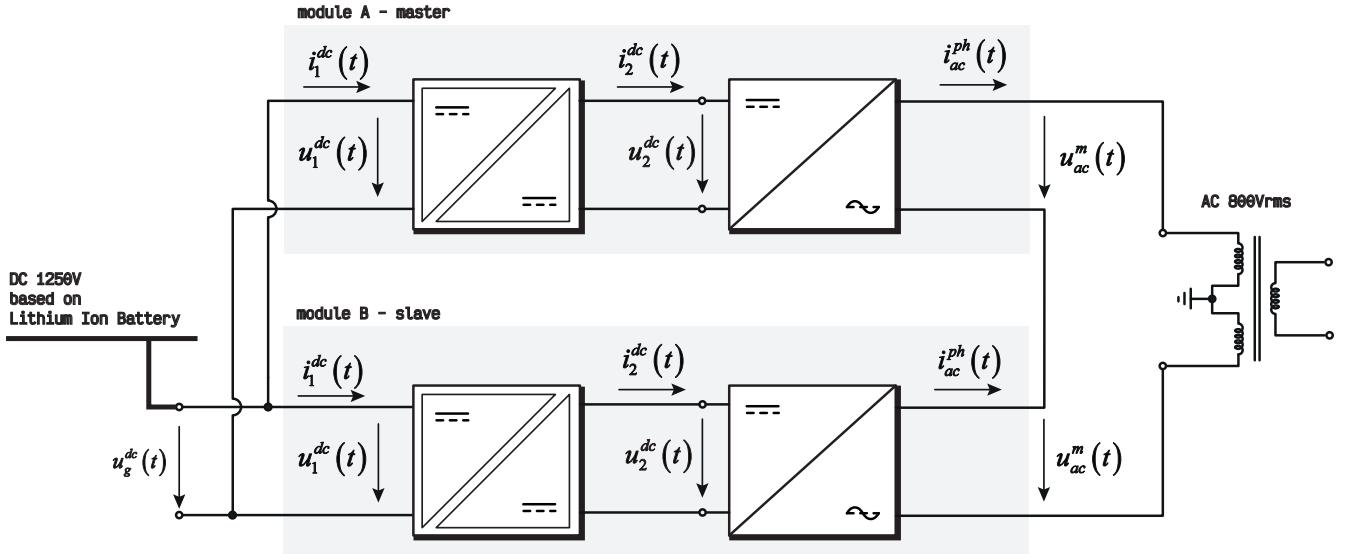


Figure 11: Simulation layout: simulation has been performance using a single phase SST composed by two single phase inverter connected in series with three difference case scenario of DCDC: three phase DAB, single phase DAB, and single phase CLLC.

4.1 SST based on Three Phase DAB and NPC Single Phase Inverter

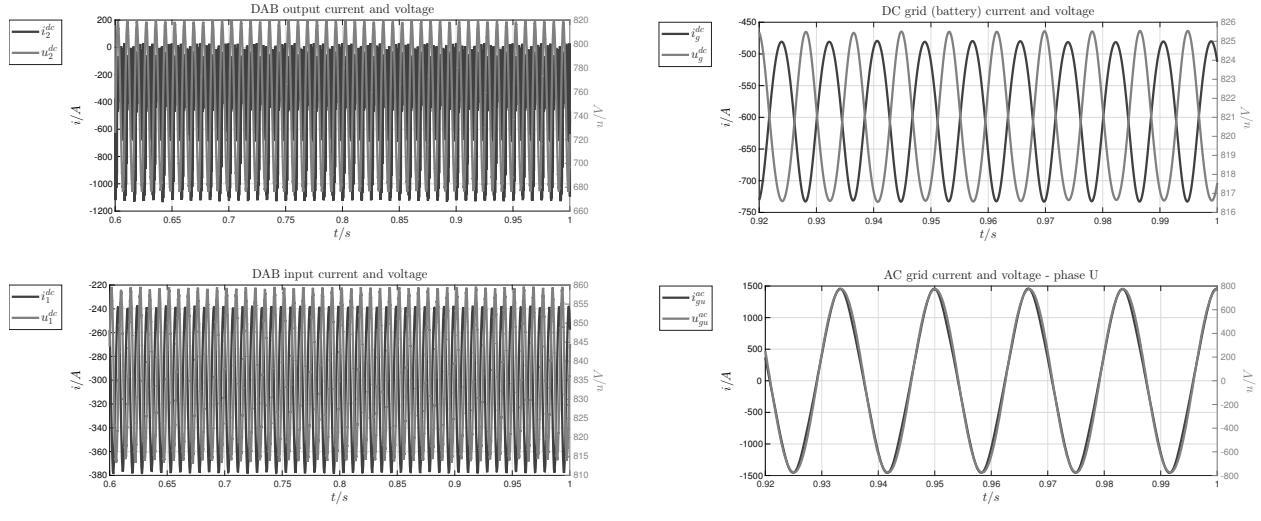
Here performance of the SST based on three phase DAB and a cascade of two three level NPC single phase inverters.

Remark - only one single phase has been simulated and total power at DC grid side is resulting in one third than in an equivalent three phase implementation.

Remark - simulations have been performed under the following condition of grids and load:

- DC grid nominal voltage (from Lithium Ion Battery) : $u_g^{dc}\Big|_{nom} = 1250 \text{ V}$;
- AC grid nominal voltage : $u_g^{ac}\Big|_{nom} = 800 \text{ V}$ - rms per phase-centertap;
- AC grid load current : $i_g^{ac} = 750 \text{ A}$ - rms;

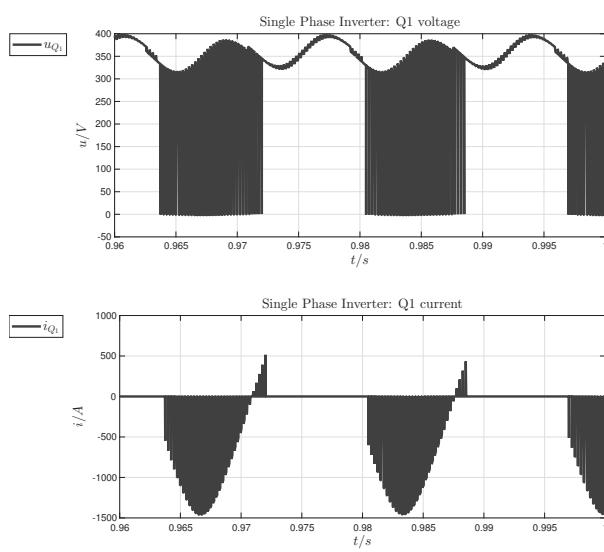
4 Simulation results



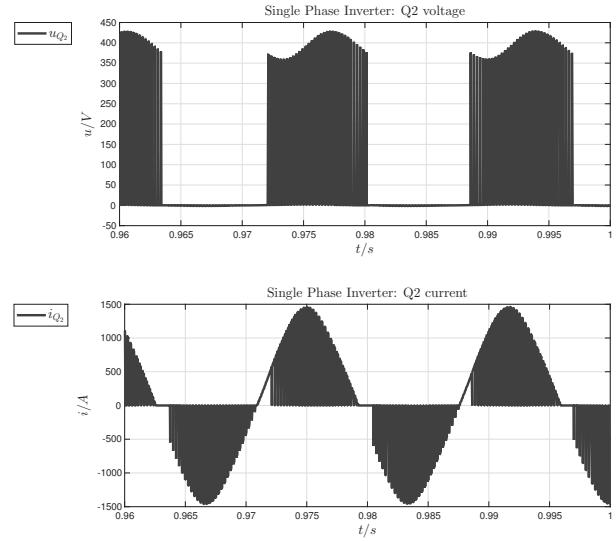
(a) Master three phase DAB input current and voltage (bottom) and outputs (top).

(b) DC grid current and voltage (top) and AC grid current and voltage (bottom).

Figure 12: Three phase DAB with NPC single phase inverter - performance of two stages single phase SST: three phase DAB input/output and grids.



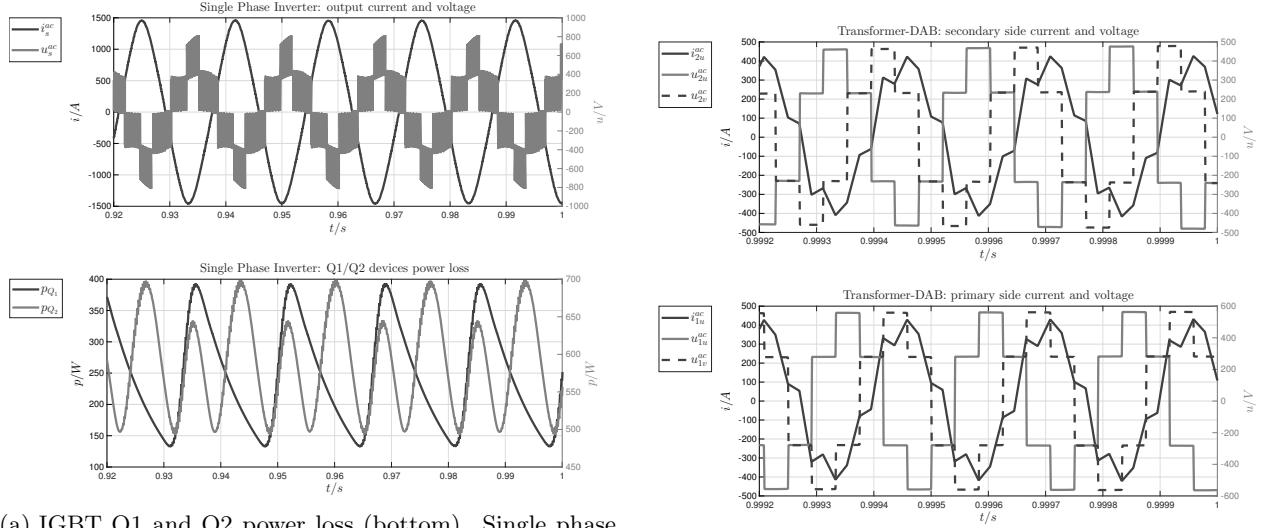
(a) Single phase inverter: Q1-IGBT voltage and current. The aim of this image is to proof the effective operative working of the three level NPC single phase inverter.



(b) Single phase inverter: Q2-IGBT voltage and current. The aim of this image is to proof the effective operative working of the three level NPC single phase inverter.

Figure 13: Three phase DAB with NPC single phase inverter - single phase inverter NPC: IGBTs voltage and current.

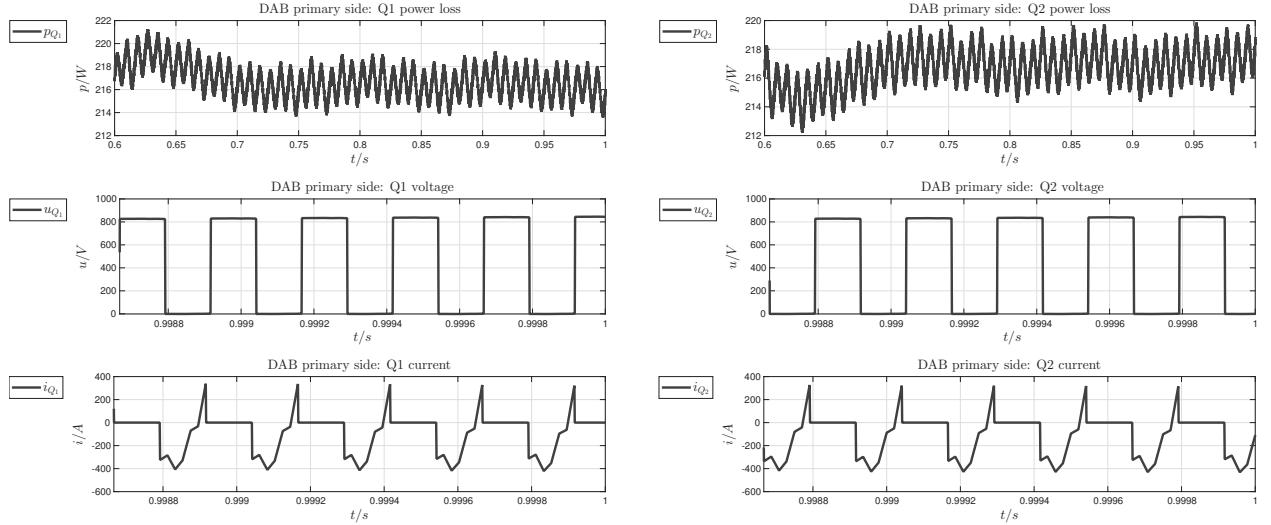
4 Simulation results



(a) IGBT Q1 and Q2 power loss (bottom). Single phase output current and voltage, before the output filter (top).

(b) Three phase DAB operative condition at nominal flow power.

Figure 14: Three phase DAB with NPC single phase inverter - single phase inverter and three phase DAB performances.

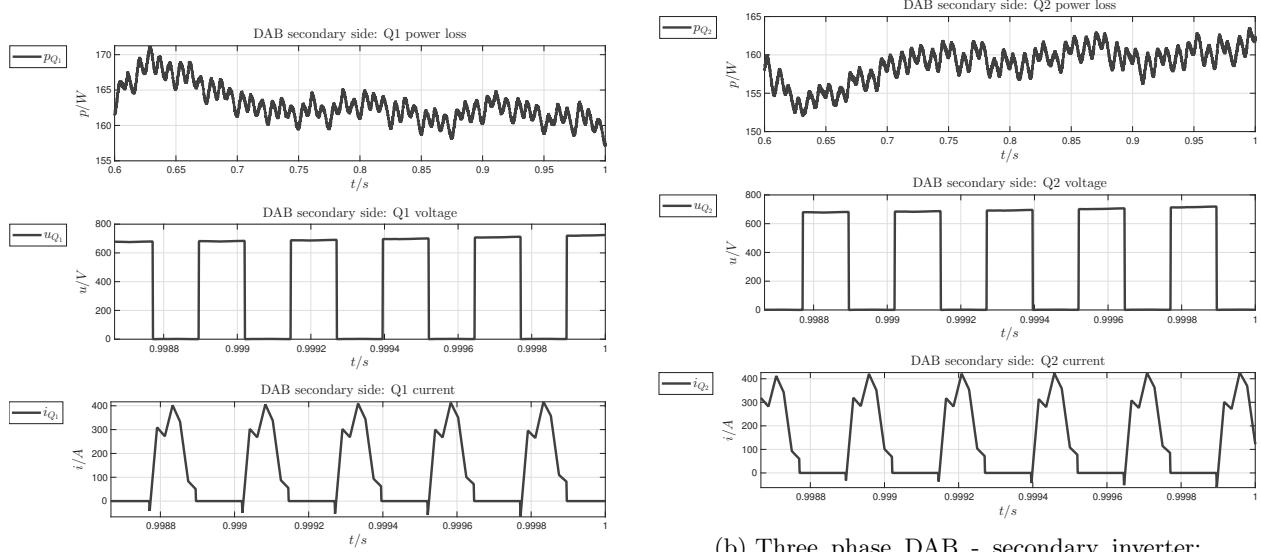


(a) Three phase DAB - primary inverter: Q1-MOSFET power loss, voltage and current.

(b) Three phase DAB - primary inverter: Q2-MOSFET power loss, voltage and current.

Figure 15: Three phase DAB with NPC single phase inverter - primary inverter devices performances.

4 Simulation results



(a) Three phase DAB - secondary inverter: Q1-MOSFET power loss, voltage and current.

(b) Three phase DAB - secondary inverter: Q2-MOSFET power loss, voltage and current.

Figure 16: Three phase DAB with NPC single phase inverter - secondary inverter devices performances.

4.2 SST based on Three Phase DAB and TNPC Single Phase Inverter

Here performance of the SST based on three phase DAB and a cascade of two three level NPC single phase inverters.

Remark - only one single phase has been simulated and total power at DC grid side is resulting in one third than in an equivalent three phase implementation.

Remark - simulations have been performed under the following condition of grids and load:

- DC grid nominal voltage (from Lithium Ion Battery) : $u_g^{dc} \Big|_{nom} = 800 \text{ V}$;
- AC grid nominal voltage : $u_g^{ac} \Big|_{nom} = 554 \text{ V}$ - rms per phase-centertap;
- AC grid load current : $i_g^{ac} = 1000 \text{ A}$ - rms;

4 Simulation results

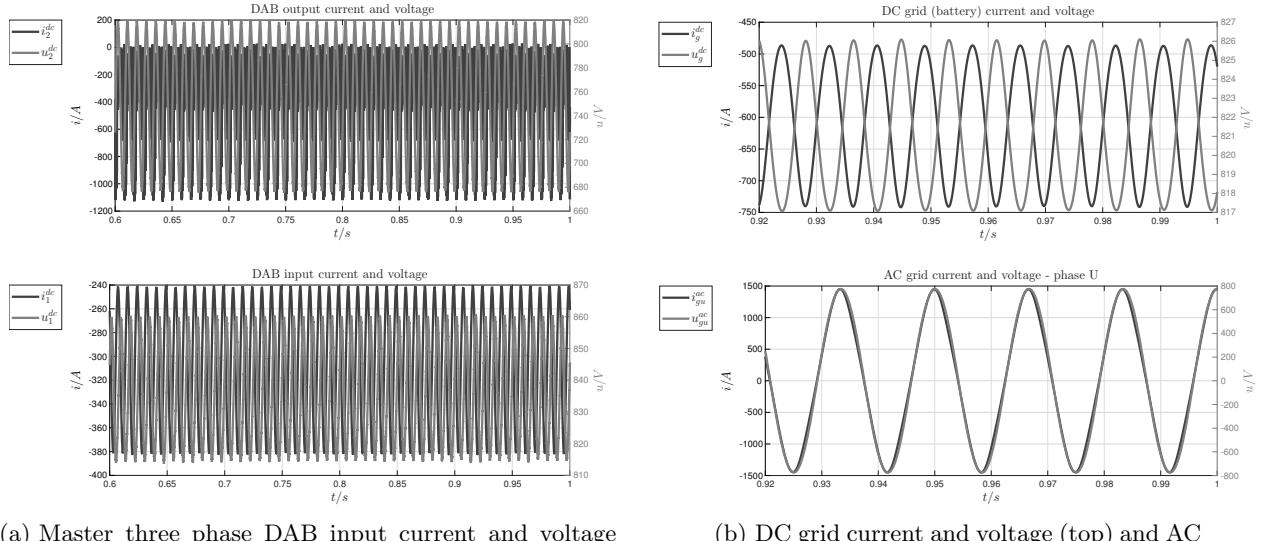


Figure 17: Three phase DAB with TNPC single phase inverter - performance of two stages single phase SST: three phase DAB input/output and grids.

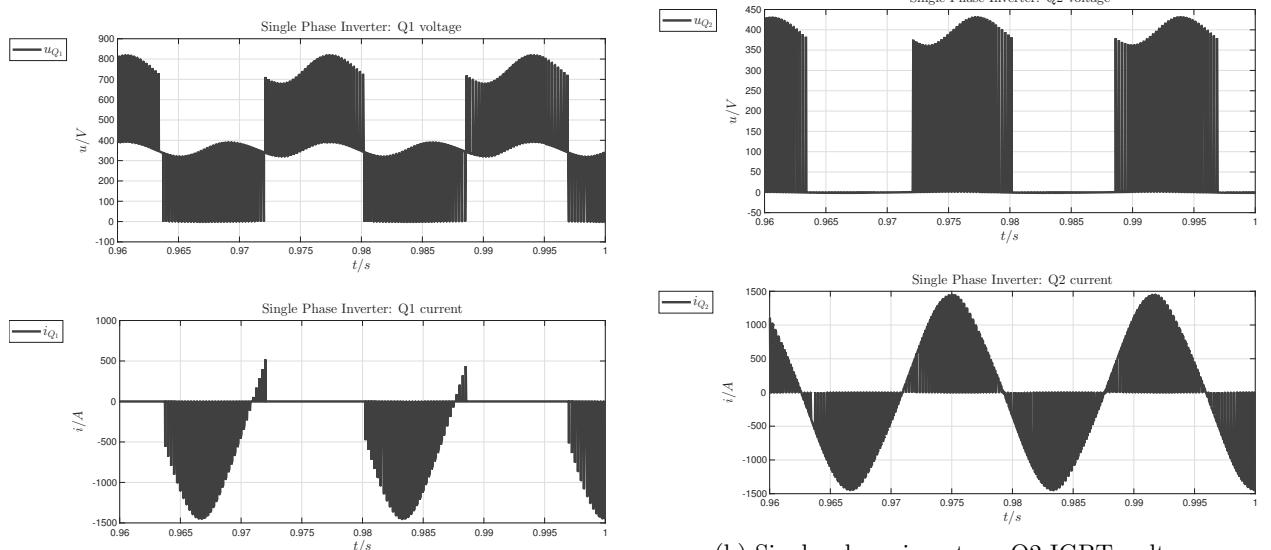
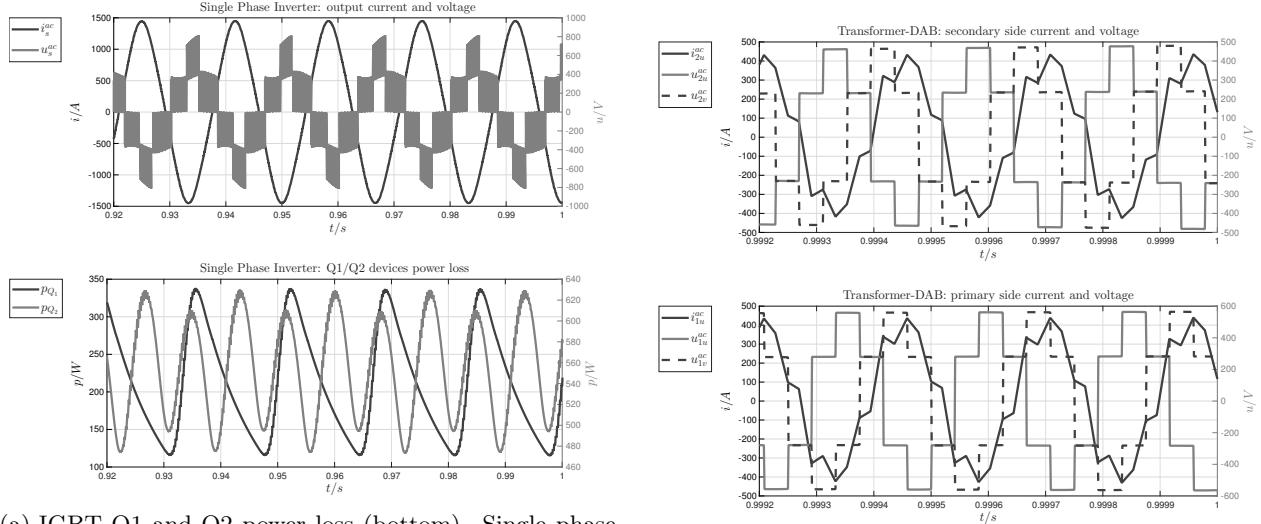


Figure 18: Three phase DAB with TNPC single phase inverter - single phase inverter TNPC: IGBTs voltage and current.

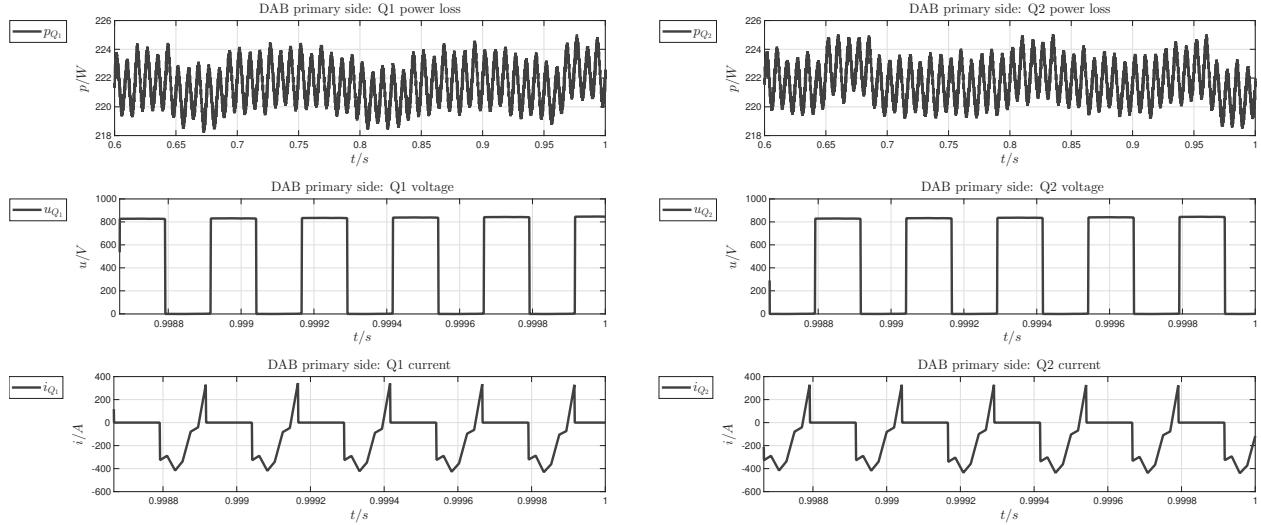
4 Simulation results



(a) IGBT Q1 and Q2 power loss (bottom). Single phase output current and voltage, before the output filter (top).

(b) Three phase DAB operative condition at nominal flow power.

Figure 19: Three phase DAB with TNPC single phase inverter - single phase inverter and three phase DAB performances.

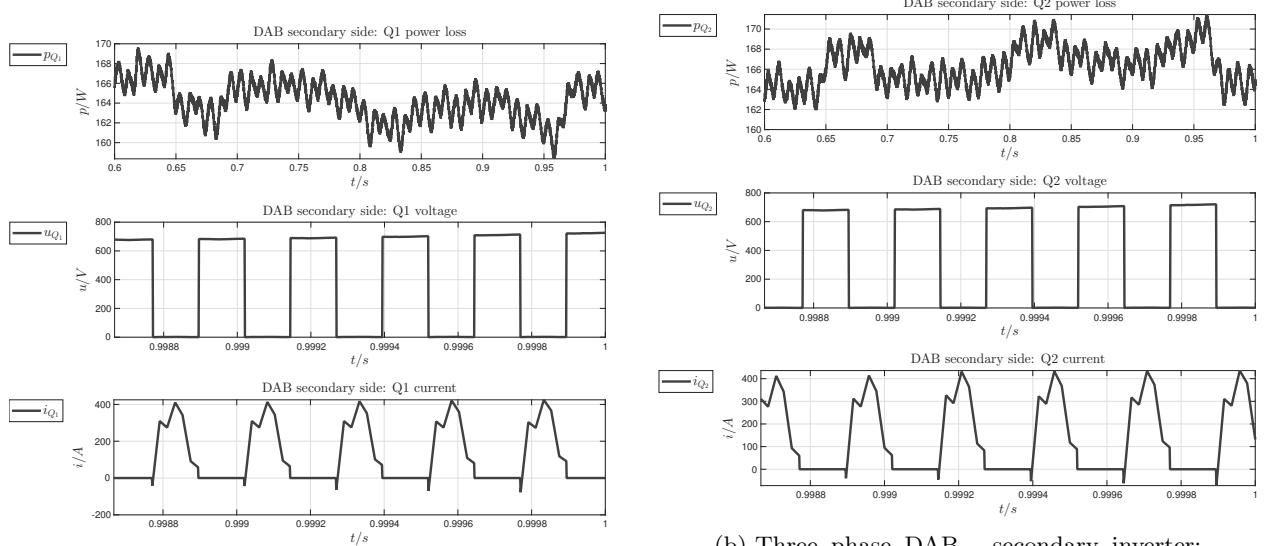


(a) Three phase DAB - primary inverter: Q1-MOSFET power loss, voltage and current.

(b) Three phase DAB - primary inverter: Q2-MOSFET power loss, voltage and current.

Figure 20: Three phase DAB with TNPC single phase inverter - primary inverter devices performances.

4 Simulation results



(a) Three phase DAB - secondary inverter: Q1-MOSFET power loss, voltage and current.

(b) Three phase DAB - secondary inverter: Q2-MOSFET power loss, voltage and current.

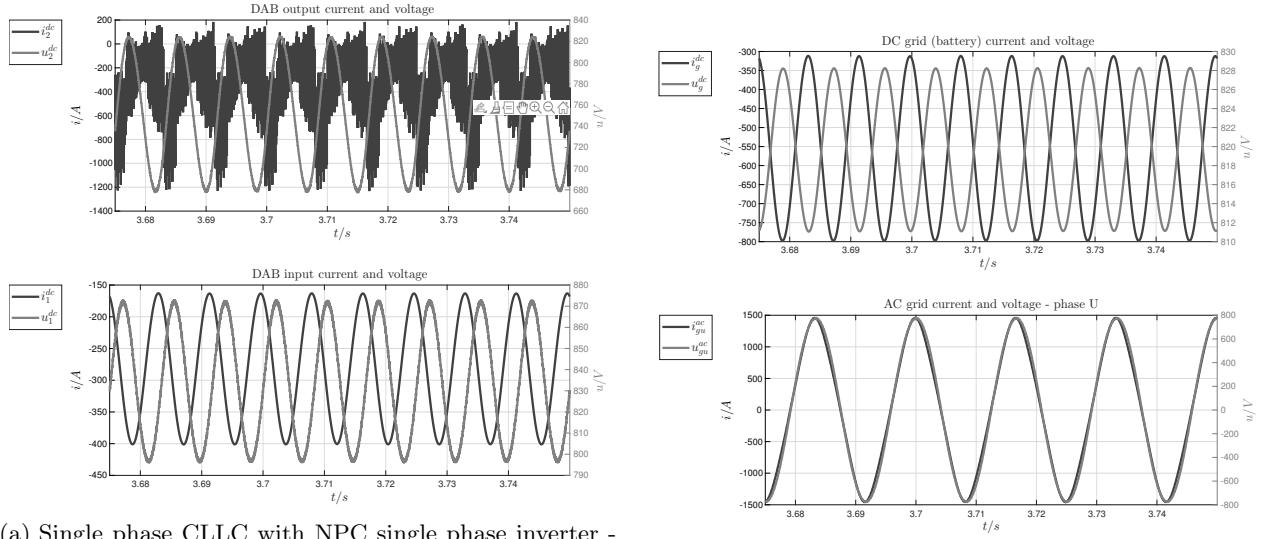
Figure 21: Three phase DAB with TNPC single phase inverter - secondary inverter devices performances.

4.3 SST based on Single Phase CLLC and NPC Single Phase Inverter

In this section the performance of the CLLC has been investigated. The control strategy of the CLLC DCDC converter has been assumed as follows

- single phase CLLC is operating at constant frequency of $f_{llc} = 9600$ Hz;
- power flow direction as well as amplitude is controlled by phase shift between primary and secondary side H-bridges;
- the above control law keep the CLLC conversion in a constant condition of zero current switching;

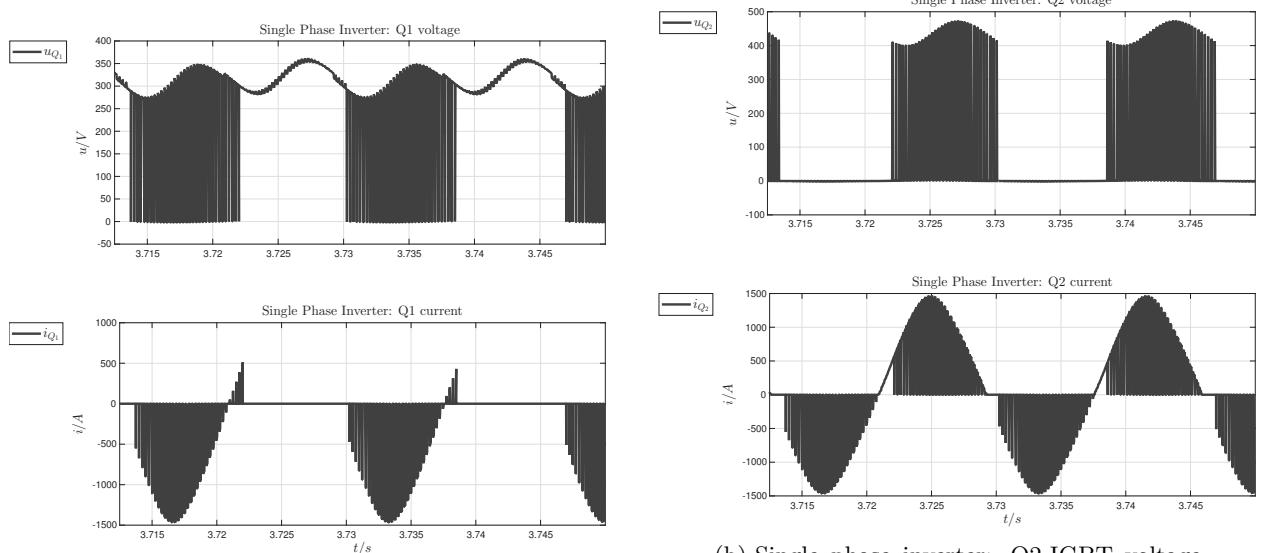
4 Simulation results



(a) Single phase CLLC with NPC single phase inverter - Master single phase CLLC input current and voltage (bottom) and outputs (top).

(b) DC grid current and voltage (top) and AC grid current and voltage (bottom).

Figure 22: Single phase CLLC with NPC single phase inverter - performance of two stages single phase SST: single phase CLLC input/output and grids.

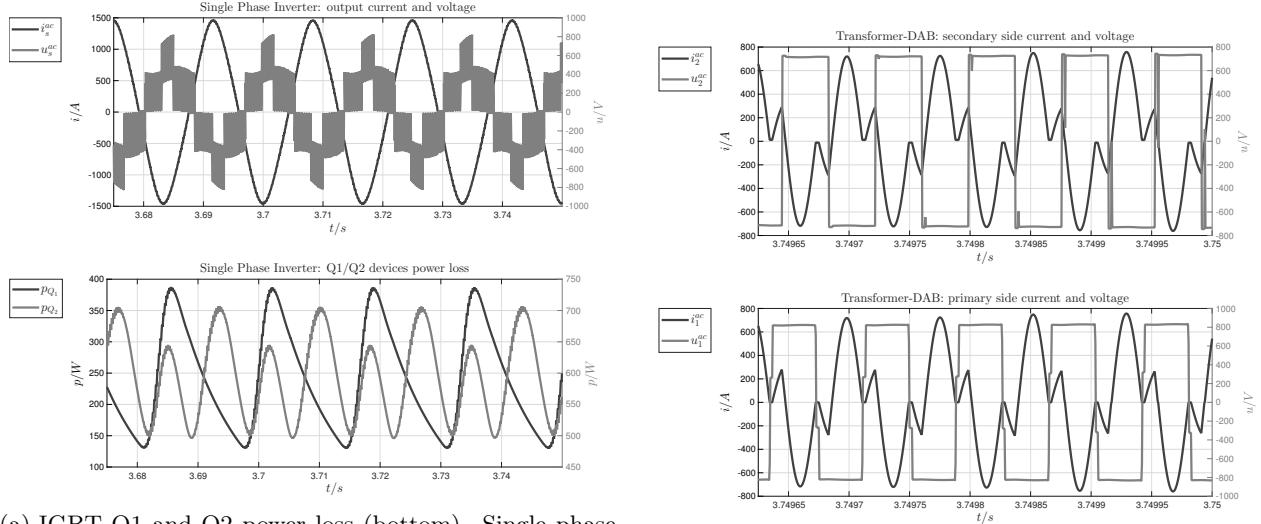


(a) Single phase inverter: Q1-IGBT voltage and current. The aim of this image is to proof the effective operative working of the three level NPC single phase inverter.

(b) Single phase inverter: Q2-IGBT voltage and current. The aim of this image is to proof the effective operative working of the three level NPC single phase inverter.

Figure 23: Single phase CLLC with NPC single phase inverter - single phase inverter NPC: IGBTs voltage and current.

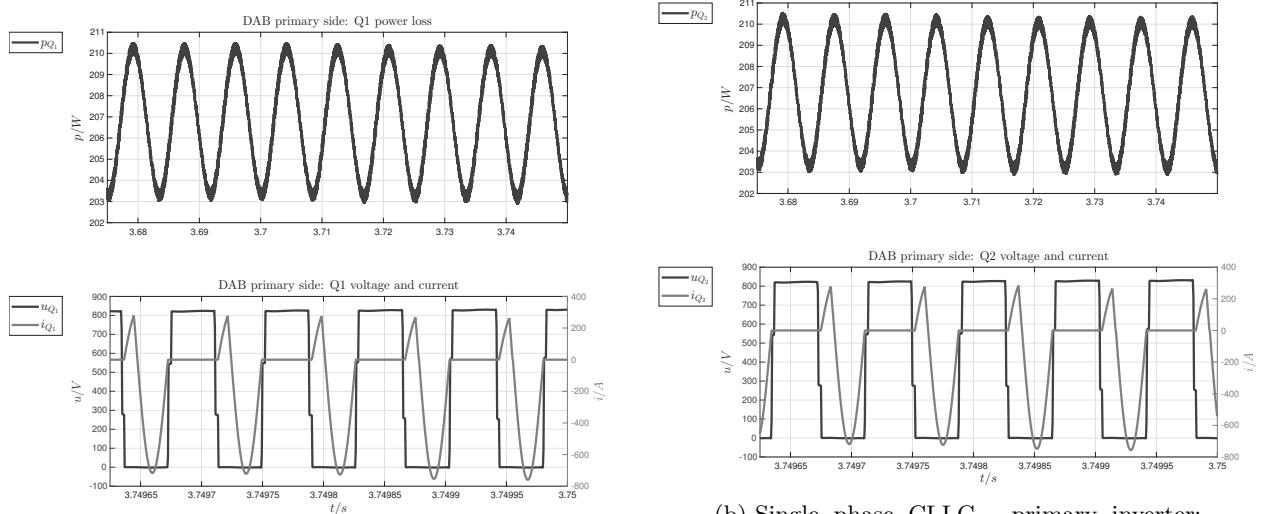
4 Simulation results



(a) IGBT Q1 and Q2 power loss (bottom). Single phase output current and voltage, before the output filter (top).

(b) Single phase CLLC operative condition at nominal flow power.

Figure 24: Single phase CLLC with NPC single phase inverter - single phase inverter and single phase CLLC performances.

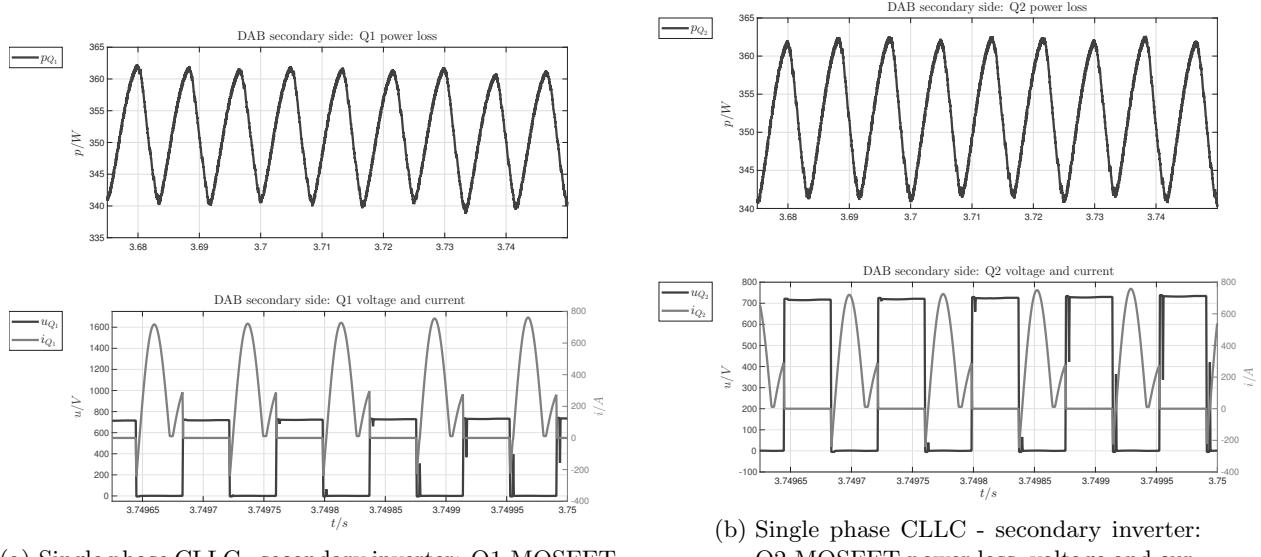


(a) Single phase CLLC - primary inverter: Q1-MOSFET power loss, voltage and current.

(b) Single phase CLLC - primary inverter: Q2-MOSFET power loss, voltage and current.

Figure 25: Single phase CLLC with NPC single phase inverter - primary inverter devices performances.

4 Simulation results



(b) Single phase CLLC - secondary inverter: Q2-MOSFET power loss, voltage and current.

Figure 26: Single phase CLLC with NPC single phase inverter - secondary inverter devices performances.

4.4 SST based on Single Phase DAB and NPC Single Phase Inverter

Single phase DAB performance.

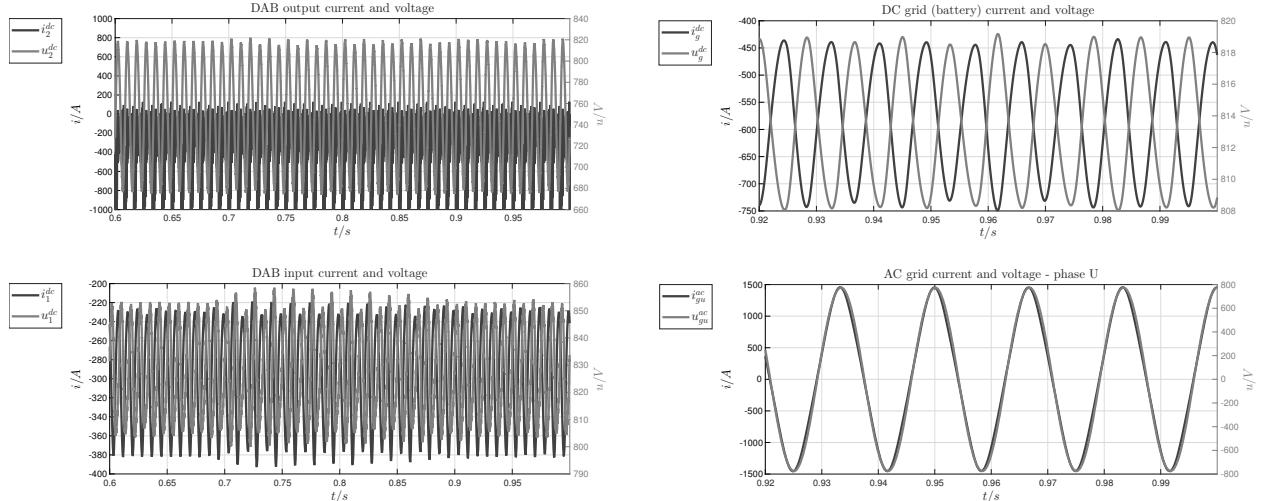
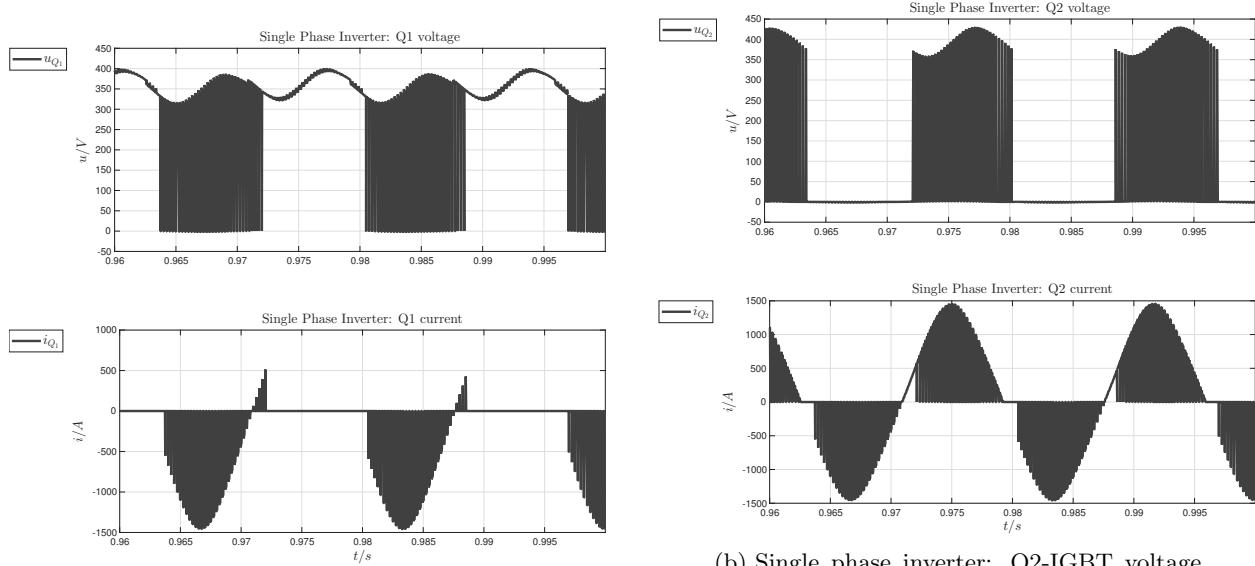


Figure 27: Single phase DAB with NPC single phase inverter - performance of two stages single phase SST: single phase DAB input/output and grids.

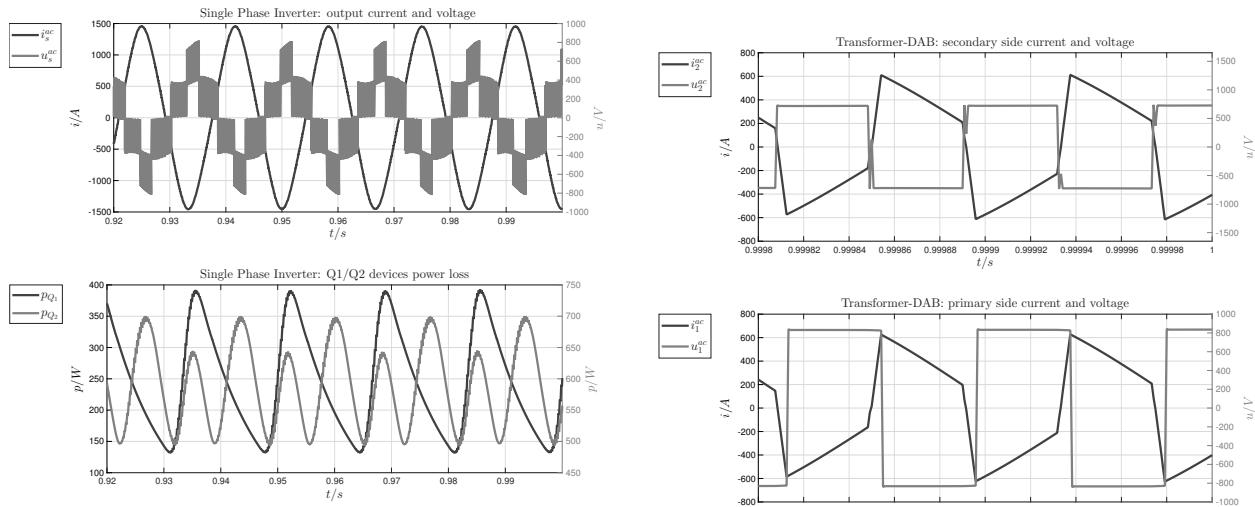
4 Simulation results



(a) Single phase inverter: Q1-IGBT voltage and current. The aim of this image is to proof the effective operative working of the three level NPC single phase inverter.

(b) Single phase inverter: Q2-IGBT voltage and current. The aim of this image is to proof the effective operative working of the three level NPC single phase inverter.

Figure 28: Single phase DAB with NPC single phase inverter - single phase inverter NPC: IGBTs voltage and current.



(a) IGBT Q1 and Q2 power loss (bottom). Single phase output current and voltage, before the output filter (top).

(b) Single phase DAB operative condition at nominal flow power.

Figure 29: Single phase DAB with NPC single phase inverter - single phase inverter and single phase DAB performances.

5 Summary of simulation results

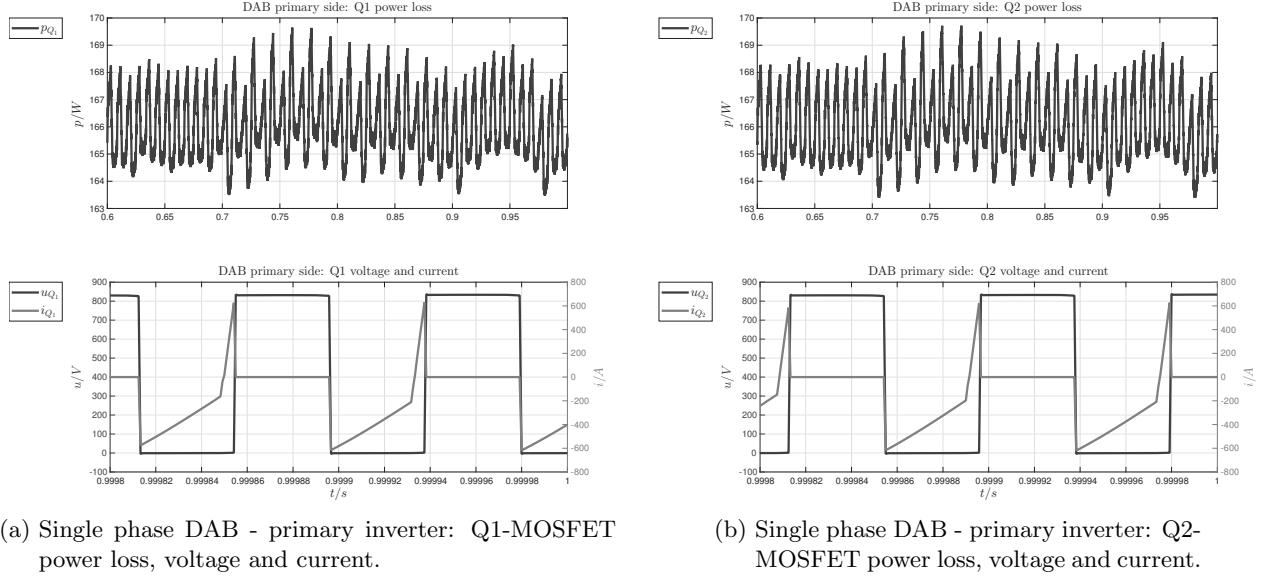


Figure 30: Single phase DAB with NPC single phase inverter - primary inverter devices performances.

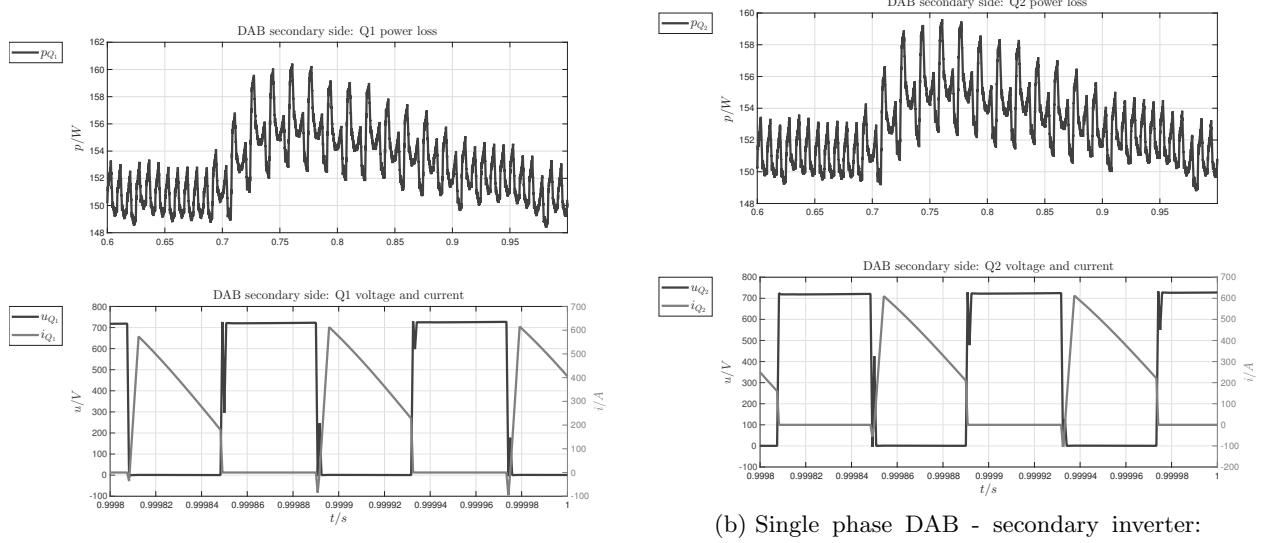


Figure 31: Single phase DAB with NPC single phase inverter - secondary inverter devices performances.

5 Summary of simulation results

In this section a summary of overall efficiency for: three phase DAB, single phase DAB, single phase CLLC is shown.

The power flow through each DC/DC/AC converter is around 250 kW, in Table 1 the total power loss concerning the semiconductors components are reported. Power loss concerning capacitors and inductors gave been not accounted at this stage.

Remark - TNPC single phase inverter will taken into account.

Table 1: Comparison of power loss for three different DC/DC architecture.

Architecture	f_{dab} [kHz]	f_{inv} [kHz]	p_{loss}^{dab} [kW]	p_{loss}^{inv} [kW]
Three phase DAB	4 kHz	4 kHz	2.27 kW	3.0 kW
Single phase CLLC	13 kHz	4 kHz	2.25 kW	3.0 kW
Single phase DAB	12 kHz	4 kHz	1.28 kW	3.0 kW

From Table 1 all solution seems promising until ZVS for single phase DAB or ZCS for CLLC are satisfied. Impact into magnetic has to be investigated.

In the following additional information are reported.

Table 2: DC/DC transformers rms main quantities.

Architecture	f_{dab} [Hz]	i_1 [A _{rms}]	i_2 [A _{rms}]	u_1 [V _{rms}]	u_2 [V _{rms}]	L_s [H]
Single phase DAB	12 kHz	375 A	375 A	830 V	752 V	11 µH
Three phase DAB	4 kHz	265 A	265 A	400 V	360 V	28 µH
Single phase CLLC	13 kHz	452 A	452 A	815 V	745 V	13 µH

Remark - in Table 2 voltages for the three phase DAB represent the *per phase* voltage and not the phase to phase, on the other hand voltages for the CLLC and single phase DAB architecture represent the voltage across the single phase transformer.

Remark - L_s accounts also the leakage inductance of the transformer.

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