Solid State Transformers:

architecture, control and simulation results.

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This document presents a preliminary analysis of Solid State Transformers (SSTs), aiming to provide a comprehensive introduction to the technology. The study proposes some potential layouts for hardware architectures and control strategies, supported by Simscape modeling and simulation results. Furthermore, the document evaluates the capabilities of the Simscape models implemented for this investigation.

1 Introduction

Solid State Transformers (SSTs) are advanced power electronic devices designed to replace traditional low-frequency transformers in modern power distribution systems. By operating at high frequency and using fully controllable conversion stages, SSTs achieve a more compact size, improved energy efficiency, and enhanced functionality compared to conventional transformers. Beyond simple voltage transformation, they provide additional services such as bidirectional power flow, voltage and reactive power regulation, and seamless integration of distributed energy resources including renewables, electric vehicles, and energy storage.

A key difference from traditional transformers is the behavior of SSTs during fault conditions. Due to their electronic nature and active current limiting, SSTs inherently restrict short-circuit currents. This prevents downstream systems from relying on conventional overcurrent-based protection schemes, which depend on high fault currents for detection. As a result, new protection strategies based on advanced sensing, high-speed control, and intelligent fault identification must be implemented. This shift in protection philosophy presents both challenges and significant opportunities for the development of more flexible, reliable, and smart power networks.

2 Global Architecture

In this chapter few general architectures for SST solutions are proposed and investigated; the SST device is intended to operate between two different grids:

- a low voltage DC grid source where many contributors can be assumed are connected e.g. energy storage, photovoltaic installations, car chargers and others;
- a three phase medium voltage AC grid source;

Figure 1 shows a single phase architecture, which basically consists by a cascade of single phase inverters, where each single phase inverter is supplied by a galvanically isolated DC/DC converter. Each single phase inverter which constitute a single are all connected in series to achieve the selected AC medium voltage; on the other hand all DC/DC input stage are connected in parallel.
Remark - to reduce the stress in term of voltage isolation, the HV/MV transformer could be built in a way to equally distribute the phase to grand voltage, as shown in Figure 1.
Remark - from control point of view the following layout can be assumed:

- DC/DC power supply control is monolithic and atomic;
- three phase active front end (AFE) control architecture can be assumed as follows

– master/slave configuration: for each phase one single phase inverter will be identified as *master* while *slave* the others;

– each single phase inverter is equipped by a single phase PLL (both *master* and *slaves*);

– an inverter current control (running on *master*);

– a voltage controlled source mode (on *slaves*).

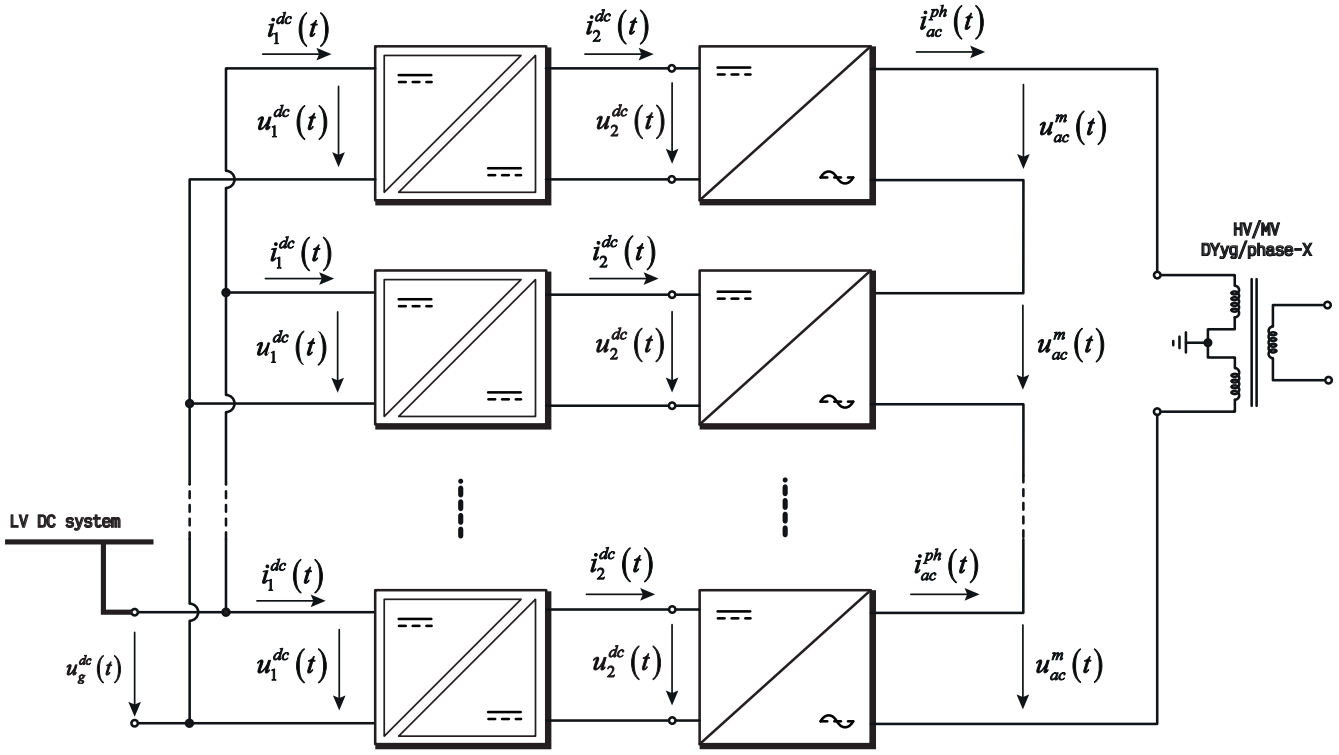


Figure 1: Single phase architecture based on galvanically isolated single phase inverter cascade.

Figure 2 shows a case scenario of global three phase architecture with a common communication bus which performs a global distributed control.

Remark - a deterministic, Ethernet based, bus controller plays a fundamental role in the *concerto* of the overall system.

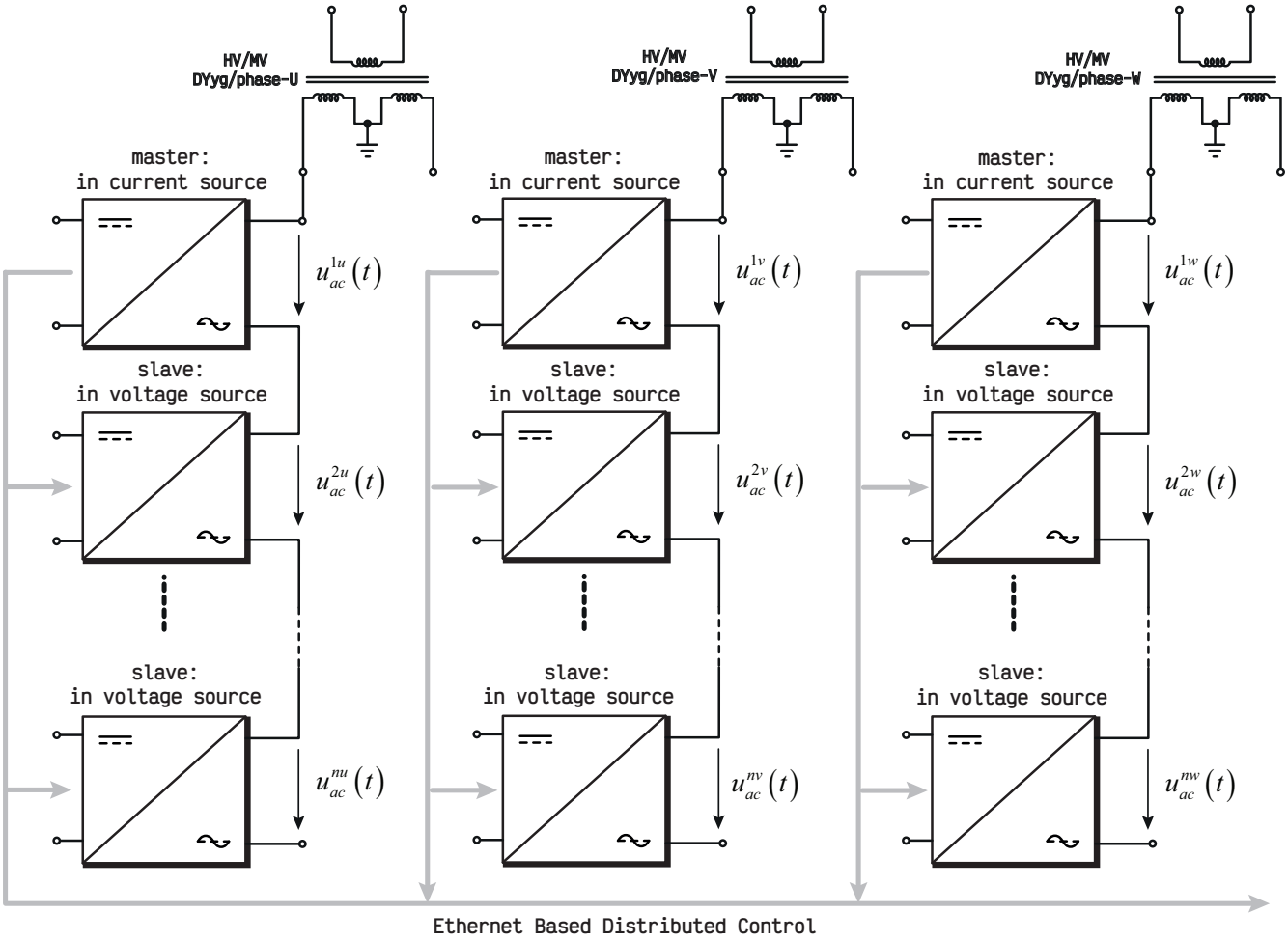


Figure 2: Global architecture for three phase system where a cascade of master/slaves single phase inverter implements the the single phase MV.

As already mentioned, the aim of this work is to evaluate the performance of different architecture and compare them. For this purpose, single phase inverter will be investigate both by a three levels NPC and three levels T-type as shown in Figure 3 and Figure 4. NPC solution permits to use lower voltage rated IGBT components while T-type will result in a more efficient conversion.
Remark - DC-voltage rate is assumed at $U_{dc}^{\text{nom}} 800\,\text{V}$.

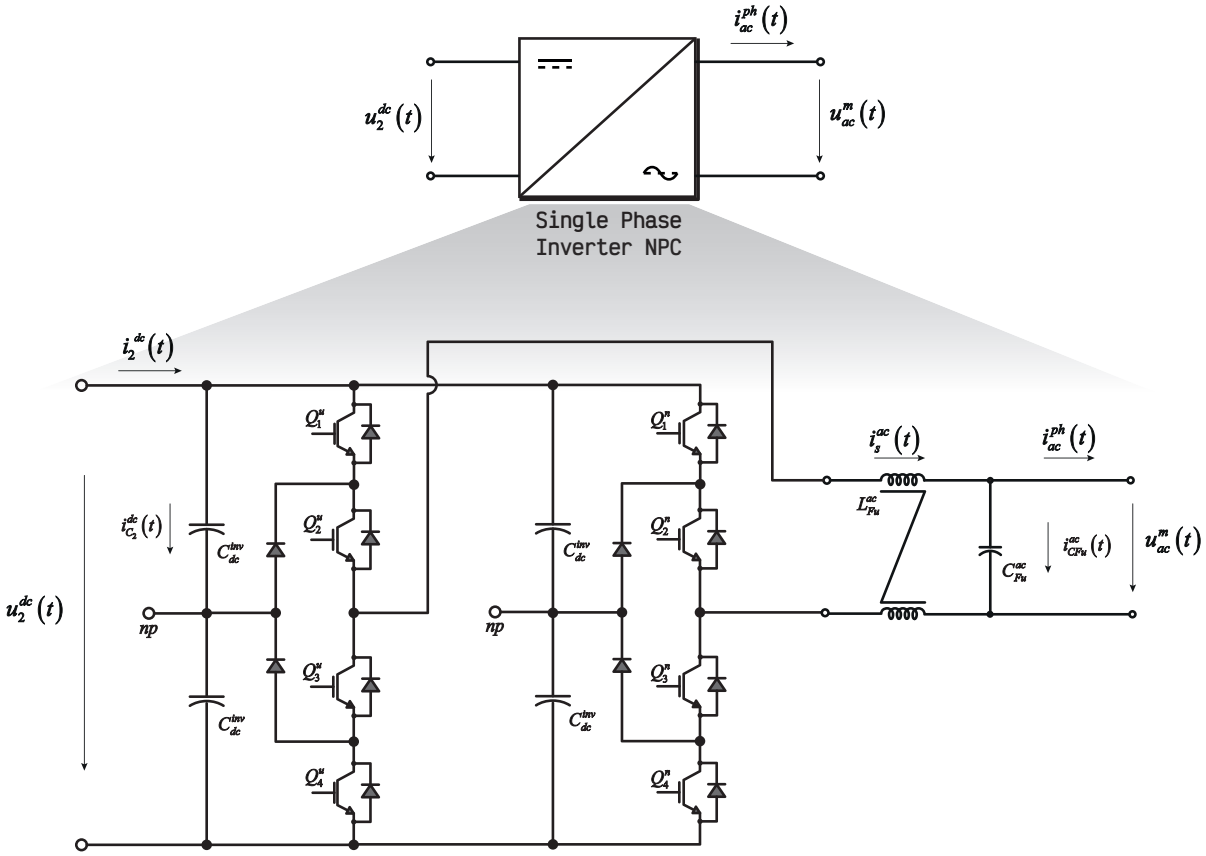


Figure 3: Single phase inverter stage: based on three level NPC.

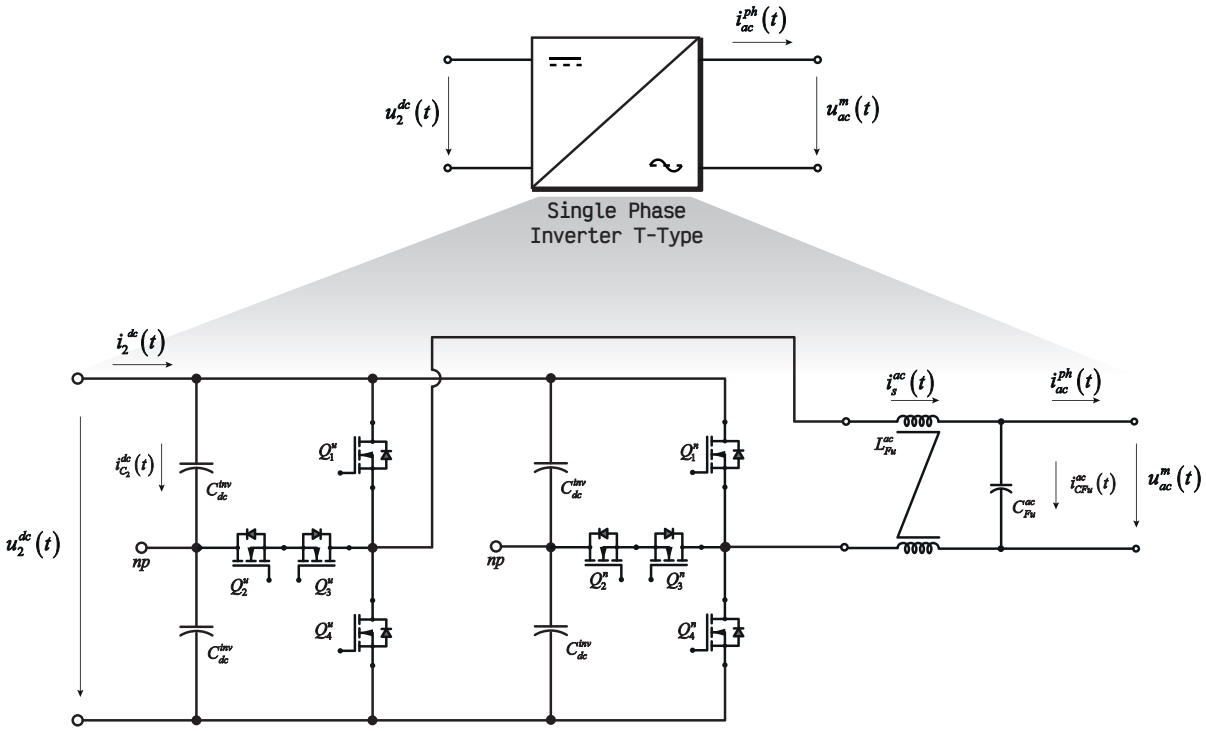


Figure 4: Single phase inverter stage: based on three level T-type.

Remark - concerning the galvanically isolated DC/DC converters the following architecture will be investigated:

- three phase DAB;
- single phase bidirectional CLLC;
- single phase DAB;

Remark - three phase DAB could have a better behaviour in terms of DC-current controllability, even if the topic will be more further investigated.

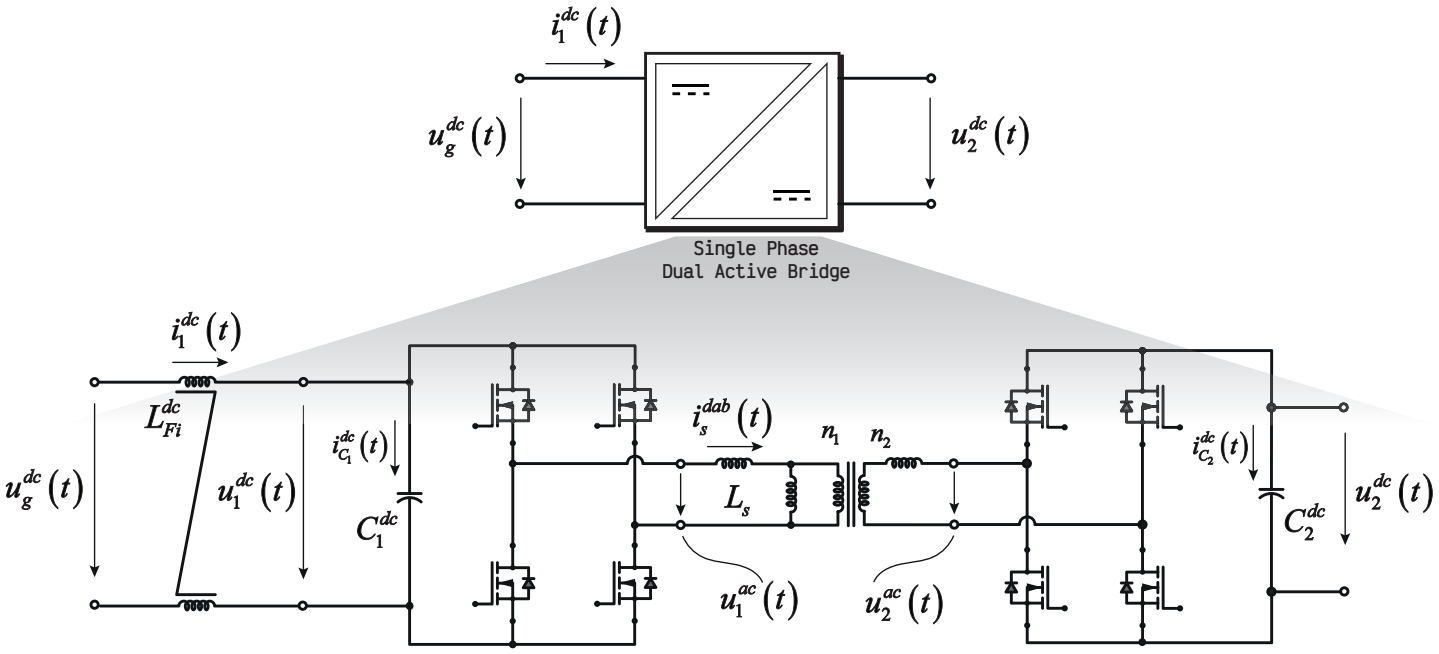


Figure 5: Single phase DAB.

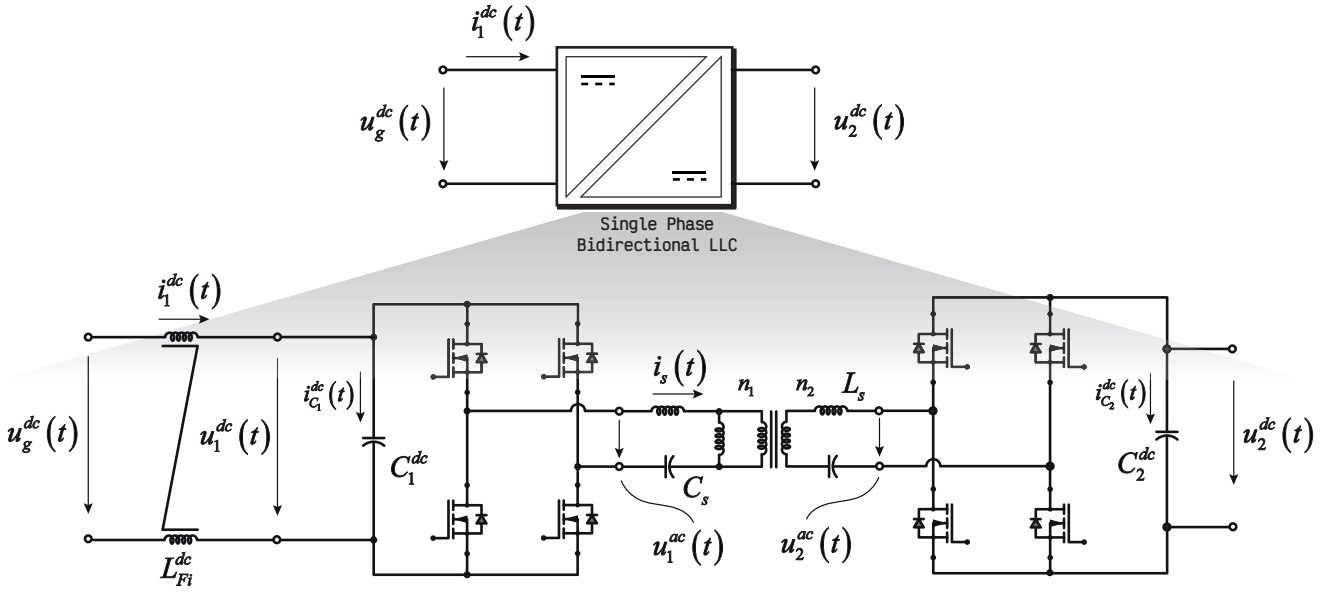


Figure 6: Single phase bidirectional CLLC.

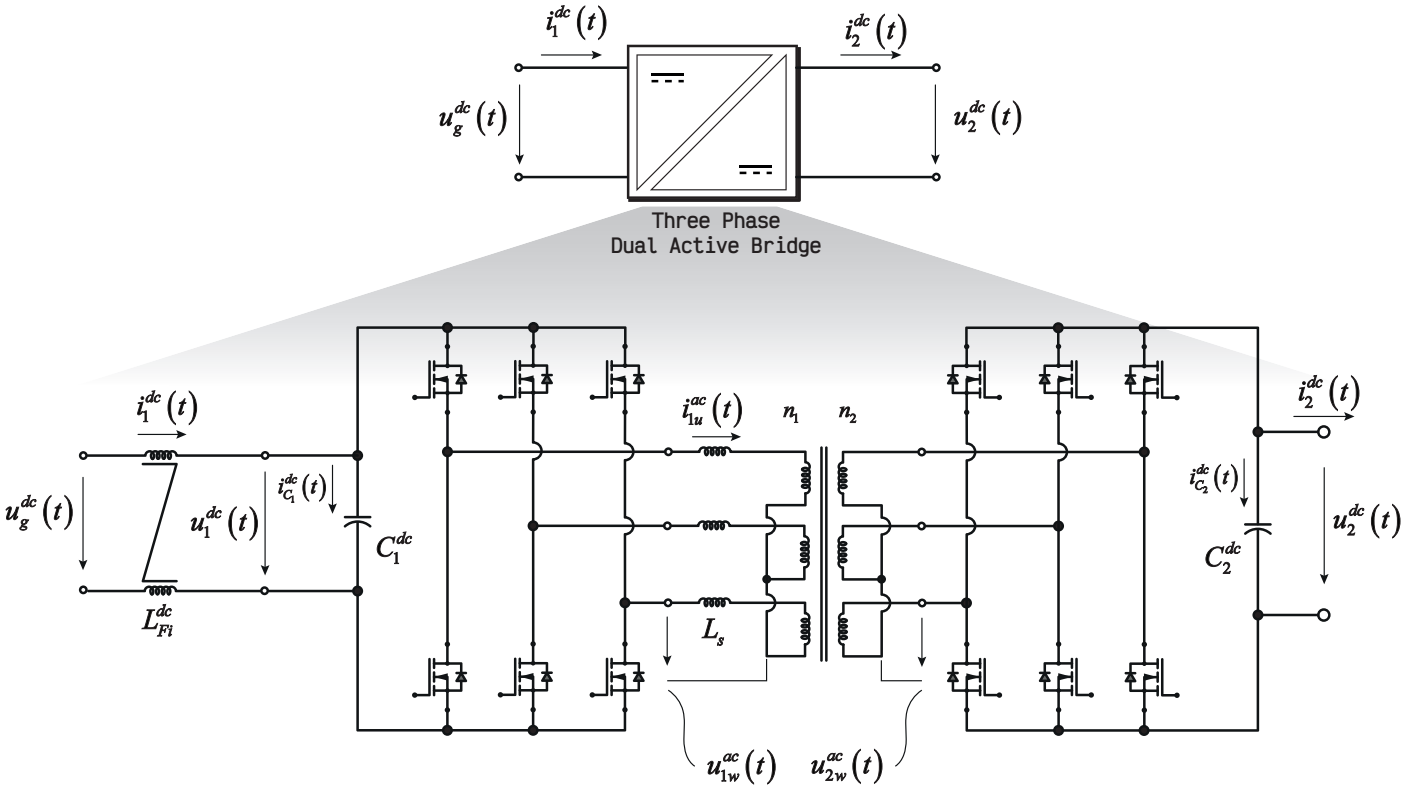


Figure 7: Three phase DAB.

3 Control Architecture

The main goal for an SST architecture should be, on one side, to keep stable a DC-grid composted by many *producers/consumers*, and to give an additional stability contribution to the AC-grid vy proper absorbing/generating both reactive as well as active power (assuming DC-grid is integrated by energy storage systems).

Diving into the inner SST control architecture, it is assumed that each DC/DC converter provides a controlled (stable at a given value) DClink voltage, $u_2^{dc}(t) = u_2^{dc}\Big|_{ref}$, while the single phase inverter will drive a current to the AC-grid according to an outer control level*, as shown in Figure 8 shows a possible control principle.

*The outer control loop here intended concerns a global strategy which unified the stability of the DC-grid as well as the stability of the AC-grid according to, e.g. an optimal control based strategy.

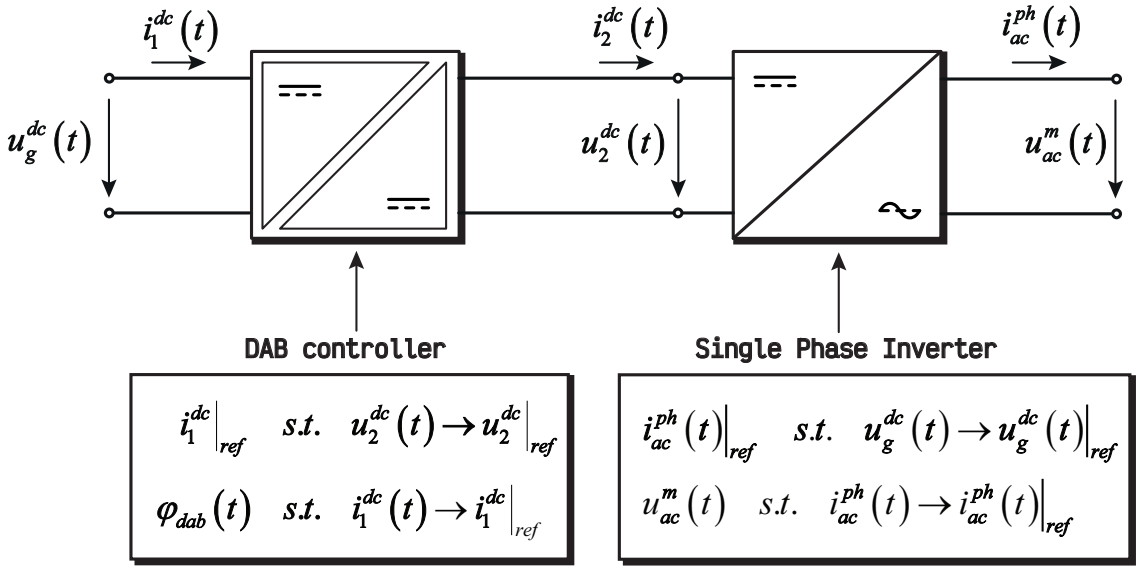


Figure 8: Fundamental control strategies of the isolated single phase inverter.

3.1 DC/DC Control Loops

DC/DC control is basically constructed by a cascade of PI-control with an outer voltage loop control followed by an inner current control loop;
Remark - ZVS condition, for the single phase DAB, is achieved with a dead-time of $t_{dt} = 400\,\text{ns}$.
Remark - ZVC condition, for the CLLC, is achieved forcing DCM.

3.2 Single Phase Lock Loop

Single phase inverter uses a single phase lock loop as shown in Figure 9

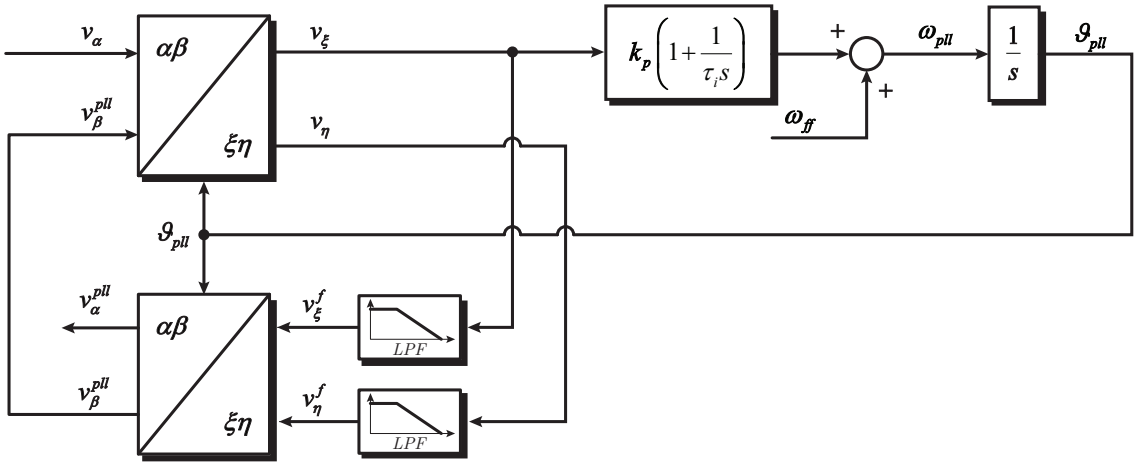


Figure 9: Single phase lock loop for grid phase estimation.

3.3 Single Phase Inverter Control Layouts

Single phase inverter has been simulated with resonant PI as well as with virtual vector control as shown in Figure 10

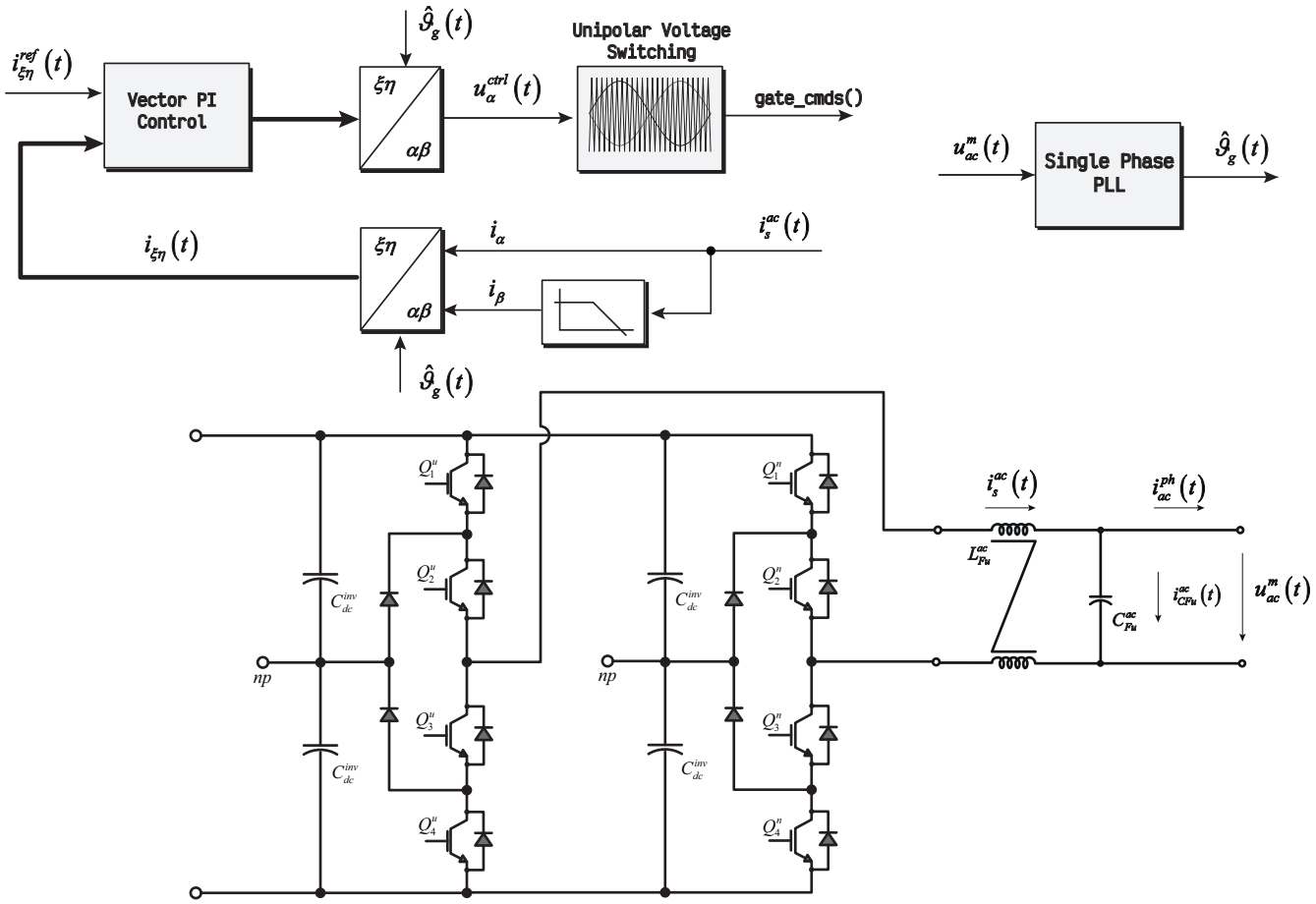


Figure 10: Control layout of the single phase inverter.
Same strategy for T-Type.

4 Simulation results

In this section simulation results of the architecture based on three phase DAB is shown, in particular the following operative conditions have been accounted:

- three phase DAB works at fundamental frequency of $f_{dab} = 4\,\text{kHz}$;
- single phase CLLC works at fundamental frequency of $f_{llc} = 13\,\text{kHz}$;
- single phase DAB works at fundamental frequency of $f_{spdab} = 12\,\text{kHz}$;
- single phase inverter operates at the switching frequency of $f_{inv}^{pwm} = 4\,\text{kHz}$, both NPC and T-Type.

Remark - the following switching devices have been used selected

- Wolfspeed **CAB450M12XM3** for the three phase DAB;
- Wolfspeed **CAB760M12HM3** for the single phase DAB and CLLC;
- Wolfspeed **CAB760M12HM3** for the NPC (the number of paralleled device is two);
- Wolfspeed **CAB760M12HM3** + **CLB800M12HM3P** for the T-Tpype (the number of paralleled device is two);

According to Figure 6 and Figure 3, the following components shall be accounted:

- $L_{Fi}^{dc} = 400\,\mu\text{H}$ - input DAB inductance with nominal current of $I_{LFu}^{nom} = 325\,\text{A}$;
- $C_1^{dc} = 3.6\,\text{mF}$ - input DAB capacitor with nominal voltage of $U_{dc1}^{nom} = 800\,\text{V}$;
- $C_2^{dc} = 3.6\,\text{mF}$ - output DAB capacitor with nominal voltage of $U_{dc2}^{nom} = 800\,\text{V}$;
- $C_{dc}^{inv} = 3.6\,\text{mF}$ - single phase DClink capacitor, with nominal voltage of $U_{dc}^{nom} = 400\,\text{V}$;
- $L_{Fu}^{ac} = 300\,\mu\text{H}$ - output single phase inverter inductance with nominal current $I_{LFu}^{nom} = 1000\,\text{A}$;
- $C_{Fu}^{ac} = 360\,\mu\text{H}$ - output single phase inverter capacitor with nominal voltage of $U_{CFu}^{nom} = 270\,\text{V}$;
- $L_s = 28\,\mu\text{H}$ - three phase DAB inductance (this value takes into account also the leakage inductance of the transformer) with nominal current of $I_{Ls}^{nom} = 250\,\text{A}$ at nominal frequency of $f_{Ls}^{nom} = 4\,\text{kHz}$;
- $L_s = 11\,\mu\text{H}$ - single phase DAB inductance (this value takes into account also the leakage inductance of the transformer) with nominal current of $I_{Ls}^{nom} = 400\,\text{A}$ at nominal frequency of $f_{Ls}^{nom} = 12\,\text{kHz}$;
- $L_s = 13\,\mu\text{H}$ - single phase CLLC inductance (this value takes into account also the leakage inductance of the transformer) with nominal current of $I_{Ls}^{nom} = 450\,\text{A}$ at nominal frequency of $f_{Ls}^{nom} = 13\,\text{kHz}$;
- $C_{s1} = C_{s2} = 10\,\mu\text{F}$ - single phase CLLC resonant capacitor ($f_{res} = 20\,\text{kHz}$) with nominal current of $I_{Cs}^{nom} = 450\,\text{A}$;

Figure 10 show the control architecture of the single phase inverter.

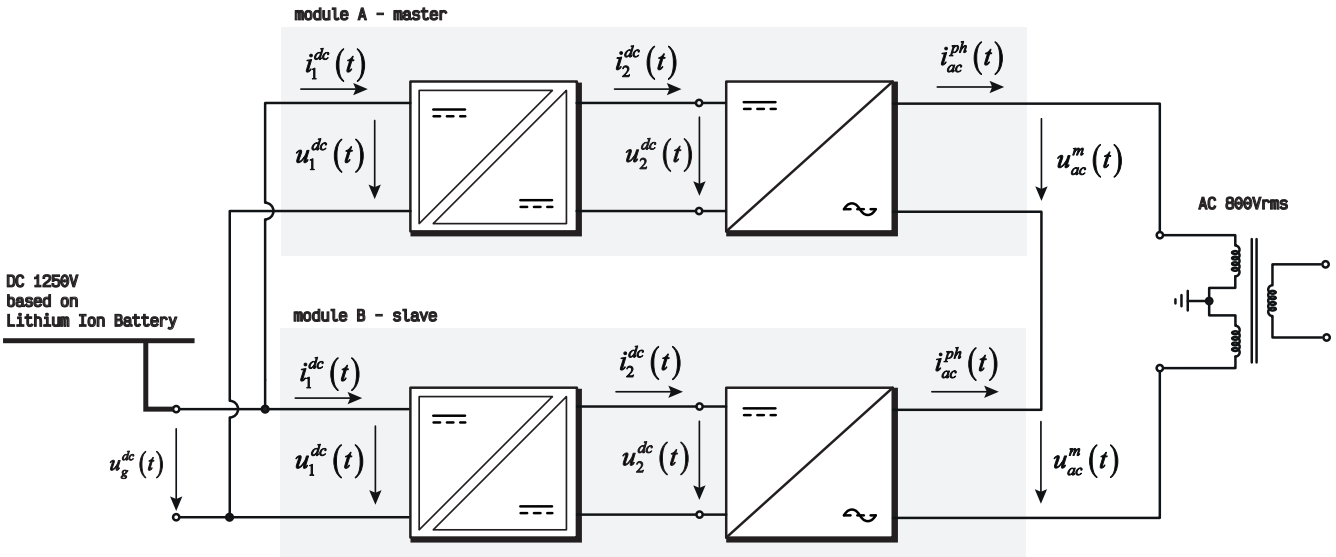


Figure 11: Simulation layout: simulation has been performance using a single phase SST composed by two single phase inverter connected in series with three difference case scenario of DCDC: three phase DAB, single phase DAB, and single phase CLLC.

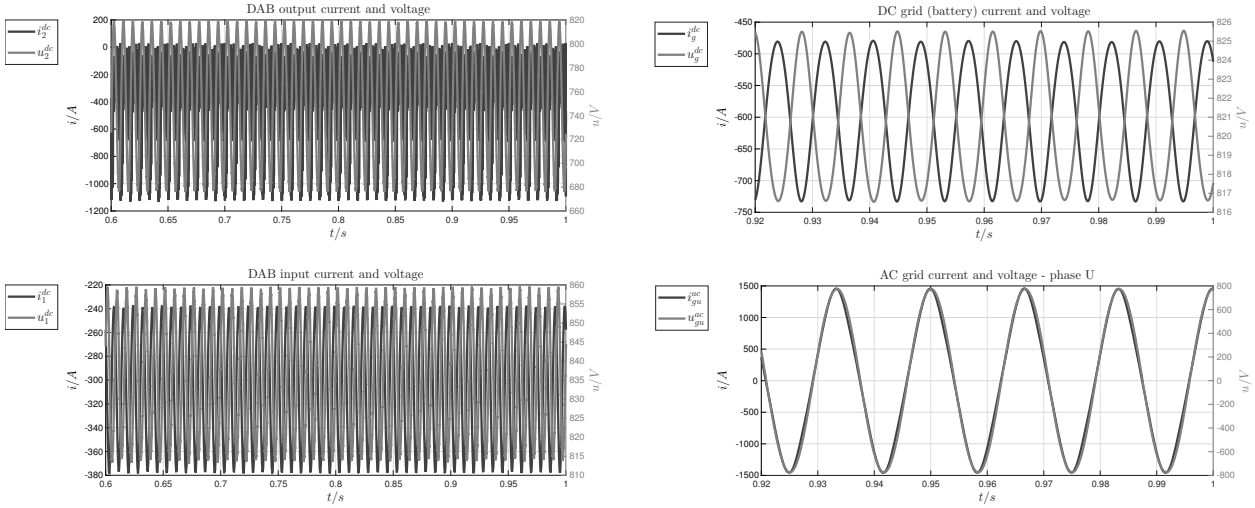
4.1 SST based on Three Phase DAB and NPC Single Phase Inverter

Here performance of the SST based on three phase DAB and a cascade of two three level NPC/T-Type single phase inverters.

Remark - only one single phase has been simulated and the total power at DC grid side is resulting in one third of an equivalent three phase implementation.

Remark - simulations have been performed under the following condition of grids and load:

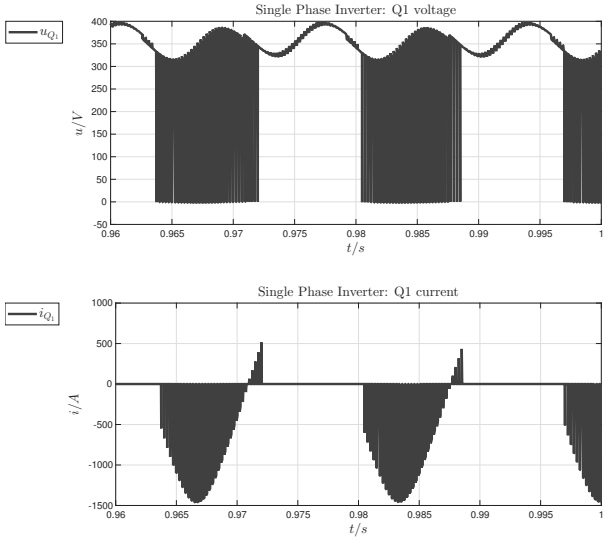
- DC grid nominal voltage (from Lithium Ion Battery) : $u_g^{dc}\Big|_{nom} = 750\,\mathrm{V} - 800\,\mathrm{V}$;
- AC grid nominal voltage : $u_g^{ac}\Big|_{nom} = 540\,\mathrm{V}$ - rms per phase-centertap;
- AC grid load current : $i_g^{ac} = 1000\,\mathrm{A}$ - rms;



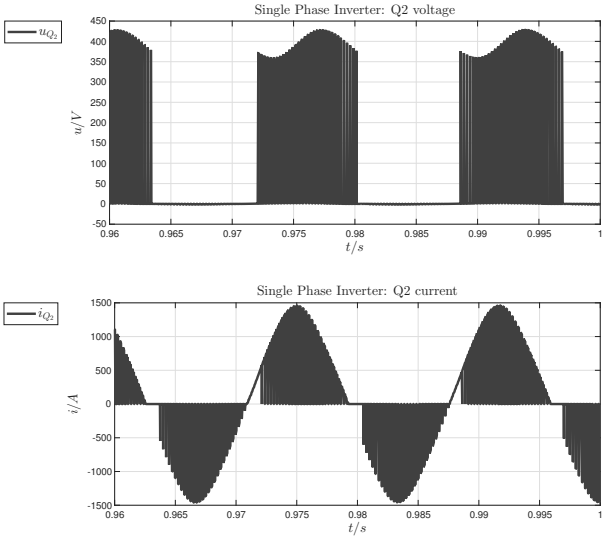
(a) Master three phase DAB input current and voltage (bottom) and outputs (top).

(b) DC grid current and voltage (top) and AC grid current and voltage (bottom).

Figure 12: Three phase DAB with NPC single phase inverter - performance of two stages single phase SST: three phase DAB input/output and grids.

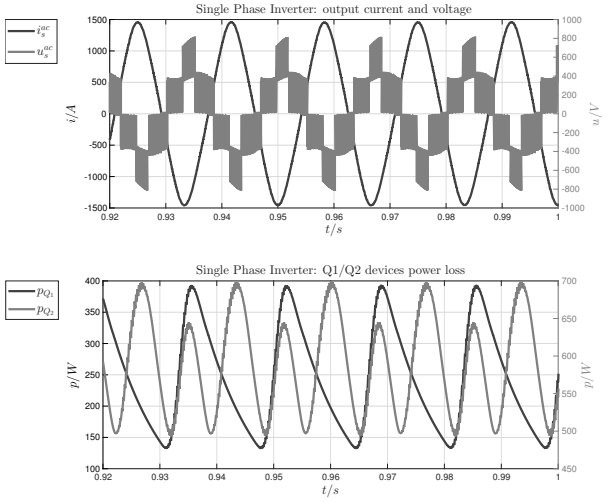


(a) Single phase inverter: Q1-IGBT voltage and current. The aim of this image is to proof the effective operative working of the three level NPC single phase inverter.

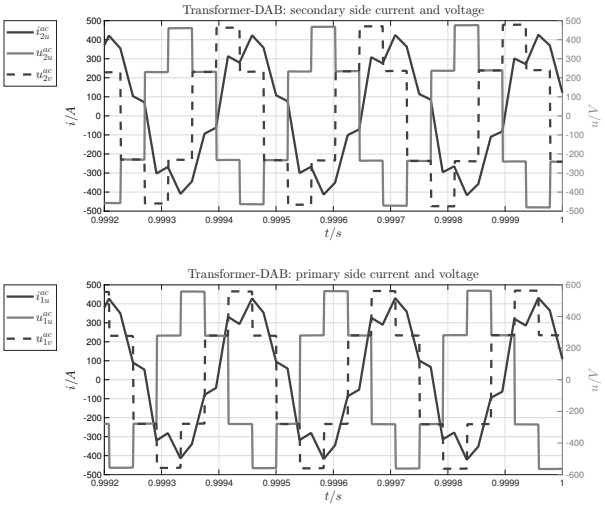


(b) Single phase inverter: Q2-IGBT voltage and current. The aim of this image is to proof the effective operative working of the three level NPC single phase inverter.

Figure 13: Three phase DAB with NPC single phase inverter - single phase inverter NPC: IGBTs voltage and current.

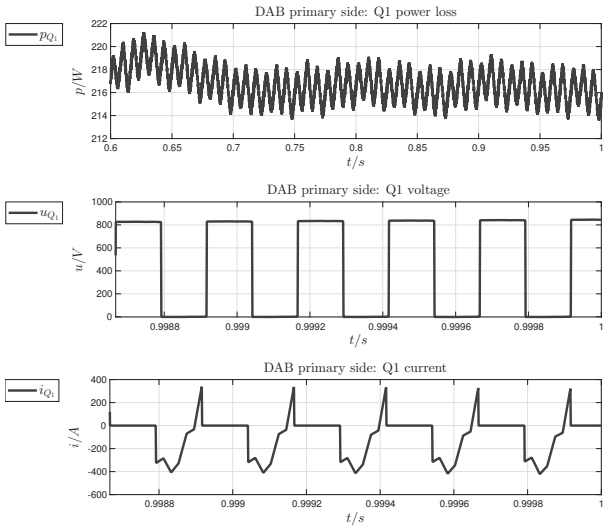


(a) IGBT Q1 and Q2 power loss (bottom). Single phase output current and voltage, before the output filter (top).

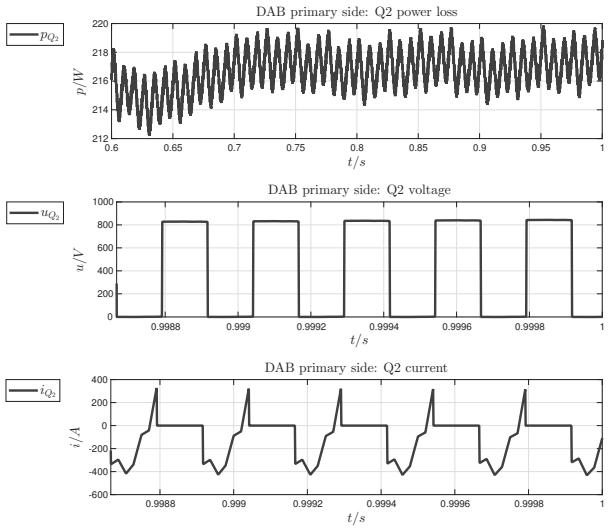


(b) Three phase DAB operative condition at nominal flow power.

Figure 14: Three phase DAB with NPC single phase inverter - single phase inverter and three phase DAB performances.

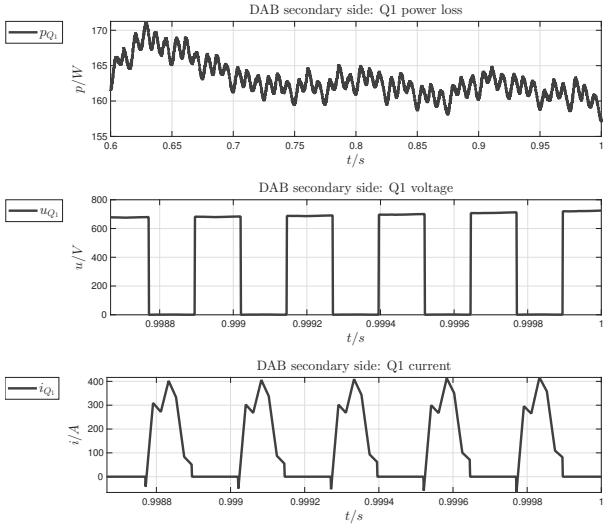


(a) Three phase DAB - primary inverter: Q1-MOSFET power loss, voltage and current.

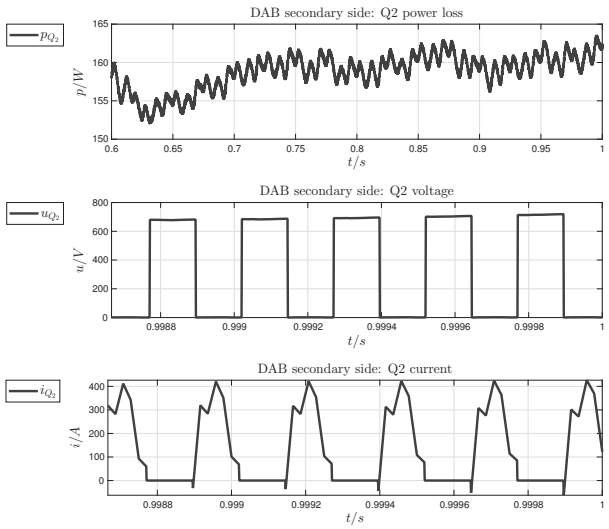


(b) Three phase DAB - primary inverter: Q2-MOSFET power loss, voltage and current.

Figure 15: Three phase DAB with NPC single phase inverter - primary inverter devices performances.



(a) Three phase DAB - secondary inverter: Q1-MOSFET power loss, voltage and current.



(b) Three phase DAB - secondary inverter: Q2-MOSFET power loss, voltage and current.

Figure 16: Three phase DAB with NPC single phase inverter - secondary inverter devices performances.

4.2 SST based on Three Phase DAB and T-Type Single Phase Inverter

Here performance of the SST based on three phase DAB and a cascade of two three level T-Type single phase inverters.

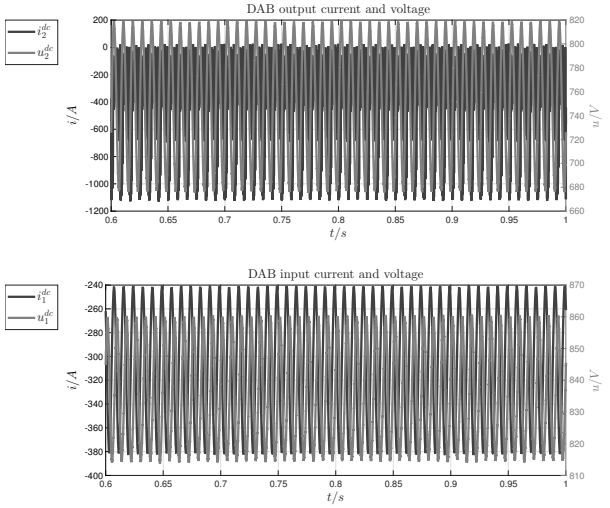
Remark - only one single phase has been simulated and total power at DC grid side is resulting in one third than in an equivalent three phase implementation.

Remark - simulations have been performed under the following condition of grids and load:

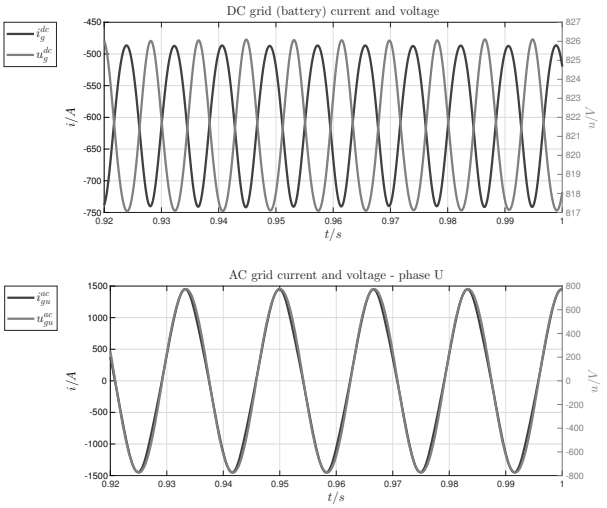
– DC grid nominal voltage (from Lithium Ion Battery) : $u_g^{dc}\Big|_{nom} = 800\,\mathrm{V}$;

– AC grid nominal voltage : $u_g^{ac}\Big|_{nom} = 554\,\mathrm{V}$ - rms per phase-centertap;

– AC grid load current : $i_g^{ac} = 1000\,\mathrm{A}$ - rms;

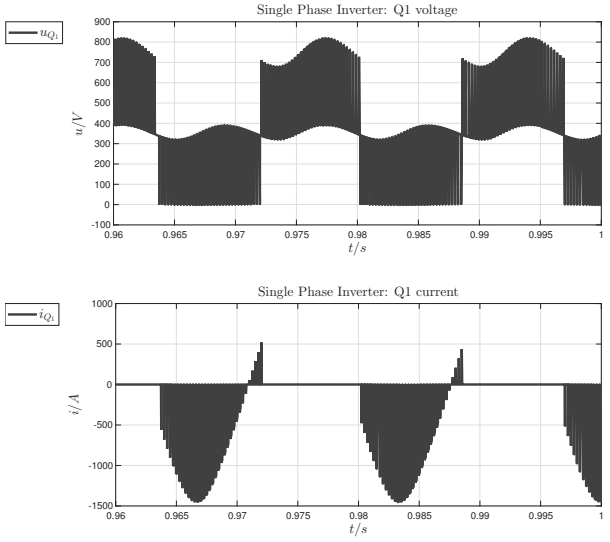


(a) Master three phase DAB input current and voltage (bottom) and outputs (top).

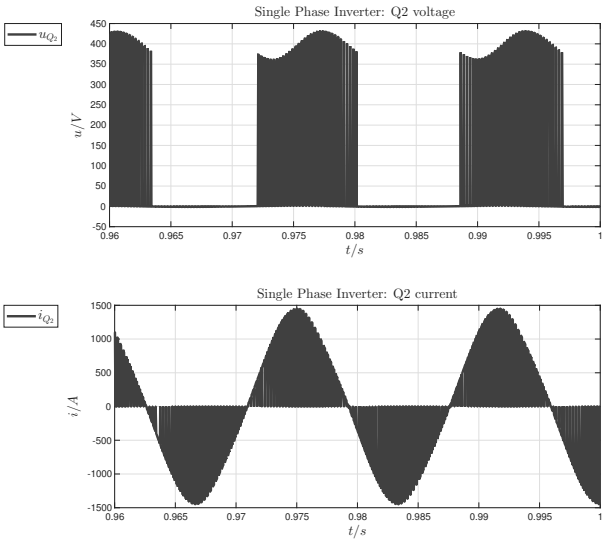


(b) DC grid current and voltage (top) and AC grid current and voltage (bottom).

Figure 17: Three phase DAB with T-Type single phase inverter - performance of two stages single phase SST: three phase DAB input/output and grids.

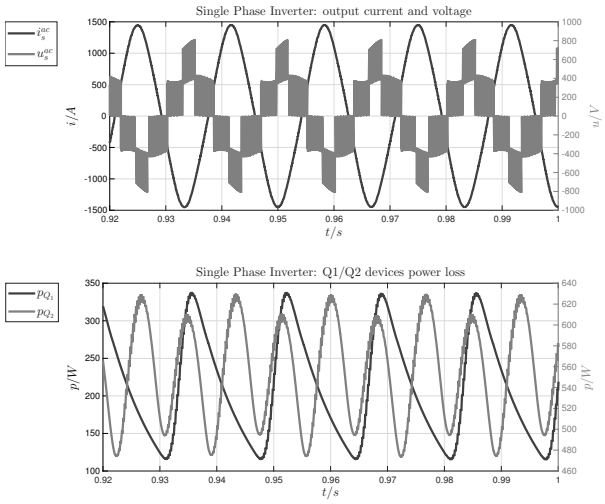


(a) Single phase inverter: Q1-IGBT voltage and current. The aim of this image is to proof the effective operative working of the three level NPC single phase inverter.

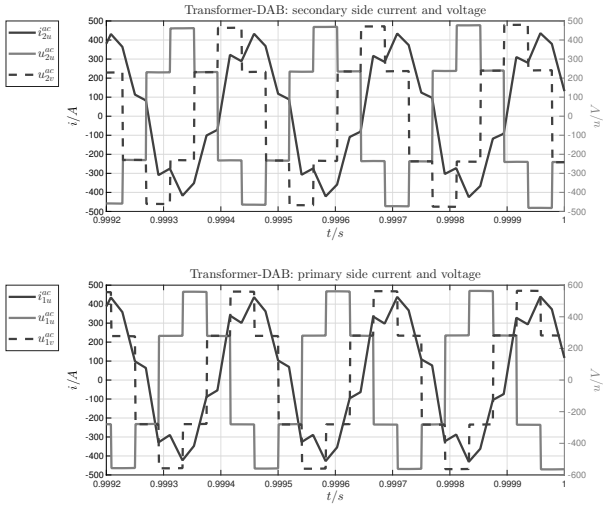


(b) Single phase inverter: Q2-IGBT voltage and current. The aim of this image is to proof the effective operative working of the three level NPC single phase inverter.

Figure 18: Three phase DAB with T-Type single phase inverter - single phase inverter T-Type: IGBTs voltage and current.

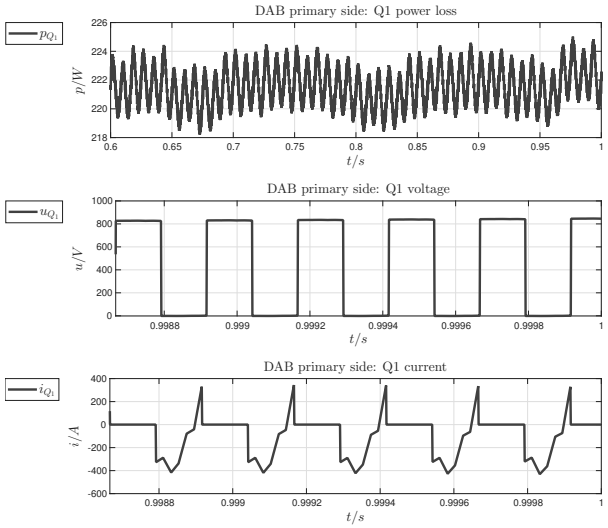


(a) IGBT Q1 and Q2 power loss (bottom). Single phase output current and voltage, before the output filter (top).

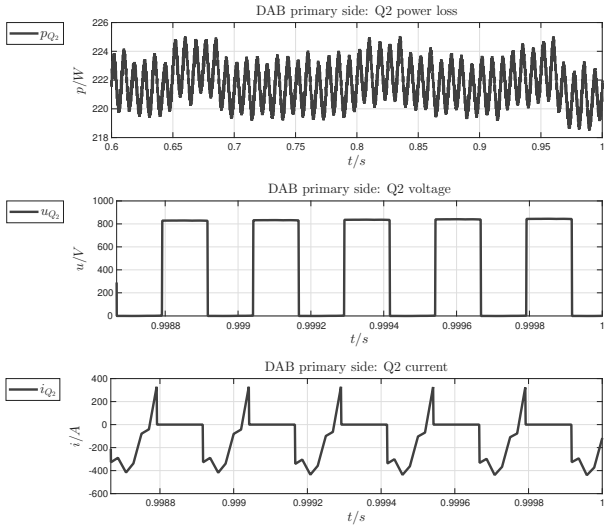


(b) Three phase DAB operative condition at nominal flow power.

Figure 19: Three phase DAB with T-Type single phase inverter - single phase inverter and three phase DAB performances.

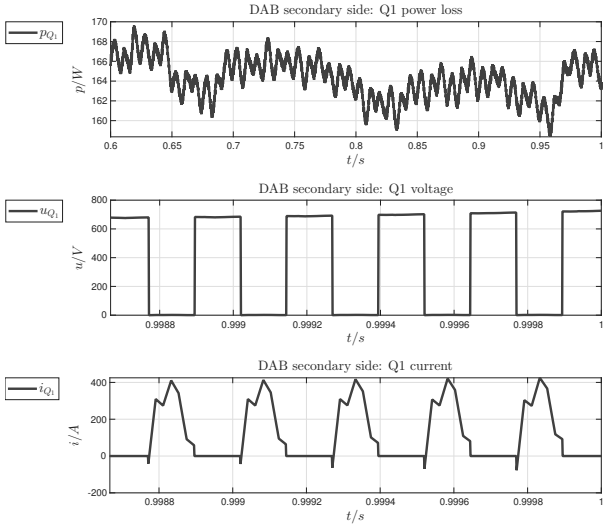


(a) Three phase DAB - primary inverter: Q1-MOSFET power loss, voltage and current.

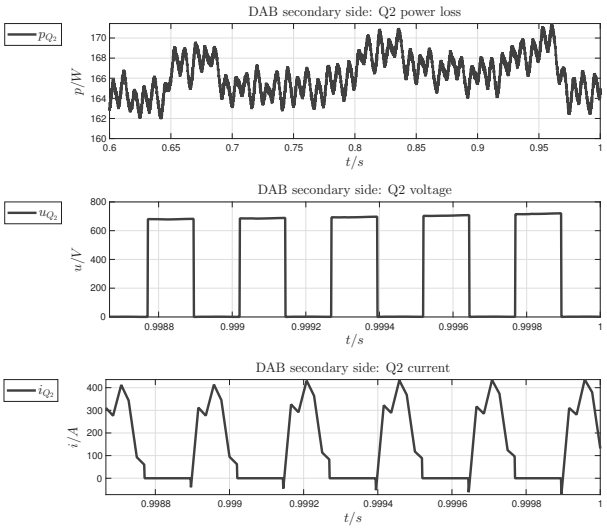


(b) Three phase DAB - primary inverter: Q2-MOSFET power loss, voltage and current.

Figure 20: Three phase DAB with T-Type single phase inverter - primary inverter devices performances.



(a) Three phase DAB - secondary inverter: Q1-MOSFET power loss, voltage and current.



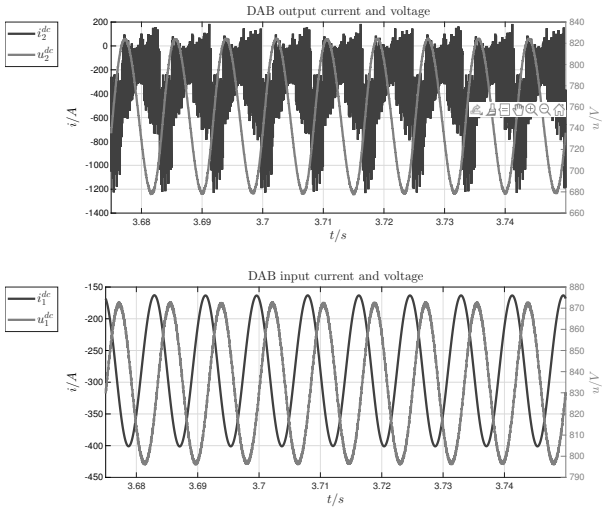
(b) Three phase DAB - secondary inverter: Q2-MOSFET power loss, voltage and current.

Figure 21: Three phase DAB with T-Type single phase inverter - secondary inverter devices performances.

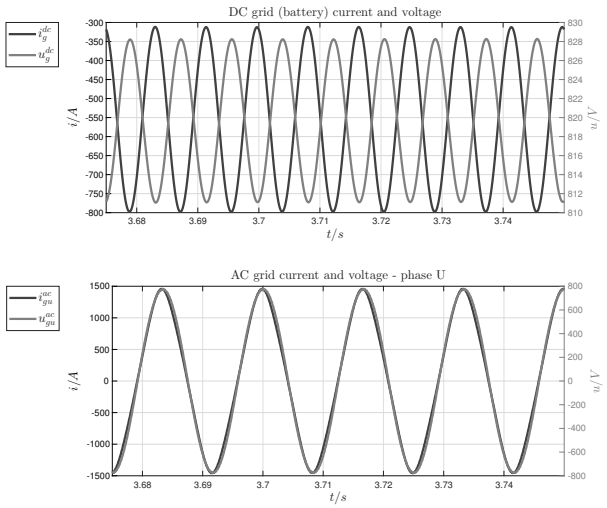
4.3 SST based on Single Phase CLLC and NPC Single Phase Inverter

In this section the performance of the CLLC has been investigated. The control strategy of the CLLC DCDC converter has been assumed as follows

- single phase CLLC is operating at constant frequency of $f_{\mathrm{llc}} = 13\,\mathrm{kHz}$;
- power flow direction as well as amplitude is controlled by phase shift between primary and secondary side H-bridges;
- the above control law keep the CLLC conversion in a constant condition of zero current switching;

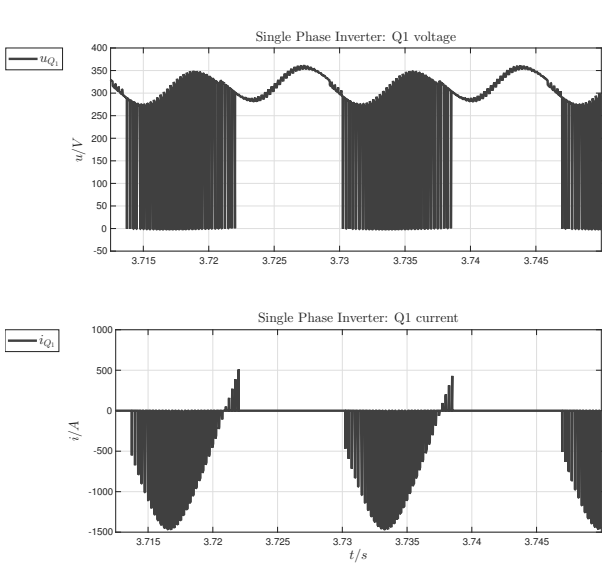


(a) Single phase CLLC with NPC single phase inverter - Mmster single phase CLLC input current and voltage (bottom) and outputs (top).

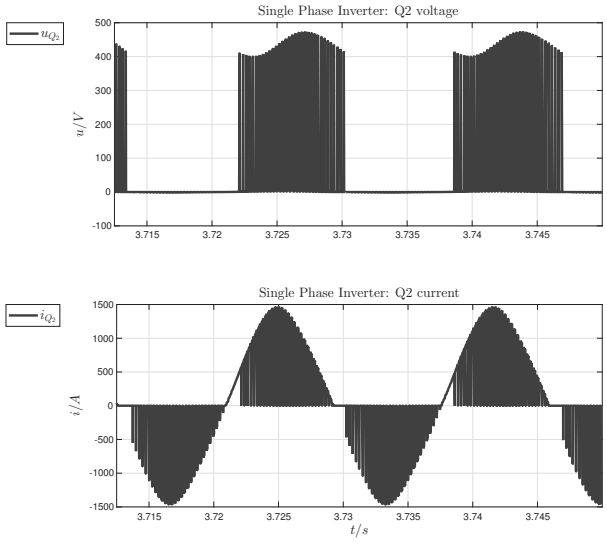


(b) DC grid current and voltage (top) and AC grid current and voltage (bottom).

Figure 22: Single phase CLLC with NPC single phase inverter - performance of two stages single phase SST: single phase CLLC input/output and grids.

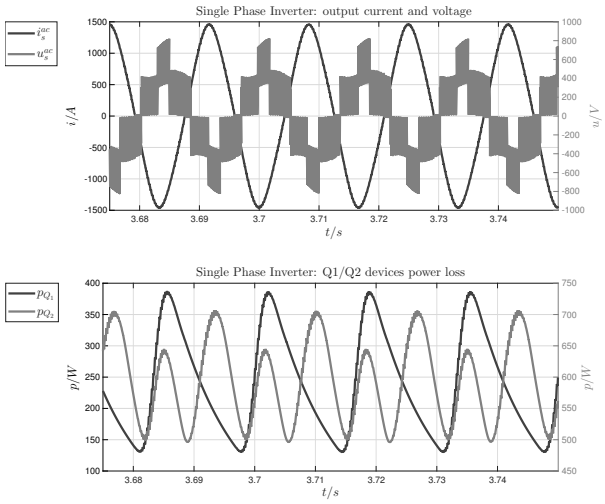


(a) Single phase inverter: Q1-IGBT voltage and current. The aim of this image is to proof the effective operative working of the three level NPC single phase inverter.

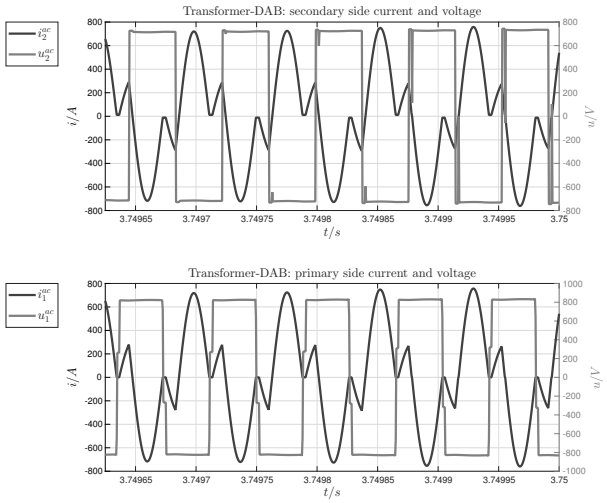


(b) Single phase inverter: Q2-IGBT voltage and current. The aim of this image is to proof the effective operative working of the three level NPC single phase inverter.

Figure 23: Single phase CLLC with NPC single phase inverter - single phase inverter NPC: IGBTs voltage and current.

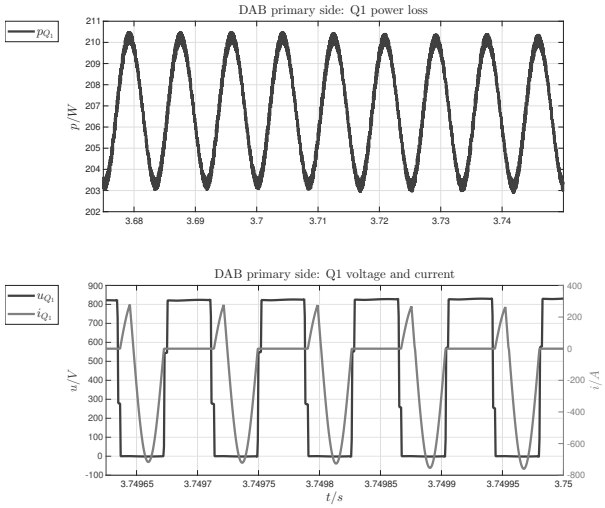


(a) IGBT Q1 and Q2 power loss (bottom). Single phase output current and voltage, before the output filter (top).

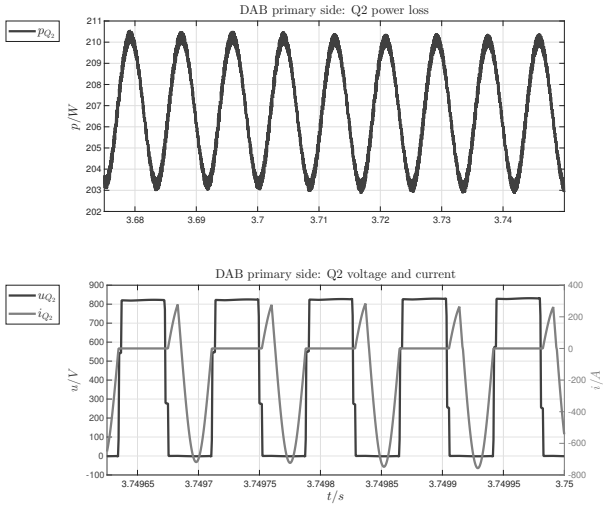


(b) Single phase CLLC operative condition at nominal flow power.

Figure 24: Single phase CLLC with NPC single phase inverter - single phase inverter and single phase CLLC performances.

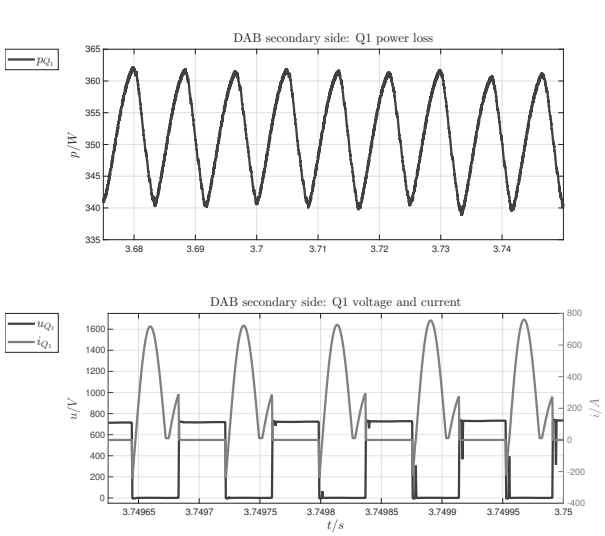


(a) Single phase CLLC - primary inverter: Q1-MOSFET power loss, voltage and current.

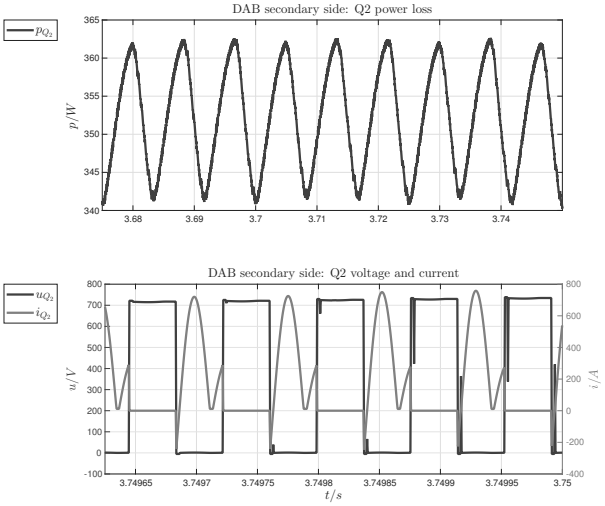


(b) Single phase CLLC - primary inverter: Q2-MOSFET power loss, voltage and current.

Figure 25: Single phase CLLC with NPC single phase inverter - primary inverter devices performances.



(a) Single phase CLLC - secondary inverter: Q1-MOSFET power loss, voltage and current.

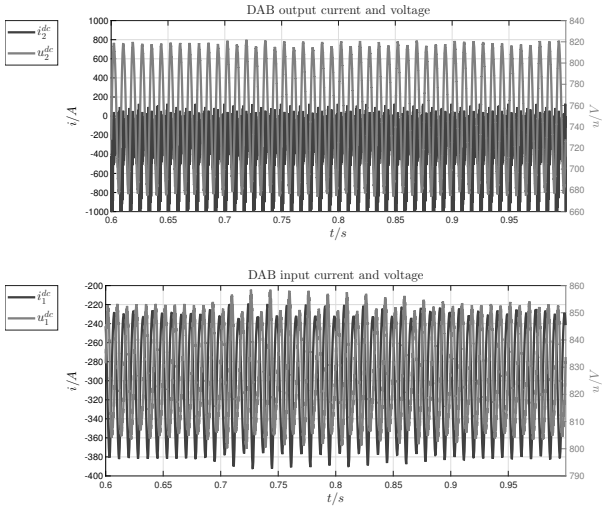


(b) Single phase CLLC - secondary inverter: Q2-MOSFET power loss, voltage and current.

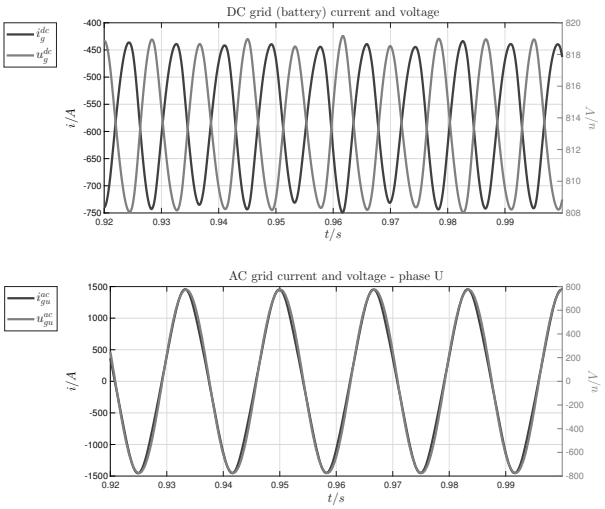
Figure 26: Single phase CLLC with NPC single phase inverter - secondary inverter devices performances.

4.4 SST based on Single Phase DAB and NPC Single Phase Inverter

Single phase DAB performance.

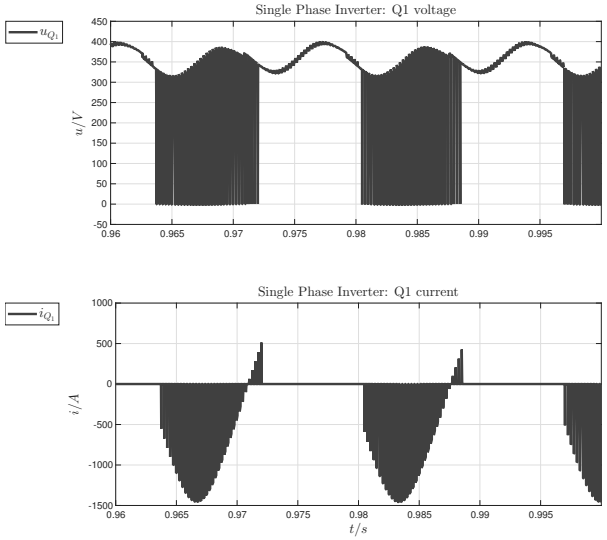


(a) Master single phase DAB input current and voltage (bottom) and outputs (top).

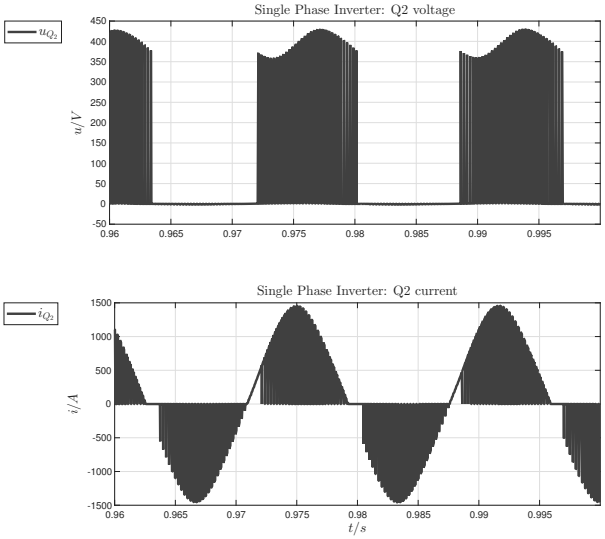


(b) DC grid current and voltage (top) and AC grid current and voltage (bottom).

Figure 27: Single phase DAB with NPC single phase inverter - performance of two stages single phase SST: single phase DAB input/output and grids.

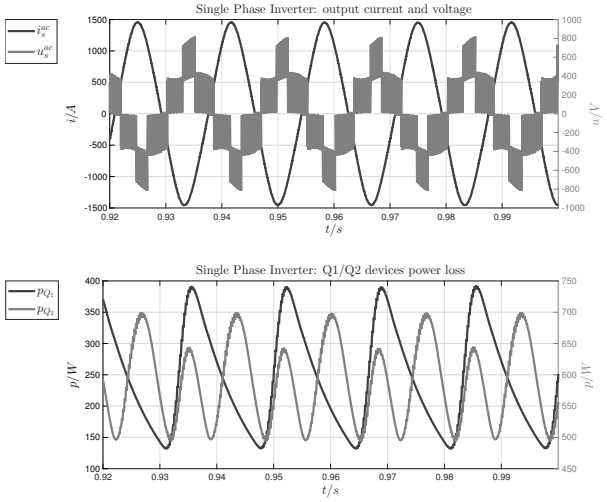


(a) Single phase inverter: Q1-IGBT voltage and current. The aim of this image is to proof the effective operative working of the three level NPC single phase inverter.

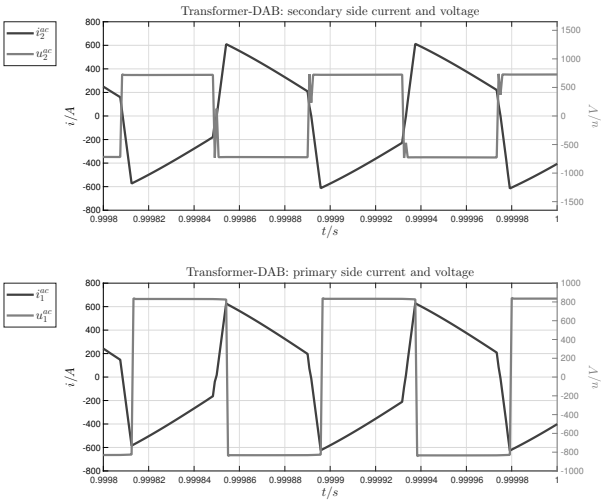


(b) Single phase inverter: Q2-IGBT voltage and current. The aim of this image is to proof the effective operative working of the three level NPC single phase inverter.

Figure 28: Single phase DAB with NPC single phase inverter - single phase inverter NPC: IGBTs voltage and current.

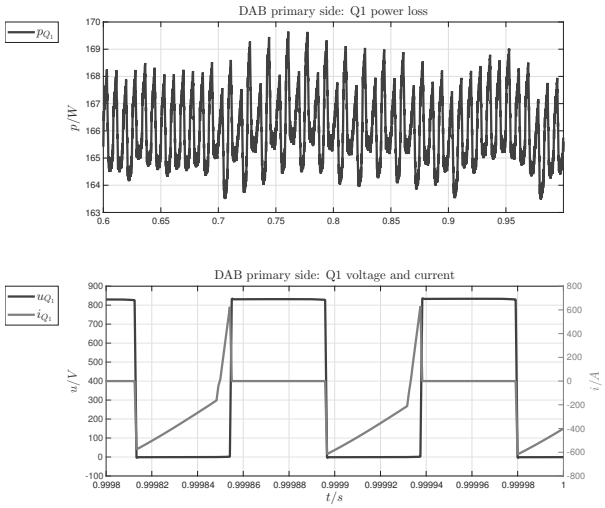


(a) IGBT Q1 and Q2 power loss (bottom). Single phase output current and voltage, before the output filter (top).

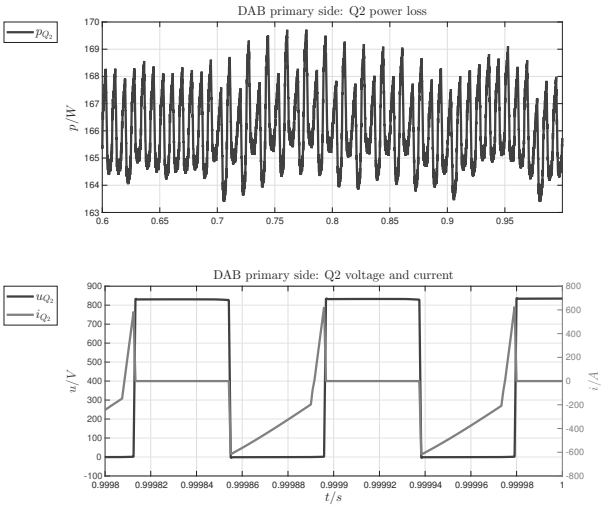


(b) Single phase DAB operative condition at nominal flow power.

Figure 29: Single phase DAB with NPC single phase inverter - single phase inverter and single phase DAB performances.

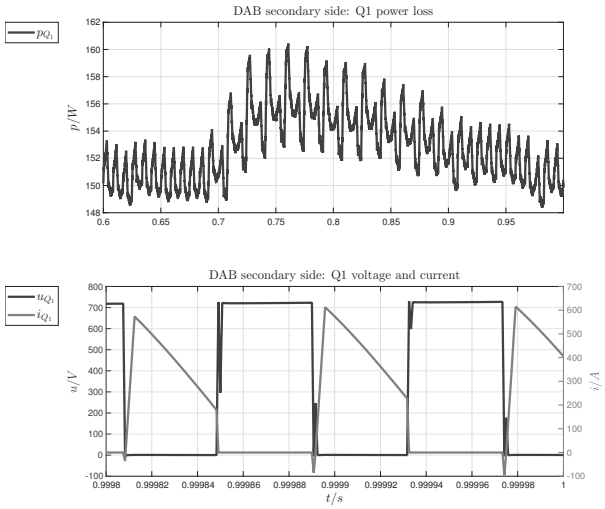


(a) Single phase DAB - primary inverter: Q1-MOSFET power loss, voltage and current.

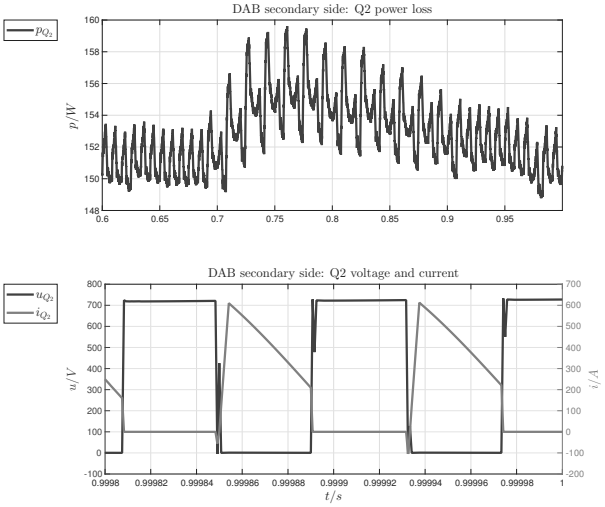


(b) Single phase DAB - primary inverter: Q2-MOSFET power loss, voltage and current.

Figure 30: Single phase DAB with NPC single phase inverter - primary inverter devices performances.



(a) Single phase DAB - secondary inverter: Q1-MOSFET power loss, voltage and current.



(b) Single phase DAB - secondary inverter: Q2-MOSFET power loss, voltage and current.

Figure 31: Single phase DAB with NPC single phase inverter - secondary inverter devices performances.

5 High-Frequency transformers design

5.1 Transformer design for 3P-DAB with T-Type single phase inverter architecture

Transformer for the three-phase DAB is built by three independent single phase transformers, as follows.
Input data:

- $u_1^b = 400\,\mathrm{V}rms$: primary side nominal voltage;
- $u_2^b = 400\,\mathrm{V}rms$: secondary side nominal voltage;

- $i_1^b = 275\,\mathrm{A}rms$: primary side nominal current;
- $i_2^b = 275\,\mathrm{V}rms$: secondary side nominal current;
- $f_b = 4\,\mathrm{kHz}$: fundamental frequency;

Design:

- core material: nanocrystalline alloy ($\mu_r = 5000$);
- core shape: C (AM-NC-320C AMMET);
  - core height: $h_{fe} = 220\,\mathrm{mm}$;
  - core length: $L_{fe} = 720\,\mathrm{mm}$;
  - core width: $d_{fe} = 50\,\mathrm{mm}$;
  - core window: $W_{fe} = 60\,\mathrm{mm}$;
  - core depth: $D_{fe} = 90\,\mathrm{mm}$;
  - relative permeability $\mu_r = 5000$;
  - maximum magnetic flux density $\hat{B} = 0.8\,\mathrm{Wb\,m^{-2}}$;
- winding material: copper foil $d = 0.5\,\mathrm{mm}$;
- winding current density: $J = 3.0\,\mathrm{A\,mm^{-2}}$;

calculus: assuming $n_1 = n_2 = 6$

$$S_{fe} = 10^4 \frac{u_1^b}{4.44\ f_b\ \hat{B}\ n_1} \approx 47\,\mathrm{cm}^2 \tag{5.1}$$

$$S_{cu} = \frac{i_1^b}{J} \approx 90\,\mathrm{mm}^2 \tag{5.2}$$

$$L_{cu} = \frac{S_{cu}}{d} \approx 180\,\mathrm{mm} \tag{5.3}$$

Remark - core will be created by the parallelization of 3 per AM-NC-320C AMMET, that results in the following iron power losses:

Specific Core Loss

$$P_\mu = 16\,\mathrm{W\,kg^{-1}} \qquad \text{at} \quad f = 4\,\mathrm{kHz}, \quad \hat{B} = 0.8\,\mathrm{Wb\,m^{-2}} \tag{5.4}$$

Core mass

$$m_{fe} = 26.35\,\mathrm{kg} \tag{5.5}$$

Core power losses

$$P_{fe} = 225\,\mathrm{W} \tag{5.6}$$

Copper power losses

$$P_{cu} = 50\,\mathrm{W} \tag{5.7}$$

Total power losses

$$P_{loss} = 3(P_{fe} + P_{cu}) = 825\,\mathrm{W} \tag{5.8}$$

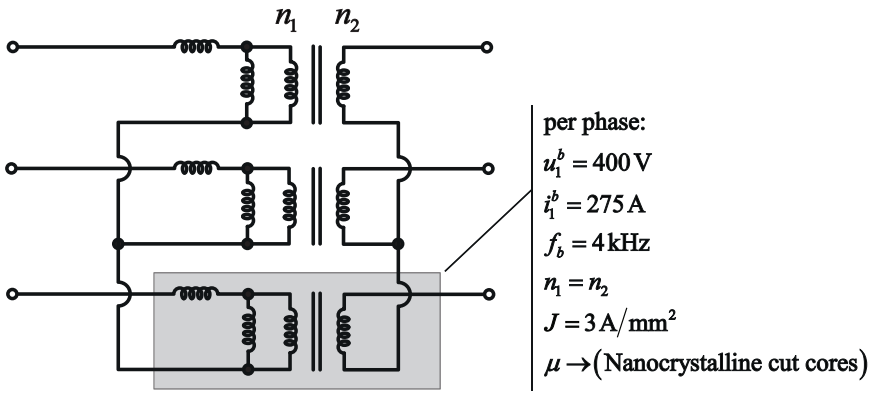
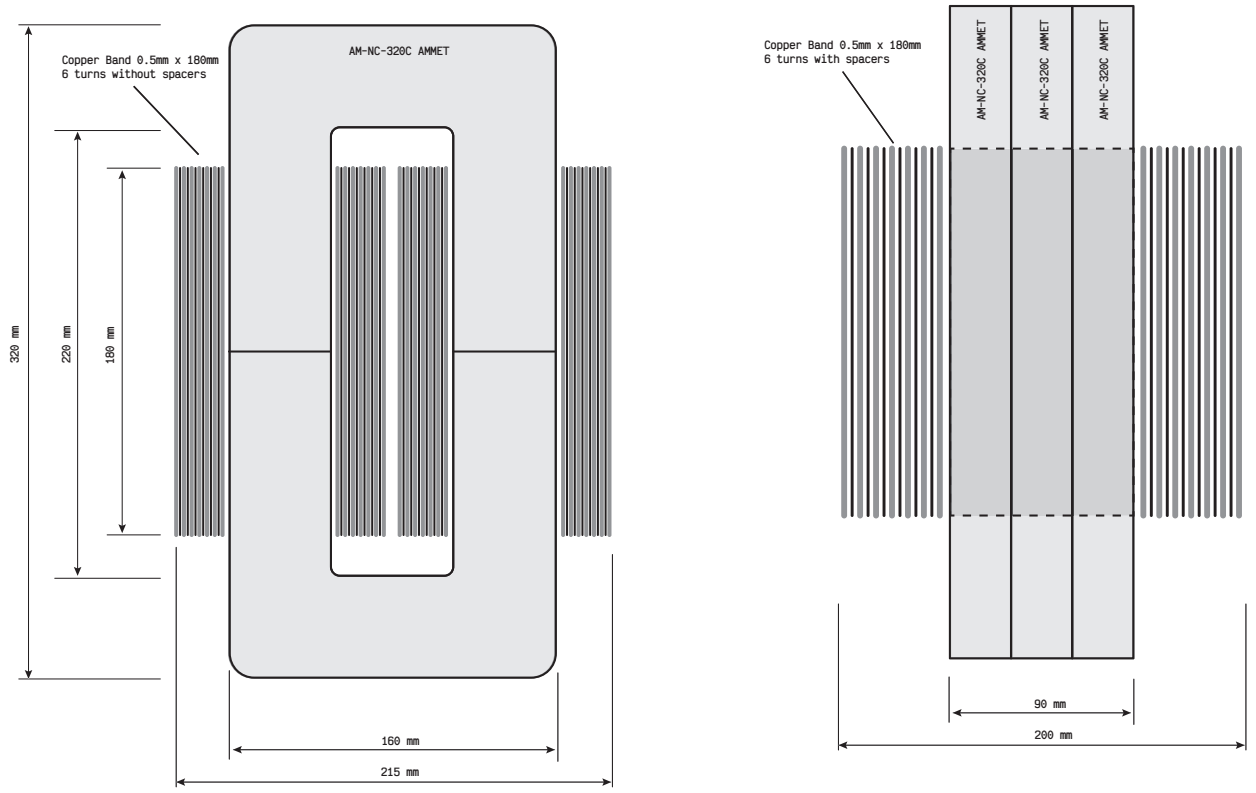


Figure 32: Transformer layout for the three-phase DAB.



(a) Single phase transformer for the three-phase DAB - front view.

(b) Single phase transformer for the three-phase DAB - side view.

Figure 33: Single phase transformer for the three-phase DAB.

5.2 Transformer design for 1P-DAB

6 Summary of simulation results

In this section a summary of overall efficiency for: three phase DAB, single phase DAB, single phase CLLC is shown.

The power flow through each DC/DC/AC converter is around 250 kW, in Table 1 the total power loss concerning the semiconductors components are reported. Power loss concerning capacitors and inductors gave been not accounted at this stage.

Remark - T-Type single phase inverter will taken into account.

Table 1: Comparison of power loss for three different DC/DC architecture.

Architecture	$f_{dab}\,[\mathrm{kHz}]$	$f_{inv}\,[\mathrm{kHz}]$	$p_{loss}^{dab}\,[\mathrm{kW}]$	$p_{loss}^{inv}\,[\mathrm{kW}]$
Three phase DAB	4 kHz	4 kHz	2.27 kW	3.0 kW
Single phase CLLC	13 kHz	4 kHz	2.25 kW	3.0 kW

Single phase DAB	12 kHz	4 kHz	1.28 kW	3.0 kW

From Table 1 all solution seems promising until ZVS for single phase DAB or ZCS for CLLC are satisfied. Impact into magnetic has to be investigated.

In the following additional information are reported.

Table 2: DC/DC transformers rms main quantities.

Architecture	$f_{dab}[\mathrm{Hz}]$	$i_1[\mathrm{A}_{rms}]$	$i_2[\mathrm{A}_{rms}]$	$u_1[\mathrm{V}_{rms}]$	$u_2[\mathrm{V}_{rms}]$	$L_s[\mathrm{H}]$
Single phase DAB	12 kHz	375 A	375 A	830 V	752 V	11 µH
Three phase DAB	4 kHz	265 A	265 A	400 V	360 V	28 µH
Single phase CLLC	13 kHz	452 A	452 A	815 V	745 V	13 µH

Remark - in Table 2 voltages for the three phase DAB represent the *per phase* voltage and not the phase to phase, on the other hand voltages for the CLLC and single phase DAB architecture represent the voltage across the single phase transformer.

Remark - L_s accounts also the leakage inductance of the transformer.

References

[1] R. De Doncker, D. M. Divan, M. H. Kheraluwala *A Three-phase Soft-Switched High-Power-Density dc /dc Converter for High-Power Applications*. Transactions of Industry Applications vol. 27 No. 1 January 1991.

[2] H. Akagi, S. Kinouchi, Y. Miyazaki *Bidirectional Isolated Dual-Active-Bridge (DAB) DC-DC Converters Using 1.2-kV 400-A SiC-MOSFET Dual Modules*. Transactions of Power Electronics vol. 1 No. 1 December 2016.

[3] F. Krismer, *Modeling and Optimization of Bidirectional Dual Active Bridge DC–DC Converter Topologies*. PhD dissertation, 2010.

[4] R. Teodorescu, M. Liserre, P. Rodrıguez, *Grid converters for photovoltaic and wind power systems*. Wiley, 2011.