

Flying Capacitor Multilevel

Single Phase Inverter

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Nomenclature

Here the list of variables and parameters used along the document:

- C_{fc}^{base} [F]: base capacitance for flying capacitors;
- R_{Cfc}^{base} [Ω]: base resistance of the base module for flying capacitors;
- L_{Cfc}^{base} [H]: base inductance of the base module for flying capacitors;
- C_{hf}^{base} [F]: base capacitance for high frequency capacitors;
- R_{Chf}^{base} [Ω]: base resistance of the base module for high frequency capacitors;
- L_{Chf}^{base} [H]: base inductance of the base module for high frequency capacitors;
- C_{fc}^n [F]: equivalent capacitance of the n-level flying capacitor;
- R_{Cfc}^n [Ω]: equivalent resistance of the n-level flying capacitor;
- L_{Cfc}^n [H]: equivalent inductance of the n-level flying capacitor;
- C_{hf}^n [F]: equivalent capacitance of the n-level high frequency capacitors;
- R_{Chf}^n [Ω]: equivalent resistor of the n-level high frequency capacitors;
- L_{Chf}^n [H]: equivalent inductance of the n-level high frequency capacitors;
- u_{in} [V]: input voltage;
- u_s [V]: half-bridge output voltage;
- u_{out} [V]: output voltage (output voltage of the LRC filter);
- i_{in} [A]: input current;
- i_s [A]: half-bridge output current;
- i_{out} [A]: output current (output current of the LRC filter);
- L_{Fu} [H]: output filter inductance;
- R_{Fu} [Ω]: output filter damping resistor;
- C_{Fu} [F]: output filter capacitance;



1 Converter Layout Description

Figure 1, Figure 3, and Figure 4 show the whole layout, the output filter, and the six-level half bridge flying capacitor respectively, in particular

- Figure 1 shows the pre-charge system;
- Figure 2 shows the electrical layout of the six-level half bridge flying capacitor.
- Figure 3 shows the output LRC filter;
- Figure 4 shows a full model of the six-level half bridge flying capacitor, where high frequency representation of stray parts are included. Configuration of the flying capacitor is also reported;

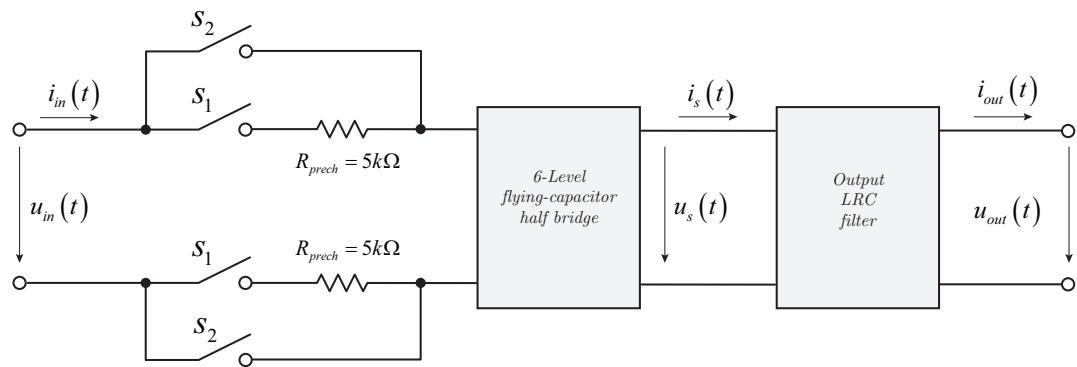


Figure 1: Auxiliary power supply.

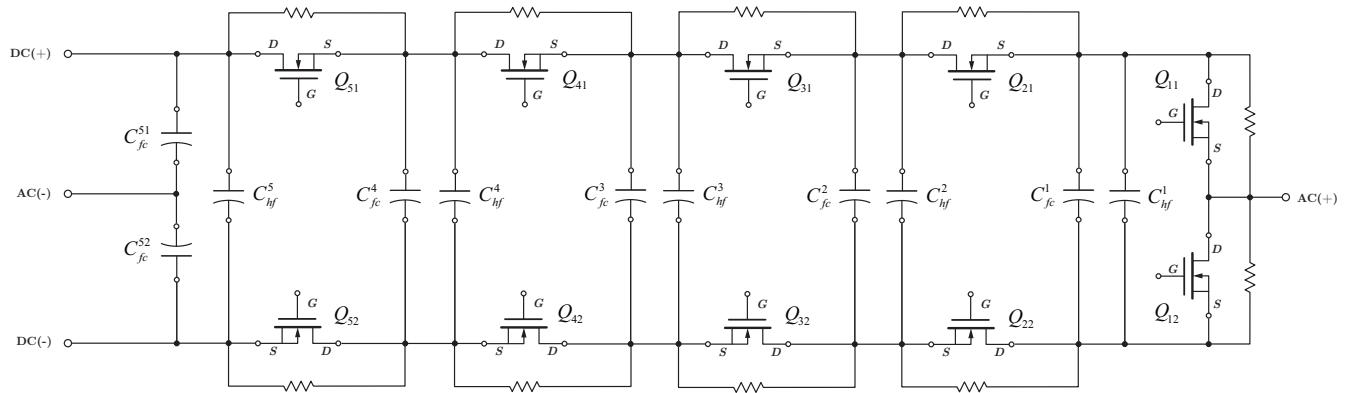


Figure 2: Half-bridge six-level flying capacitor converter.

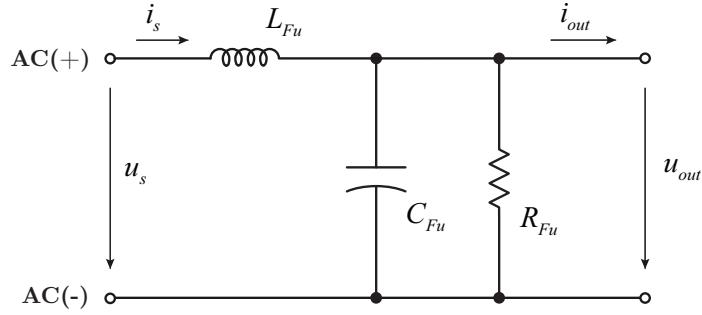


Figure 3: Output filter electrical layout.

According to Figure 4 each flying capacitor bank is created by a series-parallel connection of a *base* capacitor element, e.g. the fourth level of flying capacitor is created by four parallel harm made by for series capacitor connection ($4s$, $4p$) which results as follows

$$\begin{cases} C_{fc}^n = C_{fc}^{base} \\ R_{Cfc}^n = R_{Cfc}^{base} \\ L_{Cfc}^n = L_{Cfc}^{base} \end{cases} \quad (1.1)$$

Different approach is used for the *high-frequency* capacitors* where the connection is made only if series mode. The use of the *high-frequency* capacitor dclinks is made to reduce the effects of the high di/dt .

$$\begin{cases} C_{hf}^n = \frac{1}{n} \cdot C_{hf}^{base} \\ R_{Chf}^n = n \cdot R_{Chf}^{base} \\ L_{Chf}^n = n \cdot L_{Chf}^{base} \end{cases} \quad (1.2)$$

*The electrical layout/connection of the high-frequency capacitors to the corresponding mosfets level is made in a way to minimize the equivalent stray inductance.

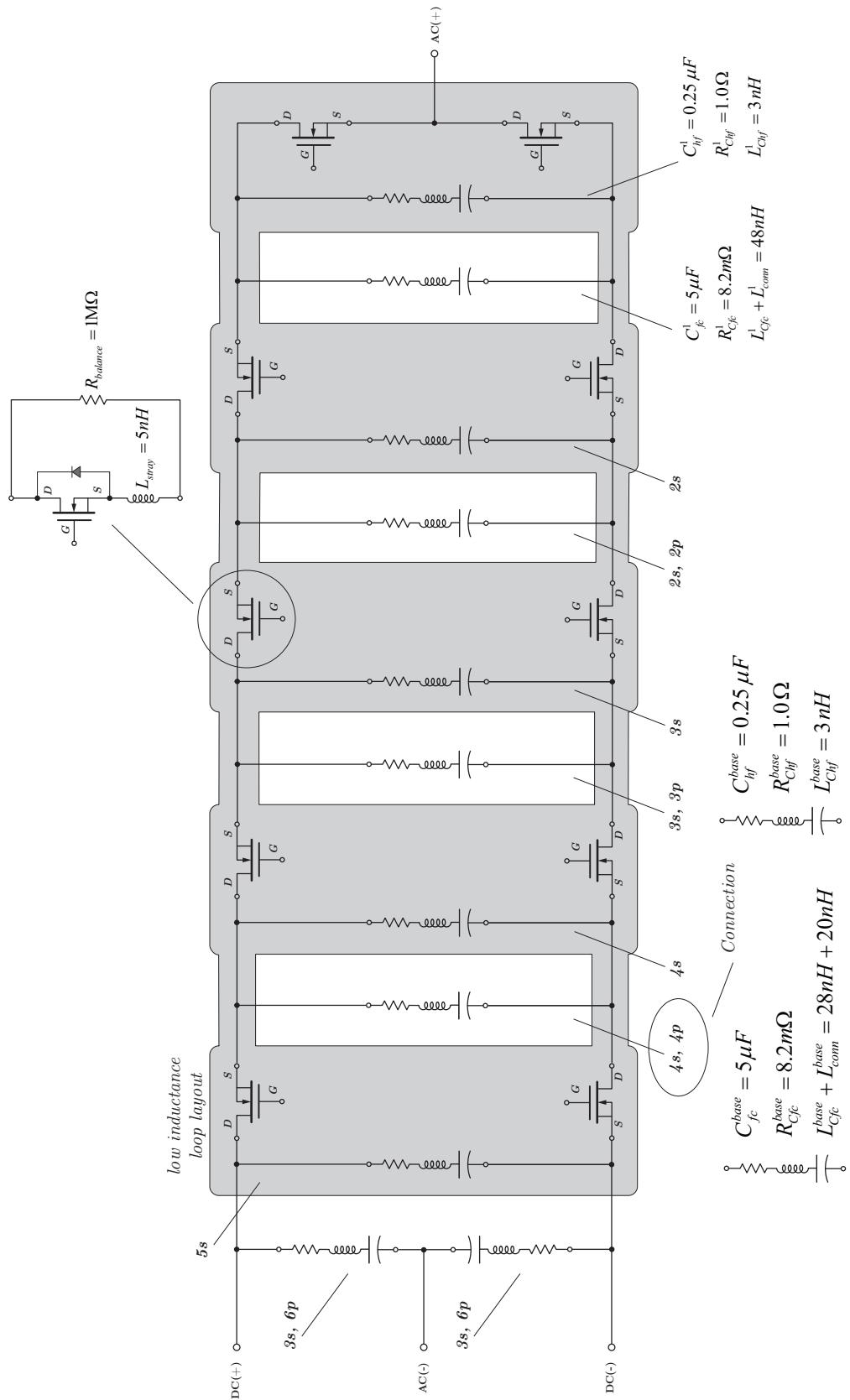


Figure 4: Half-bridge six-level flying capacitor converter - high frequency electrical model.



1.1 System pre-charge

The flying capacitors need to be precharged. A pre-charge control strategy is here proposed (see also Figure 5) as follows

- at time zero the switch s_1 is closed;
- from start od the pre-charge up to the end, a modulation index with negative ramp is applied;
- when modulation index reach the value of zero, the output control voltage starts and the load is connected.

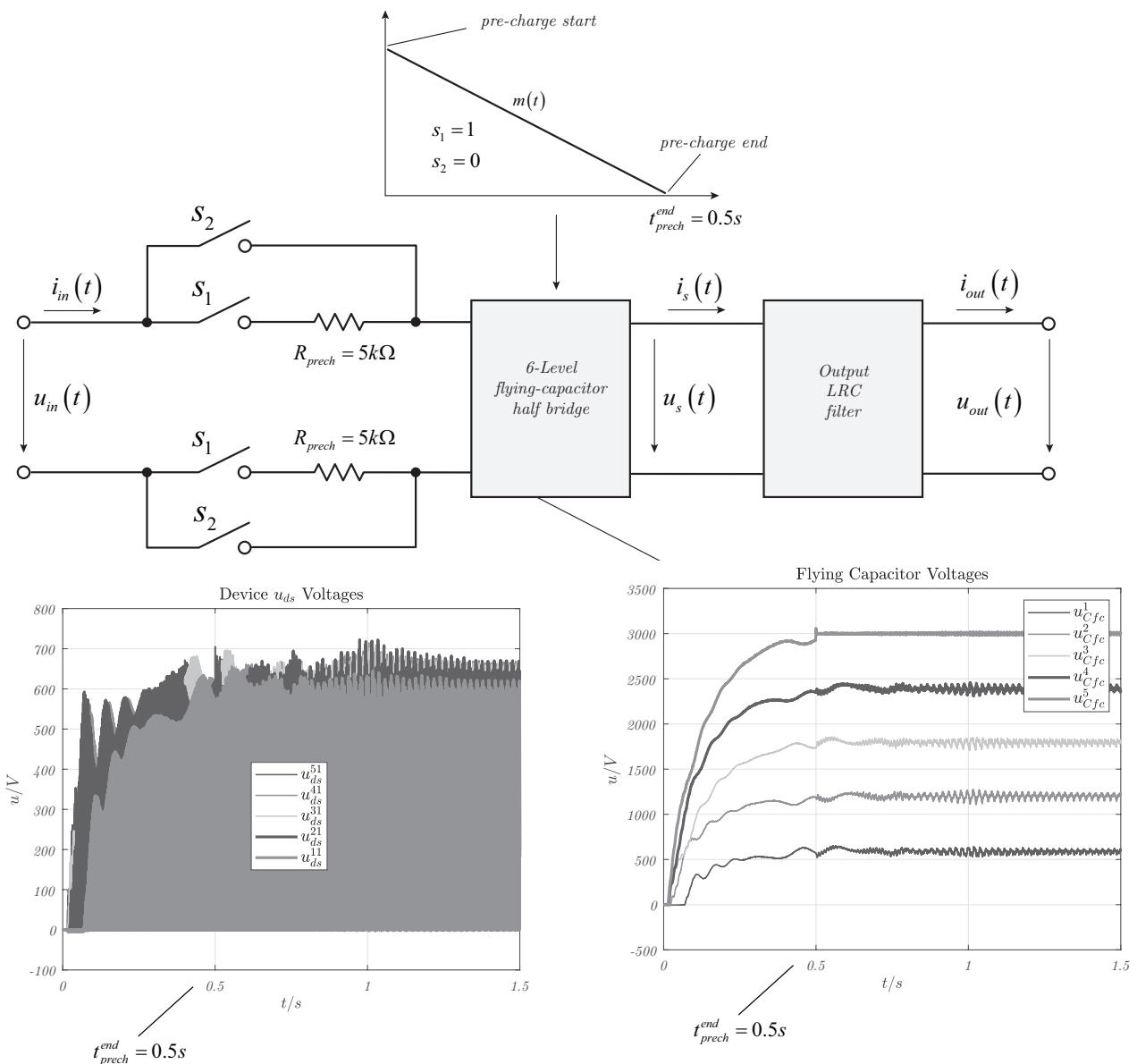


Figure 5: Flying capacitors pre-charge control strategy.

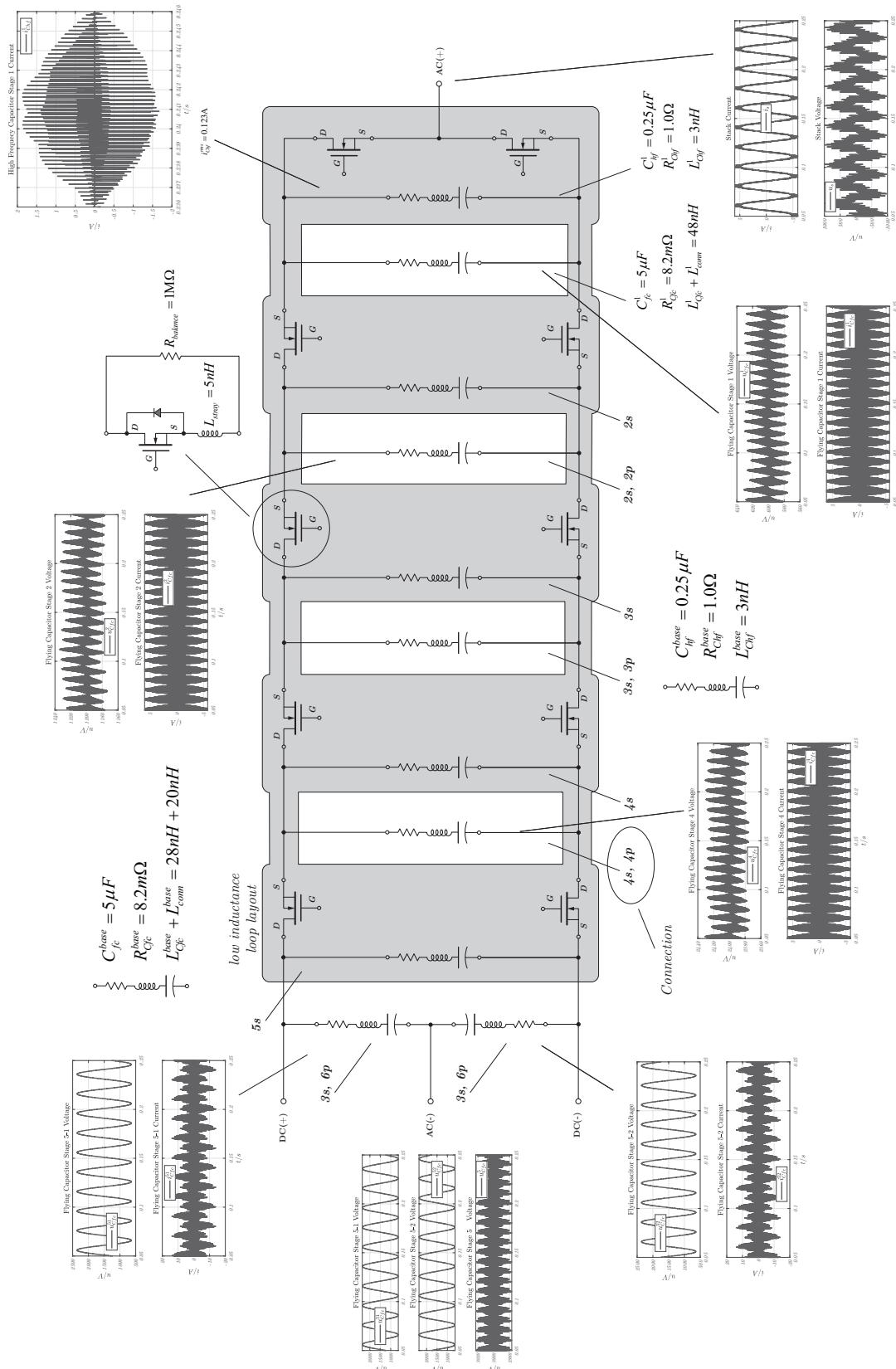


2 High Frequency Analysis

In this section the high frequency simulation results are shown. Basically the whole system has been implemented and simulated using a reasonable modelization of the stray loop inductance of the active and passive components with their wiring.

$$\begin{cases} C_{fc}^{base} = 5 \mu\text{F} \\ R_{Cfc}^{base} = 8.2 \text{ m}\Omega \\ L_{Cfc}^{base} = 28 \text{ nH} \\ L_{connection}^{base} = 20 \text{ nH} \end{cases} \quad (2.1)$$

$$\begin{cases} C_{hf}^{base} = 0.25 \mu\text{F} \\ R_{Chf}^{base} = 1.0 \Omega \\ L_{Chf}^{base} = 3 \text{ nH} \end{cases} \quad (2.2)$$





3 Control Layout

The control implementation of the single phase inverter is basically implemented using the following objects:

- a phase generator at frequency $\omega_0 = 2\pi 50 \text{ rad s}^{-1}$;
- two observers based on $\ddot{\vec{x}}(t) + \omega_0^2 \vec{x}(t) = 0$ plant;
- an outer magnitude voltage control loop;
- an inner vector current control loop, see also Figure 7.

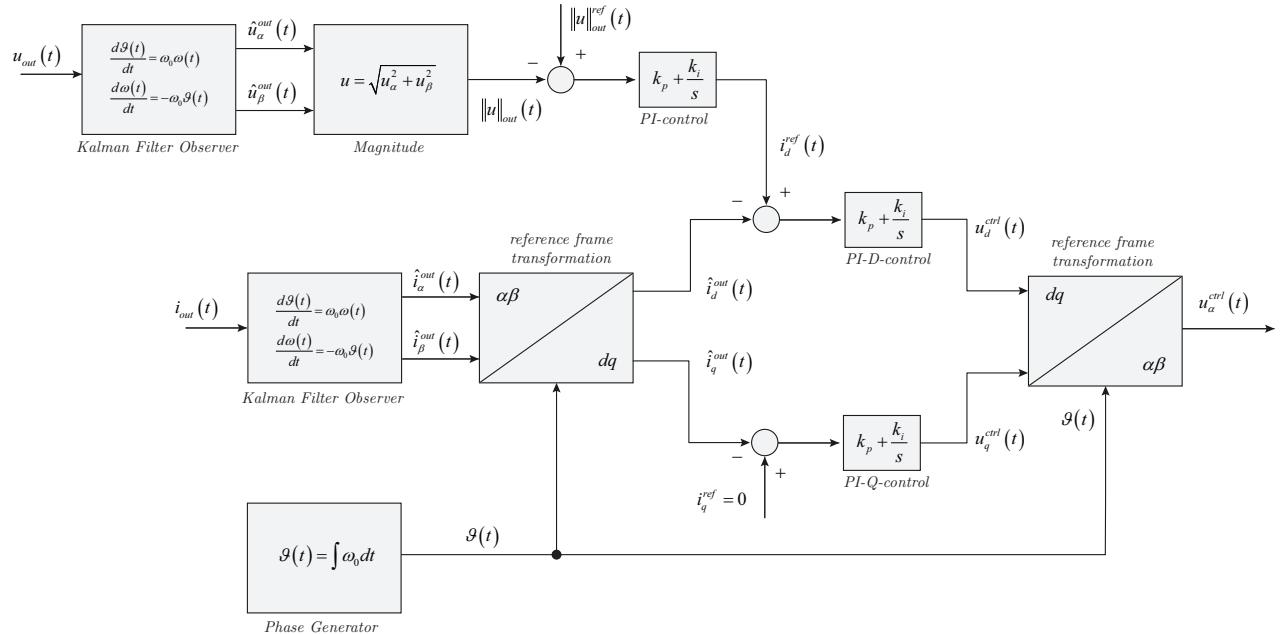


Figure 7: Control Layout.

3.1 Observer based control description

Let's try to consider the voltage and current measures as follows

$$\begin{cases} u_{out}(t) = U_{out} \cos(\vartheta) \\ i_{out}(t) = I_{out} \cos(\vartheta - \varphi) \end{cases} \quad (3.1)$$

where the argument $\vartheta(t) = \int \omega_0 dt$.

The core of the control system showed in Figure 7 lays into extrapolation of the quadrature component of both $u_{out}(t)$ and $i_{out}(t)$. From literature exist different solutions, but here the observer based method will be pursued.

The observer model can be assumed as follows

$$\ddot{\vec{x}}(t) + \omega_0^2 \vec{x}(t) = 0 \quad (3.2)$$



where its matrix representation is

$$\begin{cases} \dot{\vec{x}}(t) = \tilde{\mathbf{A}} \vec{x}(t) \\ y(t) = \mathbf{C} \vec{x}(t) \end{cases} \quad (3.3)$$

where

$$\tilde{\mathbf{A}} = \begin{bmatrix} 0 & \omega_0 \\ -\omega_0 & 0 \end{bmatrix}, \quad \mathbf{C} = \begin{bmatrix} 1 & 0 \end{bmatrix} \quad (3.4)$$

The equivalent discrete time representation of the system (3.3) can be derived as follows

$$\mathbf{A} = e^{\tilde{\mathbf{A}} t_s} = \mathcal{L}^{-1} \left[(s\mathbf{I} - \tilde{\mathbf{A}})^{-1} \right] \Big|_{t=t_s} = \begin{bmatrix} \cos(\omega_0 t_s) & \sin(\omega_0 t_s) \\ -\sin(\omega_0 t_s) & \cos(\omega_0 t_s) \end{bmatrix} \quad (3.5)$$

finally, the equivalent discrete time representation of the system (3.3) become

$$\begin{cases} \vec{x}(k+1) = \mathbf{A} \vec{x}(k) \\ y(k) = \mathbf{C} \vec{x}(k) \end{cases} \quad (3.6)$$

The state observer algorithm used to extract the quadrature component of the measured quantity $y_m(t)$ namely: $u_{out}(t)$ or $i_{out}(t)$ will be based on Kalman filter as follows

State Observer based on Kalman Filter Algorithm

$$\hat{\vec{x}}(k|k) = \mathbf{A} \hat{\vec{x}}(k|k-1) + \mathbf{B} \vec{u}(k|k-1) \quad a \text{ priori} \quad (3.7)$$

$$\mathbf{P}(k|k) = \mathbf{A} \mathbf{P}(k|k-1) \mathbf{A}^T + \mathbf{Q} \quad a \text{ priori} \quad (3.8)$$

$$\mathbf{L}(k) = \mathbf{P}(k|k) \mathbf{C}^T \left(\mathbf{C} \mathbf{P}(k|k) \mathbf{C}^T + \mathbf{R} \right)^{-1} \quad (3.9)$$

$$\hat{\vec{x}}(k+1|k) = \hat{\vec{x}}(k|k) + \mathbf{L}(k) \left(y_m(k) - \mathbf{C} \hat{\vec{x}}(k|k) \right) \quad a \text{ posteriori} \quad (3.10)$$

$$\mathbf{P}(k+1|k) = \left(\mathbf{I} - \mathbf{L}(k) \mathbf{C} \right) \mathbf{P}(k|k) \quad a \text{ posteriori} \quad (3.11)$$

where $y_m(t)$ is the measured quantity: $u_{out}(t)$ or $i_{out}(t)$.

Where Q and R have been selected as follows

$$\mathbf{Q} = \begin{bmatrix} 1 & 0 \\ 0 & t_s \end{bmatrix}, \quad \mathbf{R} = 1/t_s. \quad (3.12)$$

where $t_s = 200 \mu s$.



3.2 Modulation strategy

The modulation strategy is implemented using the interleaving mode among the levels (see Figure 8). The interleaved modulation strategy activates a kind of self flying capacitor voltage balancing ([1] and [2]), as simulation results shown.

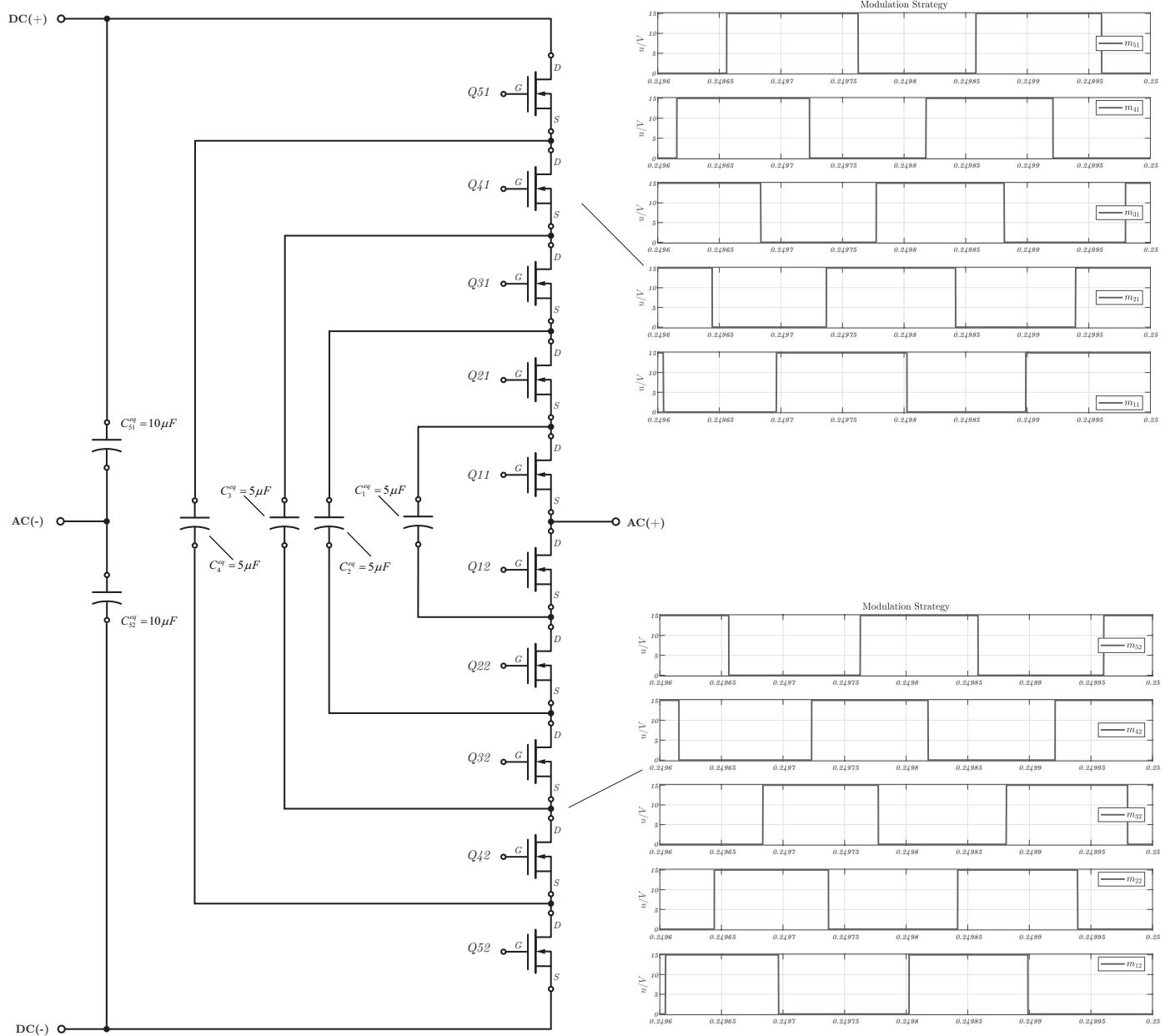


Figure 8: Modulation strategy for self flying capacitor balancing - a different overview.

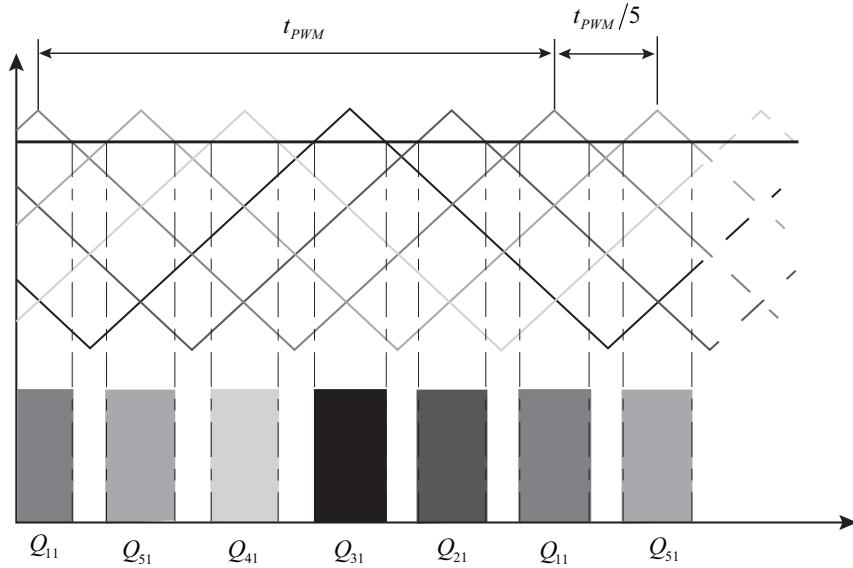


Figure 9: Modulation strategy for self flying capacitor balancing.

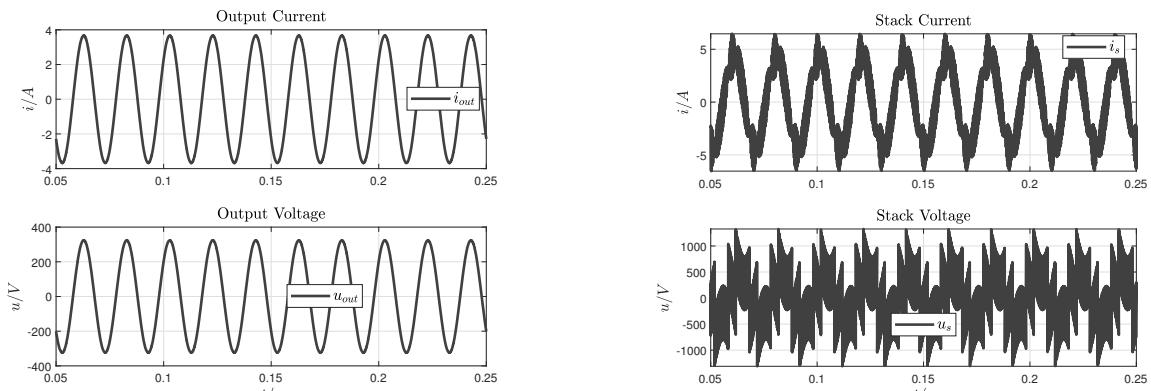
4 Simulation Results

4.1 High frequency open loop control at 5kV of input voltage.

The following set of simulation results have been realized under the following conditions

- discrete time step at $t_c = 1 \times 10^{-8}$ s;
- open loop control;
- $u_{dc} = 5$ kV;

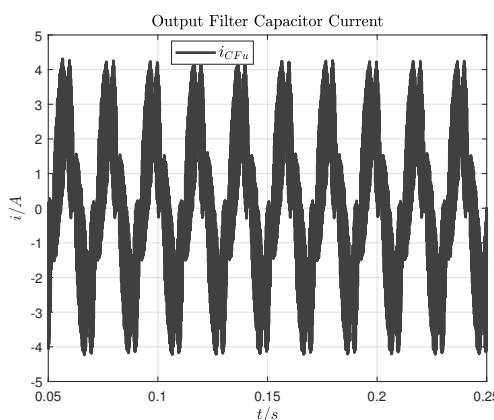
and they are intended for electronic layout evaluation.



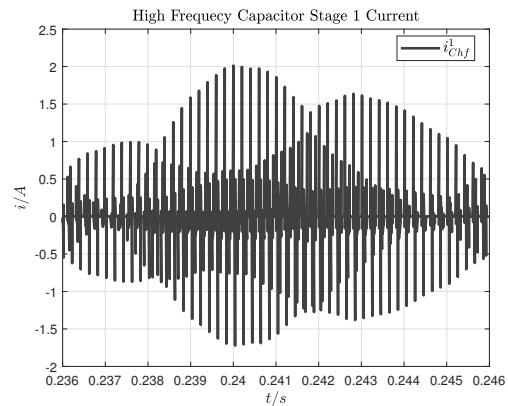
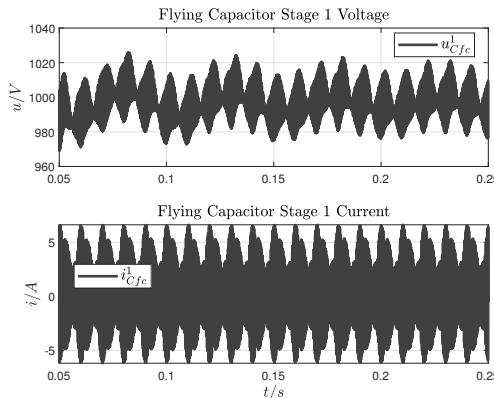
(a) Output current and voltage.

(b) Stack current and voltage.

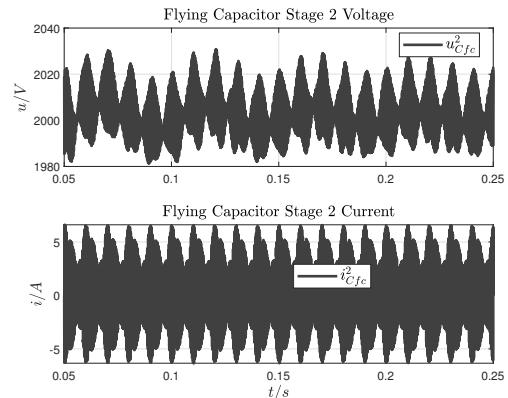
Figure 10: Output current and voltage stages, at $u_{dc} = 5$ kV.



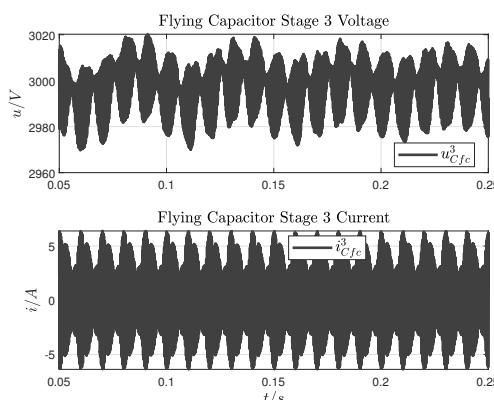
(a) Output filter capacitor current.

(b) High Frequency capacitor C_{hf}^1 current ($i_c^{rms} \approx 0.1$ A).Figure 11: Output filter capacitor current and high frequency dclink current, at $u_{dc} = 5$ kV.

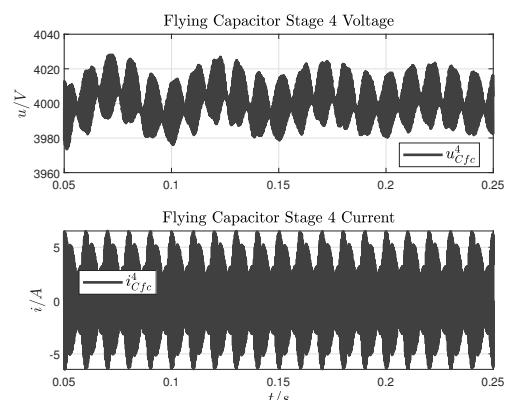
(a) Flying capacitor stage 1: current and voltage.



(b) Flying capacitor stage 2: current and voltage.

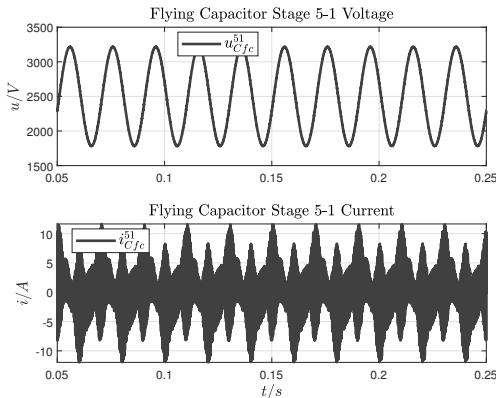
Figure 12: Flying capacitor stages 1 and 2, at $u_{dc} = 5$ kV.

(a) Flying capacitor stage 3: current and voltage.

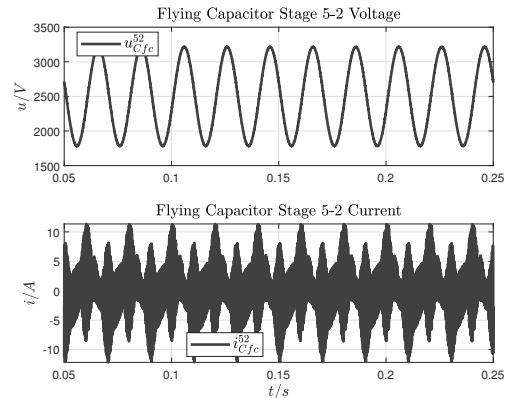


(b) Flying capacitor stage 4: current and voltage.

Figure 13: Flying capacitor stages 3 and 4, at $u_{dc} = 5$ kV.

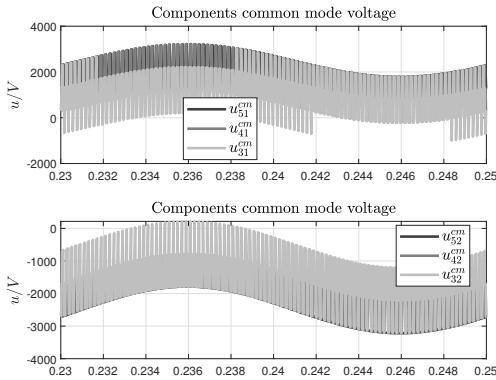


(a) Flying capacitor stage 51: current and voltage.

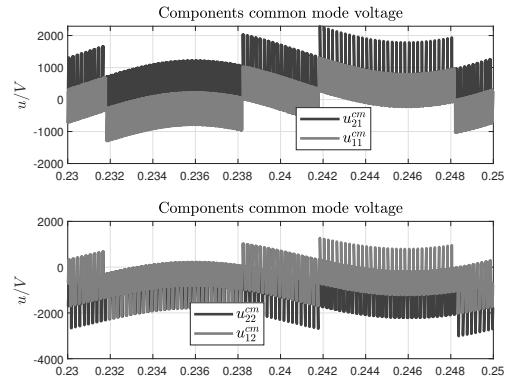


(b) Flying capacitor stage 52: current and voltage.

Figure 14: Flying capacitor stages 51 and 52, at $u_{dc} = 5$ kV.

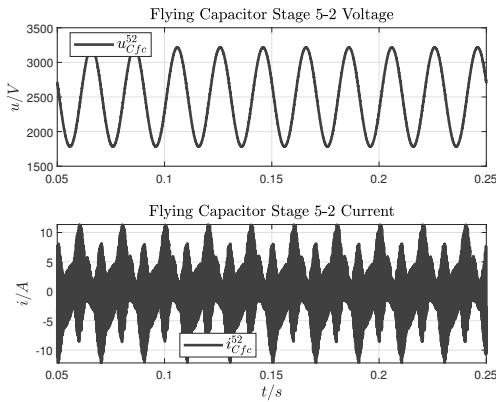


(a) Device common mode voltage (u_s): source ground voltage.

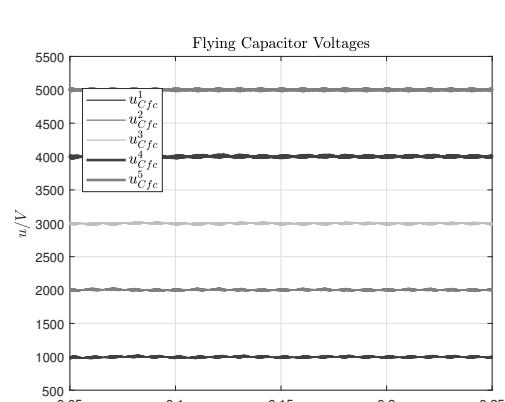


(b) Device common mode voltage (u_s): source ground voltage.

Figure 15: Device common mode voltages, at $u_{dc} = 5$ kV.

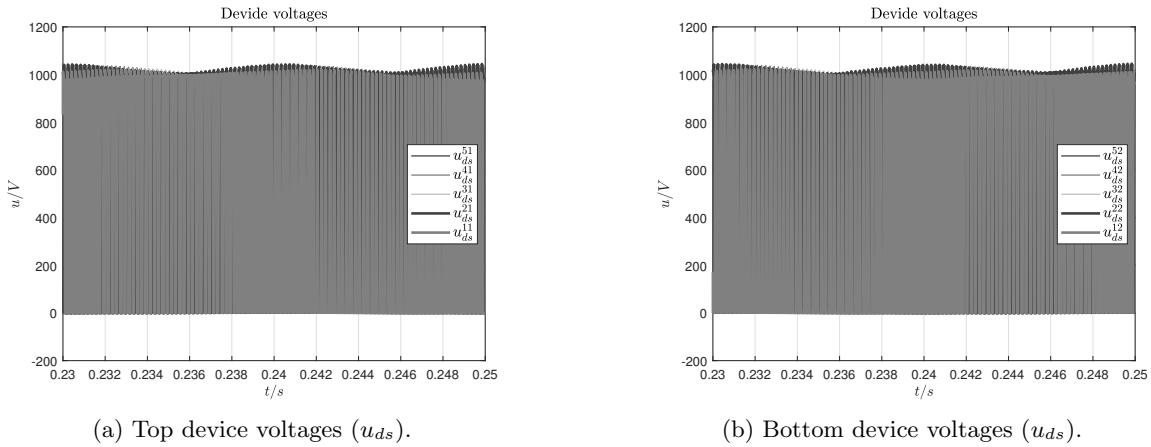
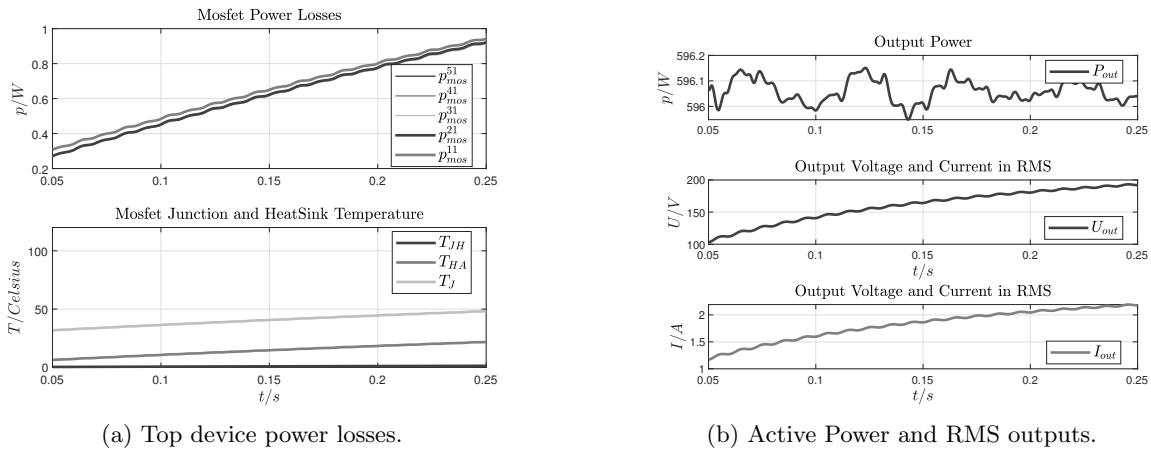


(a) Flying capacitor stage 5: current and voltage.



(b) Flying capacitor voltages.

Figure 16: Flying capacitor voltages, at $u_{dc} = 5$ kV.

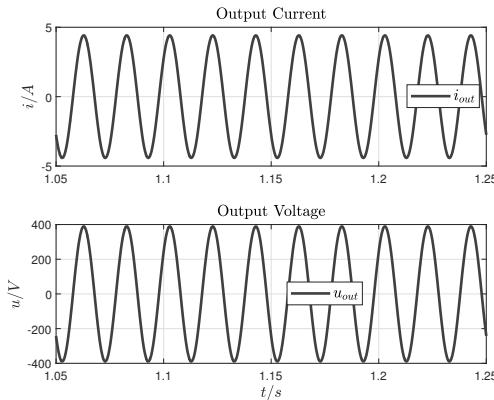
Figure 17: Device voltages (u_{ds}), at $u_{dc} = 5 \text{ kV}$.Figure 18: System Performance, at $u_{dc} = 5 \text{ kV}$.

4.2 High frequency open loop control at 3kV of input voltage

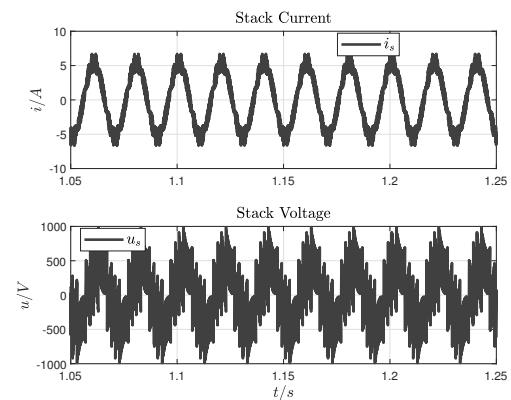
The following set of simulation results have been realized under the following conditions

- discrete time step at $t_c = 1 \times 10^{-8} \text{ s}$;
- open loop control;
- $u_{dc} = 3 \text{ kV}$;

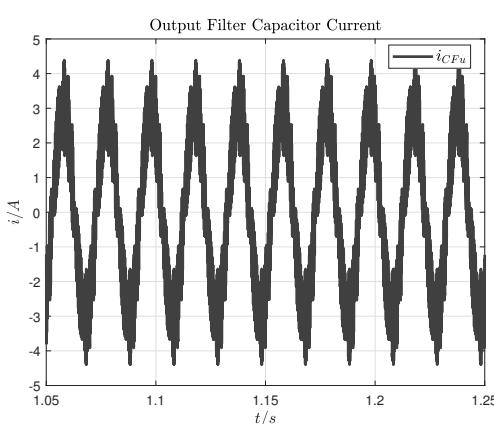
and they are intended for electronic layout evaluation.



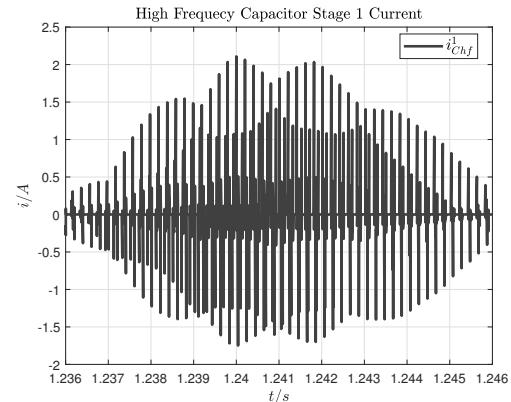
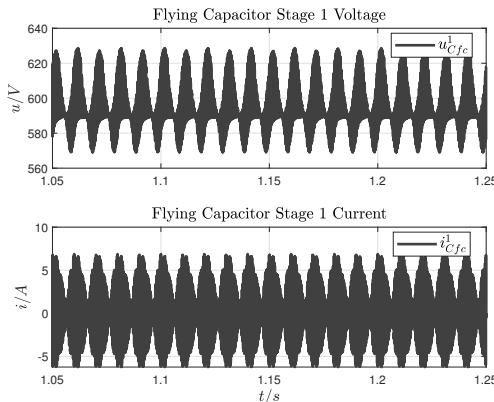
(a) Output current and voltage.



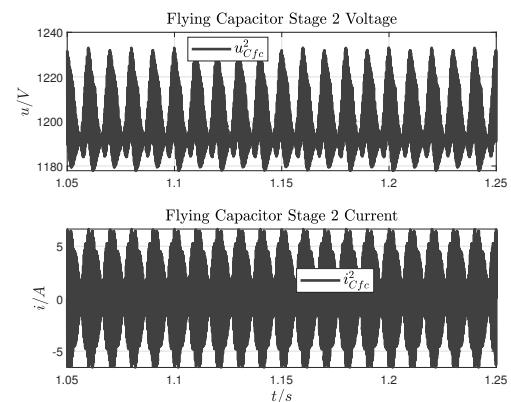
(b) Stack current and voltage.

Figure 19: Output current and voltage stages, at $u_{dc} = 3 \text{ kV}$.

(a) Output filter capacitor current.

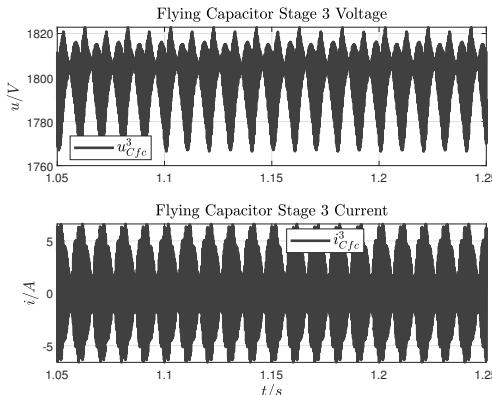
(b) High Frequency capacitor C_{hf}^1 current ($i_c^{rms} \approx 0.1 \text{ A}$).Figure 20: Output filter capacitor current and high frequency dclink current, at $u_{dc} = 3 \text{ kV}$.

(a) Flying capacitor stage 1: current and voltage.

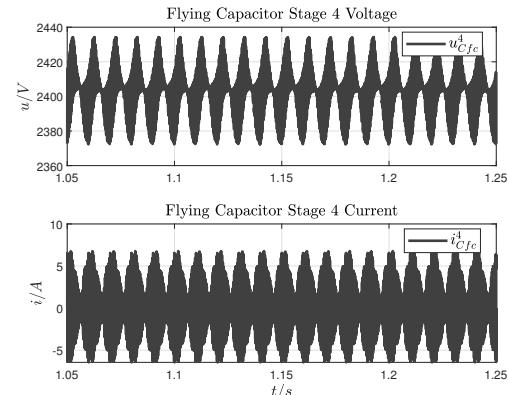


(b) Flying capacitor stage 2: current and voltage.

Figure 21: Flying capacitor stages 1 and 2, at $u_{dc} = 3 \text{ kV}$.

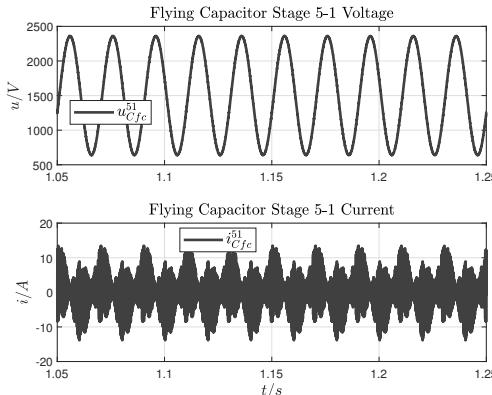


(a) Flying capacitor stage 3: current and voltage.

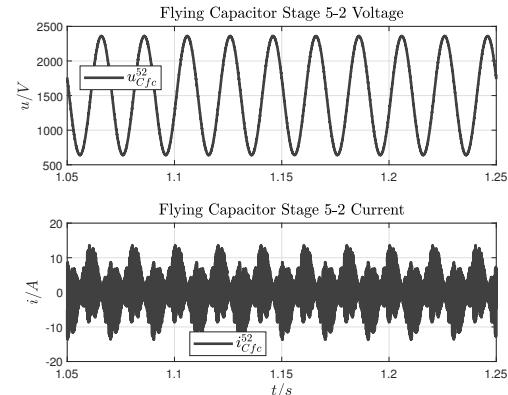


(b) Flying capacitor stage 4: current and voltage.

Figure 22: Flying capacitor stages 3 and 4, at $u_{dc} = 3\text{kV}$.

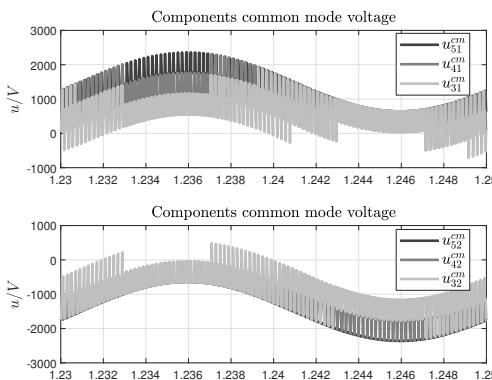


(a) Flying capacitor stage 51: current and voltage.

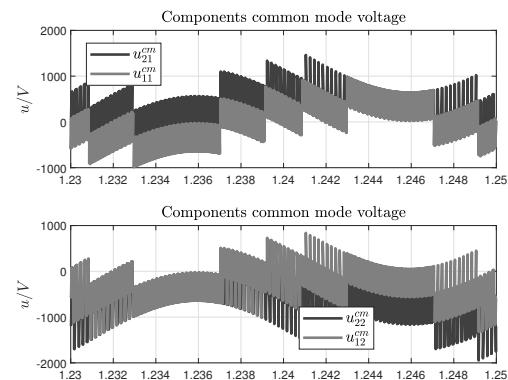


(b) Flying capacitor stage 52: current and voltage.

Figure 23: Flying capacitor stages 51 and 52, at $u_{dc} = 3\text{kV}$.

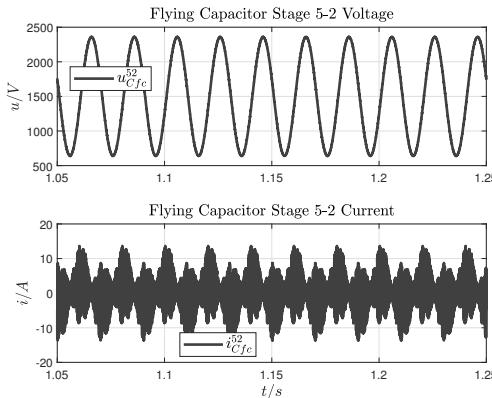


(a) Device common mode voltage (u_s): source ground voltage.

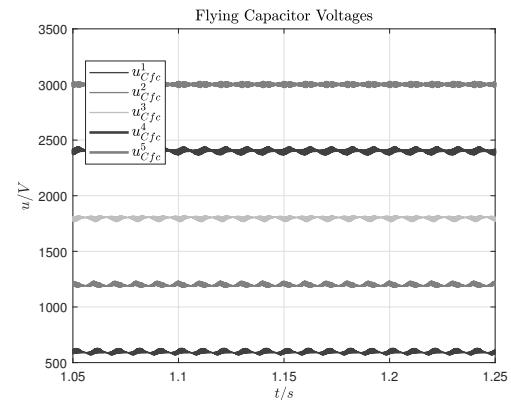


(b) Device common mode voltage (u_s): source ground voltage.

Figure 24: Device common mode voltages, at $u_{dc} = 3\text{kV}$.

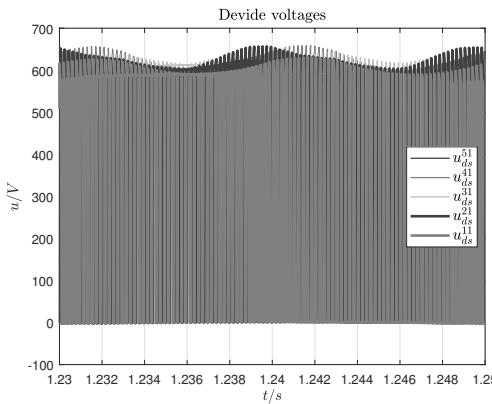


(a) Flying capacitor stage 5: current and voltage.

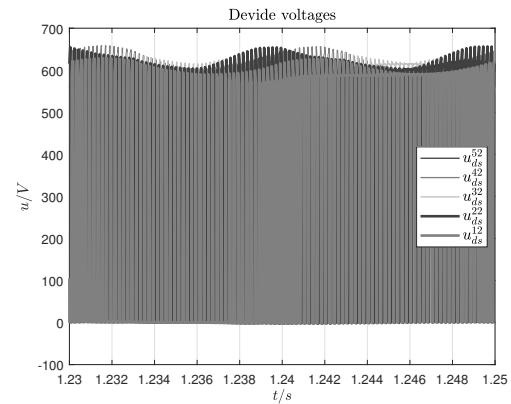


(b) Flying capacitor voltages.

Figure 25: Flying capacitor voltages, at $u_{dc} = 3$ kV.

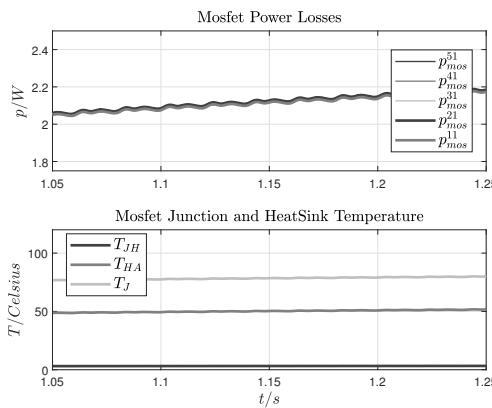


(a) Top device voltages (u_{ds}).

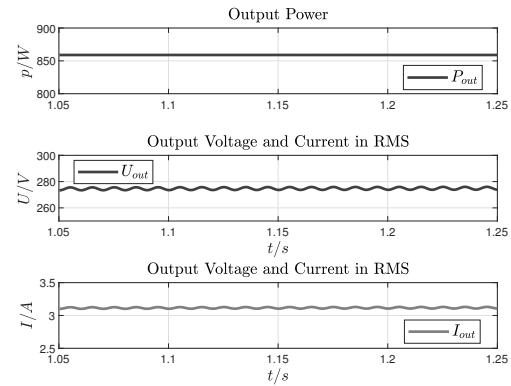


(b) Bottom device voltages (u_{ds}).

Figure 26: Device voltages (u_{ds}), at $u_{dc} = 3$ kV.



(a) Top device power losses.



(b) Active Power and RMS outputs.

Figure 27: System Performance, at $u_{dc} = 3$ kV.



4.3 Closed loop control

The following set of simulation results have been realized under the following conditions

- discrete time step at $t_c = 1 \times 10^{-6}$ s;
- closed loop control;
- $u_{dc} = 3$ kV;
- Combination of passive precharge and slope down modulation index is performed from $t_0 = 0$ s to $t_1 = 0.5$ s;
- No load voltage control is performed from $t_1 = 0.5$ s to $t_2 = 1.0$ s;
- At $t_2 = 1.0$ s a 500W step load is connected to the inverter;

and they are intended for control performance evaluation.

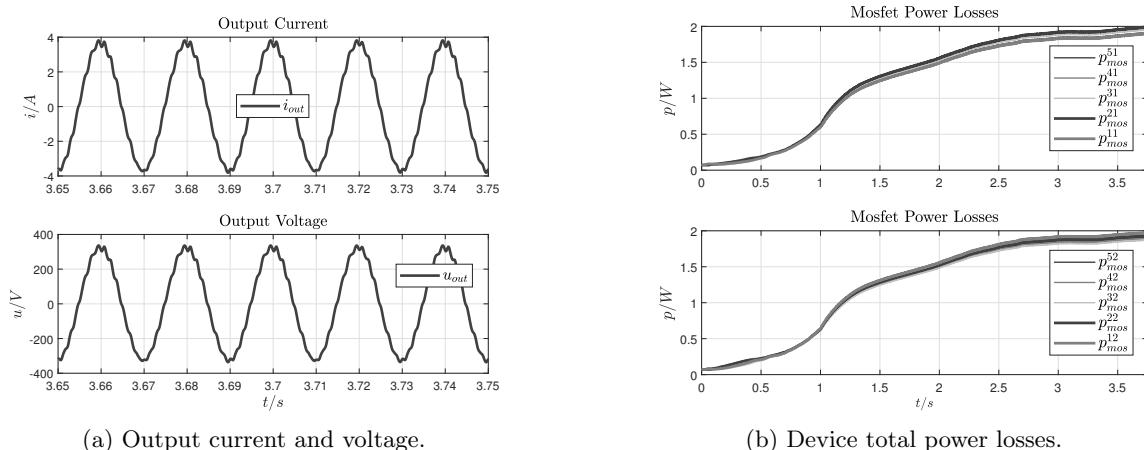


Figure 28: Performance analysis.

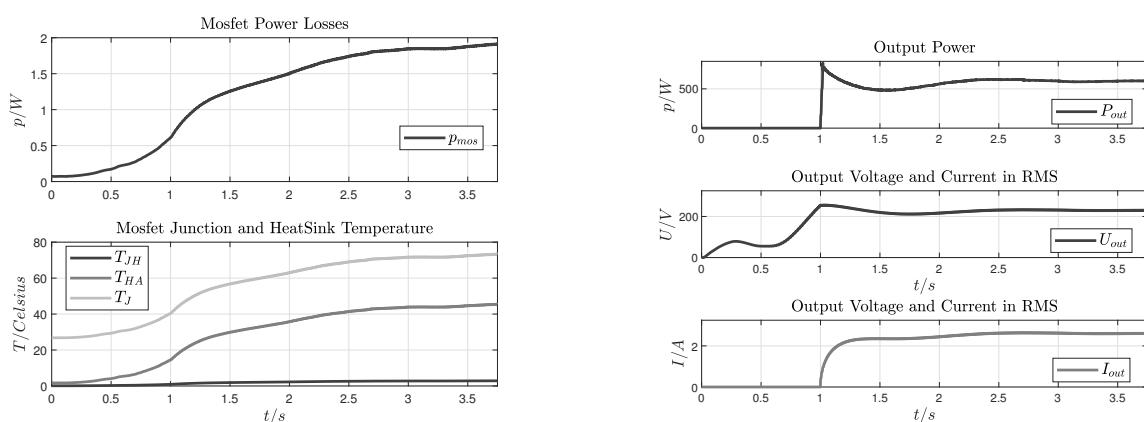


Figure 29: Performance analysis.

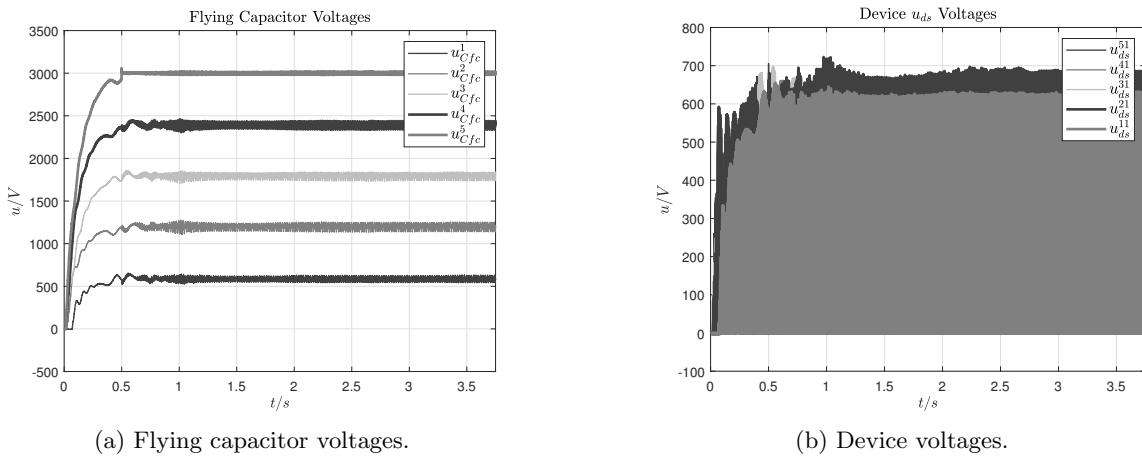


Figure 30: Performance analysis.

References

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