Jun 27, 2024 | RV Performance Events TG

Attendees: tech.meetings@riscv.org Dmitriy Ryabtsev Beeman Strong

Notes

- **Attendees**: Dmitriy, Beeman, Snehasish, Bruce, MattT, Greg
- **Slides/video** here
- Believe GEN.CYCLES should stop when hart is in wait state
    - Per priv spec, it seems mcycle doesn't do this? Should it?
        - Regardless, believe GEN.CYCLES can depart from mcycle behavior. Use the same clock, but stop at different times.
    - Otherwise GEN.CYCLES could overflow while hart is waiting, may be unexpected
- Per-hart cycles
    - Long discussion…
    - Other events are per-hart, so using per-core cycles (GEN.CYCLES) will make per-cycle ratios look really bad
        - Arguably can use this to know that you have a "noisy neighbor" sharing the core, but in many cases user doesn't know whether running ST or MT or MC
    - For per-hart cycles, specifying how to split cycles across harts is very complicated, depends upon implementation
    - Evenly distributing cycles across harts is what Intel does. But in cases where one hart uses more resources than the other, this too can result in misleading stats
        - Would probably be better to use slots than cycles, since slots are more granular. Can have some slots in the cycle allocated to one hart, and some to another.
        - But users are accustomed to per-cycle stats (e.g., IPC), so probably should have something
    - Recommend having a per-hart cycles events, but leave it up to implementations how to apportion cycles across harts in the core
        - Include guidance. Evenly distributed is the fall-back method, but could base it on allocation/dispath cycles, retire cycles, etc.
- TMA
    - TOPDOWN.SLOTS can be event or metric, for now list SLOTS_V2 as the latter but it won't remain
        - Same for BAD_SPEC
    - For SMT, there is some art to allocating unused (FE_BOUND or BE_BOUND) slots per hart
        - If only dispatch slots to one hart per cycle, then it's easy. But if not, up to implementations to figure out how to do it best.

        - If use evenly distributed cycles * pipeline width, such that each hart counts half the slots for TOPDOWN.SLOTS, there can be cases where we dispatch/retire more uops than the “total slots” count. If one hart is mostly stalled and the other is getting most of the resources. Hence a more precise method to count TOPDOWN.SLOTS is much preferred.
            - For SMT, probably want to have TOPDOWN.SLOTS be an event, or a formula only if have an accurate GEN.CYCLES.HART apportioning cycles at dispatch
    - On a ITLB or I$ miss after mispredict, is that FE_BOUND vs BAD_SPEC?
        - In this example BAD_SPEC. Recovery cycles is a count of cycles from fetch to issue, which would count through those misses
        - Agree with that approach, cleaning up the mispred may allow any miss latency to be hidden
    - MetricThreshold is guidance on what value is problematic, e.g. for TMA L1 percentages
    - Do we want more lower-level events to be standardized? **Out of time**, will take this up on the mailing list or next time

Action items

- ☐ Beeman Strong - May 23, 2024 - check on idea to count remote HITMs locally
- ☐ Beeman Strong - Apr 25, 2024 - check on how perf uses ScaleUnit