

Feb 1, 2024 | 📅 RISC-V Performance Events TG

Attendees: Beeman Strong Dmitriy Ryabtsev tech.meetings@riscv.org

Notes

- **Attendees:** Dmitriy, Beeman, Ved, Atish, Greg, Bruce, Chun
- **Slides/video** [here](#)
- Intros of acting chairs
- Review preliminary charter:

The RISC-V hardware performance monitoring counters (Zihpm) provide support for counting programmable performance events. Such events can provide insights into software execution behavior, insights that are critical when tuning a profiled workload. However, no performance events are standardized, which means profiling tools must comprehend a custom set of events specific to each hardware implementation. This prevents profiling tools from offering general-purpose, event-based analysis capabilities that can be employed regardless of the underlying hardware implementation.

The Performance Events TG will develop an ISA extension that includes a set of standard performance events and metrics (or formulas of events). For each standard event, the name and the precise hardware behavior associated with it will be specified, though the event selector value associated with the event will be left up to implementations. For each standard metric, the name and event formula, including the names of the constituent events, will be defined.

The TG will consider whether RISC-V-specific changes are needed to standard JSON file formats used by tools to map event names to event selector encodings, and to map metric names to event formulas. The TG will further prototype the end-to-end solution using Linux perf and Spike, ensuring that perf can properly translate event and metric names, and that, for deterministic events and metrics, the resulting counter and metric values match expectations.

- Should this be an ISA extension?
 - Event selectors are part of priv ISA, but we don't specify event selector values
 - No actual ISA specified here, specifying names and formulas
 - Standardizing a HW/SW ifc, maybe don't need to call it a HW or SW non-ISA extension
 - If non-ISA, what spec covers it? Will priv spec refer to it?
 - Could at least have a non-normative reference to it in priv spec
 - If non-ISA, could be required in platform spec but not profile
 - For perf, this is a key/value pair, event names/encodings. By standardizing event names, tools can use standard names with predictable behavior.
- Discussed at LPC, asked why not do it in the driver like other architectures? Argued that RV will have so many vendors it will be a mess.

- Why not standardize encodings?
 - Not needed, since we have JSON mechanism
 - Allows vendors flexibility in selecting encodings that suit their implementations
 - Also allows some flexibility in metrics, where formulas may differ across implementations (e.g., slots)
 - Charter currently says metrics will specify event formulas, but maybe we want to leave this flexible
 - In some cases an event could instead be a metric/formula, e.g. if 4 events add up to 1 then provide 3 events and the 4th is 1 minus the sum of the others. Or BAD_SPEC could be 0 if don't have a branch predictor.
 - Events should have a clear definition, while metrics may have more flexibility?
 - Some metrics should be firmly defined (e.g., cache miss rate), while others may not
 - Should probably include this in the charter
- Should the TG consider defining when events like cycles count, e.g. with WFI? Or what kind of stall cycles increment for PAUSE?
 - Yes
- Other OSs and tools may not have JSON files, e.g. Android. May come up during charter review.
 - Android uses simpleperf, very few events where events and encodings are hardcoded in header file.
 - Android OS often comes from vendor
 - Could use DT or something other than JSON
 - Do we need a discovery mechanism for SW? Register-based mechanism to get encodings?
 - May have an opportunity to do Android right, just starting
 - Can say anything beyond JSON is out of scope of TG
- Microcontrollers may have 5 standard events, OOO cores may have those + many more
 - Could have those 5 required, and others optional
 - Or could say this TG is targeting application processors?
 - Out of time, discuss on email

Action items

- ☐ Revise charter and share on email list - dmitriy.ryabtsev@syntacore.com
- Beeman Strong