Feb 29, 2024 | RISC-V Performance Events TG

Attendees: Beeman Strong, Dmitriy Ryabtsev, tech.meetings@riscv.org

Notes

- **Attendees**: MattT, Dmitriy, Ved, Beeman, BruceA, DerekH, Guillem, Shashank, Snehasish, DaiH, Robert, Greg, Hammad
- **Slides/video** here
- Reviewing revised charter (here)
- Clarified that will specify event names and meanings, not event selector encodings
    - Hence non-ISA
    - What if implementations want to be able to count multiple events in a single counter?
        - Implementations are free to do that. Can either specify the combination events in the JSON file, or have a custom mechanism based on encoding
- How to discover if the extension is implemented?
    - Unified Discovery should be able to support non-ISA/system-level stuff
- How do tools find the JSON file?
    - Use arch_id/vendor_id/imp_id to specify the right one? Or do we need more?
        - Arch_id is major uarch, imp_id is steppings, though flexible
        - Those should be sufficient to identify the right file
- What if an implementation has some HPMs that count a fixed event?
    - JSON will accommodate that. Each event has list of which counters support it, so fixed-event counters will only show up in the event it counts
- Does this include system/SoC events too? Charter isn't clear
    - System events are very important too
    - Should probably have a separate TG that defines SoC counters/eventsels and events
        - Have discussed this with DTPM SIG
    - Worried about serialized TGs, taking twice as long if two TGs
        - But don't want scope of this TG to creep, will also lead to delays
        - TGs don't have to be serialized, even if coordinating
    - May have system components provided by different vendors
        - So one extension can't say whether all components support standard event, must have separate extensions
    - Some important metrics may be counted in different places for different implementations
        - E.g., DDR BW could be in fabric, memory controller, etc
        - Something like platform spec may require the metric, with flexibility on where it lies?
    - This are not quick conversations, need a holistic approach
    - Hart events is a big enough topic for its own TG
    - Are hart-only events that useful, without system-level view?

        - Yes. System-level is important, but there's lots to do with CPU events. Most developers are accustomed to CPU events.
    - DTPM SIG should define the strategy for system-level events
- Do we need to call out including vector in the charter?
    - If so, why not call out integer, FP, load/store, etc?
    - Don't need to dive too deeply in the charter, CPU scope should cover all of the above implicitly
- May want to specify event discovery first, then the events themselves. Then designs can use the infra for their custom events.
    - JSON file format exists, can use it today
    - TG may suggest additions
- Dmitriy to update charter PR per discussion today, send to list for offline approval

Action items

- [ ]