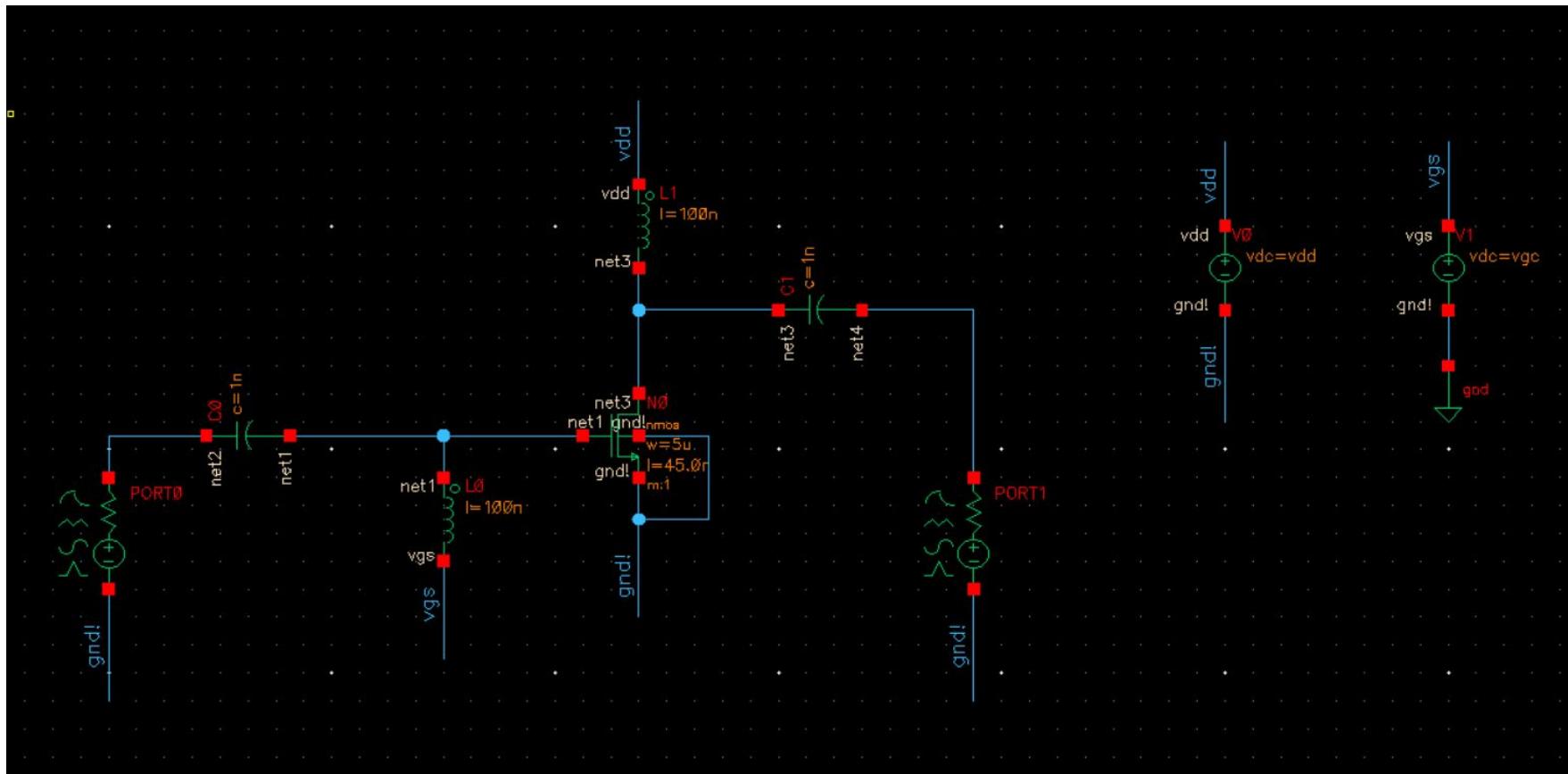




Fmax Simulation - Design





Fmax Simulation - Design Parameters

1. Transistor Dimensions:
 - Width: 5um
 - Length: 45nm
2. VDD: 1V
3. Bias Voltage: 800mV
4. Gate Capacitance: 1nF
5. Drain Capacitance: 1nF
6. Gate Inductance: 100nH
7. Drain Inductance: 100nH

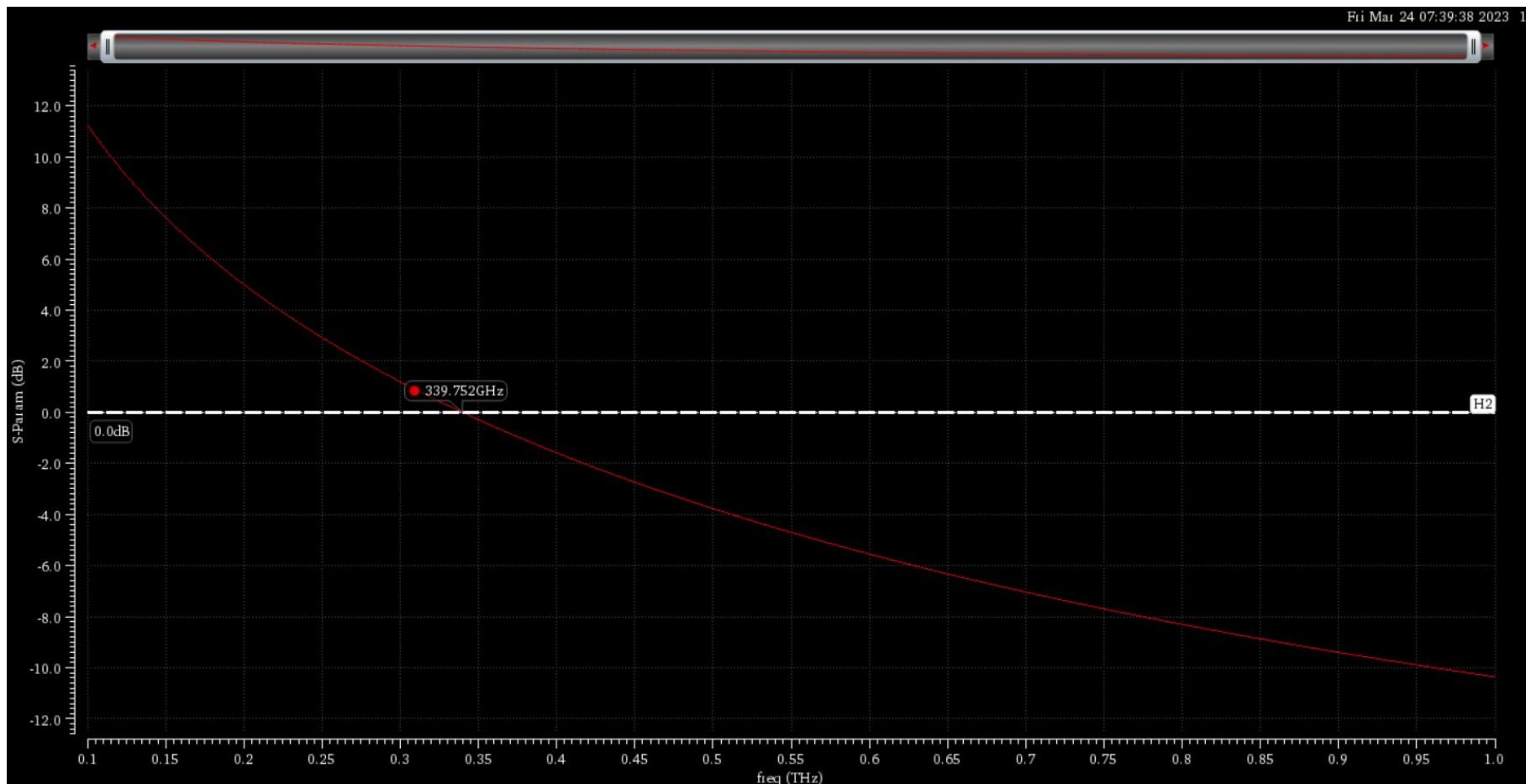


Fmax Simulation - Expression

```
dB10[abs(((ypm('sp 2 1)-ypm('sp 1 2)) * (ypm('sp 2 1)-ypm('sp 1 2)))) / abs((4 * ((real(ypm('sp 1 1)) * real(ypm('sp 2 2))) - (real(ypm('sp 1 2)) * real(ypm('sp 2 1)))))))]
```



Fmax Simulation - Output





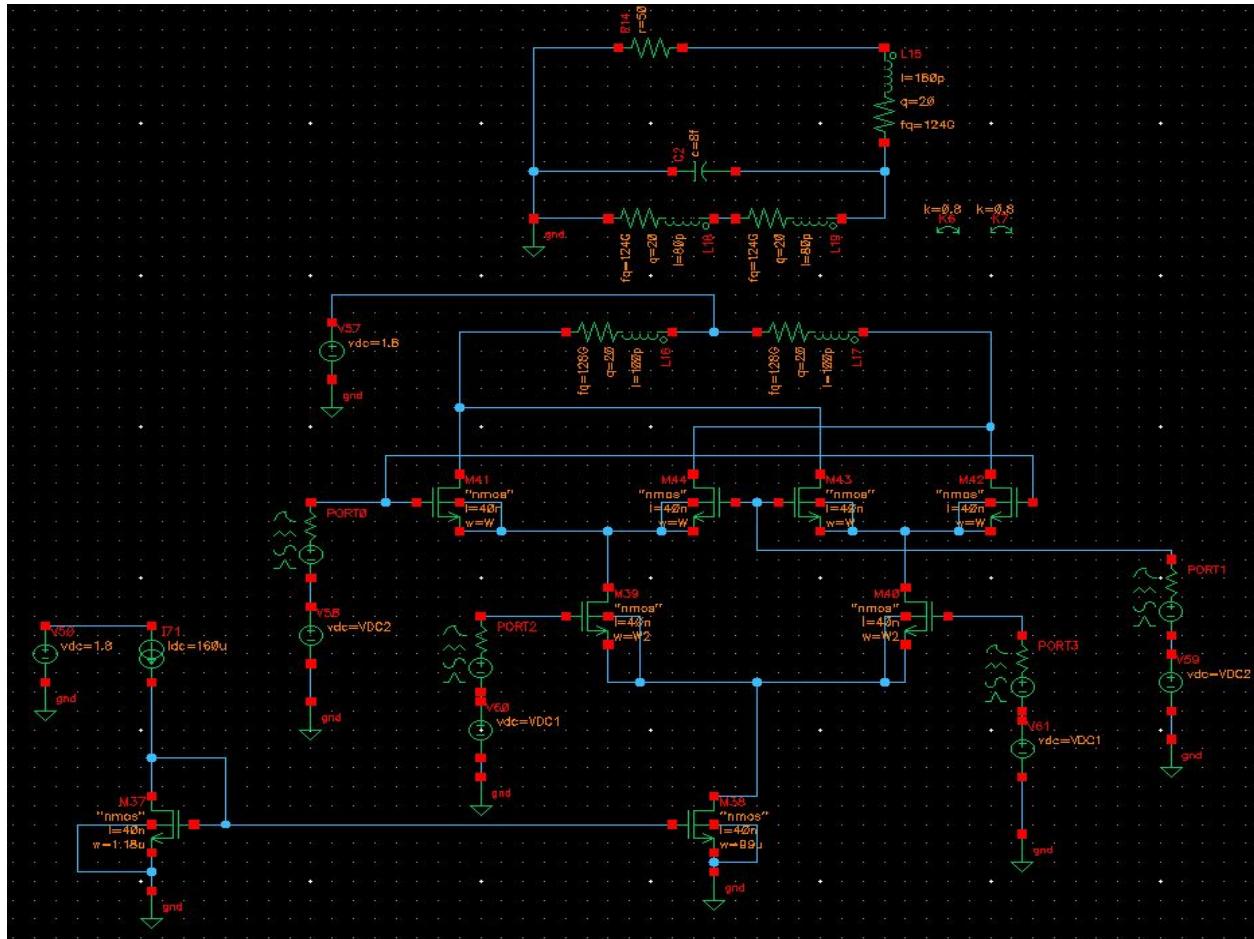
Fmax Simulation - Expression

$F_{max} = 339.752\text{GHz}$

Frequency chosen further simulations: 124GHz



Active Frequency Doubler





Active Frequency Doubler

Architecture : Gilbert Cell

Upper Transistor Pairs : 10u/40n

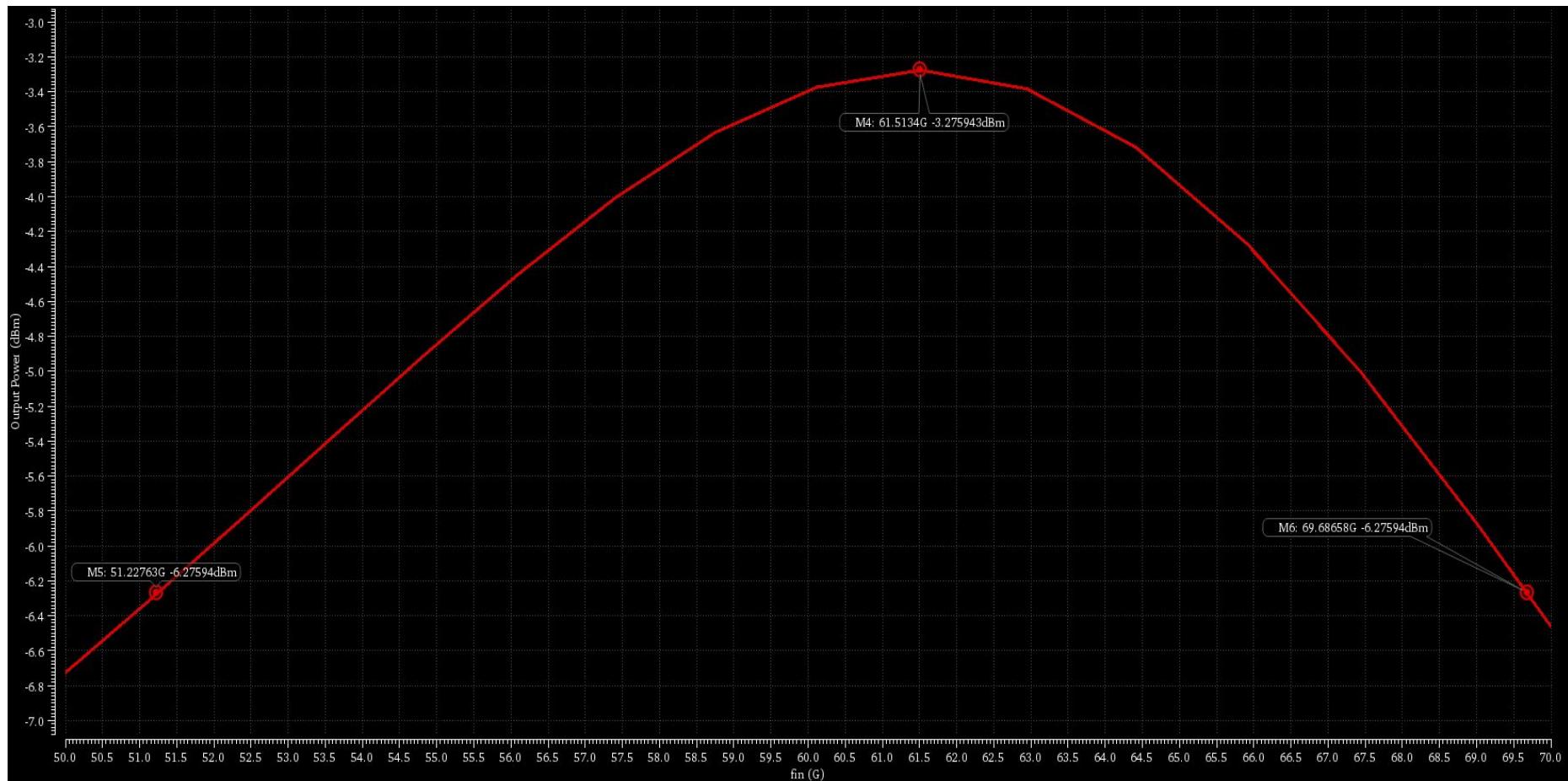
Lower Transistor Pair: 16u/40n

Matching Type : Transformer / Balun

Transformer Ratio : 100p/80p - k=0.8 - Q: 20



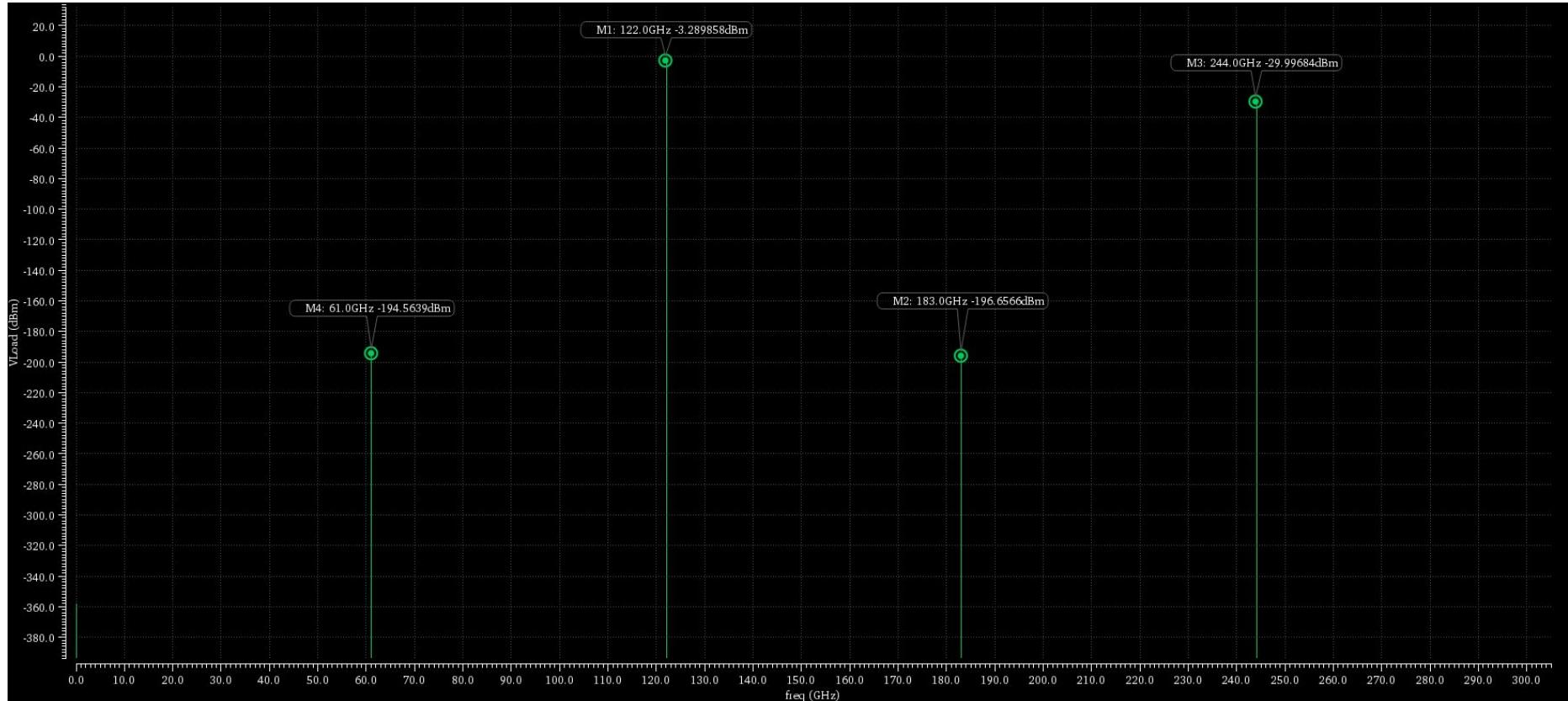
Active Frequency Doubler



HB Simulation : Output Power vs Input Frequency



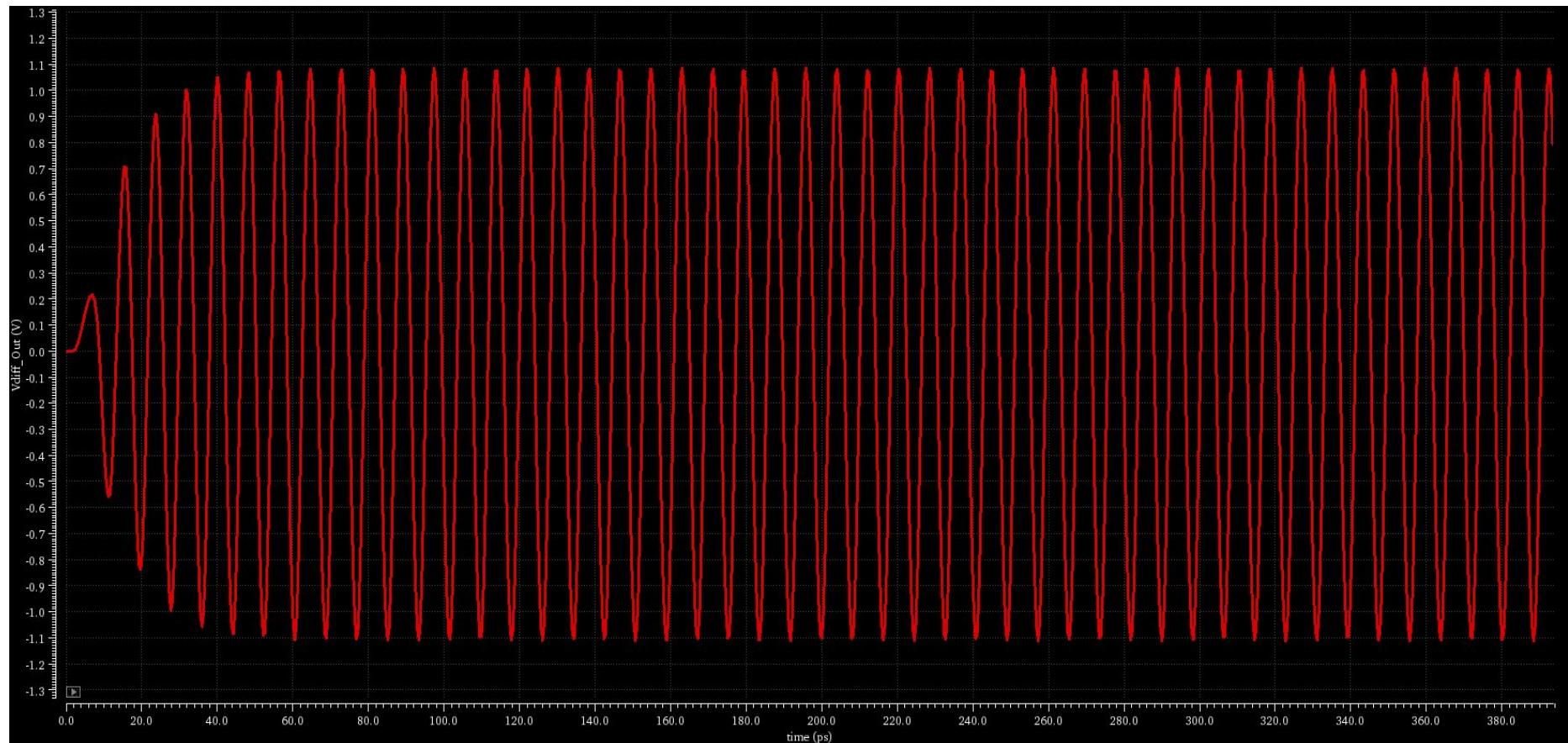
Active Frequency Doubler



HB Simulation : Output Spectrum for Fin = 61GHz



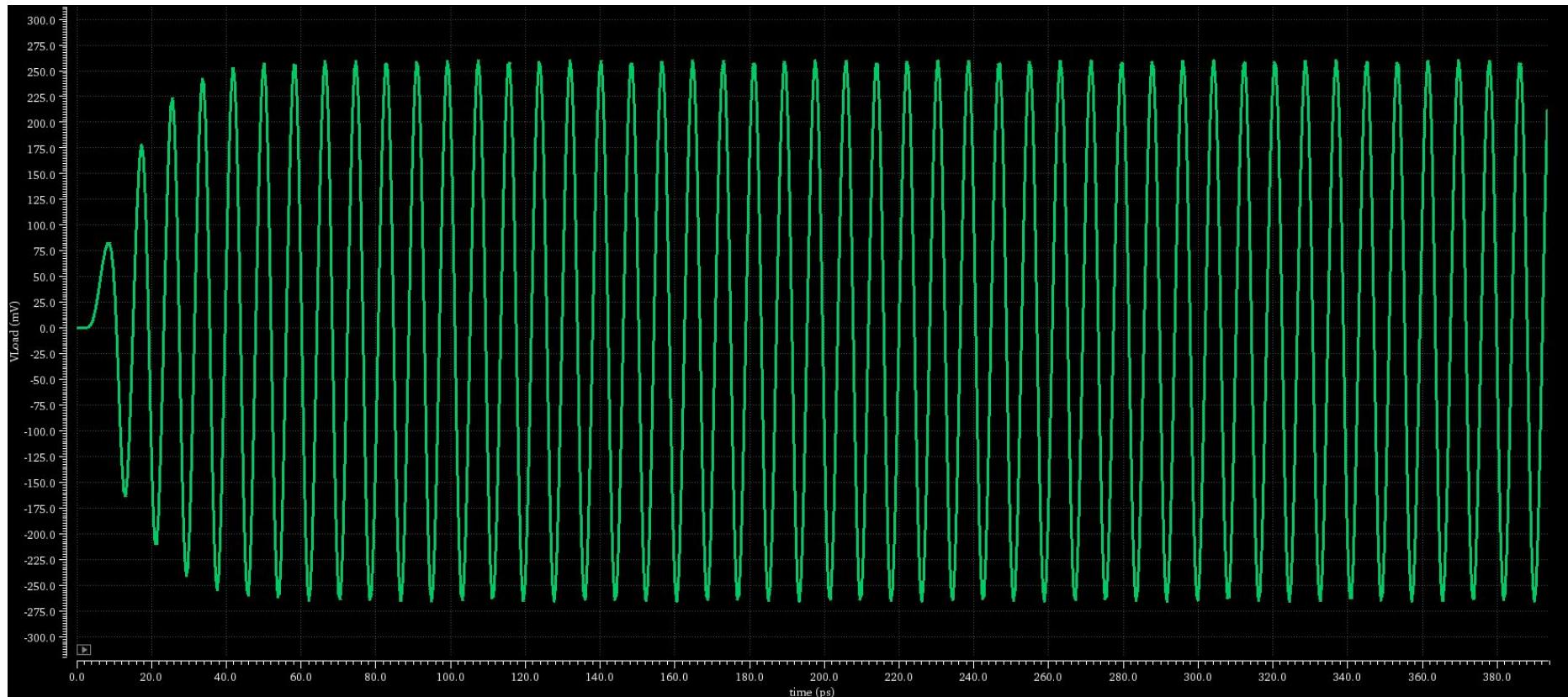
Active Frequency Doubler



HB Simulation : Output Differential Swing for Fin = 61GHz



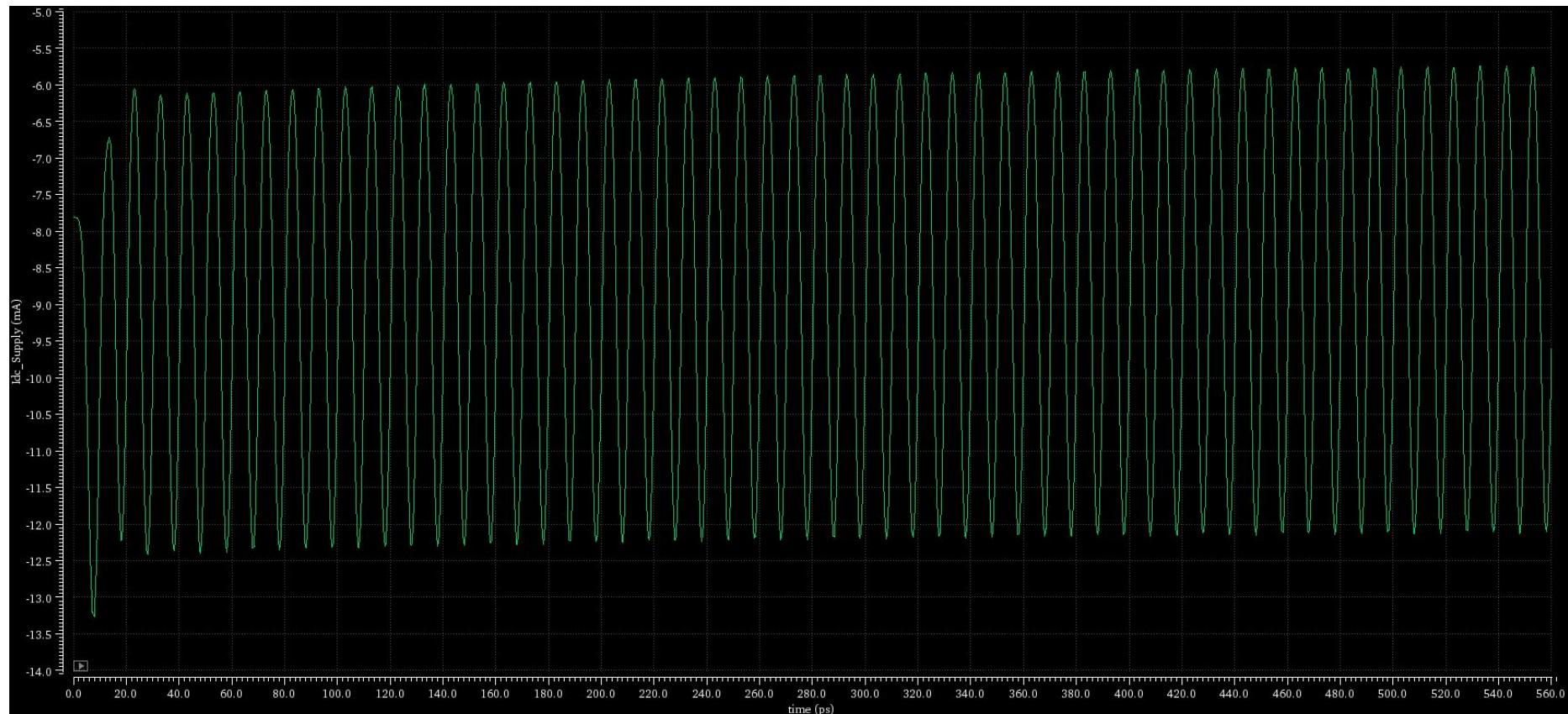
Active Frequency Doubler



HB Simulation : Output Swing for Fin = 61GHz



Active Frequency Doubler



HB Simulation : Supply DC Current for Fin = 61GHz

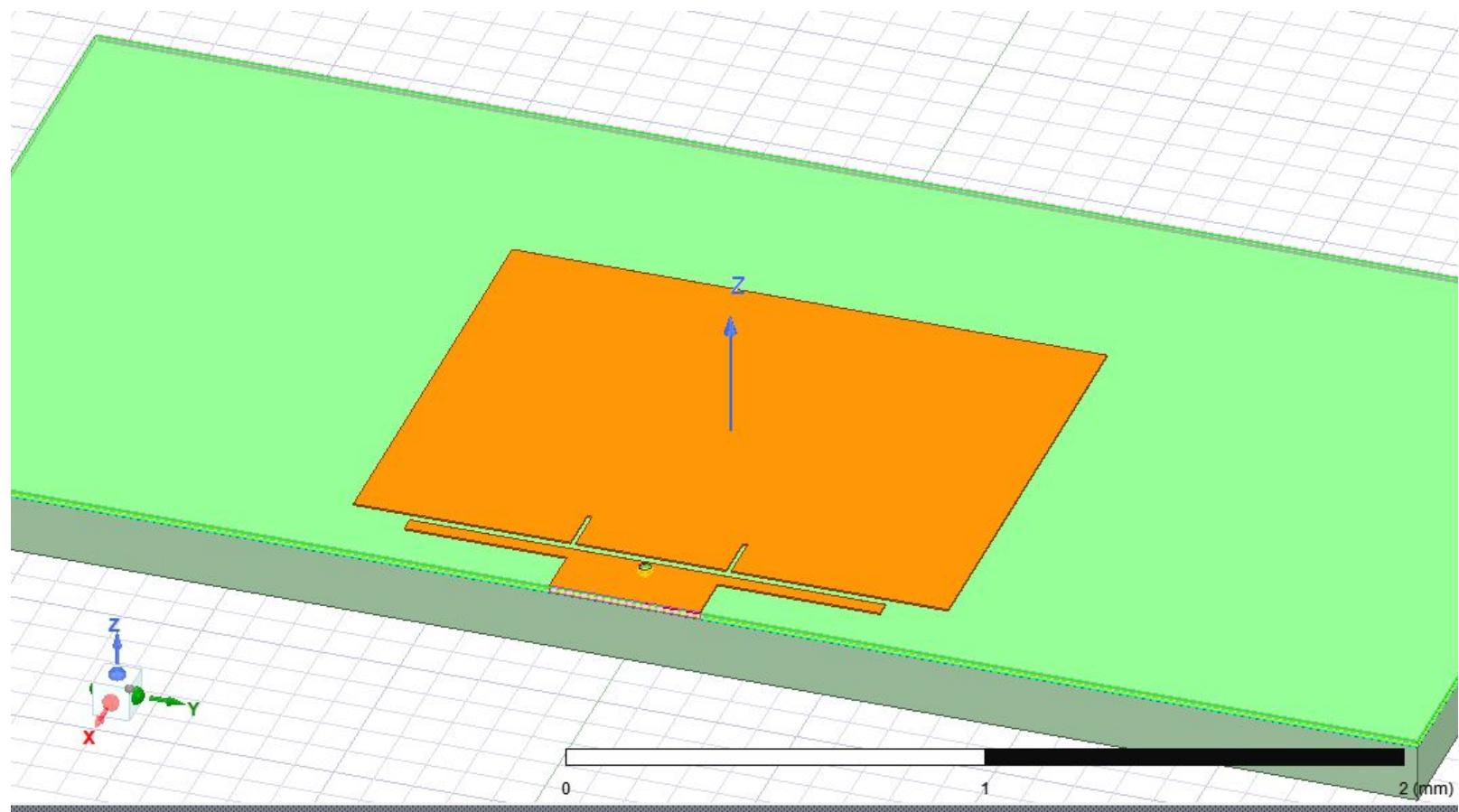


Active Frequency Doubler

	Required	Achieved
input power	6dBm	6dBm
output power	-8dBm	-3.2dBm
BW	12 GHz	36 GHz
DC Power Consumption	<50 mW	16.2 mW

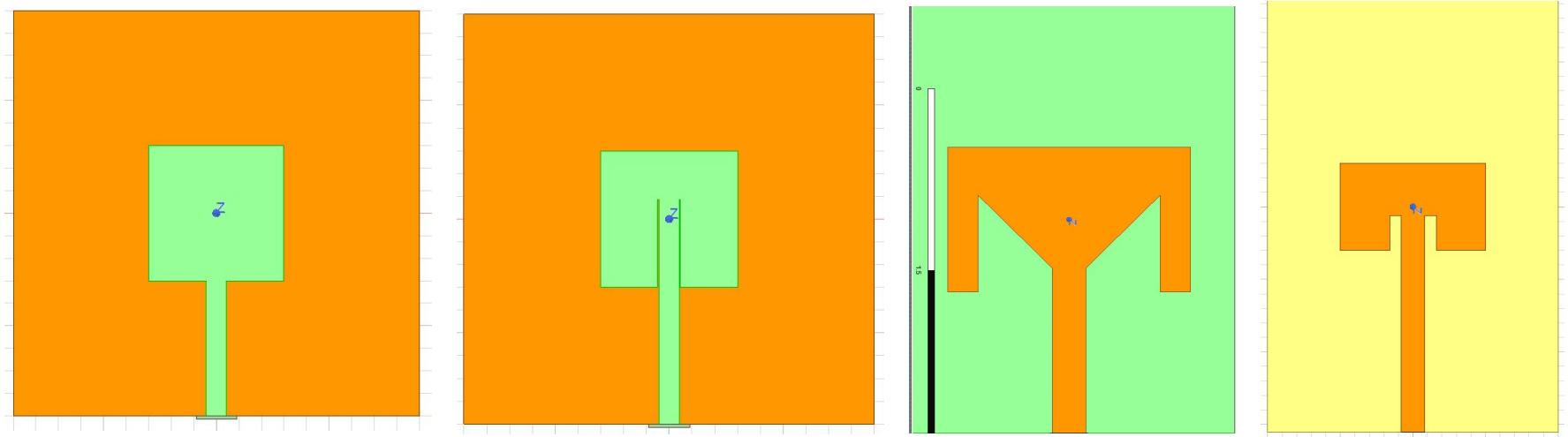


Patch Antenna





Patch Antenna- Previous Iterations

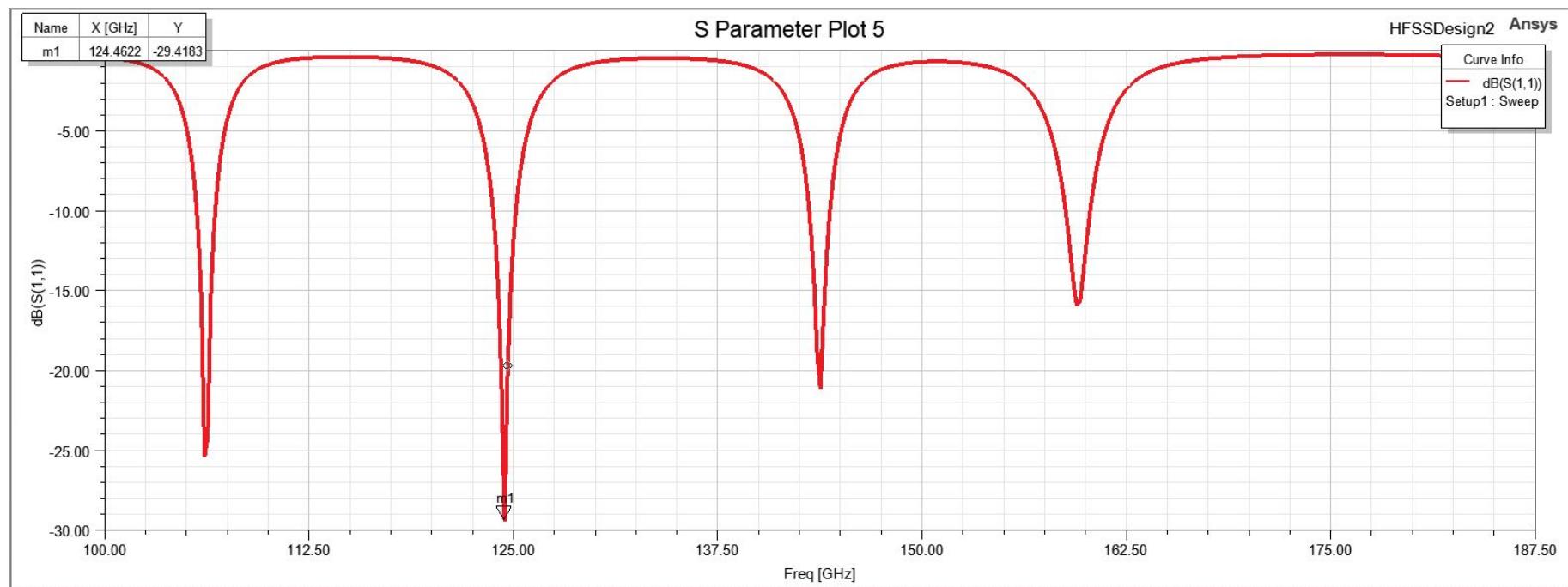


Problem:

- Interfering Frequency Harmonics
- Narrow Bandwidth



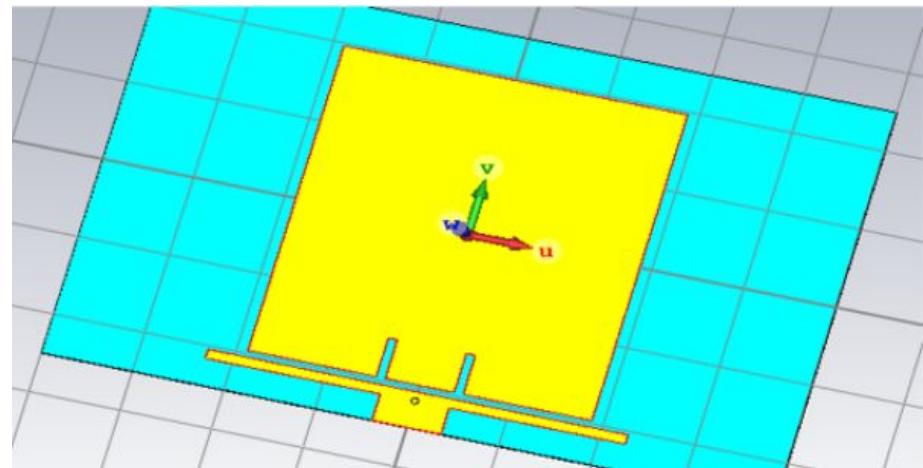
Previous Results





Proposed Design

- Quarter Length Resonators
 - provide good harmonic suppression
 - improve wideband performance





Design Characteristics

Patch Width

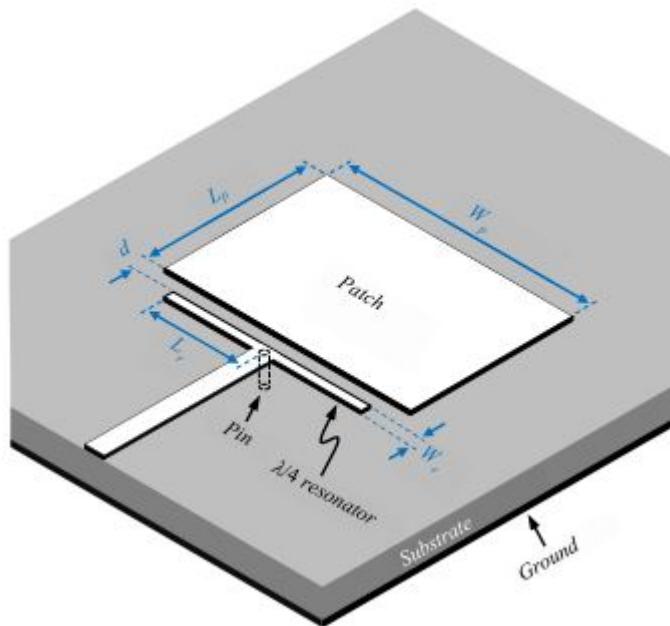
Can be a factor in optimization, differing from conventional patch antennas

Pin

Shortening pin on central plane suppress all even-order resonant modes

$\lambda/4$ resonators

form a coplanar distributed resonator



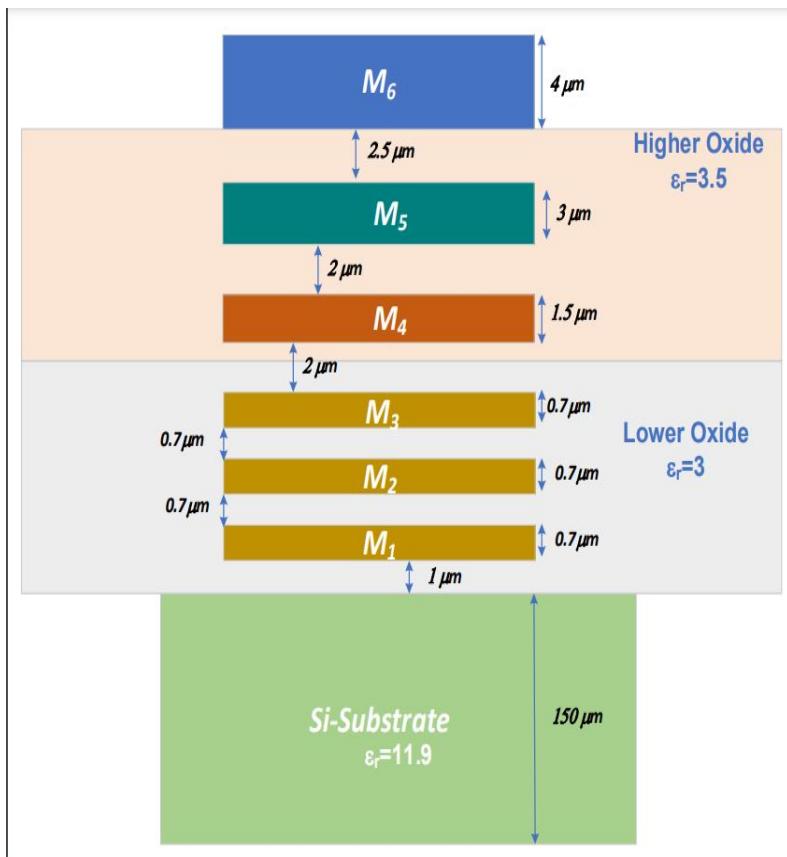
Gap Width

Optimized to make two resonant frequencies close to each other, combining into a single wideband

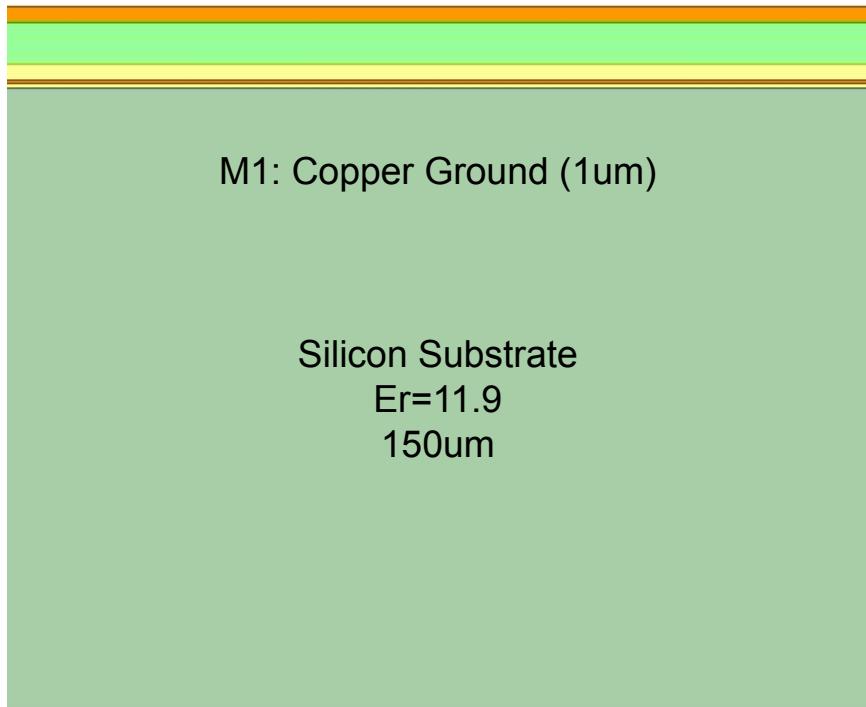
Suppress harmonic resonant modes (energy only transmitted at frequencies where both patch and $\lambda/4$ resonators are resonating)



Stack Up



M6: Copper Patch (4um)



M1: Copper Ground (1um)

Silicon Substrate
 $\epsilon_r=11.9$
150um



Calculations

$F_{max} = 311.67\text{GHz}$

$0.4F_{max} = 124\text{GHz}$

Frequency for antenna: 124GHz

$$\lambda = c/f$$

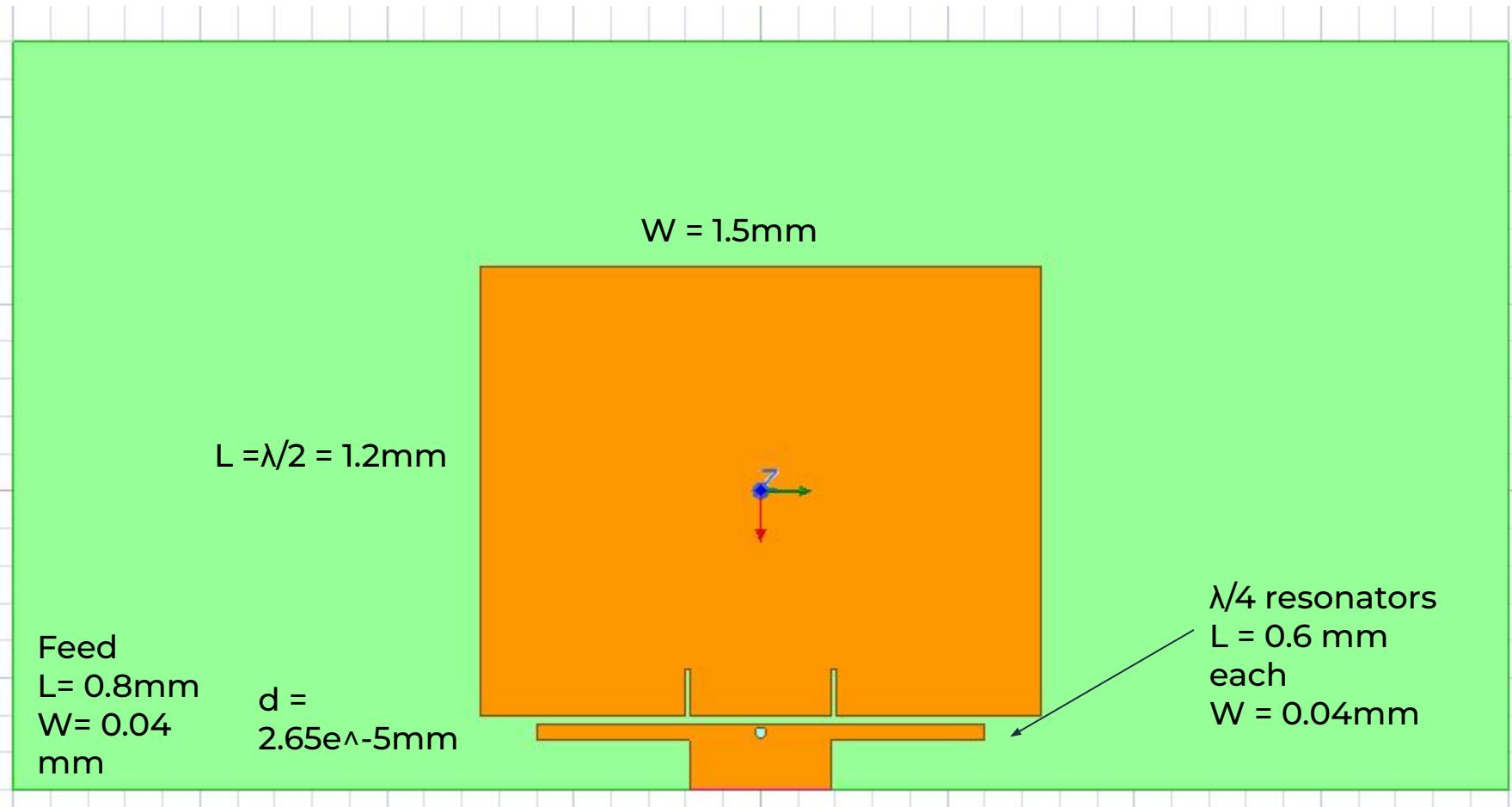
$$\lambda = \frac{c}{f} = \frac{3.0*10^8 \text{ m/s}}{124*10^9 \text{ 1/s}} = 2.419\text{mm}$$

$\lambda \sim 2.4\text{mm}$

$$\lambda/2 \sim 1.2\text{mm}$$

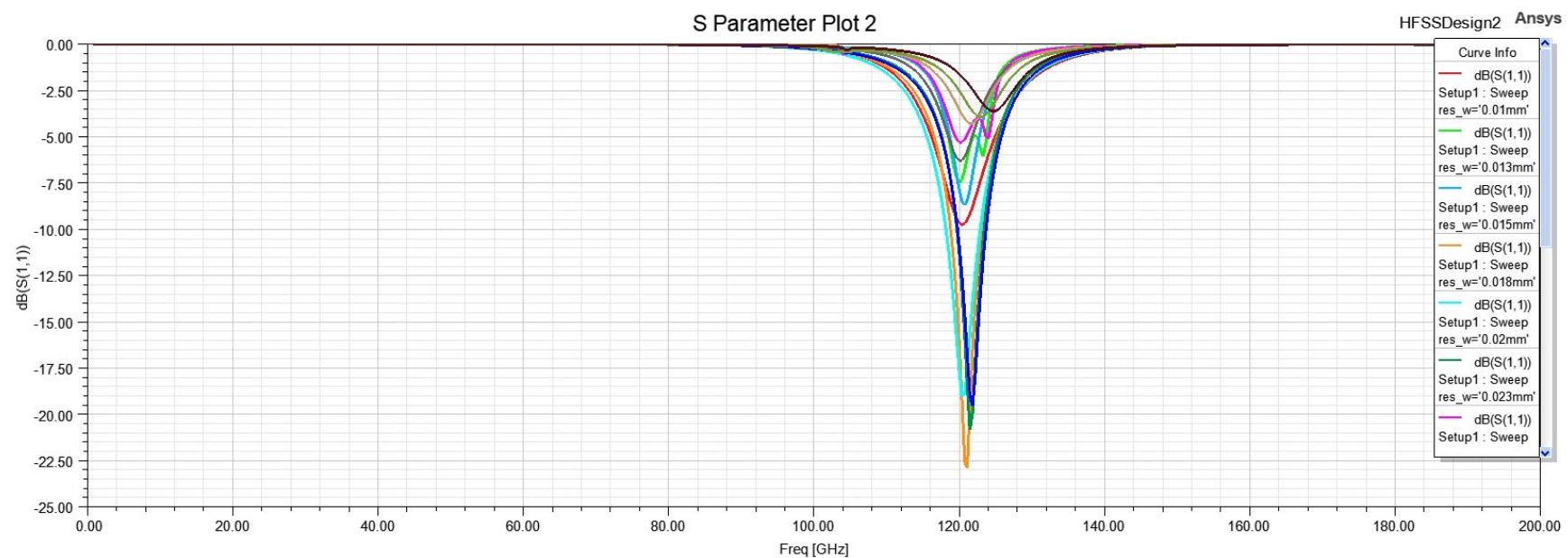


Patch Dimensions



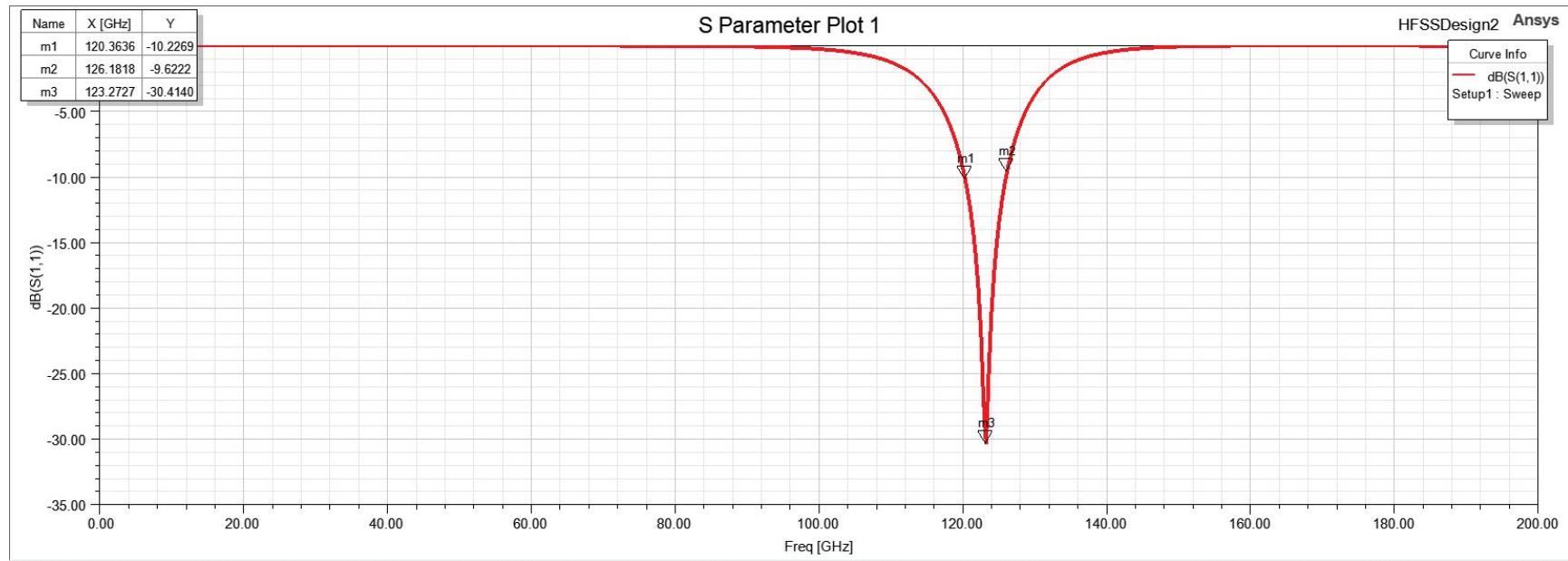


Optimetric Analysis





S Parameter Results



Goal: 5% of bandwidth below -10dB

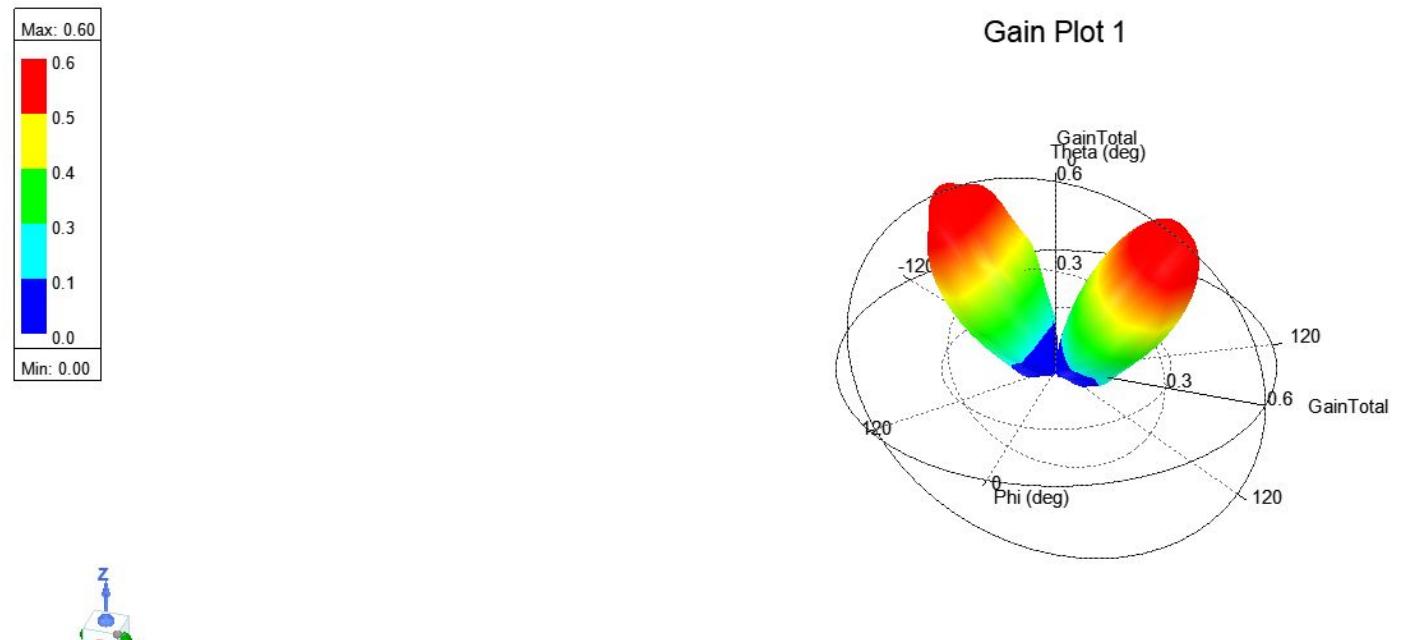
Center frequency: 124GHz

Lower frequency (-5%): 117.8GHz

Upper frequency (+5%): 130.2 GHz

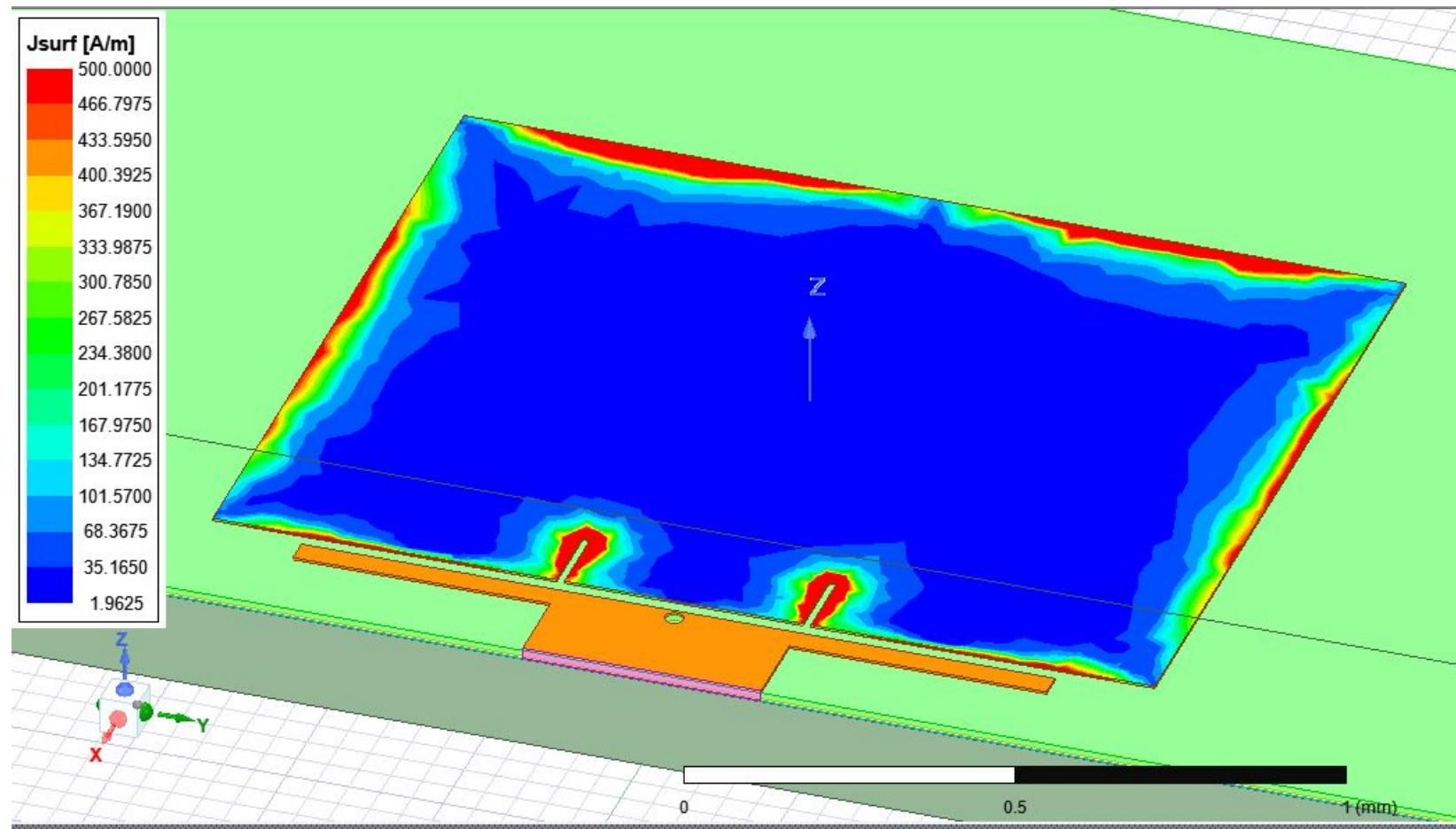


3D Polar Plot (105GHz)





J Field Results (105 GHz)





E Field Results (105 GHz)

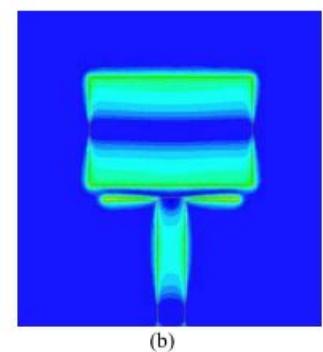
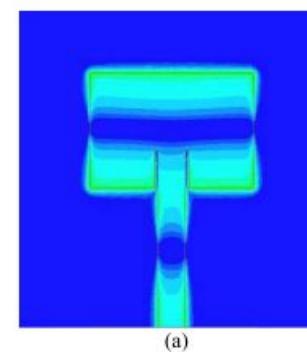
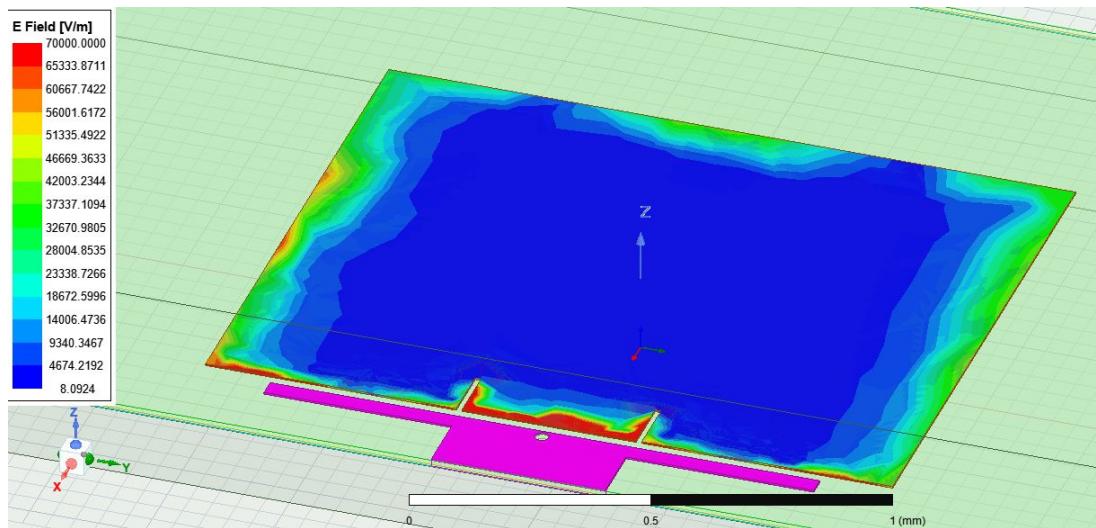


Fig. 7. Electric field distributions of two patches. (a) Traditional.
(b) Proposed.



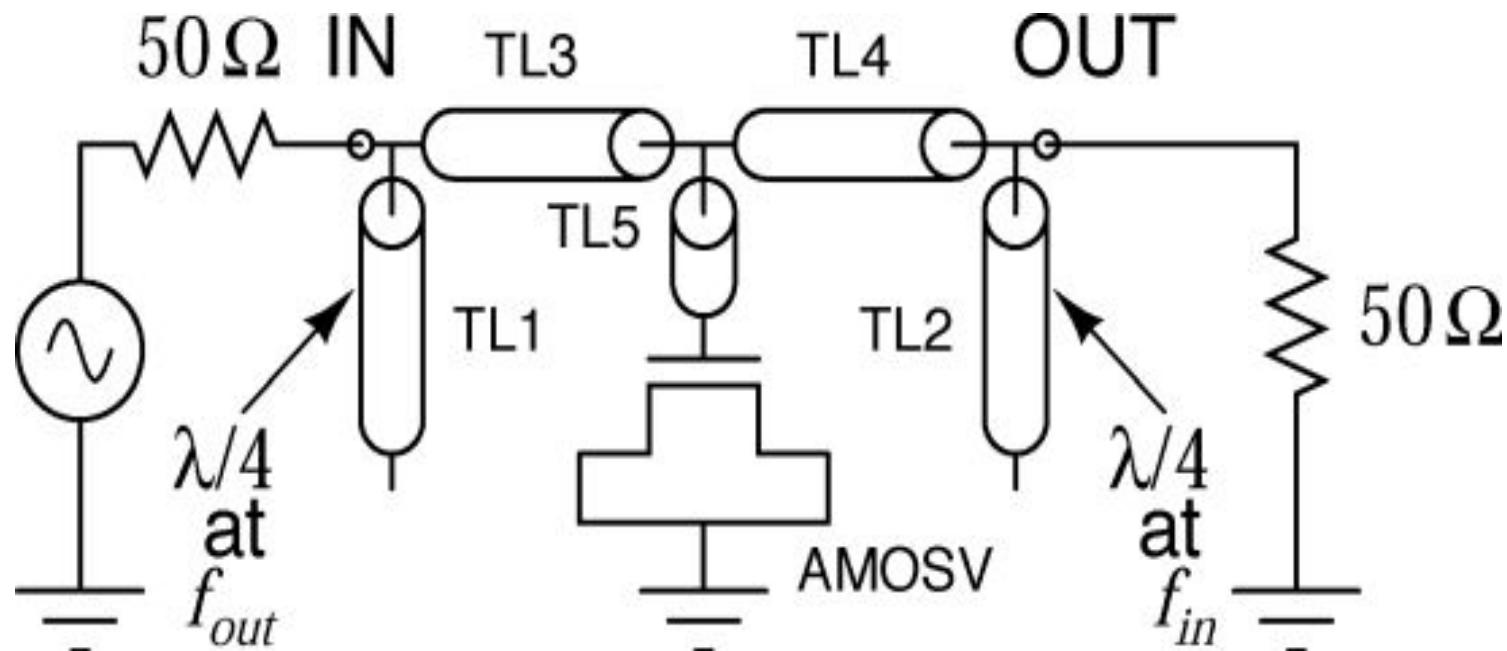
Further Improvements

- Further optimetrics to increase bandwidth
- Ensure current density, and electric field concentrated on radiating edge at 124GHz
- Wave port analysis



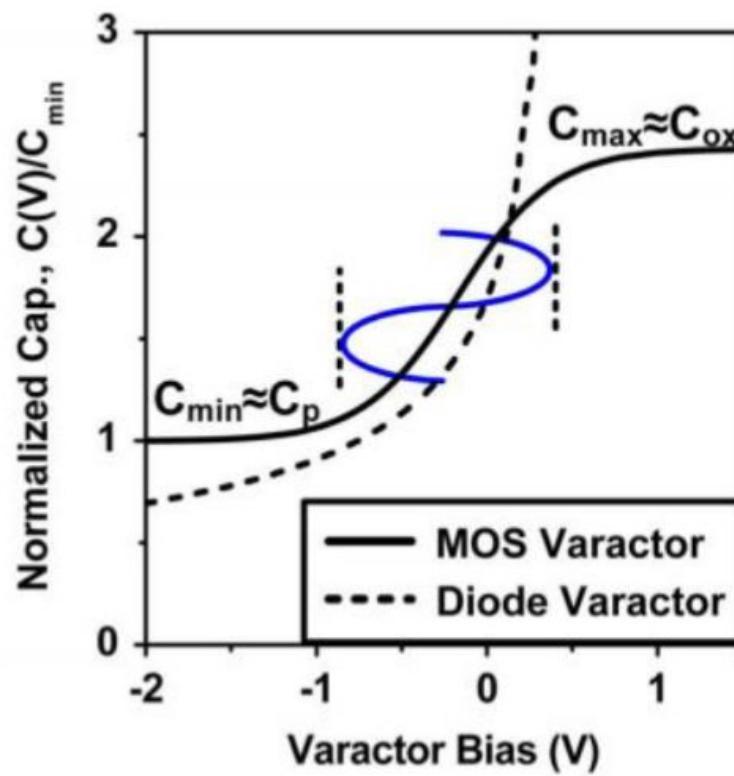
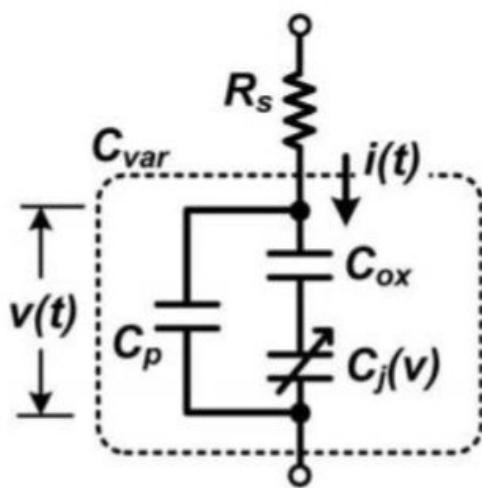
Passive Frequency Doubler

Reference: “100 GHz Parametric CMOS Frequency Doubler”



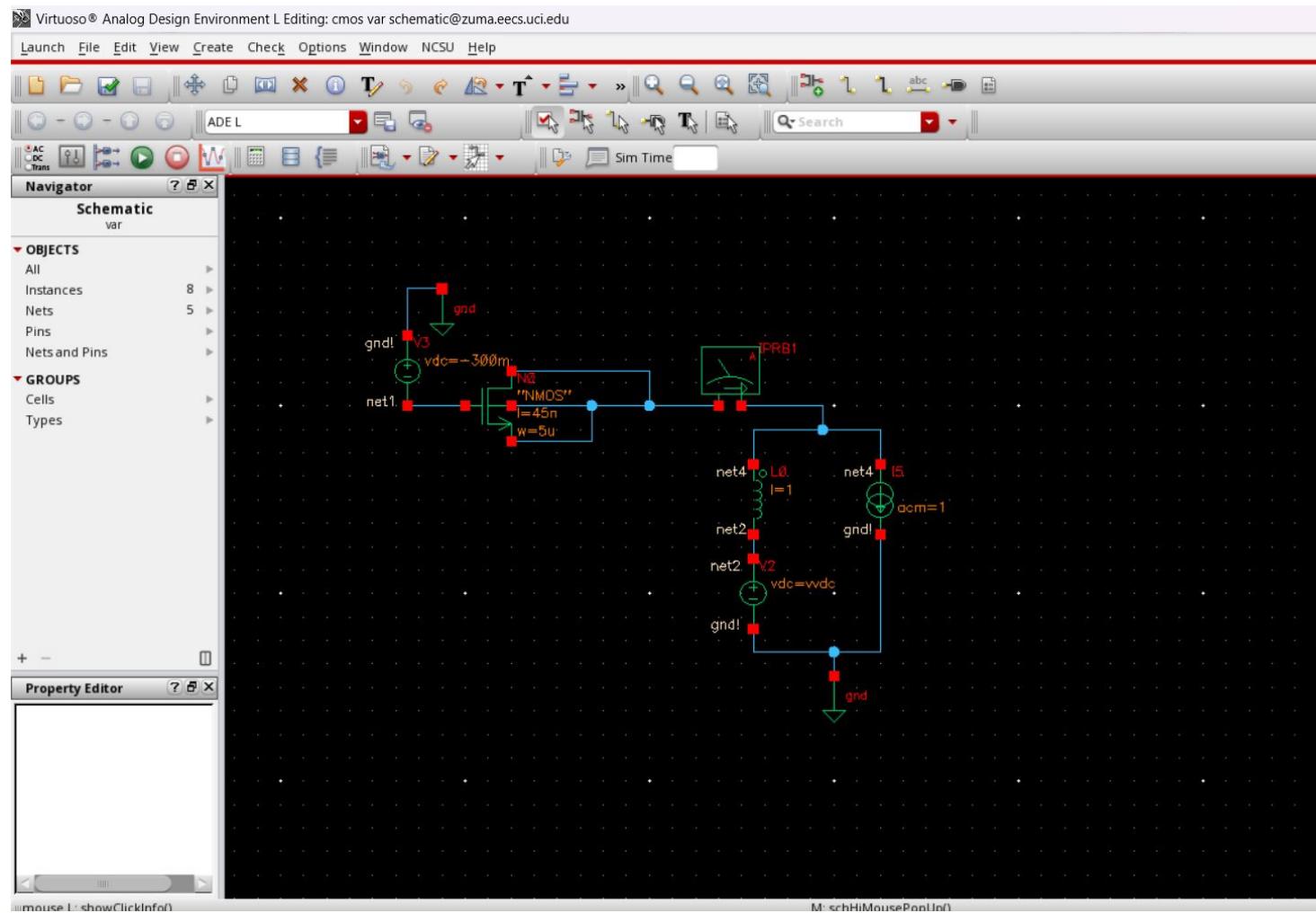


Varactor





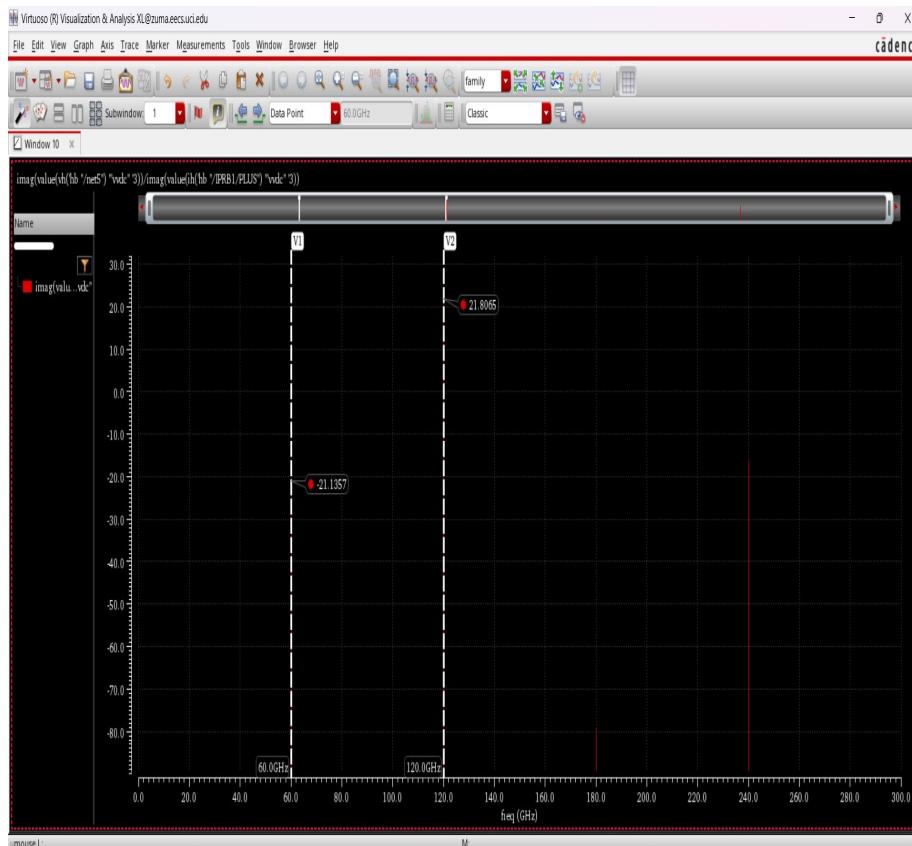
Varactor Test Bench



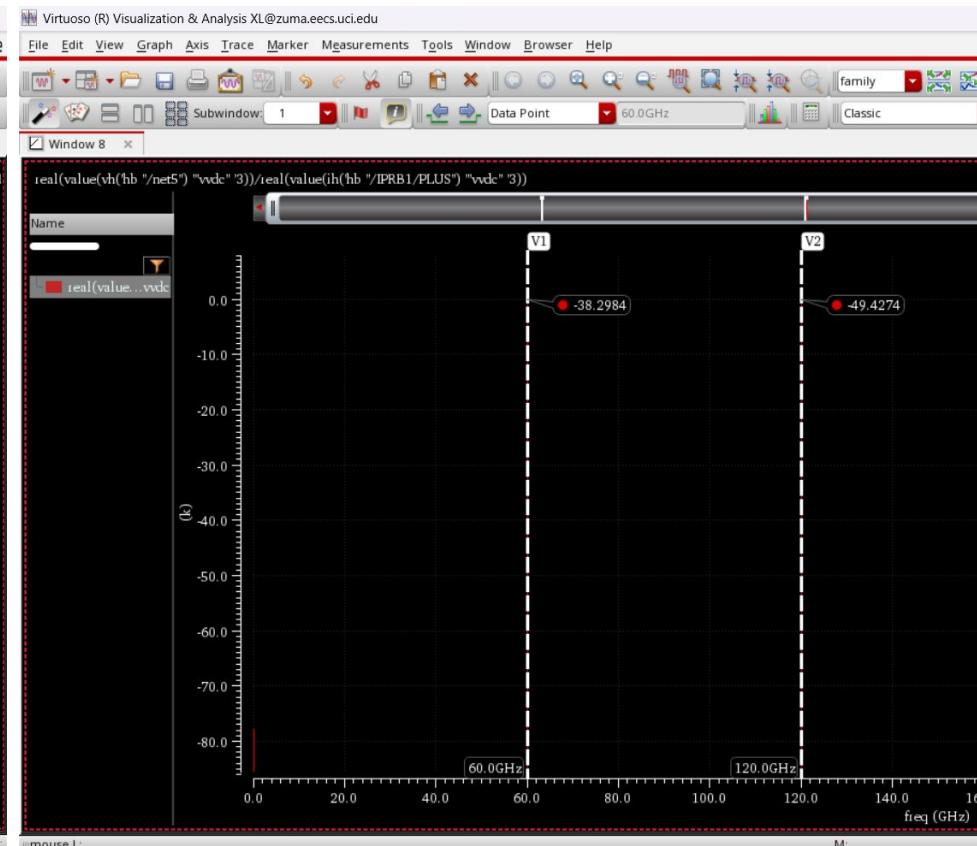


Varactor Impedance

- Imaginary

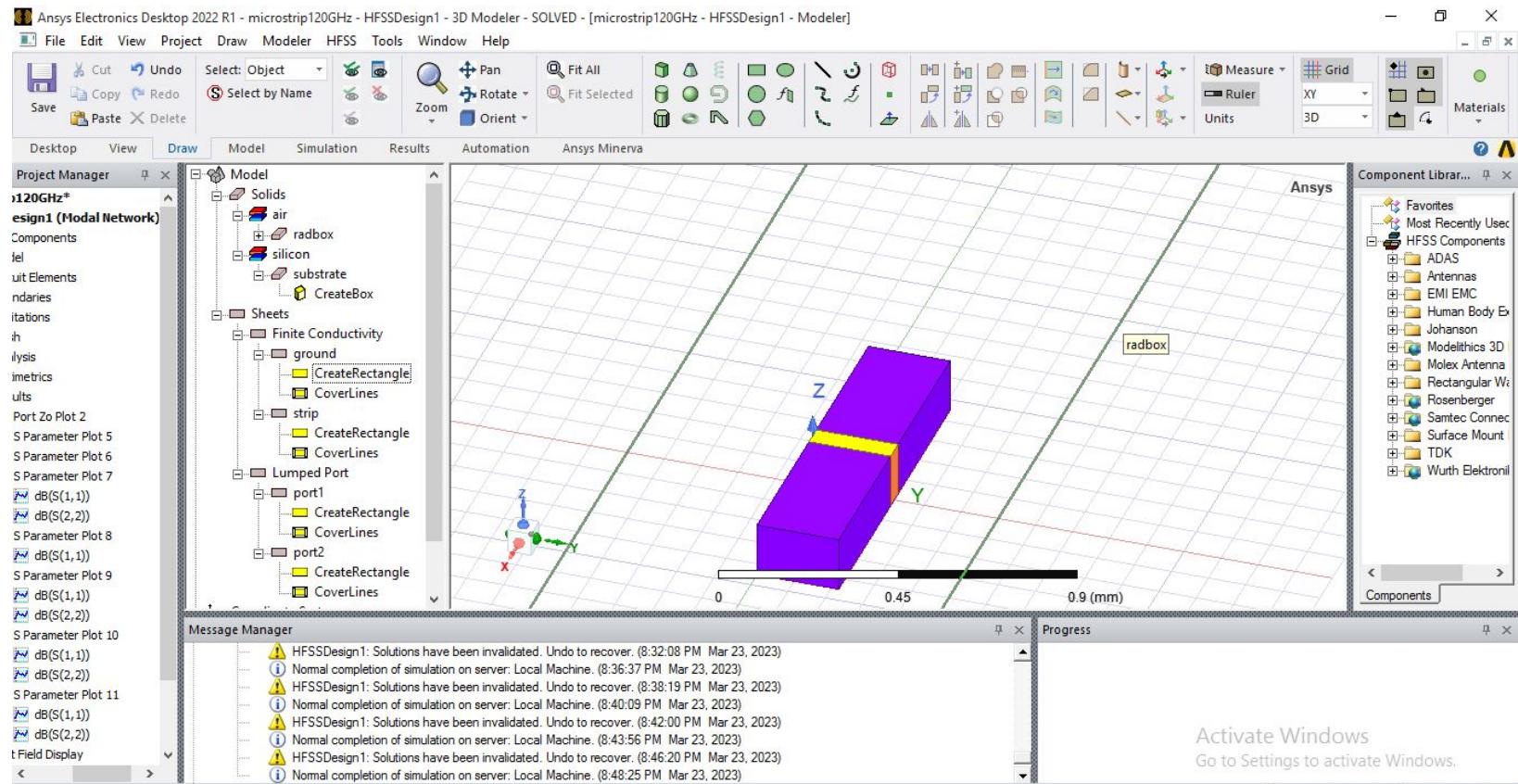


- Real





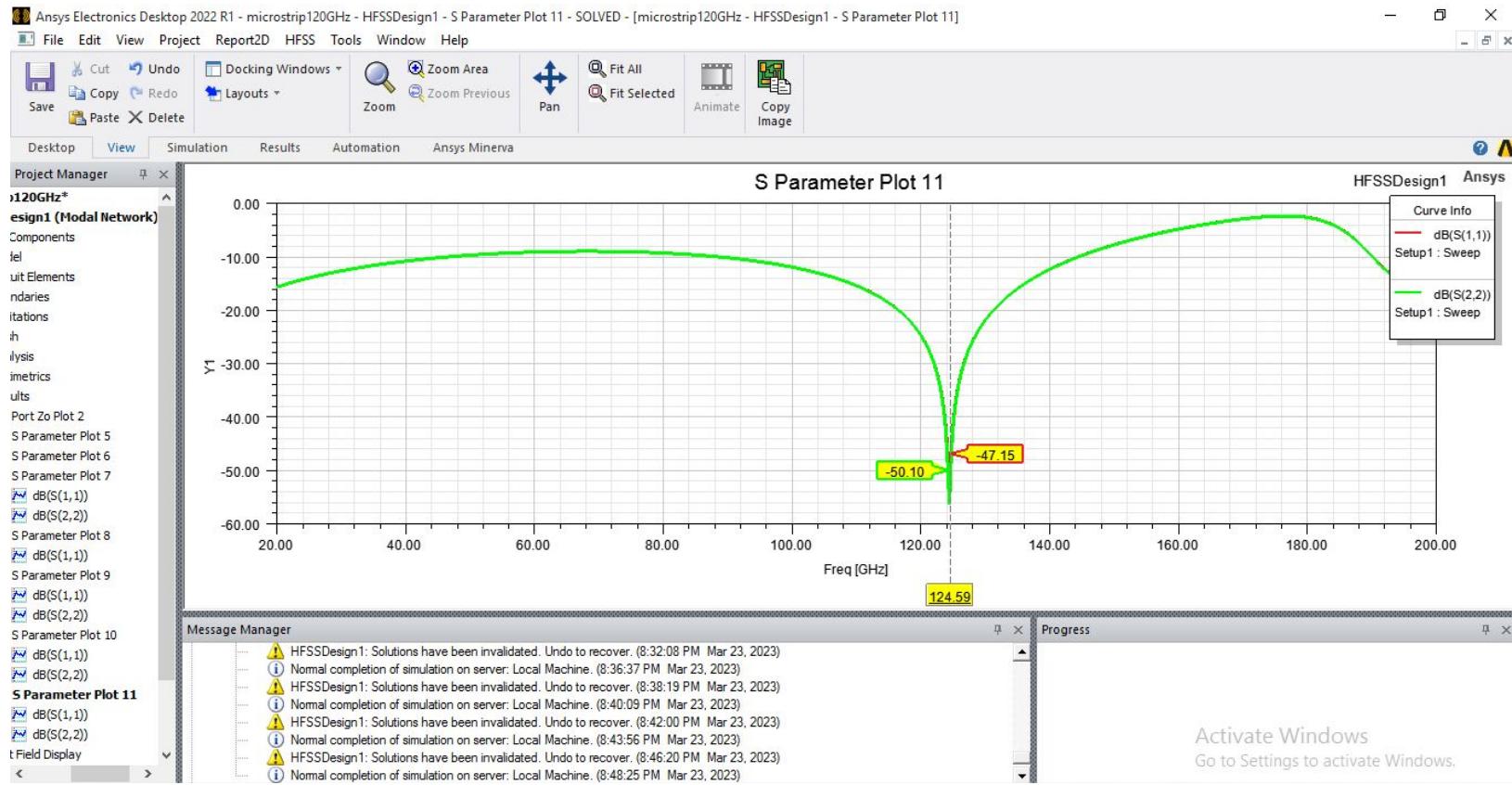
Transmission line at 124GHz



Activate Windows
Go to Settings to activate Windows.

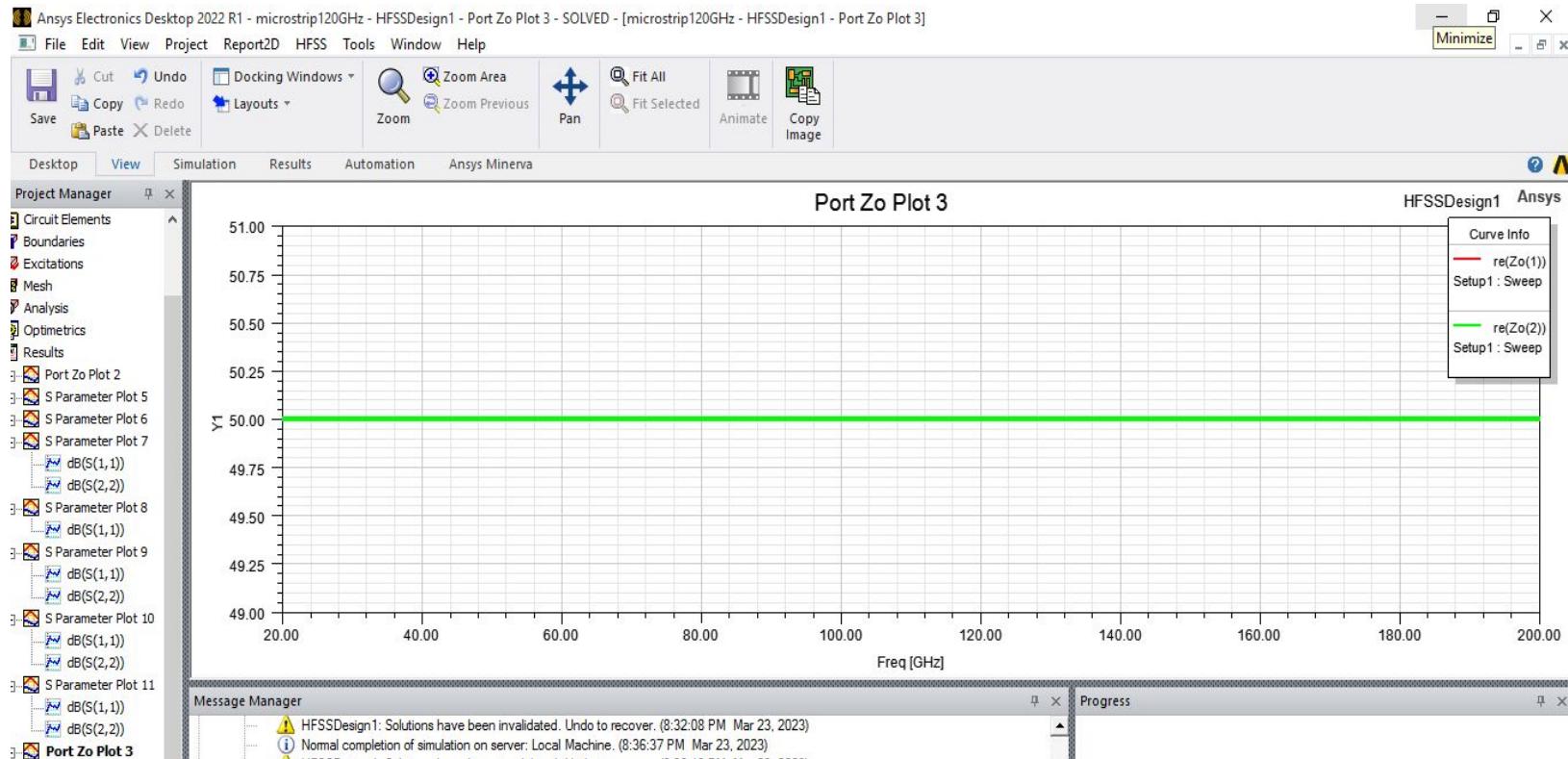


Simulation:



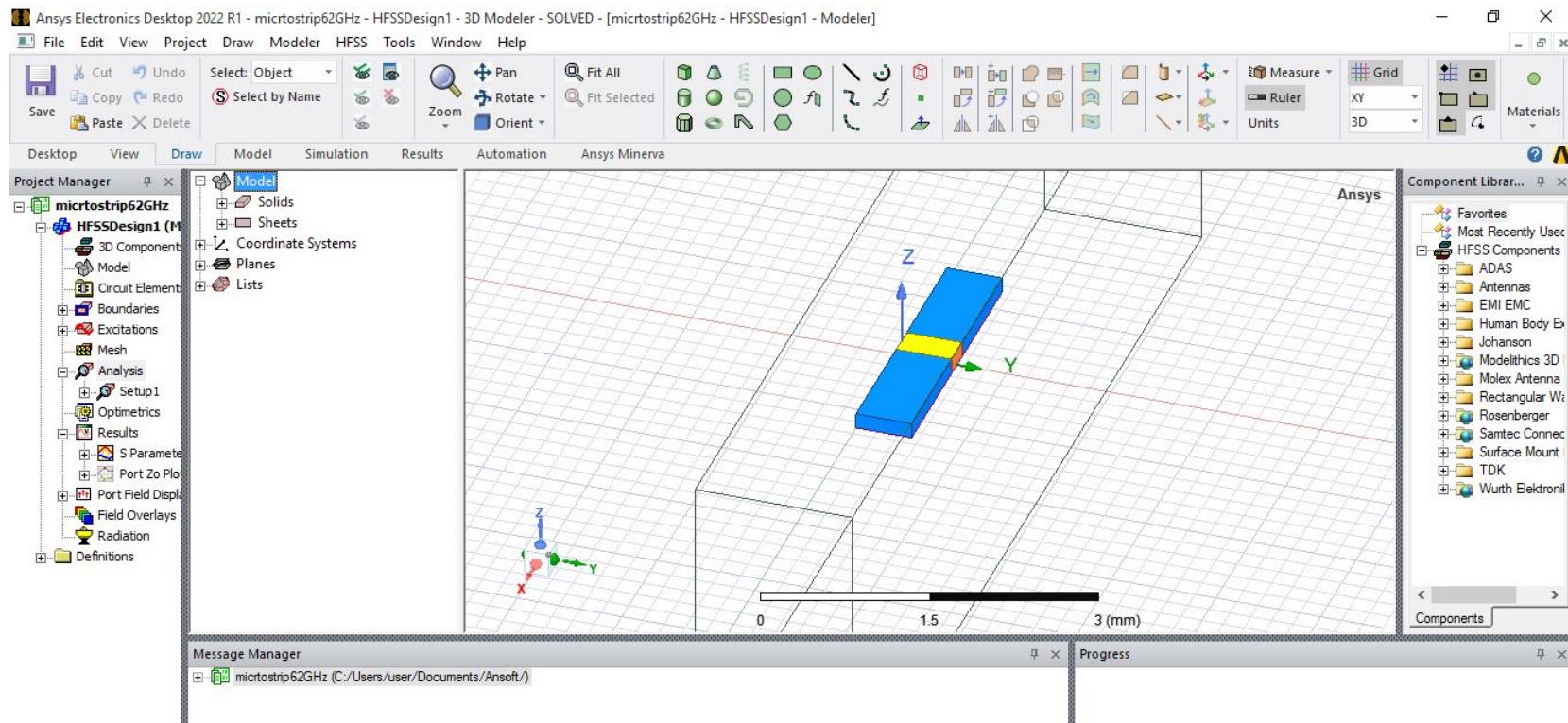


Simulation:



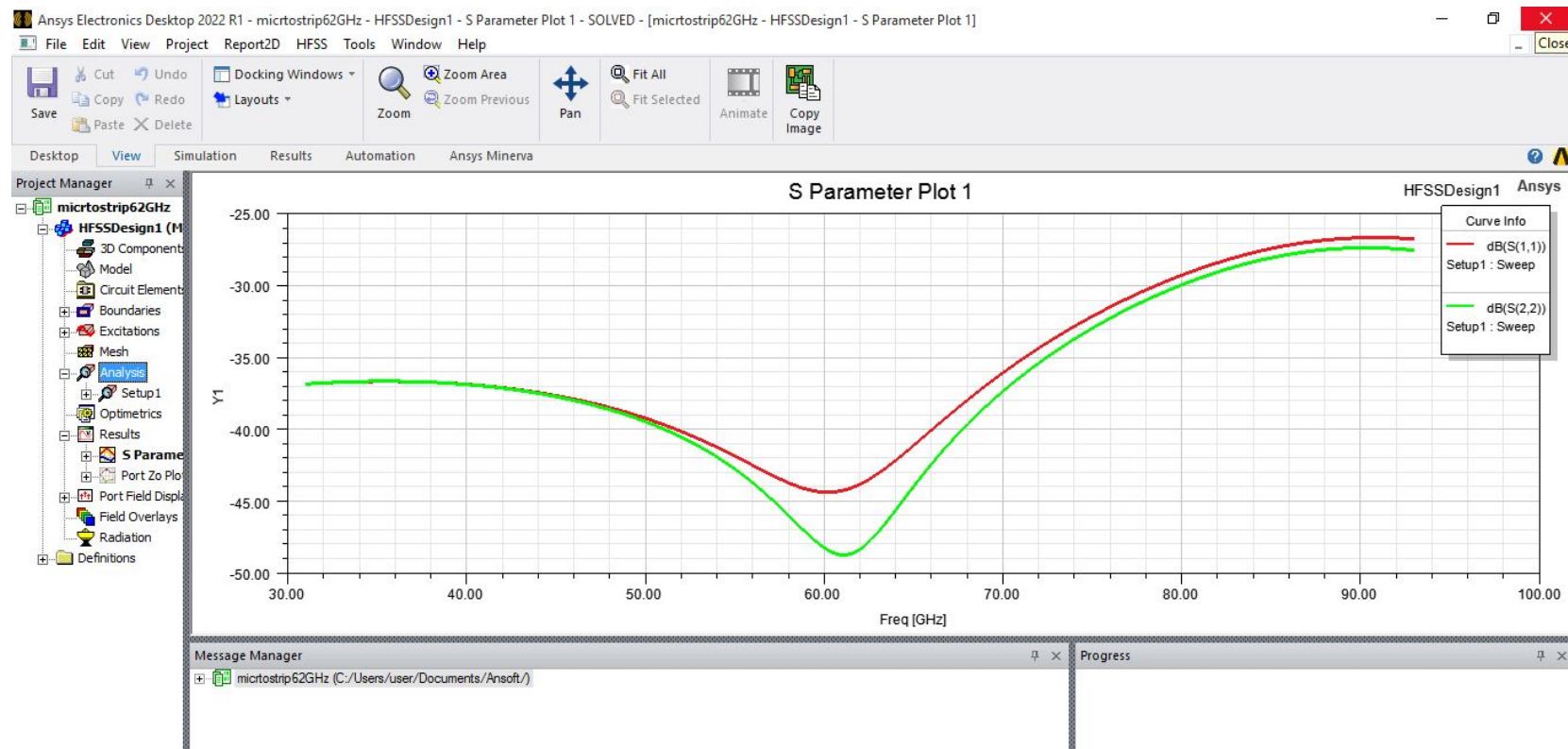


Transmission Line at 62GHz



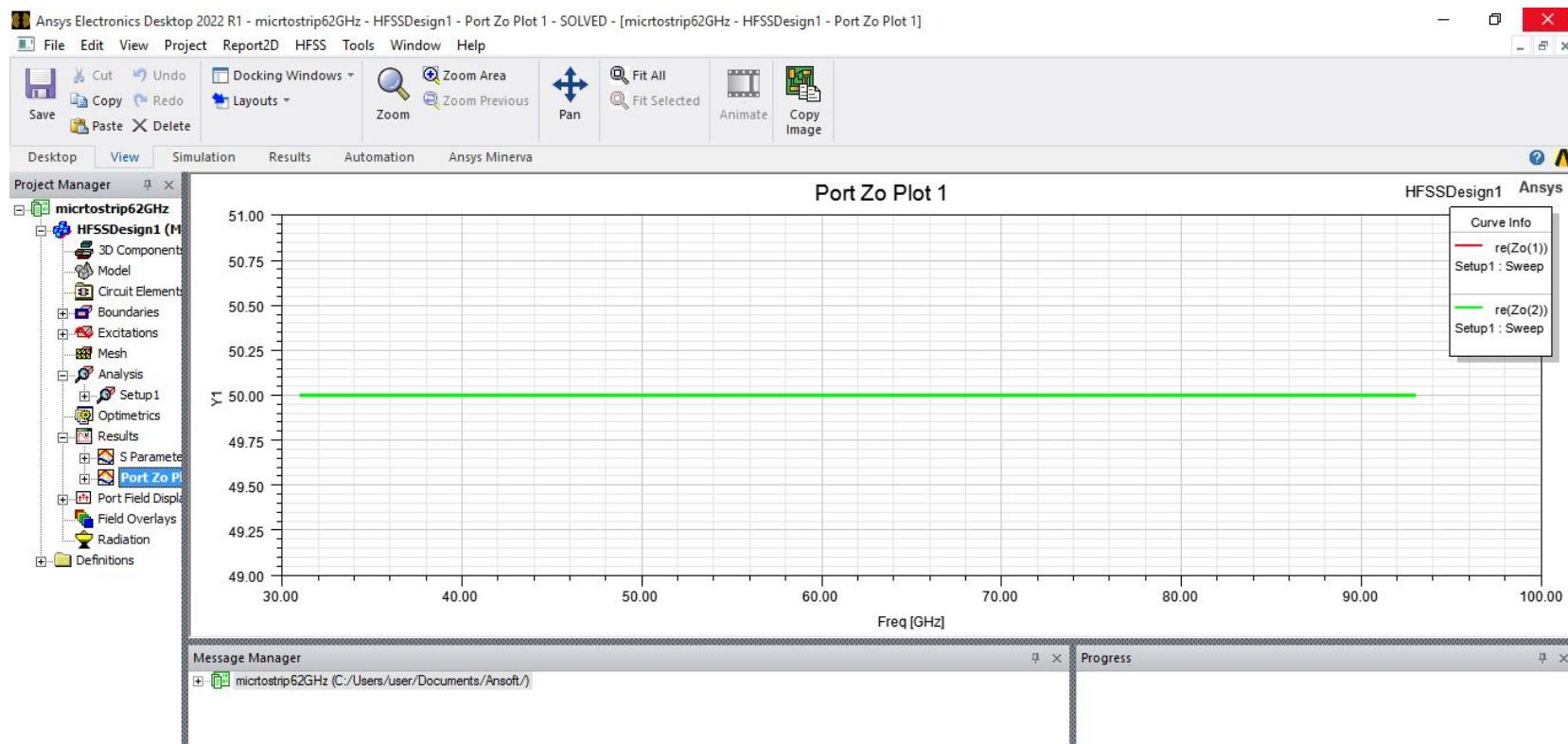


Simulation:



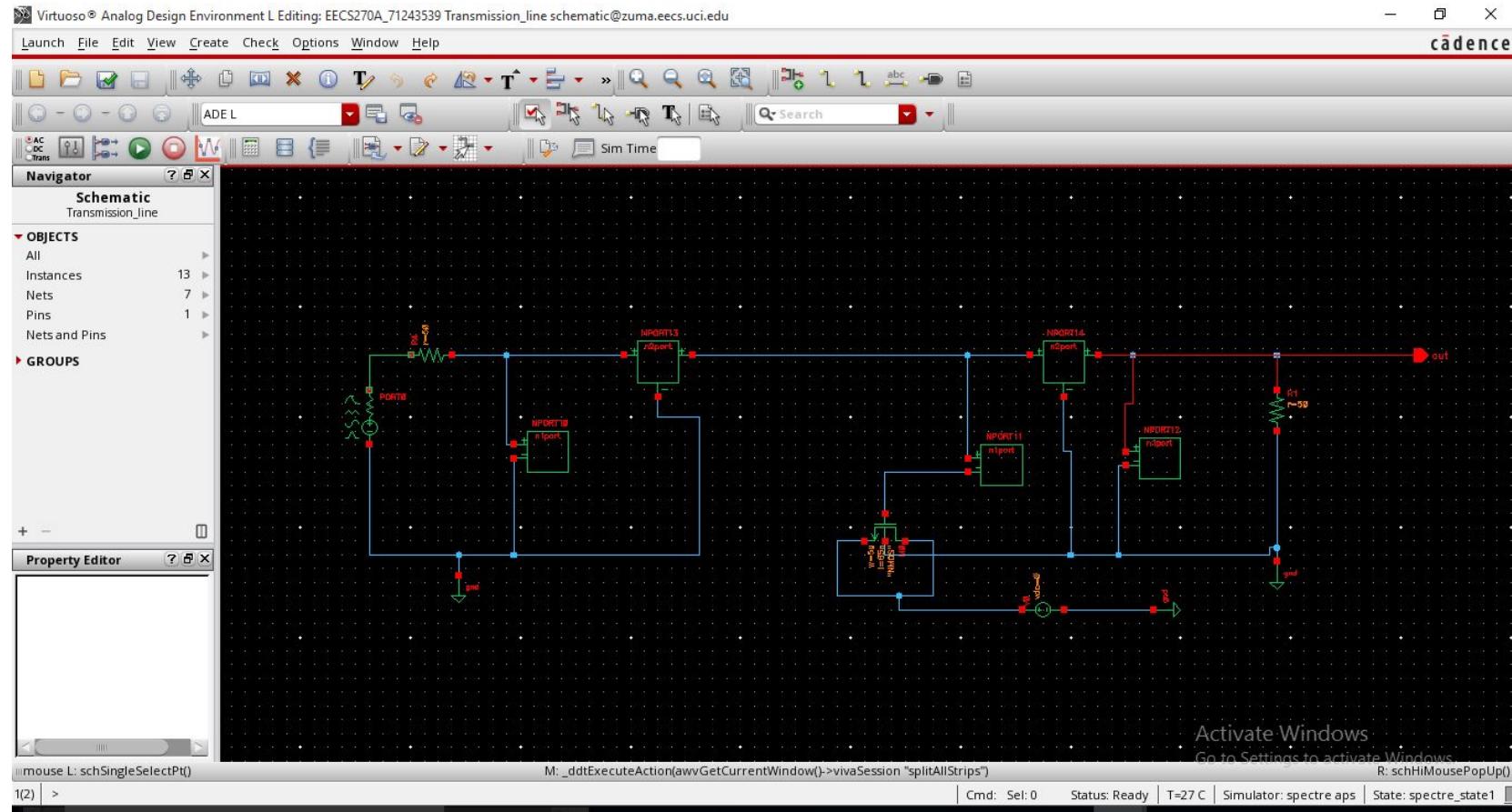


Simulation:



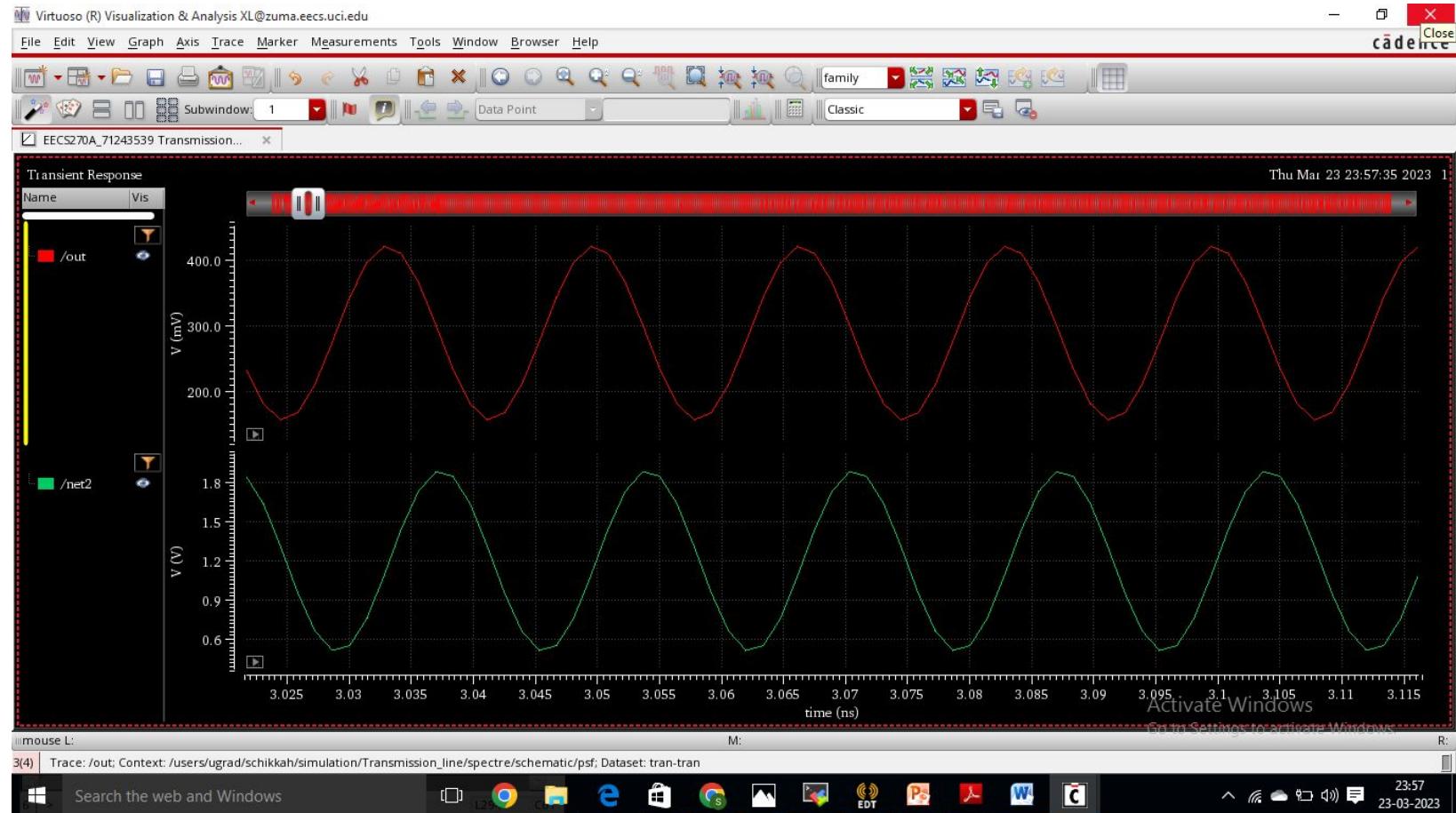


Doubler Schematic 1. with nport



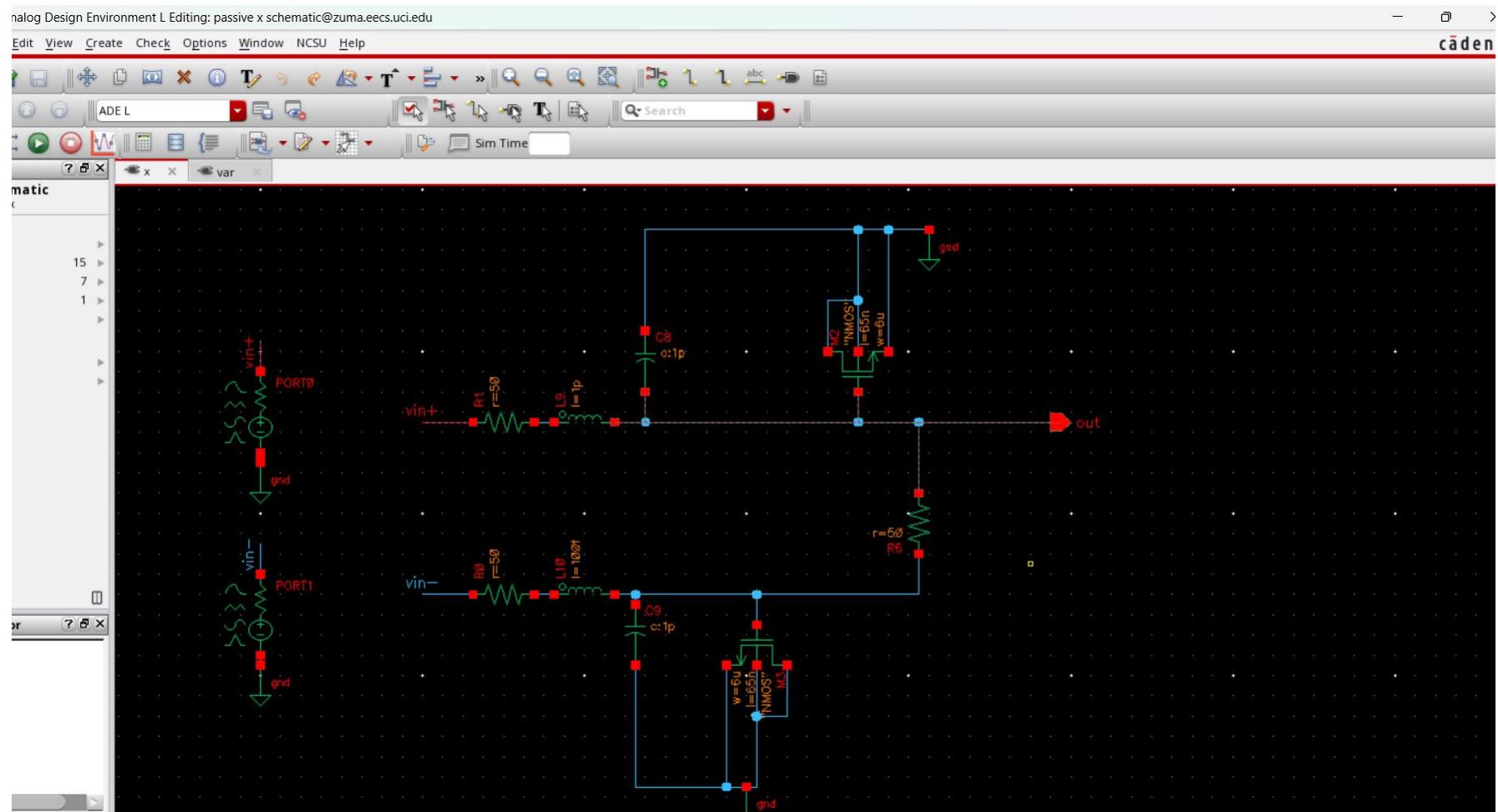


Simulation



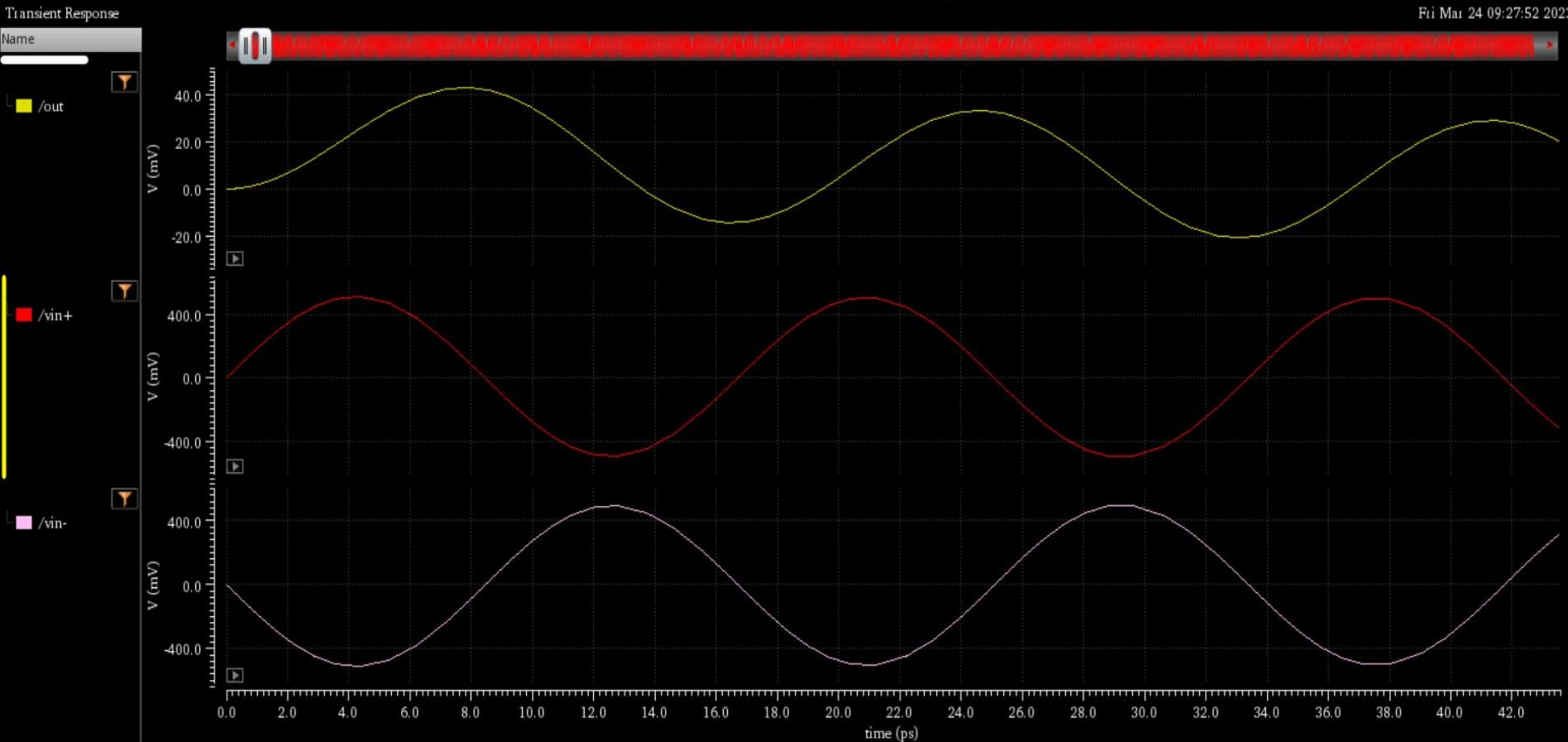


Doubler schematic 2.



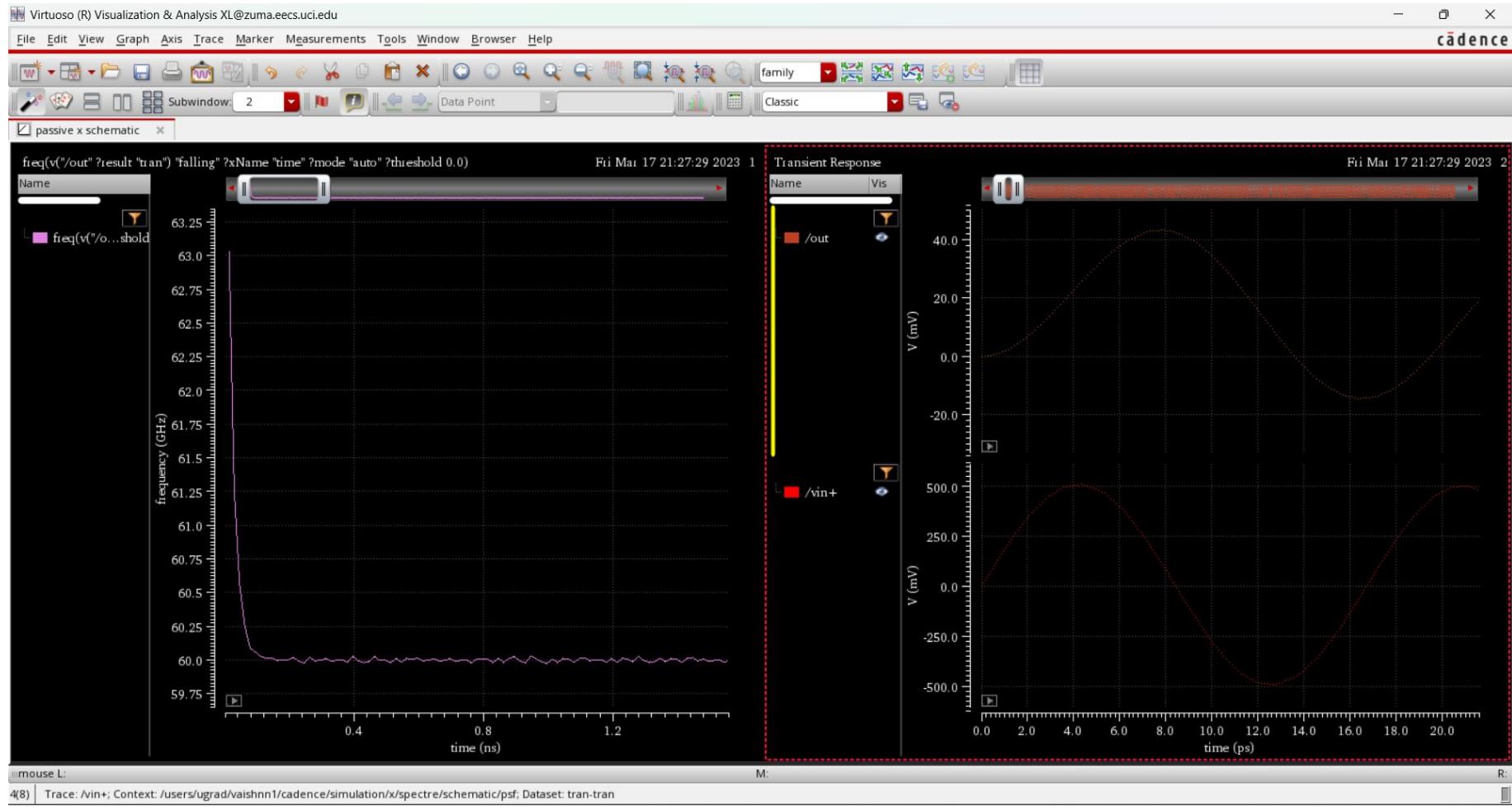


simulation



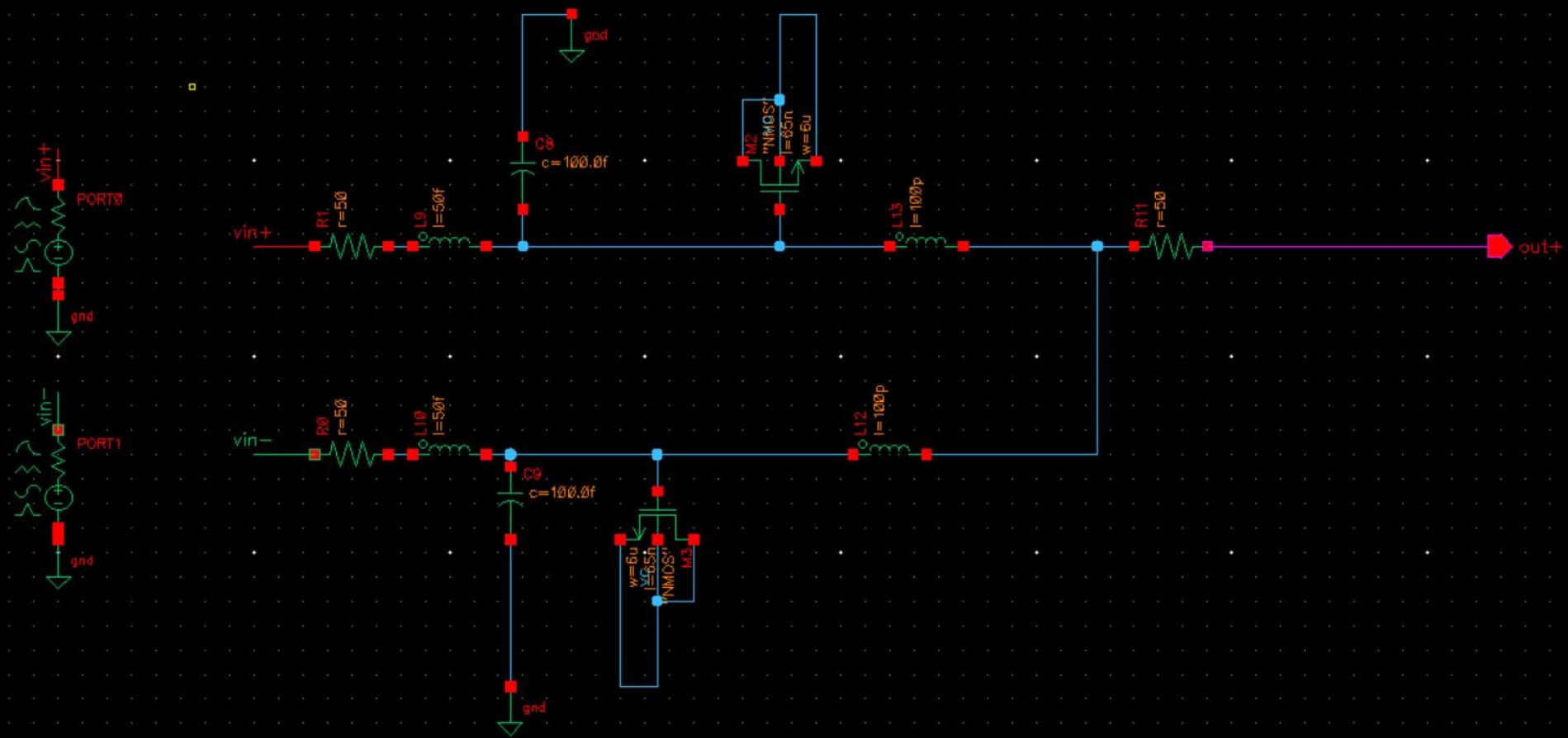


Simulation



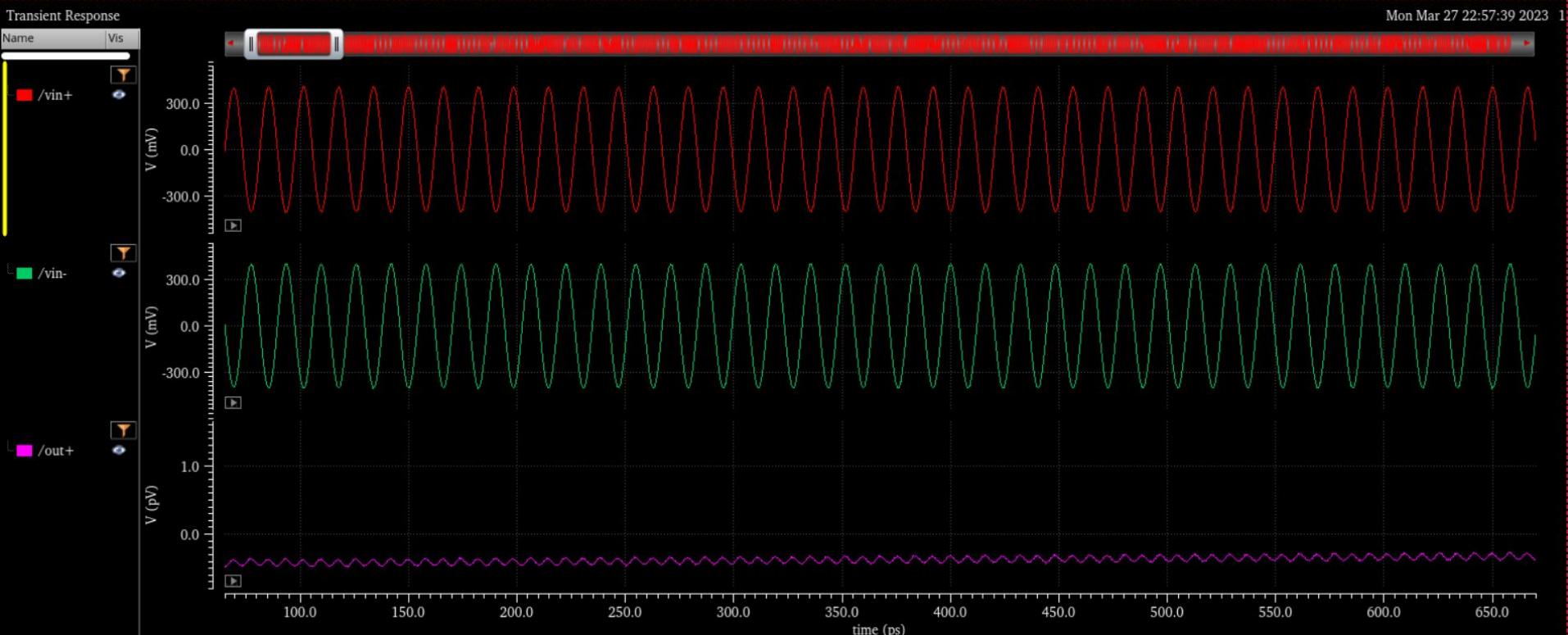


Doubler Schematic



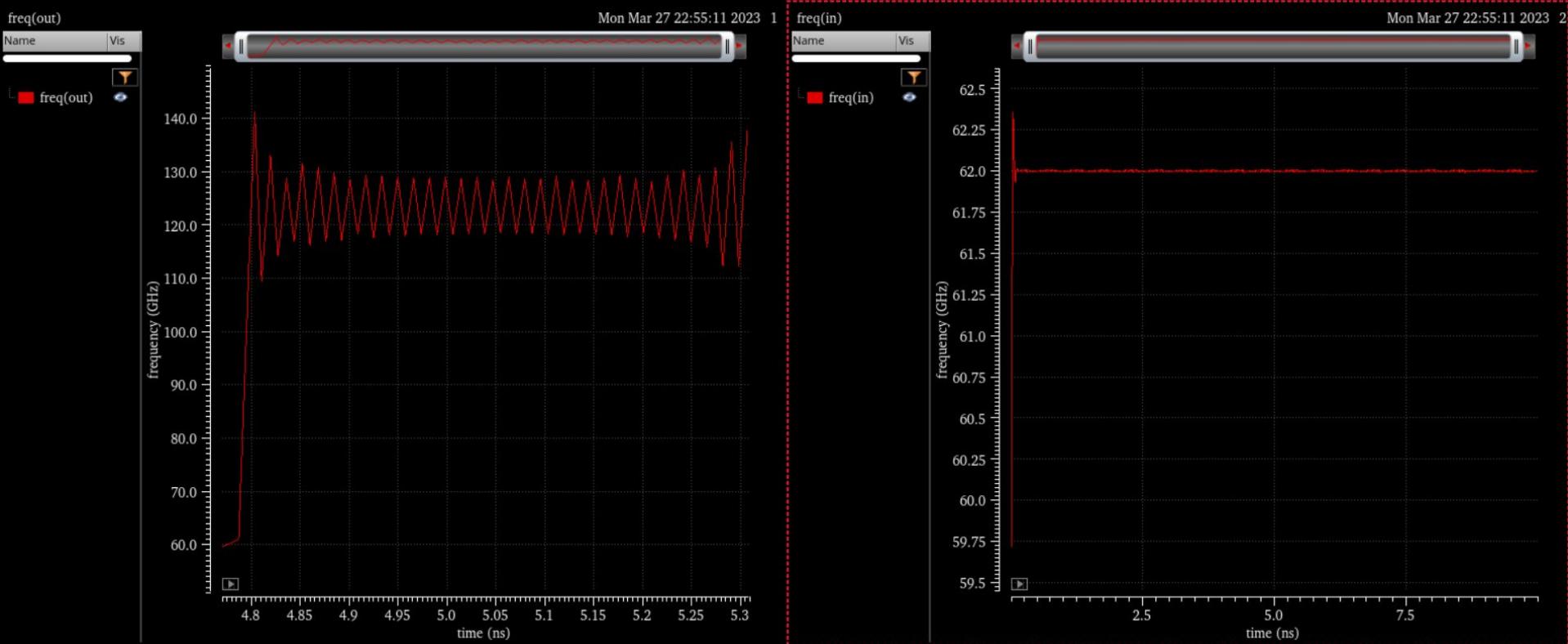


Simulation





Simulation



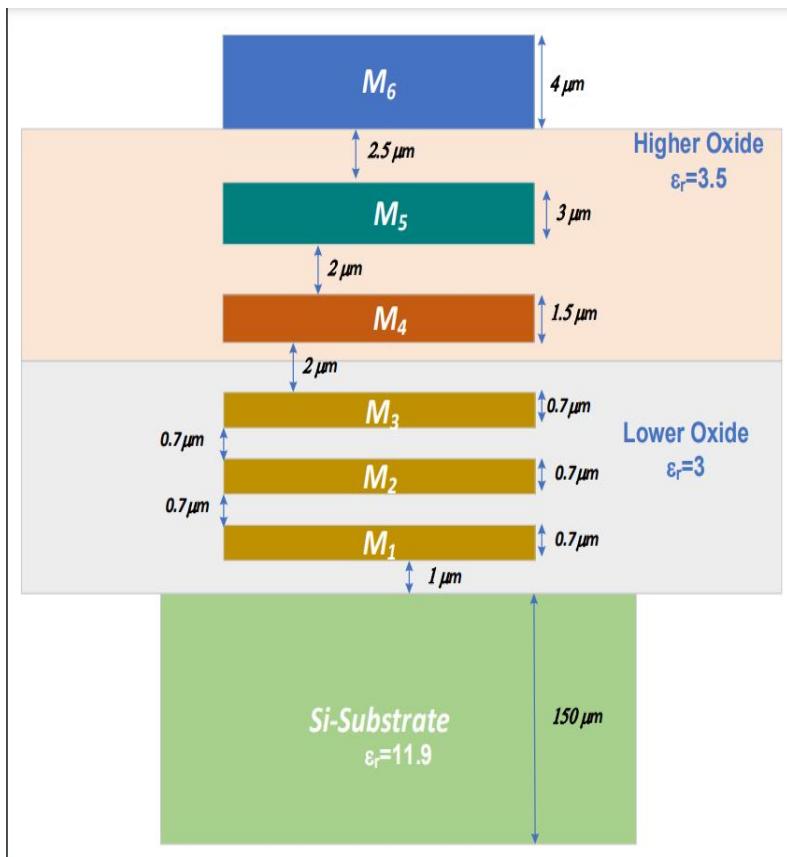


Compliance Table

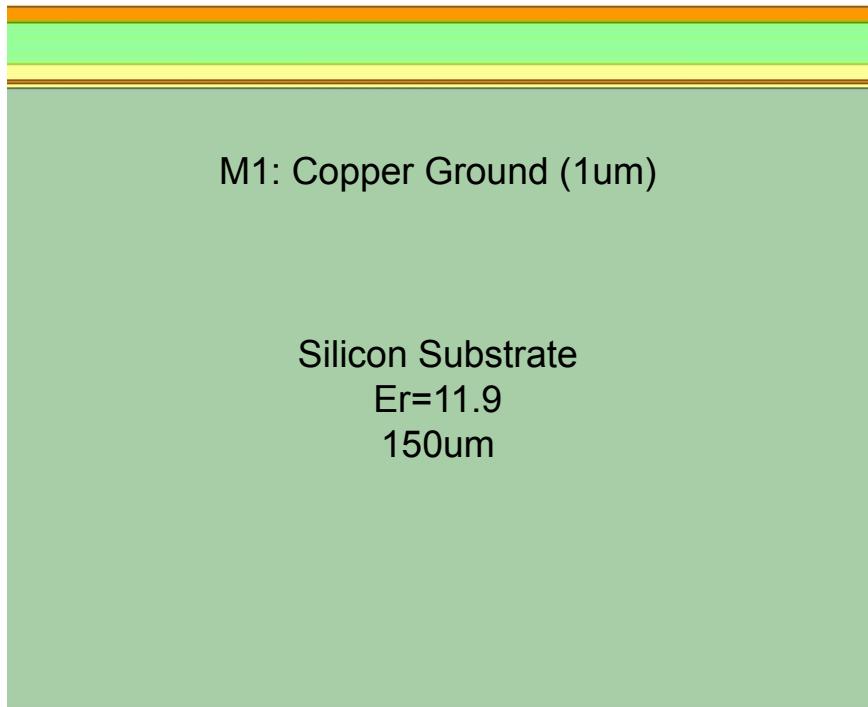
REQUIREMENT	RESULTS
Frequency Doubling	Simulation shows frequency doubling at 2 nd harmonics(124GHz) for a 62GHz input
$P_{DC} < 80\text{mW}$	~0mW



Stack Up



M6: Copper Patch (4um)

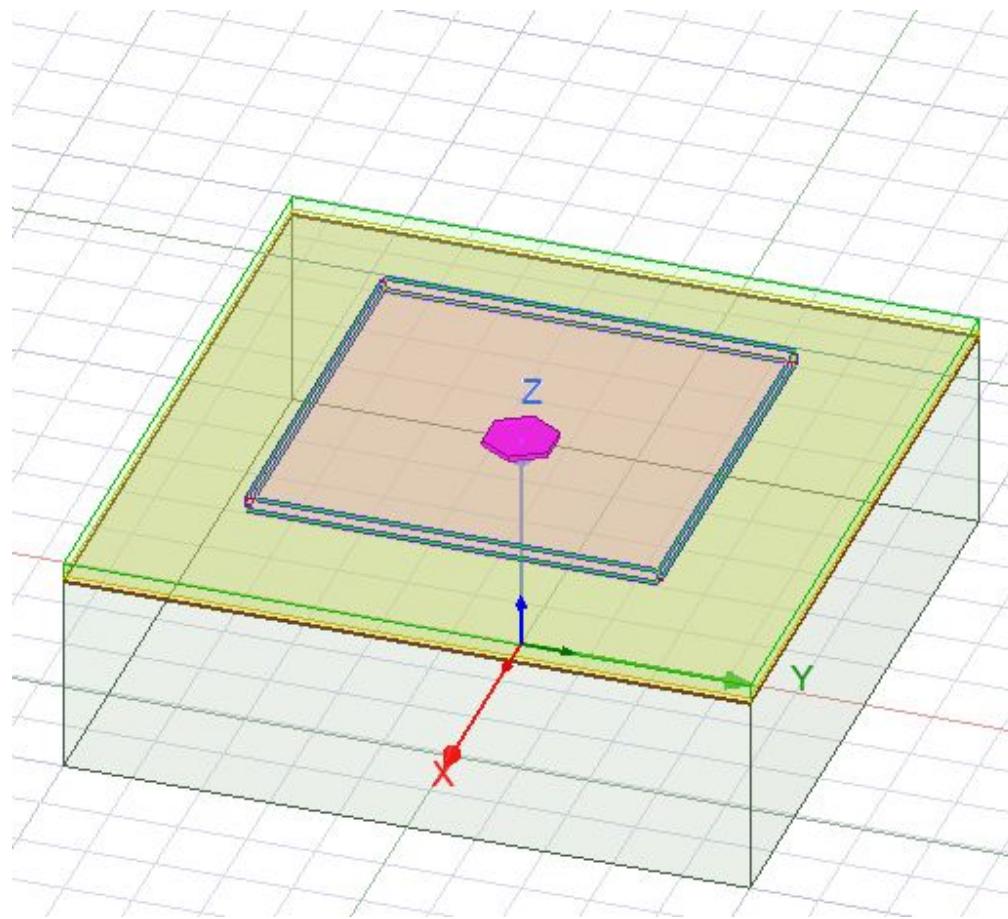


M1: Copper Ground (1um)

Silicon Substrate
 $\epsilon_r=11.9$
150um



RF Pad- Design





RF Pad- Simulation and Results

