EECS 270A- ANALOG IC DESIGN
FALL - 2022

PROJECT FINAL REPORT

DONE BY:

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TO

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SUBMITTED ON:

DECEMBER 12, 2022

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SPECIFICATIONS

Using the given 45 nm CMOS technology, design an amplifier (with more than one stage) that satisfies the listed requirements:

GBW > $230 * 10^9$

R_{in} > 500 kΩ

R_{out} < 150 Ω

DC Power Consumption < 20 mW

Output Voltage Swing > 2.9 V_{pp}

V_{dd} < 3.6V

W_{min} = 5µm

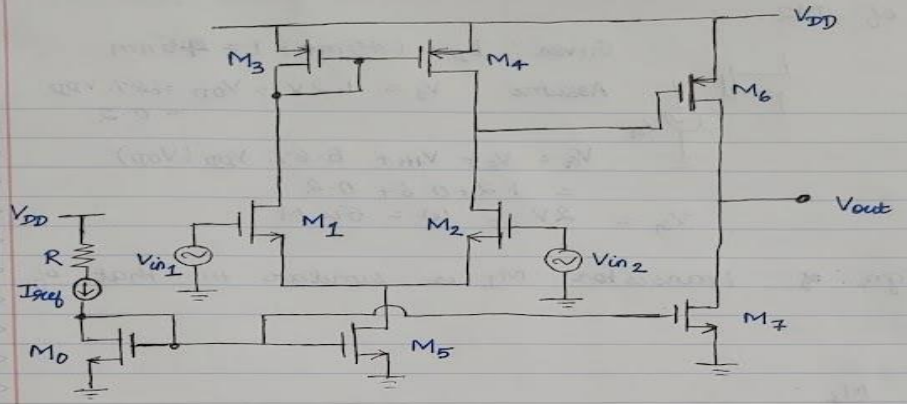
DESIGN APPROACH

The project is designed using two-stage operational amplifier. The simulation was done using Cadence Virtuoso.

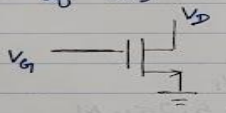
Assumptions: P = 17.5mW; V_{DD} = 3V

I = P/V: 17.5 * 10^{-3}/ 3 = 5.83mA

Assuming equal current distribution; $I_{innerStage}$=$I_{outerStage}$= 5.83 * 10^{-3}/2 = 2.91mA



Design of M_5



Given: $I_D = 2.91mA$; $V_S = 0$; $L = 45nm$

Assume: $V_{OD} = 5\% . V_{DD} = 0.15V$

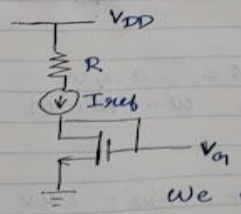
$\Rightarrow V_G = V_S + V_{th} + V_{OD} = 0 + 0.6 + 0.15$

$V_G = 0.75V$

$$I_D = \frac{1}{2} \mu_n C_{ox} \left(\frac{W}{L}\right) (V_{OD})^2$$

Substituting the values of I_D, $\mu_n C_{ox}$, L obtained from cadence, $W = 19.0u M$.

Design of M0



Given: $V_{DD} = 3V$; $I_D = 2.91mA$; $V_S = 0$; $L = $

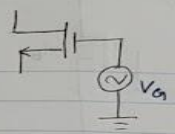
$V_{DS} = 0.75V$

$3 - 0.75 = 2.91 \times 10^{-3} \times R$

$R = 790\Omega$

We obtain $W = 18.0u M$

Design of M2:



Given: $I_D = 1.45mA$; $L = 45nm$

Assume: $V_S = 1.2V$; $V_{OD} = 66\%.V_{DD} = 0.2$

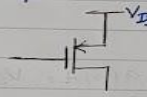
$V_G = V_S + V_{th} + 66.6\%.V_{DD}\ (V_{OD})$

$= 1.2 + 0.6 + 0.2$

$V_G = 2V$; $W = 5u\,M$

The design of transistor M_1 is similar to that of M_2 design.

Design of M_4:



Given: $I_D = 1.45mA$; $L = 45nm$; $V_S = V_{DD}$

Assume: $V_{OD} = -0.4V$

$V_G = V_S + V_{ov} + V_{th}$

$= 3 - 0.6 - 0.4$

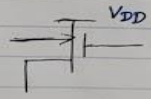
$V_G = 2.0V$; $W = 5.25u\,M$

The design of transistor M_3 is same as the design of M_4.

∴ Allowable swing of inner stage = 3 − (sum of $V_{OD4} + V_{OD2} + V_{OD5}$)

$= 2.2V$

Design of M_6:



Given: $I_D = 1.45mA$

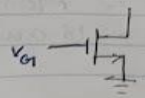
Assume: $V_{DS} = 1.8V$

$V_G = 2V$

$V_{GS} - V_{th} = 2 - 3 + 0.6 = -0.4V$

$V_{OD} = 0.4V$; $W = 10u\,M$

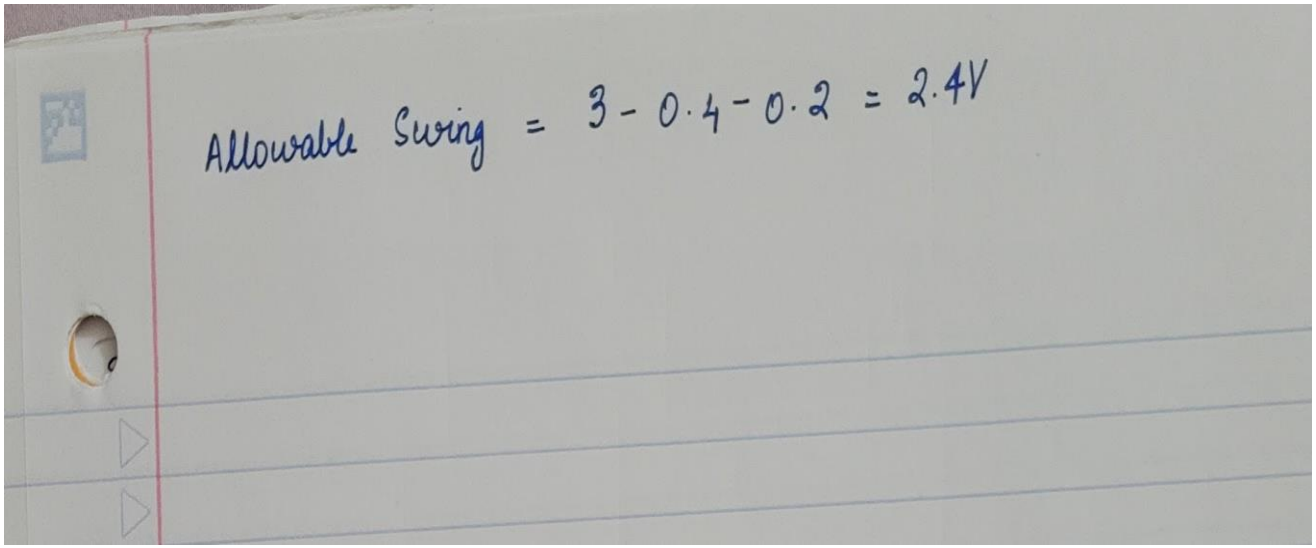
Design of M_7:



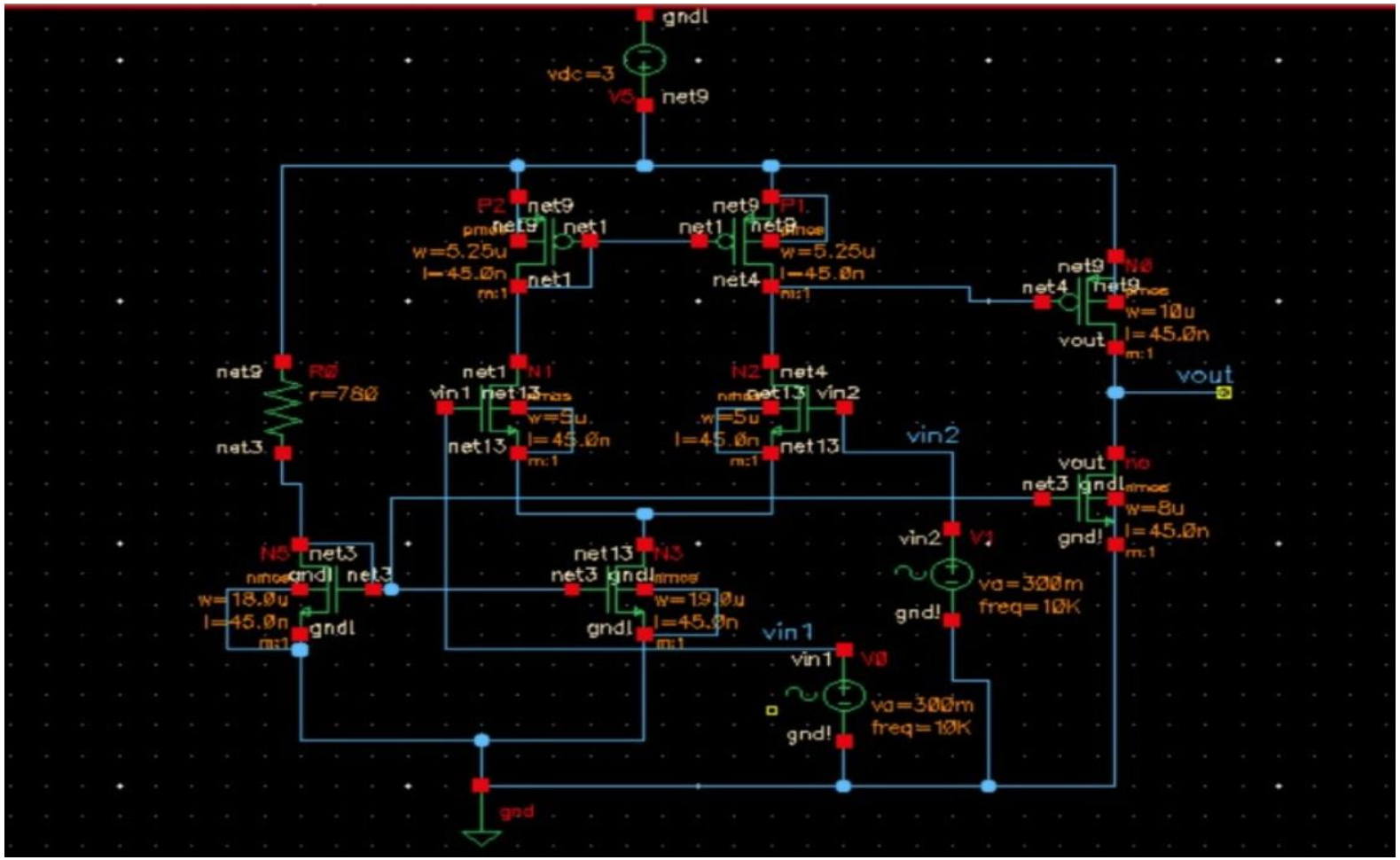
Assume: $V_{DS} = 1.2V$

$V_G = 0.75V$; $V_{GS} - V_{th} = 0.75 - 0.6 \simeq 0.2V$

$V_{OD} = 0.2V$; $W = 8u$


Allowable Swing = 3 - 0.4 - 0.2 = 2.4V

SIMULATION


gndl
vdc=3
V5
net9
P2
P1
w=5.25u
l=45.0n
net1
net4
N0
w=10u
vout
R0
r=780
net3
N1
N2
vin1
vin2
w=5u
net13
N5
N3
w=18.0u
w=19.0u
V1
va=300m
freq=10K
V0
gnd
w=8u

The values of G_m, R_{out} and region of operation of each transistors obtained are as follows:

Transistor	G_m	R_{out}	Region
M0	6.75m	1.6k	2
M1	5.3m	2.2k	2
M2	5.3m	2.2k	2
M3	3.5m	2.4k	2
M4	3.5m	2.4k	2
M5	6.75m	1.6k	2
M6	6.84m	1.19k	2
M7	9.5m	798	2

* Region 2: Saturation

RESULTS

Gain

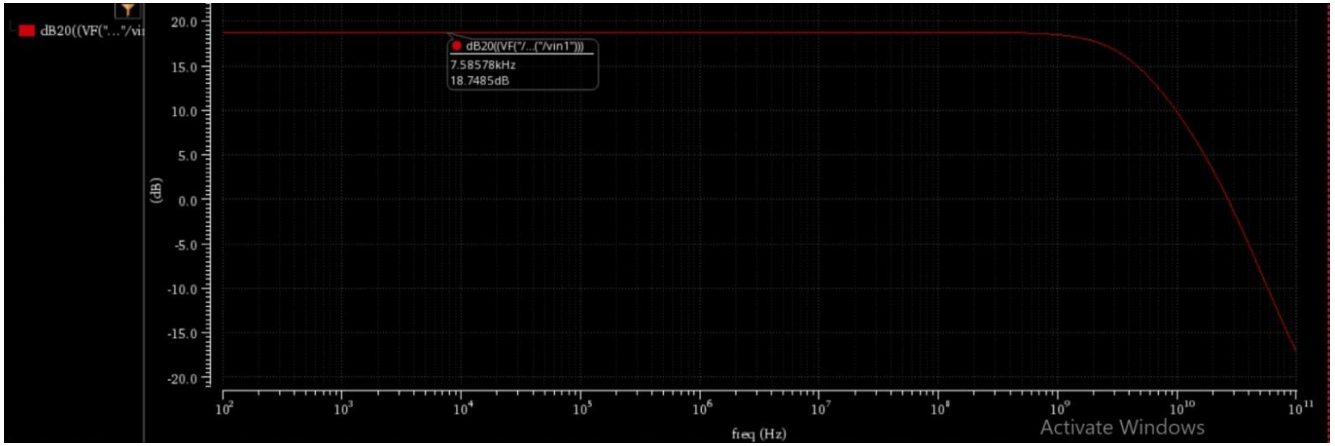
- The gain is calculated using the formula:

$$A_v = 2*g_{m1} * (r_{01} \parallel r_{03}) * g_{m6} * (r_{06} \parallel r_{07}) \text{ (V/V)}$$

Substituting the values from table given in previous table, we get:

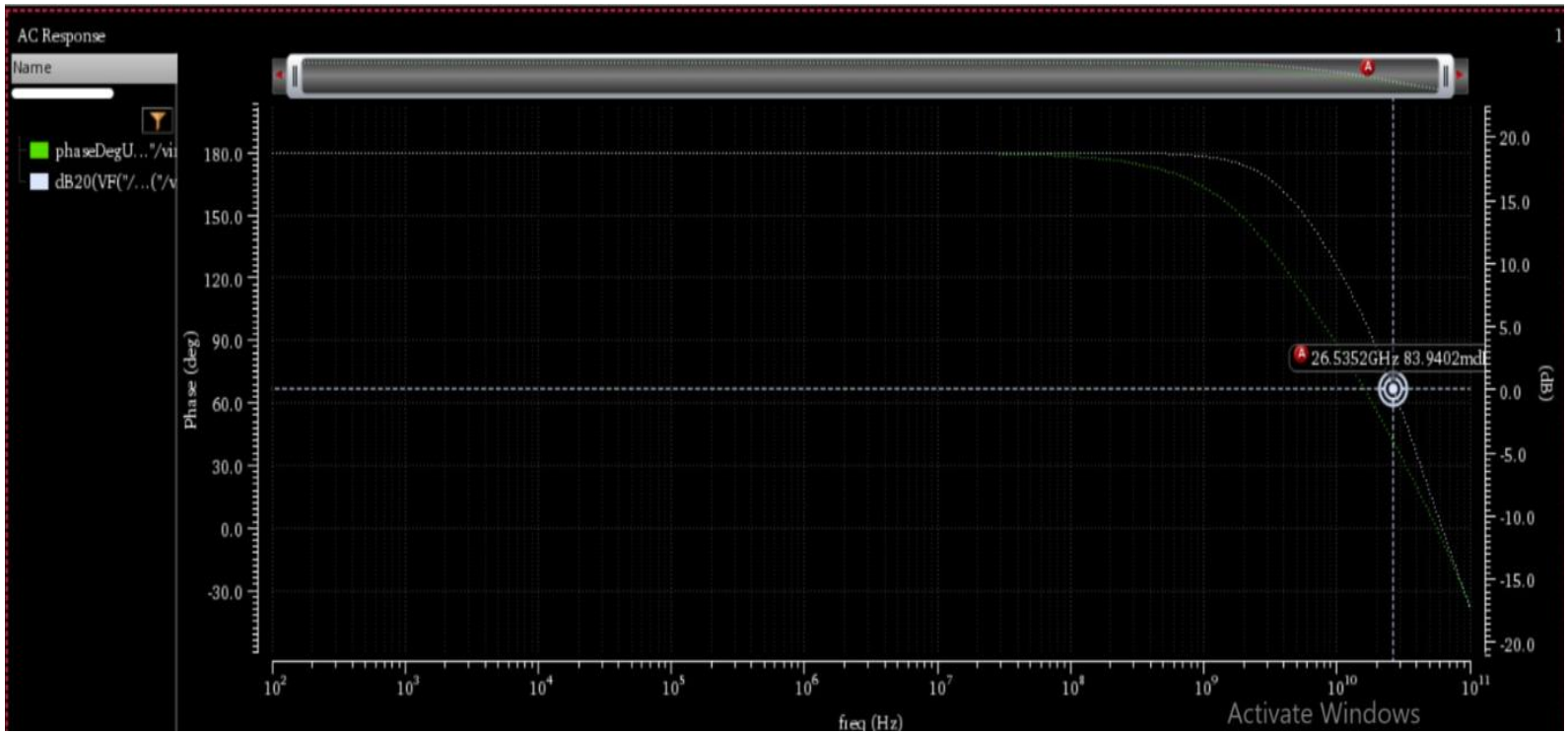
$$A_v = 8.94\text{V/V}$$

Obtained from simulation:



Gain = 8.91V/V

- **Gain Bandwidth Product**



The gain bandwidth product is found to 26 * 10^9Hz

- **Output resistance**: 478Ω