# FABRICATION APPROACHES AND APPLICATIONS OF NANOWIRES

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*Abstract* - **Nanowires are highly used in the manufacturing of high-performance circuits due to its unique electrical and mechanical properties, submicron feature and its performance in Field Effect Transistor (FET). This paper focuses on fabrication approaches of nanowires, assembly, and its practical implementation**.

Keywords: Nanowire, nanostructure, lithography, etching

## I. INTRODUCTION

Nanowires are nanostructures with diameter in the range of $10^{-9}$ to $10^{-7}$ meters. The advancement in nanotechnology towards the development of nanowires has generated tremendous interest due to its unique electrical, electronic, optical, mechanical and chemical properties. Some of the features of nanowires such as high crystallinity, high surface area to volume to ratio, and high resistance, made them to be used in nanomedicines, biomedicine, consumer electronics, and bioelectronics. The first nanoscale wire (a thin layered semiconductor structure) was developed in 1987 by scientists at Bell Laboratories. Since then, nanowires have been investigated in many fields, including optics, electronics, and biotechnology. Nanowires can be made from a wide variety of materials, including silicon, germanium, carbon, and various conductive metals, such as gold and copper.

One dimensional nanostructure represents the smallest dimension structure that can efficiently transport the charge carriers which enhances its electrical properties. Nanowires control the flow of optically encoded information with nm-scale accuracy due to which it is used in high density optical computing. Also, devices designed using optically sensitive nanowires have high potential for photovoltaic cells. The 1-D single crystalline structure is very strong and exhibits a very low number of defects per length making it robust.

The control of the synthesis and surface properties of nanowires could open-up new opportunities for nanocircuits and nanobiosensors in the field of nanoelectronics. The nanowire comes with highly potential properties especially the silicon-based nanowires, which are popularly called Silicon Nanowires (SiNWs). Moreover, silicon is the fundamental material in microelectronics. SiNWs exhibit tremendously and extraordinarily enhanced mechanical and electrical properties that are not seen in bulk (three-dimensional) silicon materials. With the control of nanowire size and concentration of dopant, the electrical sensitivity and other properties of nanowires can be tuned for the reproducibility. Nanowires comprise arrays of electrodes that form a nanometer electrical circuit.

Metal Oxide Semiconductor Field Effect Transistors (MOSFET) are largely used as fundamental building elements in electronic circuits. Also, the dimension of MOS transistors is gradually decreasing to the nanoscale based on the prediction made by Moore's law. However, their fabrication is challenging. A large number of techniques exist to fabricate silicon nanowires. These can be classified into top-down fabrication and bottom-up techniques. In top-down fabrication, lithography is used to define the fabricated structure that is then transferred from the photoresist to the substrate by etching or a similar way of structuring the already available material. In the bottom-up approach, the material is added to the substrate in a self-organized way.

Traditionally semiconductor technology is driven by top-down fabrication using lithography. This approach successfully enables to scale down device dimensions all the way to the 10 nm range. In contrast, bottom-up techniques have the potential to construct very complex structures without the need of defining

them in all details by a mask. Nevertheless, there are still some missing links to make the bottom-up approach a manufactural alternative. When it comes to silicon nanowires, both paths are possible and have their advantages and drawbacks. In the top-down fabrication, a clear path from today's planar and FinFET devices to nanowire devices can be drawn. However, the etching of the nanowire out of the bulk silicon results in non-perfect geometry and requires advanced lithography. The bottom-up approaches, on the other hand, may lead to excellent crystal quality and small diameter using a very simple process.

The physical properties afford nanowire applications in a vast network of active microelectronic research fields, including logic device scaling in very large-scale integrated circuits, sensor devices, nanomedicine, and energy harvesting. The nanowires are expected to grow significantly in the coming years due to its novel applications. Nanomedicine is the application of nanotechnology to diagnose, monitor, deliver drugs, treat diseases, and control biological systems. The applications of nanowires in nanomedicine have assisted the field of nanomedicine to flourish. In addition, nanowires are used extensively in LEDs as they permit fast communication between chips and devices. Electronics is one of the major applications of nanowires. They are used in transistors, logic devices and diodes.

## II. FABRICATION APPROACHES

### *A. TOP-DOWN APPROACH.*

Traditional top-down nanowire fabrication is a subtractive technique, like carving a statue from a block of marble, using the chemicals rather than chisels to achieve nanoscale structure. It utilizes many methods which are employed by the semiconductor industries, such as lithography and chemical etching, to convert a bulk wafer or crystal into nanowire structures. In general, top-down fabrication relies on large, expensive, and precise instrumentation to obtain the desired nanoscale structure.

The popular top-down technique for nanofabrication is lithography. This technique involves the deposition of a resist material, such as poly(methylmethacrylate) that acts like a photographic film to produce a pattern after exposure and development using a patterned mask. The resolution of photolithography is hindered by the lithographic technique and the wavelength of light used. Patterns with higher resolution can be achieved with Electron-Beam Lithography (EBL), which is a maskless direct-write exposure method. For the production of vertical nanowires, the pattern will consist of a series of circles or holes on top of a wafer of the target material. For horizontal nanowires, the pattern will be a series of lines or trenches on a layered substrate, such as Silicon-On-Insulator (SOI).

*Top-down nanofabrication of silicon nanowires using EBL*

The top-down nanofabrication process of silicon nanowires is briefly illustrated in Figure 1. Four key process steps are required to form the silicon nanowires: sample preparation, pattern design, EBL, and anisotropic etching. Details of each process step are elaborated as follows.

a. *Sample preparation* - The silicon nanowires are fabricated from SOI wafer (Soitec) with 200 nm of Buried OXide (BOX) and a 50 nm p-type Boron-doped silicon top layer (resistivity: 8.5–11.5 O.cm with doping density of 1015 atoms.cm-3). First, the SOI wafer is cleaned using standard RCA1 (mixing DI water: 5, ammonium hydroxide (27%): 1 and hydrogen peroxide (30%): 1) and RCA 2 (mixing DI water: 6, hydrochloric acid (30%): 1 and hydrogen peroxide (30%): 1) solutions to remove contaminants, followed by soaking in dilute Hydrogen Fluoride (HF) to remove the native oxide. After the cleaning process, the SOI wafer is cut into small pieces measuring 2 cm by 2 cm. Next, high-performance negative tone resists (ma-N2400 series) are spin coated on the sample and then dehydrated on a hotplate. The coated samples are then left for several minutes on a cooling plate to control the sample temperature for uniform resist characteristics. The ma-N2400 series resistors are composed of a phenolic resin (novolak) as the polymeric bonding agent and an aromatic bisazide as the PhotoActive Compound (PAC) dissolved in safer solvents, and they are very sensitive to electron beam radiation. The advantages of the ma-N2400 series are its good thermal and etch stability. These resists can be developed without swelling in an alkaline aqueous developer and do not chemically modify the surface.

b. *Nanowire pattern design* - The nanowire patterns are designed with various dimensions using RAITH

ELPHY Quantum GDSII Editor developed by Raith GmbH. ELPHY Quantum is a universal lithography system that makes it possible to produce micro- and nanostructures by means of electron beam writing using a Scanning Electron Microscope (SEM), with pattern-placement accuracy below 20 nm. Two type patterns are designed: one is an array of 20 identical nanowires with a 40-nm width and a 400-μm length and the other is an array of single nanowires with 5 different widths (40, 50, 60, 70 and 80 nm) and a 400-μm length. For both designs, the 400-μm length is designed to ensure that the nanowires come into contact with the electrode pad in the subsequent fabrication process. In addition, both patterns are designed to increase the probability of adhesion or reaction of the analytes to the nanowire surface during testing.

c. *Electron beam lithography (EBL)* - The next step is the EBL exposure process. EBL is performed with JOEL JSM 6460LA SEM equipped with a Raith ELPHY Plus pattern generator. After the EBL exposure process, the sample is left for 5 minutes before proceeding with the development process. Development is executed for various developing times using the ma-D 532 developer to determine whether the unexposed resist dissolved sufficiently. Developing times are varied from 15 to 45 seconds, depending on the thickness and type of resist. Then, the developed samples are rinsed in De-Ionized Water (DIW) for 5 minutes and blown dry with air. After rinsing, the samples are hard baked at 90°C for 60 to 90 seconds to improve the resist adhesion to the samples and its resistance to the anisotropic etching process. The developed samples are then characterized using High Power Microscopy (HPM), SEM (JEOL 6460), and Atomic Force Microscopy (AFM)

d. *Anisotropic dry etching* - Each developed sample is then loaded into a SAMCO ICP-RIE 10iP for anisotropic etch profile of silicon. This etcher can achieve anisotropic sidewall profiles in high aspect ratio openings. The resist pattern acted as a mask for the silicon etching by protecting areas where a chemical reaction between the surface materials and reactive gases is not required. The ICP-RIE is performed under a pressure of 5 mTorr and a Radio Frequency (RF) power of 500 W using CF4 (30 sccm) and O2 plasma (28 sccm) for 1 minute. The resist pattern is stripped using acetone, which reveals silicon nanowires with a good anisotropic profile. The etch profile and feature sizes of the silicon nanowires are determined by SEM and AFM. In addition, Energy-Dispersive X-ray (EDX) is carried out to identify the elemental composition of nanowires after the dry etching process.

*Benefits and Issues*

Top-down nanowire fabrication is enticing because of the ease with which ordered arrays of nanowires can be constructed. This facilitates electrical contact to the nanowires and their integration into the large-scale devices. Moreover, many of these processes are compatible with standard microelectronics industry processes, enabling their scale up.

However, the top-down fabrication approach has several drawbacks. The applicability of photolithography to these processes lessens as the desired length scales decrease, requiring the implementation of more advanced methods such as extreme ultraviolet lithography. Methods such as electron-beam and scanning probe lithographies, are direct-write techniques, requiring slow serial writing of individual elements. Parallelization of these techniques will be necessary for industrial-scale production. Nanowires formed by top-down processes also frequently lack complex electronic characteristics. The nanowires etched from a wafer, desired modulation of composition must be encoded into the wafer by techniques like Molecular Beam Epitaxy (MBE) or encoded after growth through implantation methods, this processing can greatly increase the material cost of nanowire devices compared to bottom-up techniques.

*B. BOTTOM-UP FABRICATION*

Bottom-up technique is an approach in which the silicon atoms are processed in a sequence to generate silicon nanowires. The most frequently used bottom-up fabrication techniques for silicon nanowire fabrication are Vapor Liquid Solid (VLS) phase, MBE, thermal evaporation, and chemical vapor deposition using pulse laser deposition. The preferred method is VLS.

*VLS Method*

The VLS mechanism is the most used in semiconductor nanowire production. The VLS mechanism relies on a vapor phase precursor of the nanowire material, which impinges on a liquid phase seed particle, from which unidirectional nanowire growth proceeds. Figure 2 shows a schematic sketch illustrating the widely adopted VLS growth.

Si precursors are evaporated by Si effusion cells, or pulse vapor deposition. Silicon gas precursors include monosilane (SiH4), trichlorosilane (SiHCl3) or higher order silanes. Catalyst is used as a collector of silicon. When gas precursors are used, the catalytic nature leads to lowering of the dissociation energies of the gas. Consequently, a high concentration of silicon atoms is found at the catalyst particle´s surface, leading to diffusion into the cluster. On the other hand, when employing gold catalyst clusters, the gold-silicon system can become liquid at temperatures above the eutectic point (363 °C), provided that sufficient fraction of Si is present (e.g., 18.6 at % at the eutectic temperature). In case of a constant silicon flow, silicon atoms will continue to diffuse into the Au–Si melt, although this is thermodynamically unstable. To reduce energies, the super-saturated or excess silicon atoms condense into the solid phase. Nucleation of Si occurs at the footprint of the Au–Si catalyst layer by layer. Consequently, a silicon monolith or nanowire is formed. Figure 3 shows the starting gold catalysts in Figure 3a, silicon nanowires grown on an oxidized silicon wafer in Figure 3b and a close-up view of ⟨110⟩ oriented silicon nanowires

*Benefits and Issues*

The advantages of implementing VLS are as follows: Lower reaction energy required compared to normal vapor-solid growth. Wires grow only in the areas activated by the metal catalysts and the size and position of the wires are determined by that of the metal catalysts. This growth mechanism can also produce highly anisotropic nanowire arrays from a variety of materials.

A drawback of the VLS process is that the metal catalyst could react with the target materials during growth at high temperatures, hence creating intermetallic compounds and contamination. Therefore, VLS that uses the metal element of the target metal oxide as a catalyst has been attempted by decomposing the metal oxide during growth for formation of high-quality products without contamination.

Therefore, VLS that uses the metal element of the target metal oxide as a catalyst (i.e., self-catalyst) has been attempted by decomposing the metal oxide during growth for formation of high-quality products without contamination. However, the decomposition temperature of most metal oxides is too high to control. Carbo-thermal decomposition, in which graphite powder is mixed with the metal oxide powder, can be used to reduce the decomposition temperature, but this process also has contamination problems, such as metal carbide formation.

## III. NANOWIRES ASSEMBLY

The main issue in the fabrication and synthesis of nanowire is the controlled assembly of nanowires. In solutions, nanowires are suspended directly and dropped onto substrates. After volatilizing the solutions, uniformly dispersed and assembled nanowires are generated. However, owing to the disordered structures of nanowires, large-scale nanowire arrays and integrated circuits relying on this approach are impossible to develop. Several post-growth approaches have been developed to overcome this challenge. Fluidic 5-alignment in microchannels is one of the earliest approaches for assembling nanowires. Using poly (dimethylsiloxane) mold (PDMS) fluidic channels on flat substrates, nanowire arrays are then assembled by passing nanowire suspensions through these channels at specified flow-rate with a proper functionality. Using the layer-by-layer 15 method, this technique can also be used to assemble nanowires into more complex crossed structures important for creating dense electronic device arrays. Assembly methods may be used to create nanowires with a wide variety of compositions and adaptable physical properties. Flexible electronics, electronic logic gates, renewable, and energy systems, are all using these structures. The incorporation of these nanostructures into systems could supplement current nanofabrication efforts. For instance, by compression in Langmuir-Blodgett trough, nanostructures suspended at an air-liquid interface can be formed

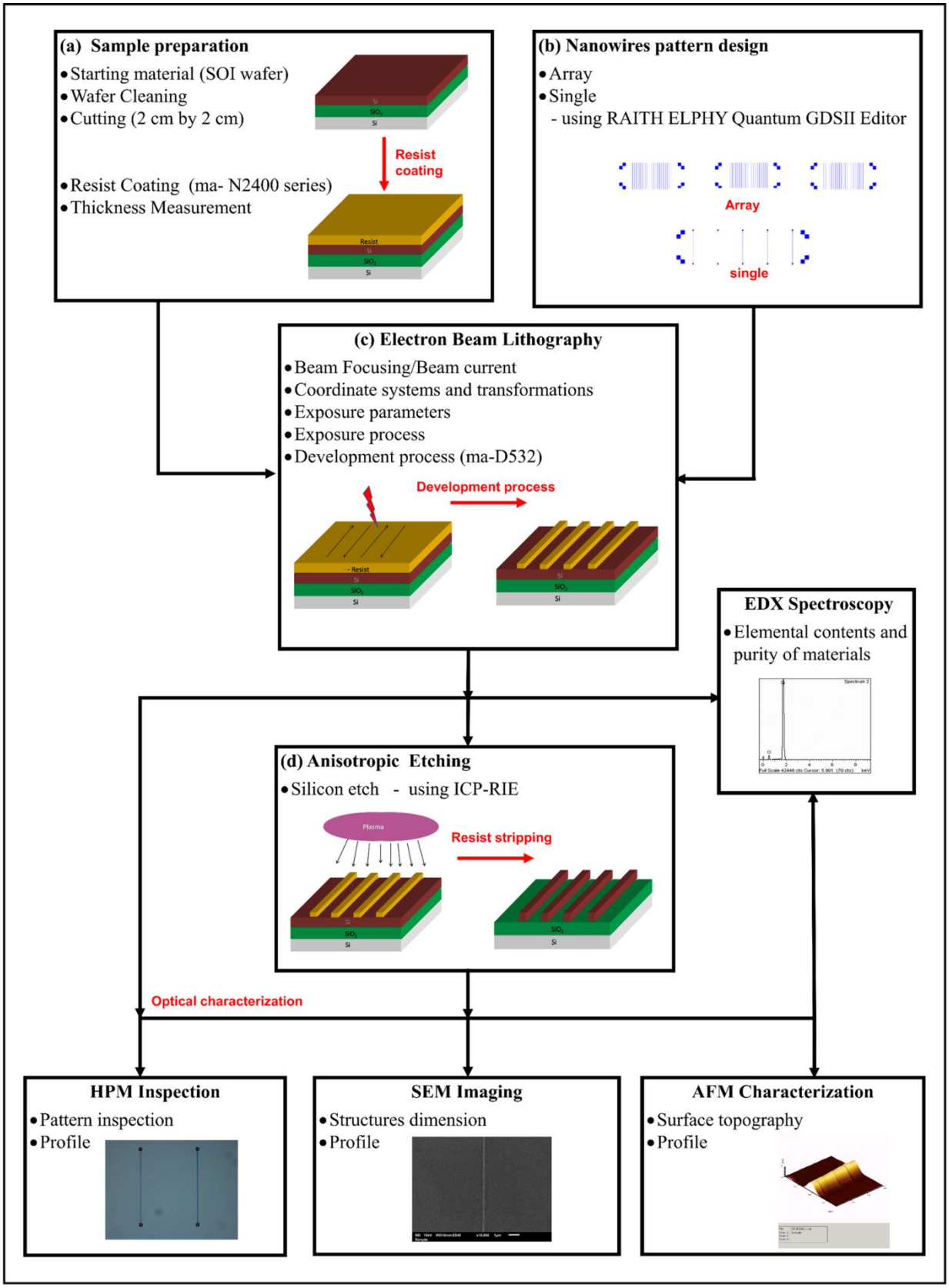
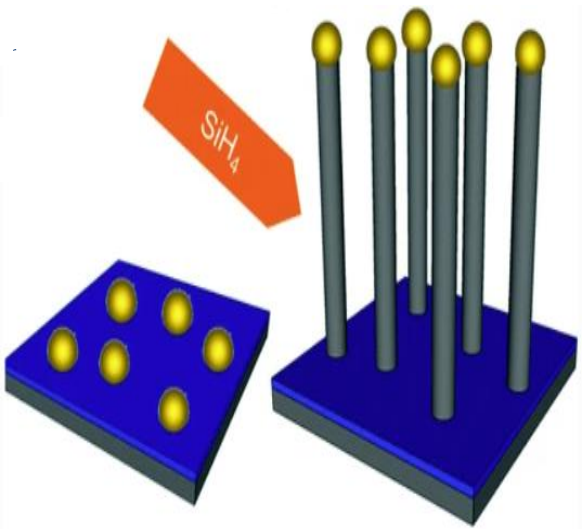
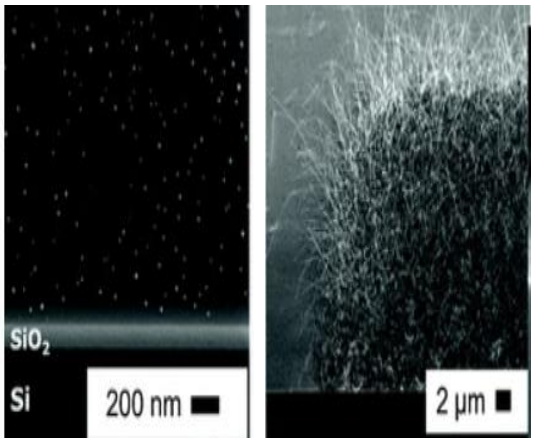



Figure 1: Top-down nanofabrication process of silicon nanowires using EBL.



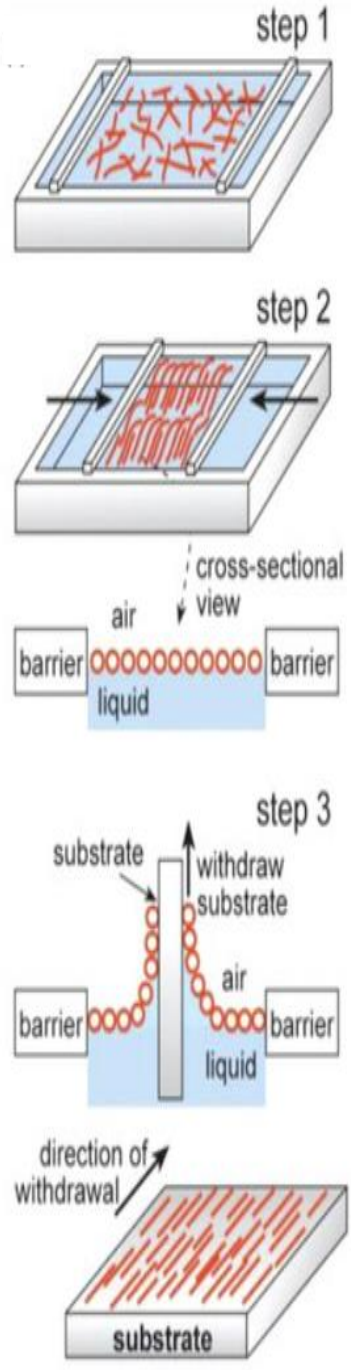

**a** **b**

Figure 2 a) Gold Particles formed on growth chamber b) VLS growth using silane as silicon precursor

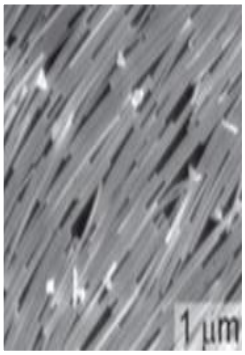



**a** **b**

Figure 3 a) catalytic gold particles formed by sub–nanometer sputter deposition of Gold and a subsequent coalescence with a combination of a thermal anneal in hydrogen atmosphere at 450 °C for 300 s and a subsequent plasma treatment b) Nanowires grown on an oxidized silicon substrate




**a**

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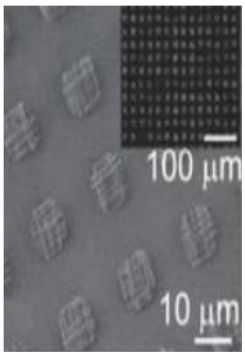


**d**

Figure 4 a) Assembly of Nanowire b) Langmuir-Blodgett approach
c) Langmuir-Schaefer approach atomic by force micrograph
d) crossed arrays of nanowires.

into dense films as indicated in Figure 4a. When the solvent withdraws from the surface of the substrate, a shear force is formed in the vertical direction, making the nanowires align in the same direction (Figure 4b). The nanowires form a close-packed structure to reduce the energy usage by the system during compression. These nanowires will then be printed onto a different substrate as shown in Figure 4c. Hierarchical structures can be created by repeating the assembly step, adjusting the orientation of the substrate into which the nanowires are transferred. As shown in Figure 4d, crossed nanowire arrays are created by removing unnecessary nanowire regions and integrating them into device architectures.

## IV. APPLICATIONS

### *a. Coronavirus (COVID-19) detection*

Nanowires are used to detect the coronavirus using a silicon nanowire biosensor. The threat is caused by the coronavirus virus, which is popularly known as SARS-CoV-2. Scientists around the world had attempted to detect the disease using several approaches. The nanowire FET biosensor is used to identify the virus based on nanomaterial, which allows high biosensor efficiency to be achieved in terms of selectivity, sensitivity, and low detection limit Silicon nanowire is also specific and sensitive to the detection of viral infections, so this can be used to diagnose the latest SARS-Cov-2 pandemic.

An example of detection technique of coronavirus using nanowire biosensor is shown in Figure 5. A nanowire biosensor was fabricated based on SOI technology and used for the detection of COVID-19 and virus-like particles. A nanowire biosensor based on silicon nanowire was developed and applied SARS-CoV nucleocapsid (N) protein. This sensor took the advantage of fibronectin-based antibody mimic proteins (AMPs) as probe agents. The antibodies possess higher affinity which provides rugged binding chemistry and higher specialty and selectivity compared to antibodies. The binding event is determined through measuring the current changes across the sensor. The antibody binds to the immobilized spike protein in the absence of the virus leading to voltage drop in the form square wave through voltammetry scope peak current. Once the virus is detected the amount of antibody binds to the immobilized viral antigen is reduced leading to the voltage to increase.

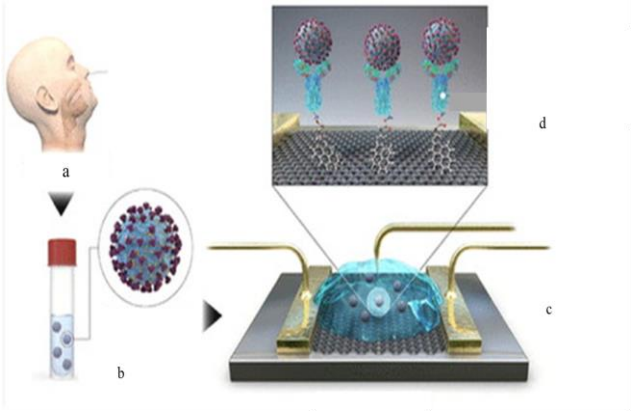


Figure 5a) Covid-19 Patient; b) SARS-CoV-2 virus; c) COVID-19 FET sensor; d) SARS-CoV-2 spike antibody

### *b. Crossed Nanowire Architecture*

Nanotechnology in the technology field increases the capability of electronics devices while dropping their weight and power consumption. It improves display screens on electronics devices, increases the density of memory chips and reduces the size of transistors used in integrated circuits. Various electronic device elements are allowed by the crossed nanowire architecture (gates, diodes, transistors, etc.) to be made with high integration density because the silicon nanowires have a small diameter. One can configure crossed nanowire FETs from one nanowire as the active channel and the gate electrode from the second crossed nanowire, separated on the silicon nanowire surface by a thin SiO2 dielectric shell, with the gate present on one or both crossed nanowire' surface. NOR gate's creation is the first example of the crossed nanowire architecture. It can be seen that when its input is both low according to expectations, only then does the gate's output go high.

### *c. Functionalization of nanowire for heavy metals detection application*

Any heavy metallic chemical substances (Cadmium, mercury, chromium, arsenic, lead and thallium) that have a relatively high density and are toxic or poisonous at low concentrations can be detected using nanowire biosensors. The smallest dimension of silicon nanowires shows strong electron transfer,

resulting in rapid detection response. An integrated silicon nanowire microfluidic chemical sensor is developed for the detection of heavy metals in water. The sensor is capable of distinguishing numerous types of heavy metal species due to its excellent detection capability. Tribonanosensors are able to selectively capture and identify radioactive heavy metal ions in wastewater. For instance, Si nanowires were tested against heavy metal lead (Pb). The device was fabricated via dry oxide etching approach with control oxygen flow rate in the oxidation furnace, a network of uniform Si nanowires was successfully fabricated. The device was functionalized by (3-aminopropyl) triethoxysilane (APTES) to save as a sensor to heavy metal. Due to the silicon electrochemical response toward heavy metal ions, linear response to three different sources of water was observed. The results indicated, Pb can be detected with high precision. These studies demonstrate the applicability of nanowires as reliable sensors for heavy metal detection in water.

## V. CONCLUSION

The paper summarized the developments in nanotechnology for various applications. Significant growth is made in nanowire application due to their unique properties. Various fabrication techniques, such as bottom-up and top-down techniques are reviewed in the paper. Both the approaches have their own merits and demerits, based on the application the approaches are chosen. Furthermore, assembly techniques of semiconductor nanowires are discussed. Nanowires are also useful in agriculture to understand plant behaviour under different environmental conditions using smart farming methods.

## VI. FUTURE SCOPE

The field nanotechnology is currently under the area of research. There are many opportunities for development in this field. In top -down approach, the EBL method has high throughput time, although it has a high resolution when compared to other methods, which can be improvised to be an efficient methodology. Trade-off between time and cost of production of nanowires. This issue can be focussed for large scale production with minimum time. Integration of nanowires with the devices is the most challenging part due to the size of the nanowire. Also, devices with nanowires should be less expensive, faster and reliable similar to conventional devices.

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