DESIGN OF DIGITAL PHASE LOCKED LOOP

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***Abstract*— In this paper, a Digital Phase Locked Loop (DPLL) is designed. DPLL is one of the most important devices in almost all electronic systems where it used for Transmitter circuit, Demodulation circuit, clock generator, frequency synthesis etc. A DPLL consists of a Phase Frequency Detector (PFD), a Charge Pump (CP), a loop filter, a current starved Voltage Controlled Oscillator (VCO), and a Divide-by-4 frequency divider. The whole design is done in a simulation tool called Cadence Virtuoso, using 65nm CMOS technology.**

***Keywords:* DPLL, PFD, CP, Loop filter, VCO, Frequency Divider**

I. INTRODUCTION

Phase locked loop (PLL) as the name itself defines that the phase difference in the oscillations will be locked in a loop that is, a system that generates oscillations while comparing the phase of the reference input in such a way that it continuously adjusts the frequency and phase to the VCO oscillations while comparing the frequency of the reference signal. Basic structure of PLL is as shown in Figure 1.

PLL circuit mainly consists of four blocks:

- Phase Frequency Detector (PFD)
- Charge Pump (CP)
- Loop filter
- Current Starved Voltage Controlled Oscillator (CSVCO)
- Frequency Divider (Feedback path)

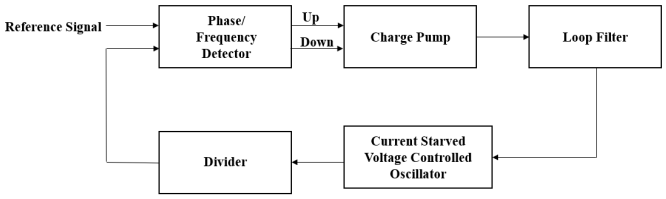

Figure 1: Block diagram of PLL

The PLL is classified into three types based on the implementation of the different blocks in it.

- Analog PLL: PLL in which all the blocks are implemented in analog. The multiplier is used as the phase detector in the analog PLL. The analog PLL finds applications in the frequency modulation and demodulation techniques.
- Digital PLL (DPLL): The phase detector is implemented in the digital class and the rest of the blocks are implemented in the analog class. The two D flip flops connected to each other with the reset path, which is known as phase frequency detector. To use DPLL as the frequency synthesizer connect the divider circuit in the feedback path. The output of the VCO is given as the input to the divider circuit which is in the feedback path and the output of the divider circuit is given as one of the inputs of the phase detector.
- All Digital PLL (ADPLL): The ADPLL consists of all the blocks in the digital class. The loop filter is replaced with the digital filter and VCO with the numerically controlled oscillator (NCO).

II. OPERATION OF DPLL

The reference clock is given as one of the inputs to the PFD which generates two output signals UP and DOWN. These are given as the inputs to the charge pump. The output of the CP is given to the loop filter which generates the required voltage which is fed to the VCO. The output of the VCO is given as another input to the PFD. When the input signal and VCO out signal are having same phase and frequency the PLL locks the signal.

Desired PLL is expected with higher lock range, less lock time and tolerable phase noise. The PLL enters lock mode when the input frequency and the output frequency is same, and it is known as lock in range.

Structure of PLL used in mm wave-THz application is shown in Figure 2. The divider chain consists of divide-by 4 Injection Locked Frequency Divider (ILFD) and Current Mode Logic (CML) blocks. True Single-Phase Clock (TSPC) is used to overcome the phase delay in the circuit.

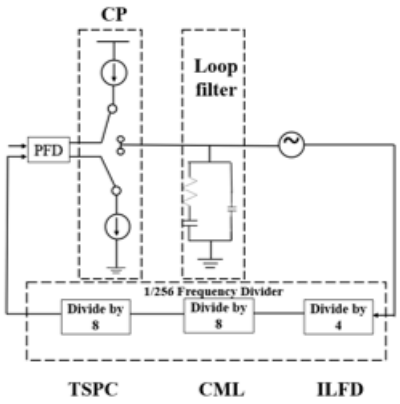

Figure 2: PLL structure

III. CIRCUIT ELEMENTS

A. Phase Frequency Detector

PFD is one of the important parts in PLL circuits. It is a circuit that measures the phase and frequency difference between two signals, i.e., the signal that comes from the FD. PFD has two outputs UP and DOWN which are signalled according to the phase and frequency difference of the input signals. Block diagram of PFD using D-flipflops and AND gate is shown in Figure 3.

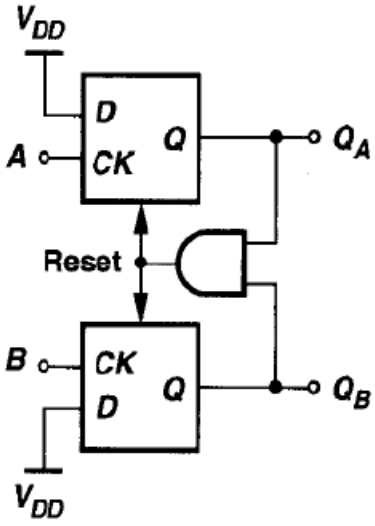

Figure 3: PFD block diagram

B. Charge Pump and Loop Filter

CP converts the phase and frequency difference signal into different range voltage, which is used to tune the VCO. A CP consists of two switched current sources that may pump charge in or out of the loop filter according to the logic states of Q_A and Q_B, as shown in Figure 4. I_1 and I_2 are generally equal and referred as Up and Down currents respectively.

In communication, higher frequencies, or higher order harmonics are considered undesirable, and it is necessary to remove those components from the output. In order to make the system more stable, it is suggested to add a resistor R in series with the capacitor C in the low pass filter. But since the CP drives the series combination of R and C, each time a current is injected in the loop filter, the control voltage experiences a large jump. Hence to minimize the ripple effect, a second capacitor is added in parallel to their series combination. The PLL filter is needed to remove any unwanted high frequency components which might pass out of the phase detector and appear in the VCO tune line. The loop filter is used to improve the performance of the PLL.

The outputs from the PFD are given to the charge pump circuit with the current source implementation in the circuit and the loop filter being integrated to the CP whose resistance and capacitances are calculated. The values of resistors and capacitances are calculated using the second order derivative. The implementation of the PFD, CP integrated along with the loop filter in cadence is shown in Figure 5.

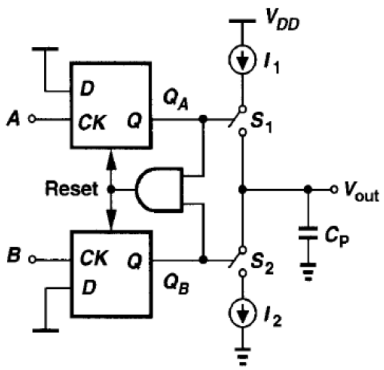

Figure 4: PFD along with CP

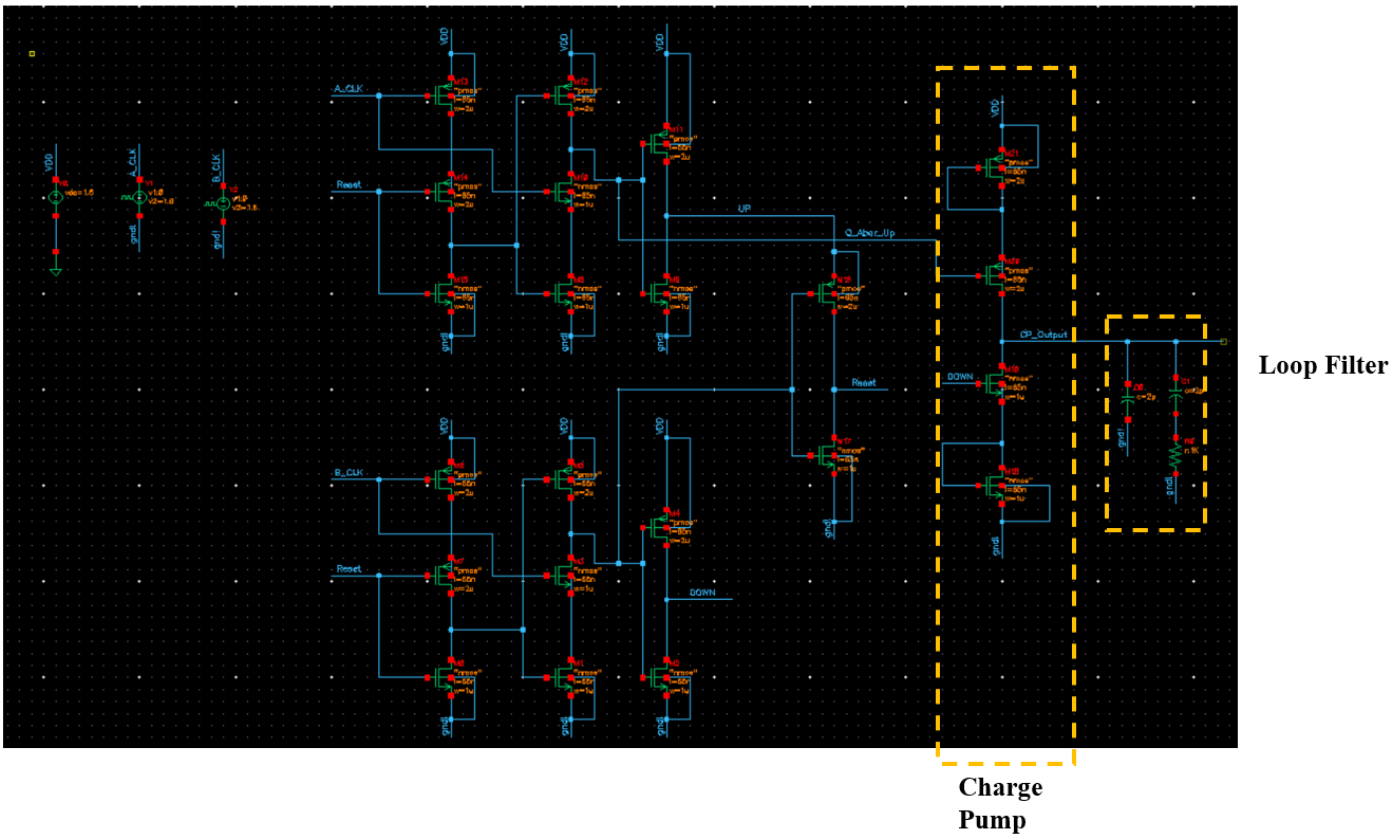

Figure 5: Circuit of PFD, CP integrated with a loop filter

C. Current Starved Voltage Controlled Oscillator

An oscillator produces periodic output, generally in the form of voltage. Most applications require control of the output frequency of the oscillator.

VCO is an electronic oscillator designed to be controlled in oscillation frequency by a voltage input. It generates a clock with a controllable frequency from -50% to +50% of its central value. The frequency of oscillation is varied by the applied DC voltage

"$V_{control}$". Current starved VCO is simple ring oscillator consisting of cascaded inverters. Cadence implementation of the three-stage Current starved VCO is indicated in Figure 6.

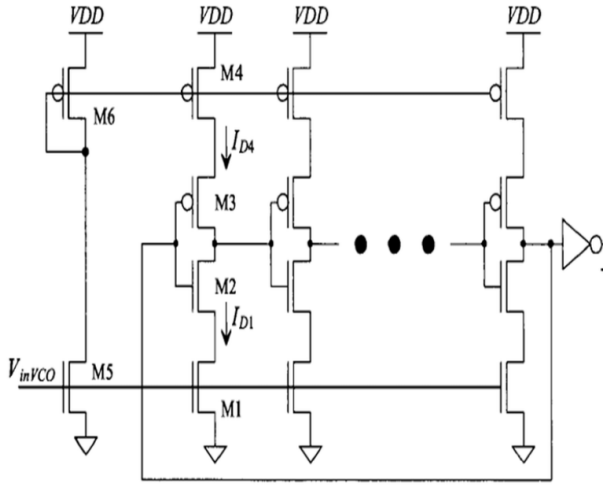

Figure 6: Basic Structure of Current Starved VCO

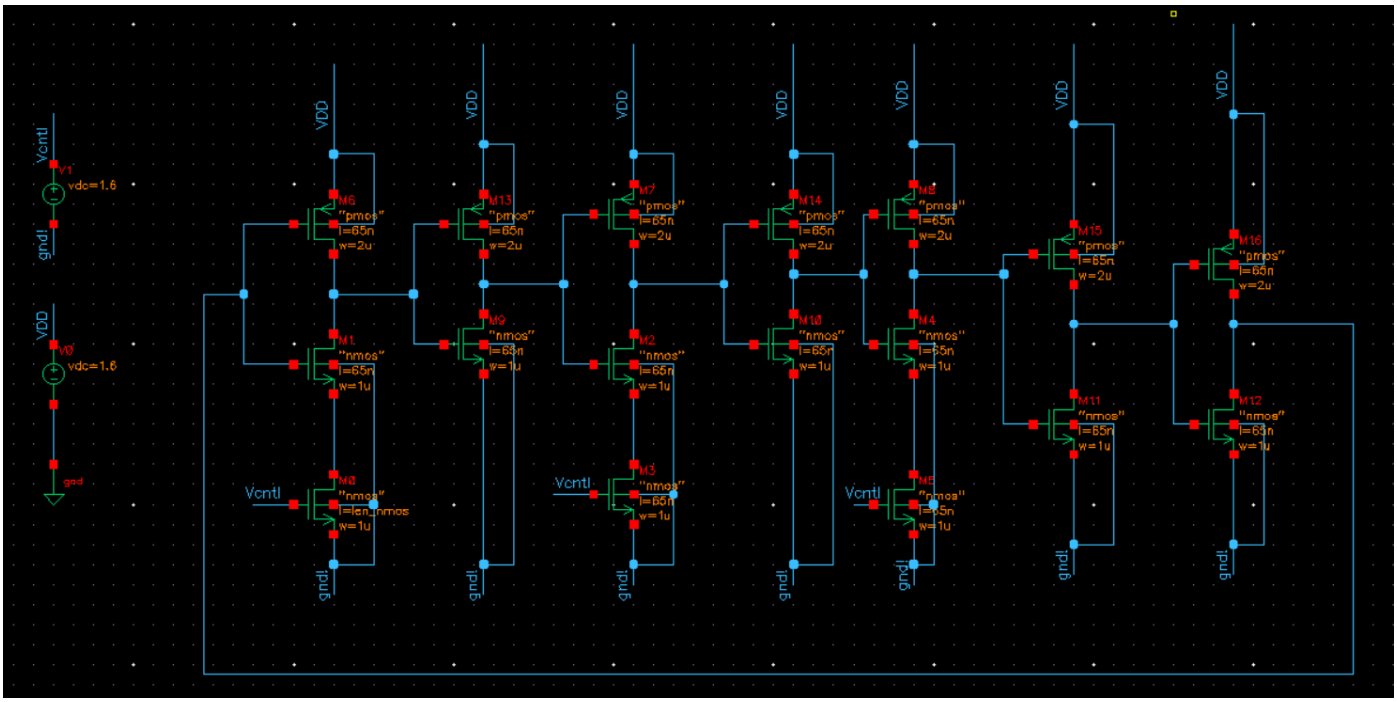

Figure 7: Implementation of current starved VCO

D. *Frequency Divider*

Frequency divider divides the VCO frequency to generate a frequency which is comparable with reference frequency. The input to the PLL is in the form of logic gates which limit the PFD operation to higher frequency. Hence frequency divider circuits are used. It is placed in feedback path which forms a closed loop. It divides the output frequency of VCO by two.

The circuit is designed to divide or drop the frequency of the high frequency signal to get the lower frequency signal for a given frequency signal by division. A divide-by-4 circuit is designed by cascading two divide-by-2 circuits. Divide-by-4 frequency divider is used to provide feedback from CSVCO to PFD. In this paper, it is implemented as shown in Figure 9. This structure reduces the time jitter of the VCO.

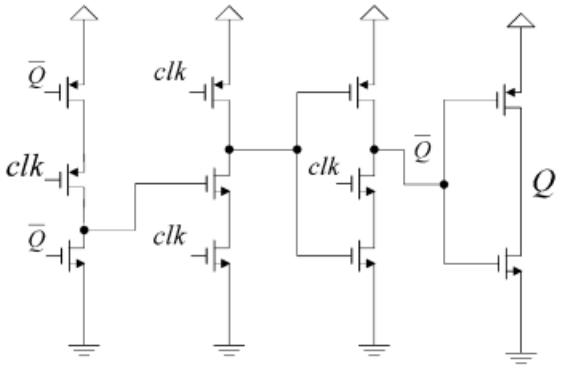

Figure 8: TSPC Divide-by-2 Frequency divider

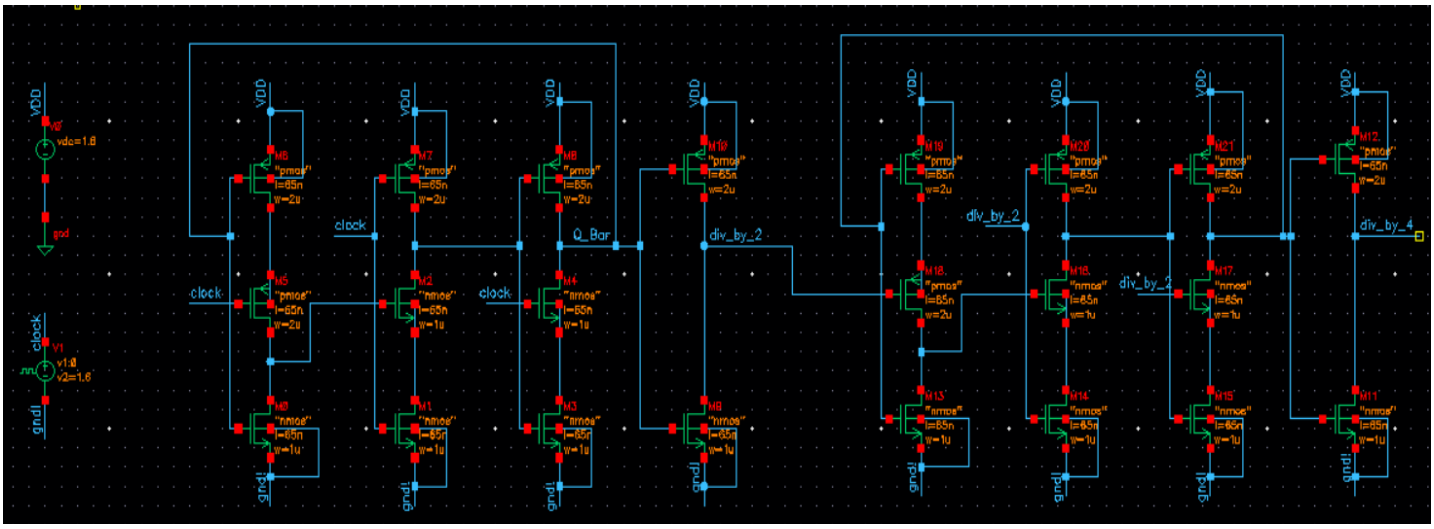

Figure 9: Divide-by-4 circuit implementation in Cadence

IV. INTERGRATION OF ELEMENTS TO DESIGN A DPLL

After the implementation of every sub-block of the DPLL such as the PFD, CP, loop filter, VCO and the divide-by-four counter, it is necessary to integrate the components to form a DPLL system. Integration of all elements form a DPLL. The implementation is as shown in the figure 10. Design parameters of the DPLL is as mentioned in Table 1.

PARAMETER	VALUE
Nmos Width (W_n)	1um
Pmos Width (W_p)	2um
Nmos Length	65nm
Pmos Length	65nm
Supply Voltage (VDD)	1.6V
Control Voltage (V_{cntl})	1.6V
Capacitance (loop filter)	2pF
Resistance (loop filter)	10k

Table 1: Design Parameters of DPLL

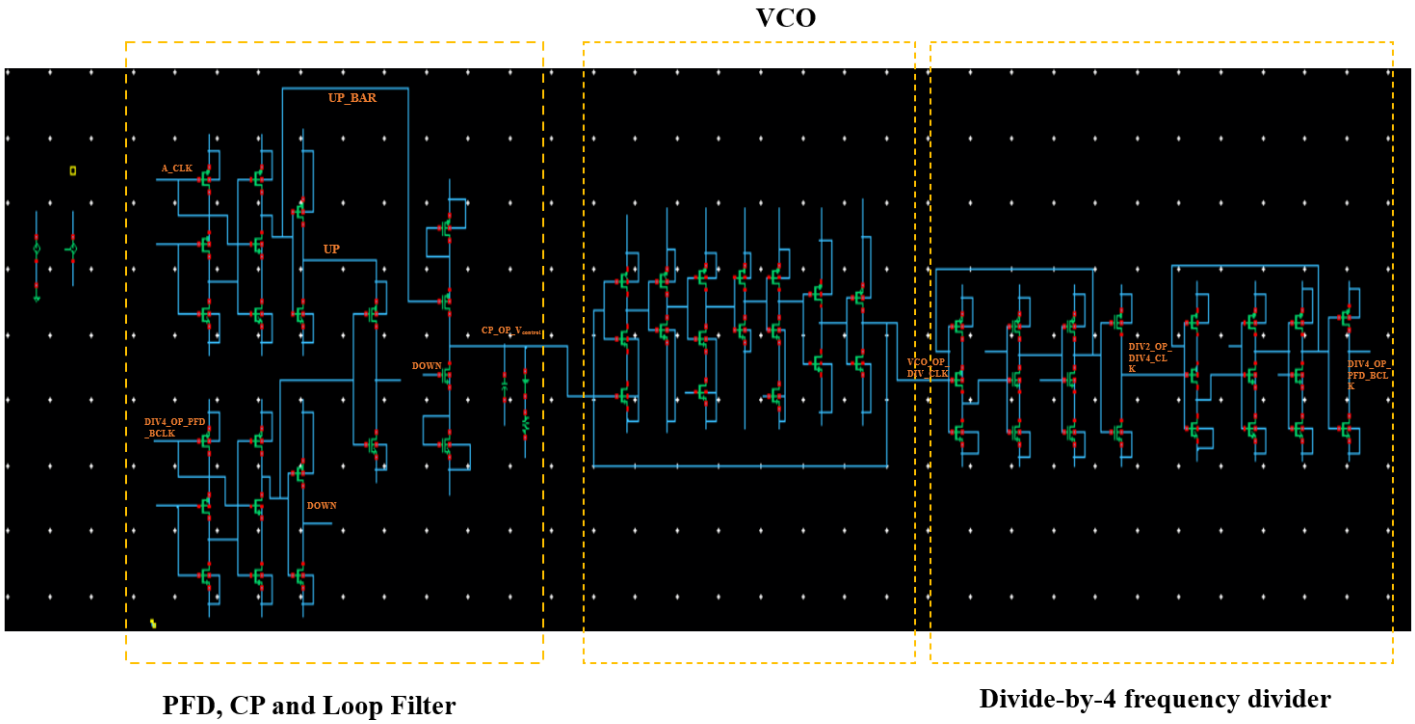

Figure 10: DPLL Schematic

V. SIMULATION RESULTS

PFD, CP and loop filter circuit designed in Figure 5 is as shown in Figure 11.

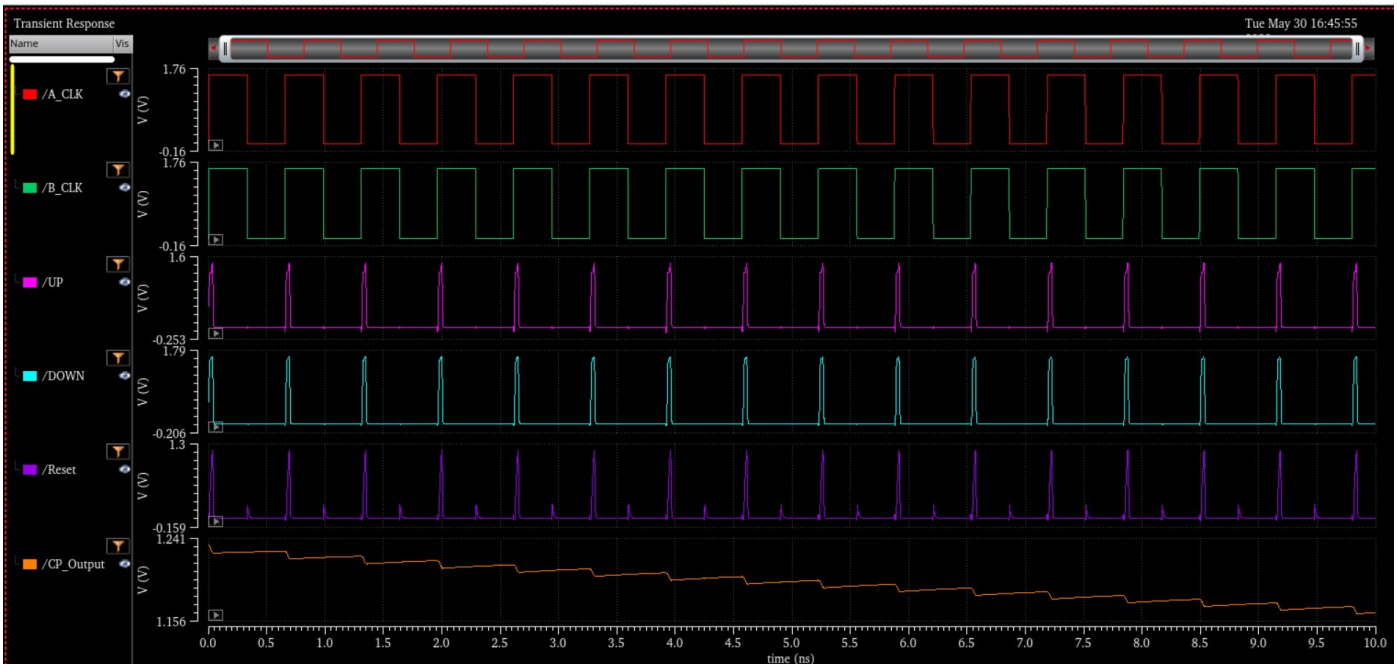

Figure 11: Output of PFD, CP and Loop Filter with input and reference in phase

Output of PFD, CP and Loop filter with input signal leading the reference signal is shown in Figure 12 and case where reference leads input signal is shown in Figure 13.

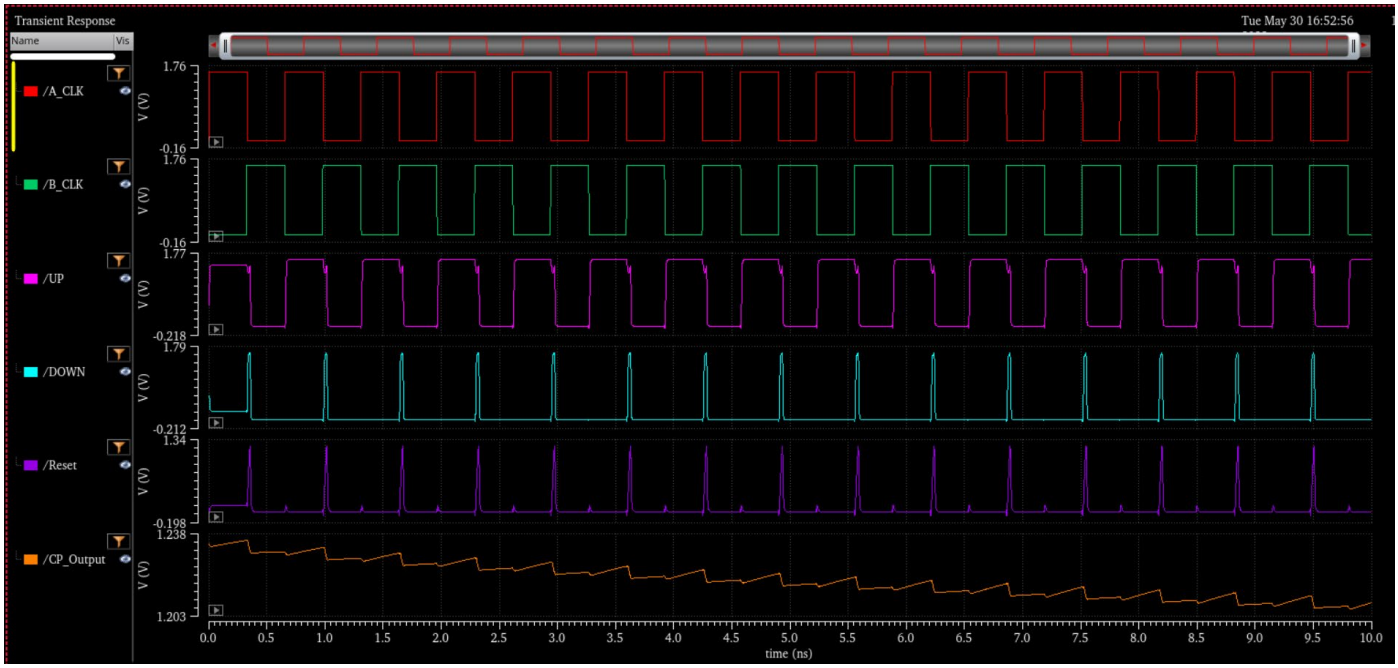

Figure 12: Output of PFD, CP and Loop Filter with input leading the reference signal

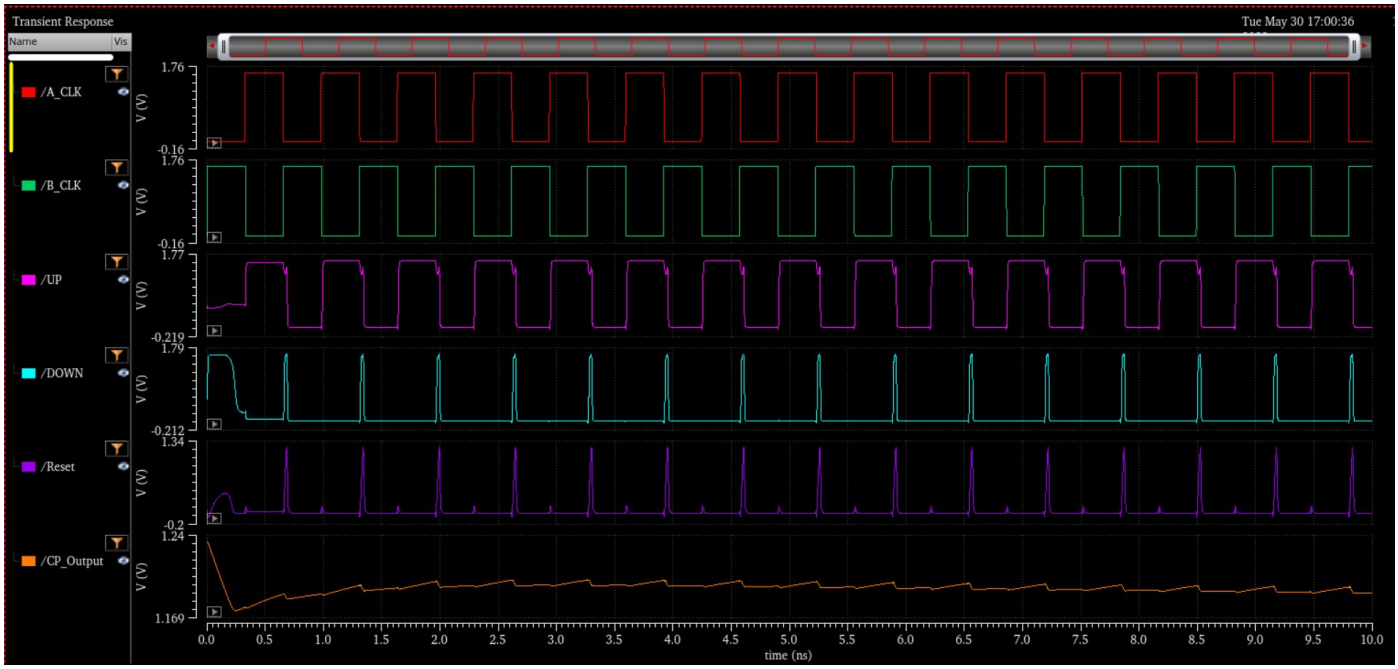

Figure 13: Output of PFD, CP and Loop Filter with reference leading the input signal

Output frequency of VCO when the control voltage and supply voltage are equal to 1.6V is about 12.25GHz.

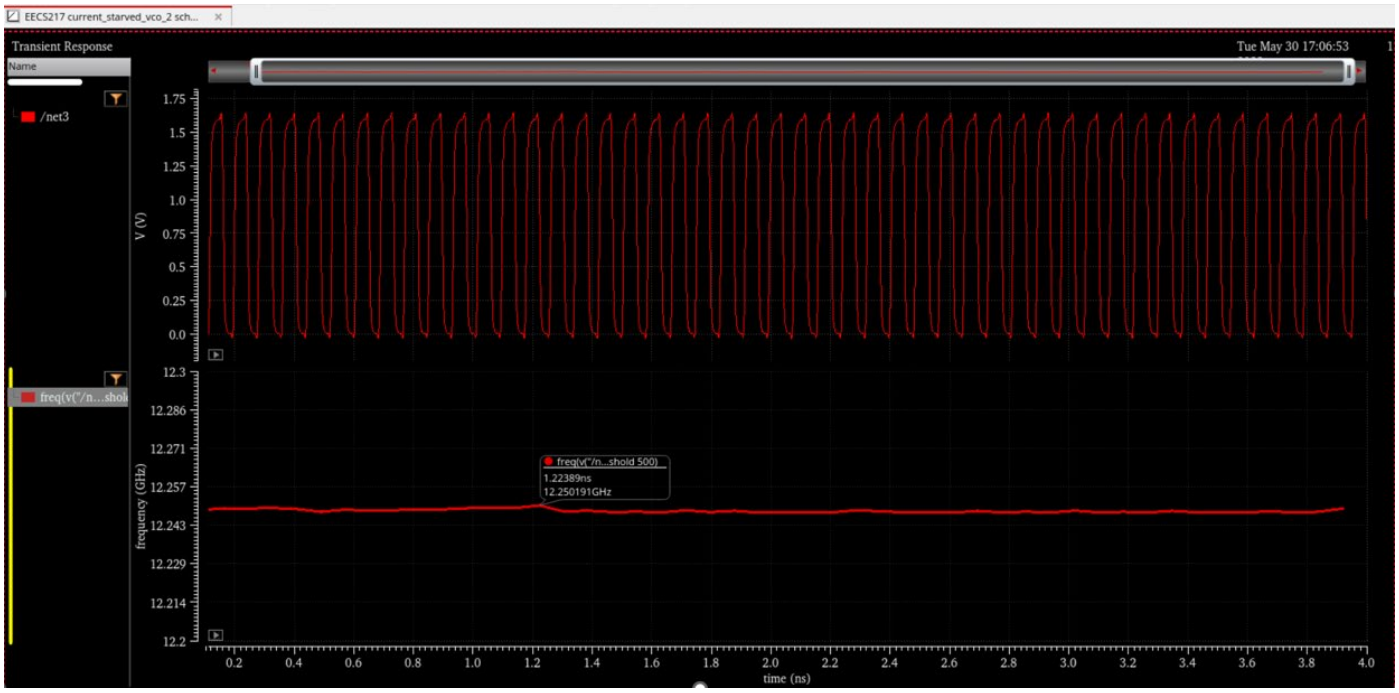

Figure 14: Output of VCO when V_{cntl} = VDD

Simulation of divide by 2 and divide by 4 frequency is shown in Figure 15.

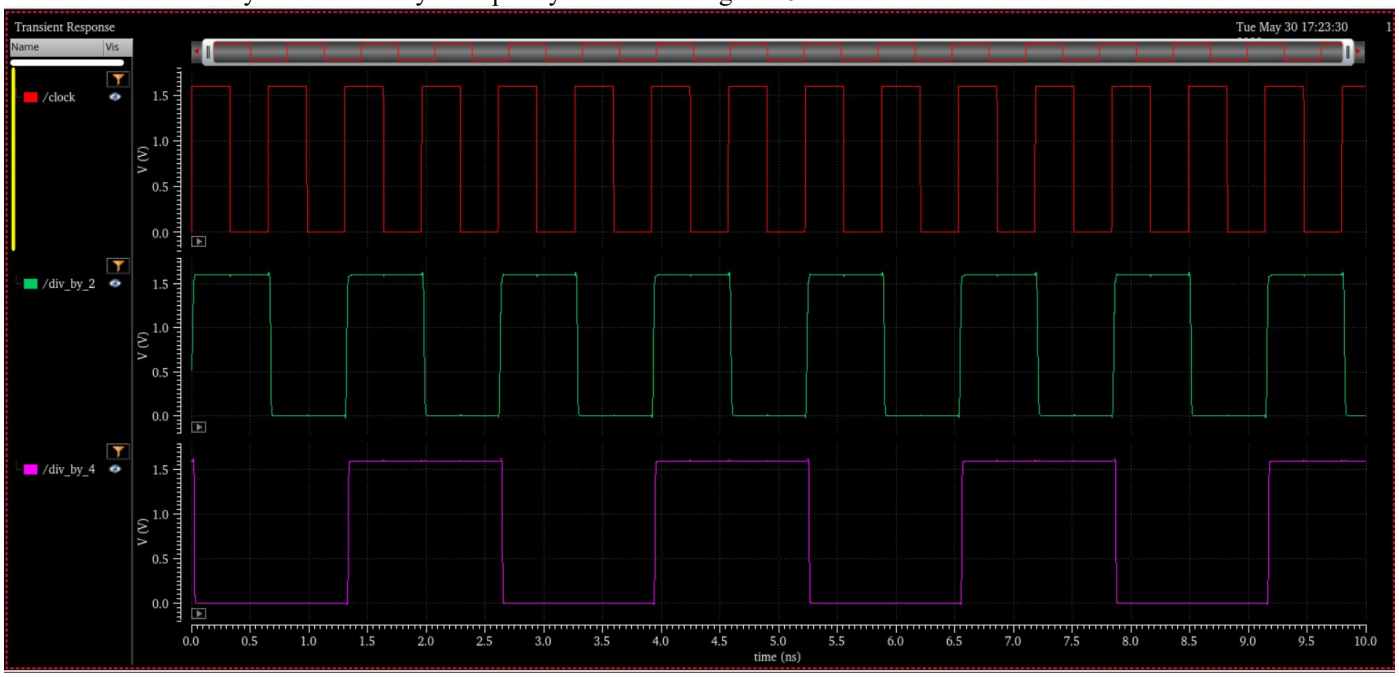

Figure 15: Output of frequency divider

Overall simulation result of the DPLL is as shown in Figure 16.

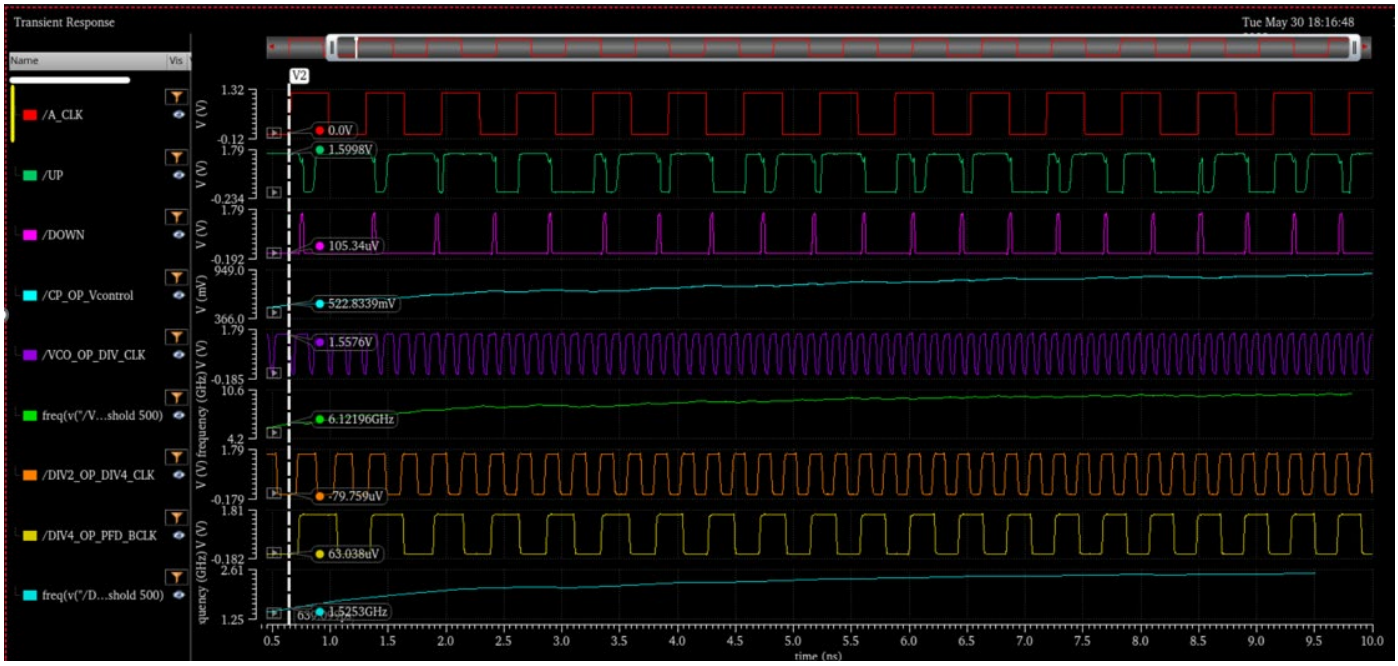

Figure 16: DPLL Simulation

Table 2 is a summary of the results observed.

Observation Parameter	Value	Conclusion
F_{max} from Figure 14	12.25GHz	-
$F_{out} = F_{max}/2$	6.125GHZ	Given in Problem statement
$F_{ref} = F_{ref}/4$	1.531GHz	Given in Problem statement
Output frequency of VCO in Figure 16	6.12GHz	Equals F_{max}
Divide-by-4 frequency divide output frequency	1.53GHz	Equals F_{ref}

Table 2: Summary of Results

When the reference clock (A_CLK) coincides with the divide-by-4 frequency divider output (DIV4_OP_PFD_BCLK), DPLL gets locked as shown in Figure 16. This locking can be seen from UP and DOWN graphs in Figure 16. When their average is 0, the DPLL is said to be locked state.

VI. APPLICATIONS OF DPLL

The most popular application of the DPLL is a frequency synthesizer. To achieve the output frequency double that of the input frequency, use the divide by 2 circuit in the feedback path. The VCO output is given as the input to the divider circuit which divides the frequency by 2 and this is fed as the input to the PFD which performs iterations to match the two signals. When the two signals are same in phase and frequency, DPLL enters into the lock mode and the output frequency is twice that of the input frequency.

VII. CONCLUSION AND FUTURE WORK

With the given specifications, a DPLL is designed that satisfies the requirements. To design a VCO by proper transistor sizing, the transistor sizing can be achieved by using optimization techniques. Also, to obtain a proper locking range, an LC oscillator could be used rather than current starved VCO.

The output frequency of the DPLL is measured to be **6.12GHz**.