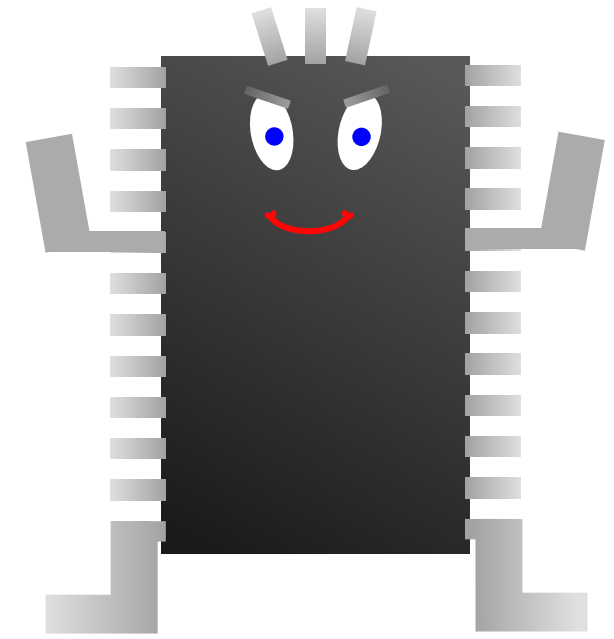


(physical) core



L1 cache

L2 cache

