SM

Instruction Cache

Instruction Buffer

Warp Scheduler

Dispatch Unit | Dispatch Unit

Register File (32,768 x 32-bit)

Core	Core	DP Unit	Core	Core	DP Unit	LD/ST	SFU
Core	Core	DP Unit	Core	Core	DP Unit	LD/ST	SFU
Core	Core	DP Unit	Core	Core	DP Unit	LD/ST	SFU
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Core	Core	DP Unit	Core	Core	DP Unit	LD/ST	SFU
Core	Core	DP Unit	Core	Core	DP Unit	LD/ST	SFU

Texture / L1 Cache

Tex | Tex | Tex | Tex

64KB Shared Memory