TCS-308

B. TECH. (CSE) (THIRD SEMESTER) END SEMESTER EXAMINATION, Oct., 2023

LOGIC DESIGN AND COMPUTER ORGANIZATION

Time: 11/2 Hours

Maximum Marks: 50

- **Note:** (i) Answer all the questions by choosing any *one* of the sub-questions.
 - (ii) Each sub-question carries 10 marks.
- 1. (a) Simplify F $(v, w, x, y, z) = \sum m (0, 2, 4, 6, 9, 13, 21, 23, 25, 29, 31)$ using K-map and implement the final output using NAND gates only. (CO1)

OR

(b) Simplify the following Boolean function $Y(A, B, C, D) = \sum m(0, 5, 7, 8, 9, 10,$

11, 14, 15)

using Quine-McCluskey minimization technique. Find the prime implicants and essential prime implicants.

(CO1)

2. (a) Realize the F (A, B, C D) = Σ m (0, 2, 3, 6, 8, 9, 12, 14) using 16:1 MUX and also 8:1 MUX with a as control variable.

(CO2)

OR

- (b) Design a 2-bit magnitude comparator and implement its logic circuit. (CO2)
- (a) Write any three differences between multiplexer and demultiplexer. Construct
 16 × 1 multiplexer with two 8 × 1 multiplexer and one 2 × 1 multiplexer.

(CO3)

OR

(b) With the help of decoder and external logic gates, design the combinational circuit defined by the following three Boolean functions: (CO3)

$$F_{1} = (\overline{y} + x)z$$

$$F_{2} = \overline{y}\overline{z} + x\overline{y} + y\overline{z}$$

$$F_{3} = (\overline{x} + y)z$$

4. (a) A sequential circuit with two D flip-flops, A and B; two input x and y; and one output z, is specified by the following next-state and output equations: (CO3)

$$A (t' + 1) = x'y + xA$$

$$B (t' + 1) = x'B + xA$$

$$z = B$$

- (i) Draw the logic diagram for the circuit
- (ii) Derive the state table.

OR

- (b) Discuss the problems of JK flip-flop. Do the following flip flop conversions: (CO3)
 - (i) D flip-flop to SR flip-flop
 - (ii) T flip-flop to J-K flip-flop

5. (a) Explain the design procedure for synchronous sequential circuits design with suitable example. (CO2)

OR

(b) Reduce the number of states in the following state table and tabulate the reduced state table and state diagram:

(CO2)

Present	Next State		Output	
State	x = 0	y = 0	x = 0	y=0
a	а	b	0	0
b	. c	d	0	0
c	а	d	0	0.
d	e	f	0	1
e	а	f	0	1
f	g	f	0	1
g.	а	f	0	1