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TCS–404

B. TECH. (CS)

(FOURTH SEMESTER)

END SEMESTER EXAMINATION,

June/July, 2022

COMPUTER ORGANIZATION

Time : Three Hours

Maximum Marks : 100

Note : (i) All questions are compulsory.

(ii) Answer any *two* sub-questions among (a), (b) and (c) in each main question.

(iii) Total marks in each main question are **twenty.**

(iv) Each sub-question carries 10 marks.

1. (a) Discuss Moore's law. Differentiate between computer architecture and computer organization. (CO1)

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(b) Consider if P is 16-bit signed integer. The 2's complement representation of P is $(F87B)_{16}$. Find the 2's complement representation of $8 \times P$. (CO1)

(c) What is Restoring Division Algorithm ? Draw its flowchart. Find 45 divided by 6 using Restoring Division algorithm for unsigned numbers, where dividend will be of 6 bits. (CO1)

2. (a) Write a sequence of instructions that will compute the value of $y = x^2 + 2x + 3$ for a given x using : (CO2)

(i) three-address instructions

(ii) two-address instructions

(iii) one-address instructions

(b) Discuss control unit, its components and functionality with the help of a diagram. Differentiate between hardwired and micro-programmed control unit. (CO2)

(c) Consider the following information for a basic computer : (CO2)

The content of the Program counter is 4AE. The content of Accumulator is 6EA3. The content of memory at address 4AE is 942E. The content of memory at address 42E is 09AC. The content of memory at address 9AC is 06B0. (All numbers are in hexadecimal). Opcode bits = 001 means the Addition operation.

The format of instruction (16 bit) assumed in question is :

Mode bit	Opcode	Address part
(1 bit)	(3 bits)	(12 bits)

What will be the final content inside the Accumulator after the instruction is fetched and executed next (solution steps are required) ?

3. (a) (i) Explain the working of DMA with its block diagram. Also explain the concept of cycle stealing mode and burst mode.

(ii) A hard disk with a transfer rate of 10 Mbytes / second is constantly

transferring data to memory using DMA. The processor runs at 600 MHz, and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation ?

(CO3)

(b) (i) Explain what Interrupt is with its classifications. Also explain the interrupt cycle with the help of a suitable diagram.

(ii) Assume, 1 GHz CPU is doing Input Output operations as per programmed I/O. CPU wants to read 50 bytes from the I/O device. So the CPU writes the Read command to the I/O interface register in 1000 cycles. The I/O operation between I/O interface and

device is done in 2000 cycles. Assume one complete I/O operation takes 1 CPU clock cycle time. Calculate the percentage of CPU Overhead, percentage of CPU utilization, Latency of I/O Operation and throughput. (CO3)

(c) What is priority interrupt ? Discuss the approach to handle priority interrupt. Explain Daisy chain method with the help of a diagram. (CO3)

4. (a) Consider a 4 set associative cache (initially empty) with total 16 cache blocks. The main memory consists of 256 blocks and the request for memory blocks is in the following order : (CO4)

0, 255, 1, 4, 3, 8, 133, 159, 216, 129, 63, 8, 48, 32, 73, 92, 155.

Show the missing contents of the cache, miss ratio and hit ratio for each of the below policies :

(i) LRU replacement policy.

(ii) FIFO replacement policy.

(iii) MRU replacement policy.

(b) Show the memory hierarchy with the help of a diagram showing speed, cost, and size variation. What do you understand by the term locality of reference ? Explain in detail spatial and temporal locality of reference with the help of a diagram. (CO4)

(c) A cache memory with a capacity of 16 kB is built using a block size 8 words. The word length is 64 bits. The size of physical address space is 4 GB : (CO4)

(i) Find the number of tag bits, line no. bits and block field bits using direct mapping.

(ii) Find the number of tag bits, set no. bits and block field bits using set associative mapping.

(iii) Find the number of tag bits and block field bits using associative mapping.

(iv) To which cache block will main memory address $(0DB63)_{16}$ will map.

(v) To which set no will main memory address $(14A231B2)_{16}$ will map.

5. (a) Discuss parallel processing. Explain in brief the classification of computers based on Flynn's Taxonomy with diagram for each. (CO5)

(b) Explain pipelining with example. Also discuss types of pipeline. An instruction pipeline consists of 4 stages : Fetch (F), Decode operand field (D), Execute (E), and Result-Write (W). The five instructions in a certain instruction sequence need these stages for the

different number of clock cycles as shown by the table below : (CO5)

Instruction	F	D	E	W
1	1	2	1	1
2	1	2	2	1
3	2	1	3	2
4	1	3	2	1
5	1	2	1	2

Find the number of clock cycles needed to perform the 5 instructions.

(c) Differentiate between : (CO5)

(i) Tightly coupled and Loosely coupled multiprocessor system.

(ii) RISC and CISC architecture.