H Roll No. 2194026

TCS–404

B. TECH. (CSE)
(FOURTH SEMESTER)
END SEMESTER EXAMINATION,
June, 2023

COMPUTER ORGANIZATION

Time : Three Hours

Maximum Marks : 100

Note : (i) All questions are compulsory.

(ii) Answer any ***two*** sub-questions among ((a), ((b) and ((c) in each main question.

(iii) Total marks in each main question are **twenty**.

(iv) Each sub-question carries 10 marks.

1. (a) Perform signed multiplication (+25) and (–7) using Booth's Multiplication Algorithm. (CO1)

(b) Compare the Von Neumann and non-Von Neumann Model with the help of a block diagram. What is meant by Von Neumann bottleneck ? (CO1)

P. T. O.

(c) What is restoring division algorithm ? Explain with the help of a flowchart. Perform division of unsigned integer 15/4 using restoring division algorithm. (CO1)

2. (a) What is Instruction format ? Explain Instruction cycle with the help of a flow chart. (CO2)

(b) (i) Mention the advantages and disadvantages of micro-programmed control and hardwired control.

(ii) Draw the block diagram and explain how data is transferred with the help of DMA.

(c) What are Shift Micro-operations ? Starting from initial value of R = 100100100, determine the sequence of binary values in R after a logical shift left, followed by a circular shift left, followed by an arithmetic shift right and circular shift right. (CO2)

3. (a) What are Interrupts ? Briefly explain various types of interrupts. (CO3)

   (b) Explain Input-Output processor with neat block diagram. Define CPU-IOP communication with diagram. (CO3)

   (c) Define I/O interface. What are the requirements of it? Explain its structure. (CO3)

4. (a) What is Memory Hierarchy ? Show the memory hierarchy with the help of a diagram showing speed, cost and size. (CO4)

   (b) Consider a direct mapped cache of size 512 KB with block size 1 KB. There are 7 bits in the tag. Find : (CO4)

      (i) Size of main memory

      (ii) Tag directory size

   (c) Explain LRU, LFU cache replacement policy and FIFO cache replacement policy with an suitable example. (CO4)

5. (a) What is pipeline ? Explain Instruction pipelining with the help of an example. (CO5)

(b) A non-pipelined system takes 60 ns to process a task. The same task is processed via 5 stage pipeline having their delays as 3 ns, 2 ns, 5 ns, 15 ns, 3 ns. The buffer registers with delay of 1 ns each are used in between the stages. What is the speedup achieved for 60 tasks ? (CO5)

(c) (i) Differentiate between RISC and CISC architecture in detail.

(ii) Differentiate between Loosely coupled and Tightly coupled multiprocessor system. (CO5)