H Roll No. 2294038

TCS–308

B. TECH. (CSE) (THIRD SEMESTER)
END SEMESTER
EXAMINATION, Dec., 2023

LOGIC DESIGN AND COMPUTER ORGANIZATION

Time : Three Hours

Maximum Marks : 100

Note : (i) All questions are compulsory.

(ii) Answer any *two* sub-questions among (a), (b) and (c) in each main question.

(iii) Total marks in each main question are **twenty**.

(iv) Each sub-question carries 10 marks.

1. (a) $A + B\overline{C} + \overline{A}C$, Implement this logic expression using NAND-NAND logic gates and NOR-NOR logic gates only.

(CO1 & CO2)

P. T. O.

(b) Simplify : (CO1 & CO2)

$F(A, B, C, D, E) = \Sigma m\ (0, 1, 6, 7, 8, 10, 11, 14, 15, 30, 31) + \Sigma d(23, 28, 29)$

using K-map and implement the final output with NAND gates only.

(c) Find the minimal sum of products for the Boolean expression : (CO1 & CO2)

$F(A, B, C, D) = \Sigma m\ (1, 2, 3, 7, 8, 9, 10, 11, 14, 15)$

using Quine-McCluskey method.

2. (a) Design a 3-bit binary to graycode converter and also draw its logic diagram. (CO3)

(b) Design a BCD to 7-segment display decoder using unused BCD combinations of BCD as don't care condition. (CO3)

(c) An 8 × 1 multiplexer has inputs A, B and C connected to selection inputs of S_2, S_1 and S_0 respectively. The data inputs I_0 through I_7 are as follows : (CO3)

$$I_1 = I_2 = 0$$

$$I_3 = I_7 = 1$$

$$I_4 = I_5 = D$$

and $$I_0 = I_6 = \overline{D}.$$

3. (a) Implement a full adder with decoder and NAND gates. The adder inputs are A, B and C. The adder produces the outputs S and C_0. (CO5)

   (b) Implement the following two given Boolean functions with a PLA. (CO5)

$$F_1(A, B, C) = \sum(0, 1, 2, 4)$$

$$F_2(A, B, C) = \sum(0, 5, 6, 7)$$

   (c) Design a synchronous Mod-6 counter, also using J K flip flops draw its logic diagram. (CO5)

4. (a) Explain the working of Johnson Counter and Universal Shift register. (CO4)

   (b) A sequential circuit has one positive edge triggered DFF and one full adder with two inputs x and y and one output S. Carry output of Full adder is connected to D input of DFF and Q output of DFF is acting as third input to Full adder. Draw the state table and state transition diagram. (CO4)

(c) The contents of four bit register are initially 1011. The register is shifted six times to the right with the serial input 101111. What are the contents of the register after each shift ? Illustrate with timing diagram. (CO4)

5. (a) Explain the following with support of flow chart : (CO4)

Programmed I/O, Interrupt driven I/O, Direct memory access.

(b) Explain the floating point arithmetic operations with the help of flowchart. (CO5)

(c) Explain various types of addressing modes. (CO5)