H Roll No. .....

TMC–102

M. C. A. (FIRST SEMESTER)
MID SEMESTER
EXAMINATION, Jan., 2023

COMPUTER ORGANIZATION AND ARCHITECTURE

Time : 1½ Hours

Maximum Marks : 50

Note : (i) Answer all the questions by choosing any ***one*** of the sub-questions.

(ii) Each sub-question carries 10 marks.

1. (a) Explain any *four* logic gates with the diagrams, and truth table with their working. Explain principle of duality. (CO1)

OR

(b) Discuss Boolean algebra. (CO1)

P. T. O.

2. (a) Minimize following Boolean expression using K-Map. (CO2)

(i) $F(x, y, z) = x'y'z + xy'z' + x'yz' + xyz$

(ii) $F(A, B, C) = (A' + B + C)(A + B' + C')(A' + B' + C')(A' + B' + C)$

OR

(b) Explain Full adder and full subtractor. (CO2)

3. (a) What do you mean De-multiplexer and decoder ? Implement half subtractor using decoder. (CO1)

OR

(b) Convert the 32 bit single precision IEEE standard 754 number shown below into its binary equivalent : (CO1)

11010110101101101011000000000000

4. (a) Draw the explain the flowchart of Booth multiplication algorithm. (CO1)

OR

(b) Explain Instruction Cycle. Draw the flow-chart of Fetch, and Decode instruction. (CO1)

5. (a) Create 32 bit single precision IEEE standard 754 representation of the binary number : (CO2)

0.000000110110100101

OR

(b) Solve the following : (CO2)

(i) $(1101)_2 + (1001)_2$

(ii) $(1101)_2 - (1001)_2$

(iii) $(234)_{10} = (?)_{BCD}$