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TCS–404

B. TECH. (CSE)

(FOURTH SEMESTER)

MID SEMESTER EXAMINATION,

April/May, 2022

COMPUTER ORGANIZATION

Time : 1½ Hours

Maximum Marks : 50

Note : (i) Answer all the questions by choosing any *one* of the sub-questions.

(ii) Each question carries 10 marks.

1. (a) Explain the Stored Program computer with respect to Von Neumann Architecture ? What is meant by Von Neumann bottleneck ? How can it be resolved ?

10 Marks (CO1)

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OR

(b) (i) What are the advantages of 2's complement over 1's complement and sign magnitude representation.

10 Marks (CO1)

(ii) Find the addition of the no. given below in 2's complement representation showing all calculations with overflow generated or underflow generated if any (8 bit range) :

(I) $(-40) + (-45)$

(II) $(+45) + (-65)$

(III) $(-103) + (-69)$

(IV) $(-120) + (-27)$

(V) $(+150) + (+101)$

2. (a) State the Booth's algorithm for multiplication of $-22^* - 19$. Draw a tracing table for the implementation of the Booth's algorithm for determining the product of two 12-bit signed numbers.

10 Marks (CO1)

OR

(b) (i) Given the following binary number in 32 bit (single precision) IEEE-754 format :

00111110011011010000000000000000. Find the decimal value closest to this floating-point number.

10 Marks (CO1)

(ii) Consider three registers R1, R2 and R3 that store number in IEEE-754 single precision floating point format. Assume that R1 and R2 contain the values (in hexadecimal notation) 0×42200000 and $0 \times C1200000$, respectively, If R = R1/R2, what is the value stored in R3 in IEEE-754 single precision floating point format ?

3. (a) You have a main memory which has 1024 locations and each location contains the contents of 2 bytes. A program is loaded from memory address 500 (in decimal).

The format of instruction assumed in question is :

Mode bit	Opcode	Address part

The instruction stored at memory address 500 is :

1	MOV	R1,900

Content at memory address 250, 900, 1000 is 450, 1000, 25 respectively. What will be the contents inside PC, MAR, MDR, IR registers after the execution of the instruction at address 500.10 Marks (CO2)

OR

(b) What is addressing mode ? Explain different types of addressing mode. Solve the following numerical : An instruction is stored at location 500 with its address field at location 501. The address field has the value 600. A processor register R1 contains the number 200. Evaluate the effective address if the address mode of the instruction is (a) direct (b) immediate

(c) relative (d) register indirect (e) index with R1 as the index register.

10 Marks (CO2)

4. (a) Discuss the various factors affecting the performance of computer ? Suppose a program (or a program task) takes 1 billion instructions to execute on a processor running at 2 GHz. Suppose also that 50% of the instructions execute in 3 clock cycles, 30% execute in 4 clock cycles, and 20% execute in 5 clock cycles. What is the execution time for the program or task ?

10 Marks (CO2)

OR

(b) An 8-bit register contains the binary value 10011100. What is the register value after an arithmetic shift right ? Starting from the initial number 10011100, determine the register value after an arithmetic shift left, and state whether there is an overflow now. 10 Marks (CO2)

5. (a) What is instruction ? What do you understand by the term instruction cycle explain with the diagram ?

10 Marks (CO2)

OR

(b) What are the bus in context to computer system ? Explain the single bus organization with diagram.