Graphic Era
HILL UNIVERSITY
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University under section 2(f) of UGC Act, 1956

Mid Term (Odd) Semester Examination October 2024

Roll no...../.....

Name of the Course and semester: B.Tech III
Name of the Paper: Logic Design and Computer Organization
Paper Code: TCS 308

Time: 1.5 hour Maximum Marks: 50

Note:

(i) Answer all the questions by choosing any one of the sub questions
(ii) Each question carries 10 marks.

Q1. (10 Marks) CO1

a. Design 4:1 Multiplexer using 2:1 Multiplexer.
Implement the Boolean expression $F(A, B, C) = \sum m(0, 2, 5, 6)$ using 4 : 1 multiplexer.

OR

b. What is Decoder? Design 3 to 8 line decoder using two 2 to 4 line decoder also draw the logic circuit & truth table.

Q2. (10 Marks) CO1 & CO2

a. What do you mean by a half adder? Explain with the help of block diagram, truth table and logic diagram.

OR

b. Explain serial in serial out shift register. The content of a 4 bit register is initially 1101. The register is shifted six times to the right with the serial input being 101101. What is the content of the register after each shift?

Q3. (10 Marks) CO1

a. What is the difference between combinational circuit and sequential circuit? Also draw the logic diagram for both the circuit.

OR

b. Write a short note on:
i. Magnitude Comparator
ii. 2 bit Binary Multiplier

Q4. (10 Marks) CO2

a. simplify the following Boolean function,
$F(A, B, C, D) = m(3, 9, 11, 12, 13, 14, 15) + d(1, 4, 6)$ using Quine-Mc Clusky tabular method.

OR

b. Implement AND, OR and NOT gate using NAND gate.

Q5. (10 Marks) CO2

a. Draw and explain the characteristic table and excitation table of D and T Flip-Flip.

OR

b. Convert JK Flip Flop to T Flip Flop with required truth table and logic diagram.