Roll No.

H

## TCS-402/TIT-402

## B. Tech. (CSE/IT) (Fourth Semester) End Semester EXAMINATION, 2014

**COMPUTER ORGANIZATION** 

Time: Three Hours]

[ Maximum Marks: 100

Note: (i) This question paper contains two Sections: Section A (Part I and II) and Section B.

- (ii) Answer all questions in Section A (Part I) briefly in not more than 50 words. Each question carries 2 marks.
- (iii) Answer any *four* questions from Section A (Part II). Each question carries 6 marks.
- (iv) Answer any *four* questions from Section B. Each question carries 14 marks.

## Section-A

## Part-I

2 each

- 1. Attempt all questions briefly in not more than 50 words:
  - (i) Differentiate between macro-operation and micro-operation.

K-57

P. T. O.

- (ii) What is control function?
- (iii) Define computer organization.
- (iv) Describe various types of Interrupts.
- (v) Explain virtual memory concept.
- (vi) What is pipelining?
- (vii) Define hit and miss ratio.
- (viii) What is the difference between direct and indirect address instruction? Explain with example.
- (ix) Describe the various functional units of a computer.
- (x) Why Input-Output interface is required ? Explain.

Part—II 6 each

- 2. Write short notes on any four of the following:
  - (a) What is cache coherence?
  - (b) What is the difference between Static RAM and Dynamic RAM?
  - (c) What are the differences between Hardwired C. U. and Micro-programmed C. U.?
  - (d) Explain serial communication protocol 'RS 232'.
  - (e) Distinguish between a memory word and a control word.
  - (f) What are the characteristics of multiprocessors?

3. (a)

Note: At

(b)

4. (a)

(b)

5. (

K-57

Section—B

14 (7+7) each

Note: Attempt any four questions.

3. (a) Draw the block diagram of Hardwired Control Unit. Also draw the timing diagram of the statement:

$$D_4T_5:SC \leftarrow 0$$

- (b) Draw and discuss the various stages of memory hierarchy for the computer system.
- 4. (a) Find the value of  $(-13) \times (+9)$  using Booth algorithm to multiply two signed 2's complement numbers.
  - (b) What is the use of stack in a computer ? What are the basic operations performed over stack?
- 5. (a) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register has the value 200. Evaluate effective address if the addressing mode of the instruction is:
  - (i) direct
  - (ii) immediate
  - (iii) relative
  - (iv) register indirect
  - (v) index with R1 as the index register.
  - (b) What are instruction pipeline conflicts? Explain.
- 6. (a) Draw the flowchart of instruction cycle and explain each step.

io

on?

nization.

ry concept.

s of Interrupts.

ruction? Explain with

s functional units of a

interface is required ?

I 6 each

our of the following:

A CONTRACT

between Static RAM and

nces between Hardwired ammed C. U. ?

nunication protocol 'RS

a memory word and a

characteristics of

K-57

P. T. O.

- (b) Differentiate between Memory reference, Register reference and I/O instructions.
- (a) Draw the block diagram of Addition and Subtraction of signed magnitude operands and explain it.
  - (b) Explain Daisy Chaining Priority Interrupt.
- 8. (a) (i) How many 128 × 8 RAM chips are required to provide a memory capacity of 2048 bytes?
  - (ii) How many lines of the address bus must be used to access 2048 bytes of Memory? How many of these lines will be common to all chips?
  - (iii) How many lines must be decoded for chip select? Specify the size of the decoders.
  - (b) Discuss the complete working of DMA by putting all the resources such as CPU, RAM and I/O together.

290

TCS-402/TIT-402

K-57

1. Attempt a words:

(i) Wh

(ii) Ca

(iii) De

K-45

Roll No.

TCS

B. Tech. (
End Seme

DESIGN A

Time: Three Hour Note: (i) This

> Secti (ii) Ansv

brie que

(iii) Ans (Par

(iv) Ans