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TCS–802

B. TECH. (CS) (EIGHTH SEMESTER) END SEMESTER EXAMINATION, 2018

ADVANCED COMPUTER ARCHITECTURE

Time : Three Hours

Maximum Marks : 100

Note : (i) This question paper contains five questions with alternative choice.

(ii) All questions are compulsory.

(iii) Instructions on how to attempt a question are mentioned against it.

(iv) Each part carries **ten** marks. Total marks assigned to each question are **twenty.**

1. Attempt any *two* questions of choice from (a), (b) and (c). (2×10=20 Marks)

   (a) State Amdahl's Law. Suppose we have a technique of Speeding-Up performance of Fraction of a program by a factor of 4. Then what fraction of the program is chosen such that it results overall Speed-Up gained is = 2.

(b) Explain Feng's classification in Computers based on serial *vs.* parallel processing.

(c) Explain Flynn's Taxonomy in Computer Architecture Concepts.

2. Attempt any *two* questions of choice from (a), (b) and (c). (2×10=20 Marks)

(a) Define dependency and hazard. What is data hazard in instruction pipelining concept ? Mention all types of data hazards and explain them with appropriate examples. 2, 2, 6

(b) Considering a 4-stage (S_1, S_2, S_3 and S_4) instruction pipelining and there are 4 instructions (I_1, I_2, I_3 and I_4) to be executed. Values given in the table indicate delay time (in ns) for individual stages :

	S_1	S_2	S_3	S_4
I_1	2	3	2	1
I_2	3	2	3	2
I_3	3	3	4	3
I_4	2	2	1	1

(i) What is the total time needed to execute all the instructions using pipelining ? 4

(ii) Calculate speed-up, efficiency and throughput achieved. 6

(c) Explain Structural Dependency and Control Dependency with examples.

3. Attempt any *two* questions of choice from (a), (b) and (c). (2×10=20 Marks)

(a) Discuss Associative and Set Associative memory mapping techniques. "N-way set associative mapping is basically fully Associative mapping."—Justify the statement (where N = Number of cache lines).

(b) Suppose that a direct-mapped cache has 2^{10} cache lines, with 2^4 bytes of data per cache line. If the cache is used to store blocks for a byte addressable memory of size 2^{30} bytes, then how many bytes of space will be required for storing the tags ?

(c) Consider a direct mapped cache memory with total 4 lines (0 – 3) and main memory with 128 blocks. The following block request is mapped by the CPU (if FIFO policy is used for cache block replacement) :

0, 7, 2, 9, 15, 8, 16, 54

Then which blocks will be present at cache finally after completion of all block requests ?

4. Attempt any *two* questions of choice from (a), (b) and (c). (2×10=20 Marks)

   (a) Explain Von-Neumann architecture in computer architecture.

   (b) Provide a comparative discussion between Reduced Instruction Set Computers (RISC) and Complex Instruction Set Computers (CISC) with respect to their architecture.

   (c) Define Temporal locality and Spatial locality concept. Explain inclusion property of memories. Discuss the basic concepts of Virtual memory.

5. Attempt any *two* questions of choice from (a), (b) and (c). (2×10=20 Marks)

   (a) What is the benefit of ILP (Instruction Level Parallelism) ? Mention various techniques for increasing ILP.

   (b) Discuss the issues in memory consistency in : 5, 5

      (i) Centralized-shared memory architecture

      (ii) Distributed-shared memory architecture

   (c) Write notes on the following : 5, 5

      (i) Array and Vector processors

      (ii) VLIW (Very Large Instruction Word) processor.