H

Roll No. 2399001

TCS–308

B. TECH. (CSE) (THIRD SEMESTER)
MID SEMESTER
EXAMINATION, Dec., 2023
LOGIC DESIGN AND COMPUTER ORGANIZATION

Time : 1½ Hours

Maximum Marks : 50

Note : (i) Answer all the questions by choosing any ***one*** of the sub-questions.

(ii) Each sub-question carries 10 marks.

1. (a) Minimize the following using Karnaugh map : (CO1)

$F = \Sigma m\,(1, 4, 7, 10, 13) + \Sigma d\,(5, 14, 15)$

$F = \pi M\,(0, 2, 4, 7, 8, 10, 12)$

OR

(b) Reduce the expression : (CO1)

(i) $F = \overline{\overline{A}B + \overline{A} + AB}$

(ii) $F=(B+BC)(\overline{B}+BC)(B+C)$

P. T. O.

2. (a) Reduce the following function using tabular method : (CO1)

$$F = \sum m(0, 1, 2, 8, 10, 11, 14, 15)$$

OR

(b) Why multiplexer is called data selector ? Realize the logic function F (A, B, C, D) = $\sum m$ (2,4,6,7,9,10,11, 12,15) using : (CO1)

(i) 16 : 1 MUX

(ii) 8 : 1 MUX

3. (a) Explain SR F-F and discuss problems of Master Slave Flip-Flop. (CO1)

OR

(b) Differentiate encoder and decoder. Design a BCD to Gray code converter. (CO1)

4. (a) What is the general procedure of designing a combinational circuit ? Using the procedure steps design a adder. (CO2)

OR

(b) Convert the following : (CO2)

(i) SR to T

(ii) D to JK

5. (a) Design a mod-6 synchronous counter using JK flip-flop. (CO2)

OR

(b) Differentiate between the following : (CO2)

(i) Combinational and Sequential circuits

(ii) Synchronous and Asynchronous circuits