H Roll No. .....

TMC–102

M. C. A. (FIRST SEMESTER)
END SEMESTER
EXAMINATION, Jan., 2023

COMPUTER ORGANIZATION AND ARCHITECTURE

Time : Three Hours

Maximum Marks : 100

Note : (i) All questions are compulsory.

(ii) Answer any *two* sub-questions among (a), (b) and (c) in each main question.

(iii) Total marks in each main question are **twenty**.

(iv) Each sub-question carries 10 marks.

1. (a) Recall the 4 types of number systems. Define base of each of them. Explain any *three* logic gates with the truth table. Underline the properties of computer memory hierarchy. (CO1)

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Or

(b) List and explain any *five* addressing modes. (CO3)

(c) State the importance of Handshaking in data transfer between sender and receiver. Underline the working of following : (CO3)

(i) Source initiated handshaking

(ii) Destination initiated handshaking

2. (a) Compare combination and sequential circuits. Describe properties of both. Describe race around condition. Describe working of RS Flip-Flop with a neat diagram. (CO1)

Or

(b) Identify the importance of Direct Memory Access (DMA). Discuss the structure of DMA. Implement following Boolean expression using decoder : (CO3)

$F(A, B, C) = AB'C' + A'BC' + A'B'C + ABC$

(c) Identify the importance of full adder. Explain in with diagram and truth table. Implement full adder with the help of 3×8 line decoder. (CO1)

3. (a) Differentiate between multiplexer and de-multiplexer. Explain 8×1 multiplexer and 1×4 de-multiplexer. (CO1)

Or

(b) Demonstrate the working of following types of address mapping in relation to cache memory : (CO4)

(i) Associative mapping

(ii) Direct mapping

(iii) Set associative mapping

(c) Interpret the meaning of error detection and correction codes. Demonstrate the working of parity method of error detection and correction. Assume, a receiver receives 10110111 information from a sender using even parity method. Check whether there is any error in the received message or not. (CO4)

4. (a) Analyse the importance of memory interleaving with a neat diagram. Discuss cache coherence. Analyse the structure hard disk. (CO4)

Or

(b) Differentiate between shared memory architecture and distributed architecture of parallel processor. Analyze various types of pipeline hazards. (CO5)

(c) Analyze the importance of RAID with respect to single disk. Categorize different levels of RAID. Explain advantages of each level. (CO4)

5. (a) Construct following Boolean expressions using logic gates : (CO1)

(i) $A'B'C' + A'B'C + A'BC + A(B + C)$

(ii) $(w + x' + y' + z)(w' + x' + y + z)$

$(w + x + y + z) + wxyz$

Or

(b) Describe the Flynns taxonomy of parallel machine models. An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the number 200. Evaluate the effective address if the addressing mode of the instruction is (a) direct; (b) immediate; (c) relative; (d) register indirect. (CO5)

(c) Solve following : (CO1)

(i) $(1101)_2 = (?)_8$

(ii) $(345.2)_8 = (?)_{16}$

(iii) $(24.4)_{10} = (?)_5$

(iv) $(ABC)_{16} = (?)_2$

(v) $(1001)_{10} = (?)_8$