H Roll No. .....

TCS–301

B. TECH. (THIRD SEMESTER)
END SEMESTER
EXAMINATION, Jan., 2023

LOGIC DESIGN

Time :Three Hours

Maximum Marks : 100

Note : (i) All questions are compulsory.

(ii) Answer any *two* sub-questions among (a), (b) and (c) in each main question.

(iii) Total marks in each main question are **twenty**.

(iv) Each sub-question carries 10 marks.

1. (a) (i) Prove that : (CO1)

$(AB + CD) = ((AB)'.(CD)')'$

(ii) $(A + B).(C + D) = ((A + B)' + (C + D)')'$ with the fact that AND-OR configuration is equivalent to NAND-NAND and OR-AND configuration is equivalent to NOR-NOR configuration. 3+3=6

P. T. O.

(b) Simplify using K-map. (CO1)

$f(A, B, C, D, E, F) = \pi M (4, 5, 6, 7, 8, 12, 13, 16, 17, 18, 19, 21, 22, 25, 28, 32, 35, 37, 38, 39, 40, 53)$. 7

(c) Simplify the following by finding the essential prime implicants : (CO1)

$f(A, B, C, D) = \Sigma (1, 3, 4, 5, 10, 11, 12, 13, 14, 15)$. 7

2. (a) Design a 3-bit majority circuit which gives output '1' when input variables have more number of '1's then '0's. (CO2)

(b) Construct 5 to 32 line decoder using 3 to 8 decoder and 2 to 4 decoder as enable circuits. (CO2)

(c) Realize circuit $f(A, B, C, D) = \Sigma (0, 2, 5, 7, 11, 14)$ using 8 : 1 mux with D as control variable. (CO2)

(d) Design combinational circuits : (CO2)

$F1 (A, B, C) = \Sigma (3, 5, 6)$

$F2 (A, B, C) = \Sigma (1, 4)$

$F3 (A, B, C) = \Sigma (2, 3, 5, 6, 7)$ using decoder and NAND gates. 4×5=20

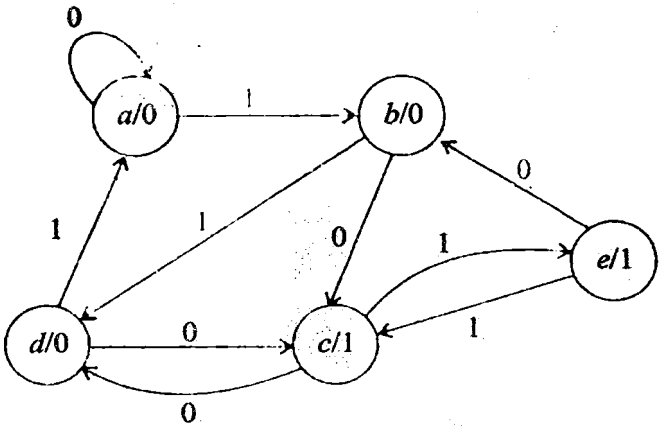
3. (a) Realized JK flip-flop and T Flip-flop from D-flip-flop. Draw the relevant diagram for conversion and deduce the characteristics equation. 8 (CO3)

   (b) A sequential circuit has two JK flip-flops, two inputs x and y and one output Z. Draw the logic diagram (Circuit diagram). Deduce the state table and state diagram. 8 (CO3)

$J_A = Bx + \bar{B}y : K_A = \bar{B}x\bar{y}, J_B = \bar{A}x$

$k_B = A = x\bar{y}, Z = A\bar{x}\,\bar{y} + B\bar{x}\,\bar{y}.$

4. (a) Reduce that state transition diagram by row elimination method and implication table method. Deduce the output of the new states for the input string 0110110101110. 10 (CO3)



(b) How data 01101001 is transferred through SIPO with suitable circuit diagram realized with JK flip-flop. How the circuit gets modified if the data transferred in SISO and PIPO configuration. 10 (CO4)

5. (a) Design synchronous 4-bit Up/Down Counter using JK flip-flop. 6 (CO5)

(b) Design mod 6 counter using T flip-flop. 6 (CO5)

(c) Design asynchronous sequential logic circuit that has 2 inputs A & B, one output 'x'. Output goes high when A = 1 and B makes transition from 1 to 0. X remains high as this A = 1 and B = 0. It becomes '1' when A = 1 and B goes from 1 to 0. Draw the state transition diagram, state reduction table, modified state diagram and circuit diagram. 8 (CO5)