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TCS–802

B. Tech. (CS) (Eighth Semester)
End Semester EXAMINATION, 2017
ADVANCED COMPUTER ARCHITECTURE

Time : Three Hours] [*Maximum Marks : 100*

Note : (i) This question paper contains *five* questions.

(ii) All questions are compulsory.

(iii) Instructions on how to attempt a question are mentioned against it.

(iv) Total marks assigned to each question are **twenty**.

1. Attempt any *two* questions of choice from (a), (b) and (c). (2×10=20 Marks)

   (a) Explain Feng's classification in computer architecture.

   (b) Explain Amdahl's Law and its impact on performance enhancement. What is "Speed $Up_{overall}$" for Amdahl's Law ? Generate the formula.

(c) Explain the following :

(i) Speed Up

(ii) CPU Time

(iii) Throughput

(iv) CPI

(v) IC

2. Attempt any *two* questions of choice from (a), (b) and (c). (2×10=20 Marks)

(a) What is Cache Coherence Problem ? How can this problem be resolved ?

(b) Discuss "Direct Mapping" and "Associative Mapping" techniques. Draw a comparative discussion on both the techniques.

(c) Consider a set associative cache memory with 4 sets (0 – 3) and total 8 cache blocks (0 – 7) and main memory with 128 blocks. The following block request is mapped by the CPU (if LRU policy is used for cache block replacement in set Associative cache organization).

0 5 3 9 7 0 16 55

If we use 2–way set associative, then what will be the cache set and cache block pair in which main memory block 7 is present ?

3. Attempt any *two* questions of choice from (a), (b) and (c). (2×10=20 Marks)

(a) Explain VLIW architecture in detail.

(b) What is "super pipelining" and how is it different from normal pipelining ? Explain with the help of a diagram.

(c) Explain the below mentioned concepts :

(i) Virtual memory organization

(ii) Data flow computers

4. Attempt any *two* questions of choice from (a), (b) and (c). (2×10=20 Marks)

(a) An instruction pipeline is having 4 stages if there exists 20% branch instruction out of which 60% of them are conditional, 30% of which satisfy the condition. If penalty for branch is 3 cycle and penalty associated with a conditional branch instruction whose condition is not satisfied is 1 cycle. If clock time is 10 ns then what is the average access time for an instruction (in ns) ?

(b) Discuss "Data Dependencies" and "Control Dependencies" in instruction pipelining concept.

(c) Answer the following questions :

(i) Explain Instruction pipelining.

(ii) Consider a pipeline with 5 stages. Assume the 1st stage takes 5 units of time, 2nd takes 2 units of time, 3rd takes 3 unit of time, 4th takes 1 unit of time and 5th takes 4 unit of time. Calculate the speed up factor of pipeline.

5. Attempt any *two* questions of choice from (a), (b) and (c). (2×10=20 Marks)

(a) What are the issues in memory consistency in Centralized-Shared memory architecture concept ?

(b) Write short notes on the following :

(i) Hit rate and Miss rate

(ii) Cluster Computers

(iii) Inclusion property of memory

(iv) Superscalar processors

(c) Explain Von-Neumann architecture in computer architecture.