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TCS–404/TIT–404

B. TECH. (CS/IT) (FOURTH SEMESTER) END SEMESTER EXAMINATION, 2018

COMPUTER ORGANIZATION

Time : Three Hours

Maximum Marks : 100

Note : (i) This question paper contains five questions with alternative choice.

(ii) All questions are compulsory.

(iii) Instructions on how to attempt a question are mentioned against it.

(iv) Each part carries **ten** marks. Total marks assigned to each question are **twenty.**

1. Attempt any *two* questions of choice from (a), (b) and (c). (2×10=20 Marks)

(a) Write short notes on the following : 10

(i) Interprocessor Arbitration

(ii) Difference between multiprocessors and multicomputers.

(iii) RAID

(iv) Instruction pipeline

(b) Multiply two numbers –7 and + 8 using Booth's algorithm, using 5 bits. 10

(c) (i) Convert the following pairs of numbers to 5-bit signed 2's complement binary numbers and add them. State whether an overflow occurs in each case : 5

(I) –14 and 11

(II) –10 and –12

(ii) Mention the functions of the processor registers : 5

(I) PC

(II) MAR

(III) MDR

(IV) IR

(V) Control Unit

2. Attempt any *two* questions of choice from (a), (b) and (c). (2×10=20 Marks)

(a) (i) Explain the sequence of events the happen during a fetch operation. 5

(ii) Explain the features of RISC processor. 5

(b) Explain the difference between hardwired and microprogrammed control unit with the help of diagram. 10

(c) (i) Given the following binary number in 32bit (single precision) IEEE-754 format : 5

00111110011011010000000000000000. What is the decimal value of closest to this floating-point number ?

(ii) A float type variable X is represented using the single-precision 32-bit floating point format IEEE-754 standard and assign the decimal value of –14.25. What is the representation of X in hexadecimal notation ? 5

3. Attempt any *two* questions of choice from (a), (b) and (c). (2×10=20 Marks)

(a) Show how the operation C = A + B can be implemented in a single accumulator computer by : 10

(i) Three-address instruction

(ii) Two-address instruction

(iii) One-address instruction

(iv) Zero-address instruction

(b) (i) The following transfer statements specify a memory. Explain a memory operation in each case : 5

(I) M[AR] ← R3

(II) R2 ← M[AR]

(ii) Define the following : 5

(I) Cache coherency

(II) Microinstruction

(III) Micro-operations

(IV) Control memory

(V) RISC

(c) (i) An 8-bit register contains the binary value 10011100. What is the register value after an arithmetic shift right ? Starting from the initial number 10011100, determine the register value after an arithmetic shift left, and state whether there is an overflow. 5

(ii) Starting from an initial value of R = 11011101, determine the sequence of binary values in R after a logical shift-left, followed by a circular shift-right, followed by a logical shift-right and a circular shift-left. 5

4. Attempt any *two* questions of choice from (a), (b) and (c). (2×10=20 Marks)

(a) (i) What is direct memory access (DMA) ? Why are the read and write control lines in a DMA controller bi-directional ? 5

(ii) Why does DMA have priority over the CPU when both request a memory transfer ? 5

(b) (i) What is input-output interface ? Draw and explain block diagram of input-output interface. 5

(ii) Explain different types of instruction formats. 5

(c) Consider a 16-bit processor in which the following appears in main memory, starting at location 200 : 10

Address ↓

200	Load to AC	Mode
201	500	
202	Next to instruction	

The first part of the first word indicates that this instruction loads a value into an accumulator. The mode field specifies an addressing mode or source register R1 which has a value 400. There is a base register that contains the value 100. The value 500 *n* location 201, may be the part of address calculation. Assume that location 399 contains the value 999,

location 400 contains the value 1000 and so on.

(i) What will be the effective address and operand to be loaded by using Register Indirect Mode ?

(ii) What will be the effective address using indirect addressing mode ?

(iii) What will be the effective address using immediate addressing mode ?

5. Attempt any *two* questions of choice from (a), (b) and (c). (2×10=20 Marks)

(a) (i) What do you mean by shared memory multiprocessors ? 5

(ii) What is priority Interrupt ? Explain daisy chaining priority with the help of suitable diagram. 5

(b) Consider a 4-stage pipeline processor. The number of cycles needed by the four instructions I1, I2, I3, I4 in stages S1, S2, S3, S4 is shown below : 10

	S1	S2	S3	S4
I1	2	1	1	1
I2	1	3	2	2
I3	2	1	1	3
I4	1	2	2	2

For (i = 1 to 2) {I1, I2, I3, I4}

What is the number of cycles needed to execute the following loop ?

(c) (i) Explain vector processing. What is the difference between vector and array processing ? 5

(ii) What is asynchronous data transfer ? Explain in detail. 5