

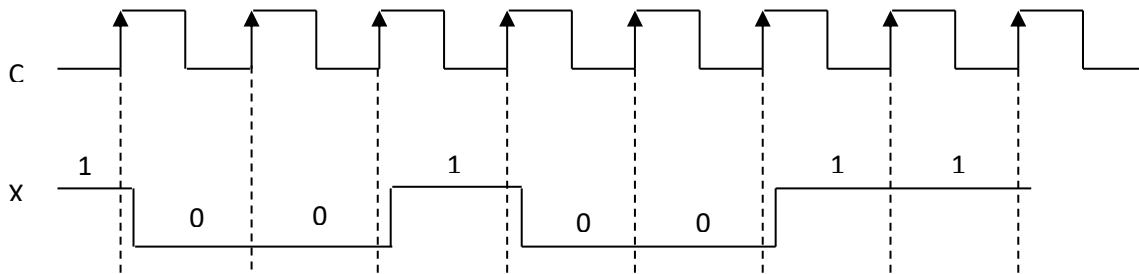
DLP-Mid2-2016

1 Design a 3 bit synchronous UP-DOWN counter. An UP-DOWN counter is one capable of counting both upwards and downwards based on how the user wants it to count. Draw the state diagram. Design for the Flip Flop inputs, get the Boolean expression for the same. Also draw the final circuit.

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a) Design a sequential synchronous circuit that complements every alternate bit in a serial input bit stream, with state diagram.

b). Now given an input waveform, X such as below plot the states of the flip flops and outputs with the clock.



3. Given a clock of frequency f , design a circuit that produces a clock pulse of frequency $f/5$. Also make sure that the ON time and OFF time of the output clock are also equal.

4. Given a 4 bit binary number X ($X = x_3 x_2 x_1 x_0$) devise a circuit that outputs $8X + 2X$. Specify the number of functional blocks you are going to use and why? (You can use 8 bit blocks for instance and as many as you like as long as you can justify.) Specify the sequence of operations you would perform. You may if you want assume manual control of clocks. Draw the final circuit with precise interconnection between blocks and control inputs/signals if any.

5. Consider a ripple counter that counts from 0 – 14. If each of the basic gates have a delay 5ns and if each Flip Flop can be considered as a 4 level implementation with basic gates what should be the minimum time period of the clock to the FF corresponding to the least significant bit. Provide clear and precise arguments.