The RISC-V Debug Specification

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Preface

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Chapter 1. Introduction

When a design progresses from simulation to hardware implementation, a user's control and understanding of the system's current state drops dramatically. To help bring up and debug low level software and hardware, it is critical to have good debugging support built into the hardware. When a robust OS is running on a core, software can handle many debugging tasks. However, in many scenarios, hardware support is essential.

This document outlines a standard architecture for debug support on RISC-V hardware platforms. This architecture allows a variety of implementations and tradeoffs, which is complementary to the wide range of RISC-V implementations. At the same time, this specification defines common interfaces to allow debugging tools and components to target a variety of hardware platforms based on the RISC-V ISA.

System designers may choose to add additional hardware debug support, but this specification defines a standard interface for common functionality.

1.1. Terminology

advanced feature
An advanced feature for advanced users. Most users will not be able to take advantage of it.

AMO Atomic Memory Operation.

BYPASS JTAG instruction that selects a single bit data register, also called BYPASS.

component A RISC-V core, or other part of a hardware platform. Typically all components will be connected to a single system bus.

CSR Control and Status Register.

DM Debug Module (see Chapter Chapter 3).

DMI Debug Module Interface (see Section Section 3.1).

DR JTAG Data Register.

DTM Debug Transport Module (see Section Chapter 15).

DXLEN Debug XLEN, which is the widest XLEN a hart supports, ignoring the current value of in .

essential feature An essential feature must be present in order for debug to work correctly.

GPR General Purpose Register.

hardware platform A single system consisting of one or more *components*.

hart A hardware thread in a RISC-V core.

IDCODE 32-bit Identification CODE, and a JTAG instruction that returns the IDCODE value.

IR JTAG Instruction Register.

JTAG Refers to work done by IEEE's Joint Test Action Group, described in IEEE 1149.1.

legacy feature A legacy feature should only be implemented to support legacy hardware that is present in a system.

Minimal RISC-V Debug Specification A subset of the full Debug Specification that allows for very small implementations. See Chapter Chapter 3.

NAPOT Naturally Aligned Power-Of-Two.

NMI Non-Maskable Interrupt.

physical address address that is directly usable on the system bus.

recommended feature A recommended feature is not required for debug to work correctly, but it is so useful that it should not be omitted without good reason.

SBA System Bus Access (see Section Section 3.10).

specialized feature A specialized feature, that only makes sense in the context of some specific hardware.

TAP Test Access Port, defined in IEEE 1149.1.

TM Trigger Module (see Section [trigger]).

virtual address An address as a hart sees it. If the hart is using address translation this may be different from the physical address. If there is no translation then it will be the same.

xepc The exception program counter CSR (e.g.) that is appropriate for the mode being trapped to.

1.2. Context

This specification attempts to support all RISC-V ISA extensions that have, roughly, been ratified through the first half of 2023. In particular, though, this specification specifically addresses features in the following extensions:

1. A
2. C
3. D
4. F
5. H
6. Sm1p13
7. Ss1p13
8. Smstateen
9. V
10. Zawrs
11. Zcmp
12. Zicbom

13. Zicboz
14. Zicbop

1.2.1. Versions

Version 0.13 of this document was ratified by the RISC-V Foundation's board. Versions 0.13.*x* are bug fix releases to that ratified specification.

Version 0.14 was a working version that was never officially ratified.

Version 1.0 is almost entirely forwards and backwards compatible with Version 0.13.

1.2.1.1. Bugfixes from 0.13 to 1.0

Changes that fix a bug in the spec:

1. Fix order of operations described in [sbdata0]. #392
2. Resume ack is set after resume, in Section 3.5. #400
3. [sselect] applies to [svalue] . #402
4. [mte] only applies when action=0. #411
5. [aamsize] does not affect Argument Width. #420
6. Clarify that harts halt out of reset if [haltreq] =1. #419

1.2.1.2. Incompatible Changes from 0.13 to 1.0

Changes that are not backwards-compatible. Debuggers or hardware implementations that implement 0.13 will have to change something in order to implement 1.0:

1. Make haltsum0 optional if there is only one hart. #505
2. System bus autoincrement only happens if an access actually takes place. ([sbdata0]) #507
3. Bump [version] to 3. #512 , Require debugger to poll [dmactive] after lowering it. #566
4. Add [pending] to [icount] . #574
5. When a selected trigger is disabled, [tdata2] and [tdata3] can be written with any value supported by any of the types this trigger supports. #721
6. [tcontrol] fields only apply to breakpoint traps, not any trap. #723
7. If [version] is greater than 0, then [hit0] (previously called [mcontrol].`hit`) now contains 0 when a trigger fires more than one instruction after the instruction that matched. (This information is now reflected in .) #795
8. If [version] is greater than 0, then bit 20 of [mcontrol16] is no longer used for timing information. (Previously the bit was called [mcontrol].`timing`.) #807
9. If [version] is greater than 0, then the encodings of [size] for sizes greater than 64 bit have changed. #807

1.2.1.3. Minor Changes from 0.13 to 1.0

Changes that slightly modify defined behavior. Technically backwards incompatible, but unlikely to be noticeable:

1. [stopcount] only applies to hart-local counters. #405
2. [version] may be invalid when [dmactive]=0. #414
3. Address triggers ([mcontrol]) may fire on any accessed address. #421
4. All trigger registers ([csrTrigger]) are optional. #431
5. When extending IR, [bypass] still is all ones. #437
6. [ebreaks] and [ebreaku] are WARL. #458
7. NMIs are disabled by [stepie]. #465
8. R/W1C fields should be cleared by writing every bit high. #472
9. Specify trigger priorities in [priority] relative to exceptions. #478
10. Time may pass before [dmactive] becomes high. #500
11. Clear MPRV when resuming into lower privilege mode. #503
12. Halt state may not be preserved across reset. #504
13. Hardware should clear trigger action when [dmode] is cleared and action is 1. #501
14. Change quick access exceptions to halt the target in [acQuickaccess]. #585
15. Writing 0 to [tdata1] forces a state where [tdata2] and [tdata3] are writable. #598
16. Solutions to deal with reentrancy in [nativetrigger] prevent triggers from *matching*, not merely *firing*. This primarily affects behavior. #722
17. Attempts to access an unimplemented CSR raise an illegal instruction exception. #791

1.2.1.4. New Features from 0.13 to 1.0

New backwards-compatible feature that did not exist before:

1. Add halt groups and external triggers in Section 3.6. #404
2. Reserve some DMI space for non-standard use. See [custom], and [custom0] through . #406
3. Reserve trigger [type] values for non-standard use. #417
4. Add [nmi] bit to [itrigger]. #408 and #709
5. Recommend matching on every accessed address. #449
6. Add resume groups in Section 3.6. #506
7. Add [relaxedpriv] . #536
8. Move [scontext], renaming original to [mscontext], and create [hcontext]. #535
9. Add [mcontrol6], deprecating [mcontrol]. #538
10. Add hypervisor support: [ebreakvs], [ebreakvu], [v], [hcontext], [mcontrol], [mcontrol6], and [priv]. #549
11. Optionally make [anyunavail] and [allunavail] sticky, controlled by [stickyunavail]. #520
12. Add [tmexttrigger] to support trigger module external trigger inputs. #543
13. Describe [mcontrol] and [mcontrol6] behavior with atomic instructions. #561
14. Trigger hit bits must be set on fire, may be set on match. #593
15. Add [sbytemask] and [sbytemask] to [textra32] and [textra64]. #588

16. Allow debugger to request harts stay alive with keepalive bit in [keepalive]. #592
17. Add [ndmresetpending] to allow a debugger to determine when ndmreset is complete. #594
18. Add [intctl] to support triggers from an interrupt controller. #599

1.2.1.5. Incompatible Changes During 1.0 Stable

Backwards-incompatible changes between two versions that are both called 1.0 stable.

1. [nmi] was moved from [etrigger] to [itrigger], and is now subject to the mode bits in that trigger.
2. #728 introduced Message Registers, which were later removed in #878.
3. It may not be possible to read the contents of the Program Buffer using the `progbuf` registers. #731
4. [tcontrol] fields apply to all traps, not just breakpoint traps. This reverts #723. #880

1.3. About This Document

1.3.1. Structure

This document contains two parts. The main part of the document is the specification, which is given in the numbered chapters. The second part of the document is a set of appendices. The information in the appendices is intended to clarify and provide examples, but is not part of the actual specification.

1.3.2. ISA vs. non-ISA

This specification contains both ISA and non-ISA parts. The ISA parts define self-contained ISA extensions. The other parts of the document describe the non-ISA external debug extension. Chapters whose contents are solely one or the other are labeled as such in their title. Chapters without such a label apply to both ISA and non-ISA.

1.3.3. Register Definition Format

All register definitions in this document follow the format shown below. A simple graphic shows which fields are in the register. The upper and lower bit indices are shown to the top left and top right of each field. The total number of bits in the field are shown below it.

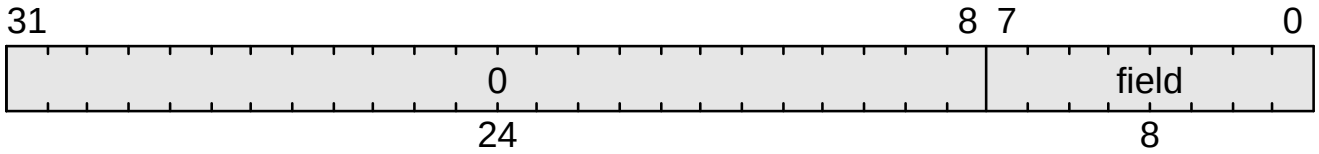
After the graphic follows a table which for each field lists its name, description, allowed accesses, and reset value. The allowed accesses are listed in [access]. The reset value is either a constant or "Preset." The latter means it is an implementation-specific legal value.

Parts of the register which are currently unused are labeled with the number 0. Software must only write 0 to those fields, and ignore their value while reading. Hardware must return 0 when those fields are read, and ignore the value written to them.

This behavior enables us to use those fields later without having to increase the values in the version fields.

Names of registers and their fields are hyperlinks to their definition, and are also listed in the index on page [singlestep].

1.3.3.1. Long Name (shortname, `at 0x123`)



Field	Description	Access	Reset
field	Description of what this field is used for.	R/W	15

R	Read-only.
R/W	Read/Write.
R/W1C	Read/Write ones to Clear. Writing 0 to every bit as no effect. Writing 1 to every bit clears the field. The result of other writes is undefined.
WARZ	Write any, read zero. A debugger may write any value. When read this field returns 0.
W1	Write-only. Only writing 1 has an effect. When read the returned value should be 0.
WARL	Write any, read legal. A debugger may write any value. If a value is unsupported, the implementation converts the value to one that is supported.

Table 1. Register Access Abbreviations

1.4. Background

There are several use cases for dedicated debugging hardware, both in native debug and external debug. Native debug (sometimes called self-hosted debug) refers to debug software running on a RISC-V platform which debugs the same platform. The optional Trigger Module provides features that are useful for native debug. External debug refers to debug software running somewhere else, debugging the RISC-V platform via a debug transport like JTAG. The entire document provides features that are useful for external debug.

This specification addresses the use cases listed below. Implementations can choose not to implement every feature, which means some use cases might not be supported.

- Accessing hardware on a hardware platform without a working CPU. (External debug.)
- Bootstrapping a hardware platform to test, configure, and program components before there is any executable code path in the hardware platform. (External debug.)
- Debugging low-level software in the absence of an OS or other software. (External debug.)
- Debugging issues in the OS itself. (External or native debug.)
- Debugging processes running on an OS. (Native or external debug.)

1.5. Supported Features

The debug interface described in this specification supports the following features:

1. All hart registers (including CSRs) can be read/written.
2. Memory can be accessed either from the hart's point of view, through the system bus directly, or both.

3. RV32, RV64, and future RV128 are all supported.
4. Any hart in the hardware platform can be independently debugged.
5. A debugger can discover almost [1] everything it needs to know itself, without user configuration.
6. Each hart can be debugged from the very first instruction executed.
7. A RISC-V hart can be halted when a software breakpoint instruction is executed.
8. Hardware single-step can execute one instruction at a time.
9. Debug functionality is independent of the debug transport used.
10. The debugger does not need to know anything about the microarchitecture of the harts it is debugging.
11. Arbitrary subsets of harts can be halted and resumed simultaneously. (Optional)
12. Arbitrary instructions can be executed on a halted hart. That means no new debug functionality is needed when a core has additional or custom instructions or state, as long as there exist programs that can move that state into GPRs. (Optional)
13. Registers can be accessed without halting. (Optional)
14. A running hart can be directed to execute a short sequence of instructions, with little overhead. (Optional)
15. A system bus manager allows memory access without involving any hart. (Optional)
16. A RISC-V hart can be halted when a trigger matches the PC, read/write address/data, or an instruction opcode. (Optional)
17. Harts can be grouped, and harts in the same group will all halt when any of them halts. These groups can also react to or notify external triggers. (Optional)

This document does not suggest a strategy or implementation for hardware test, debugging or error detection techniques. Scan, built-in self test (BIST), etc. are out of scope of this specification, but this specification does not intend to limit their use in RISC-V systems.

It is possible to debug code that uses software threads, but there is no special debug support for it.

[1] Notable exceptions include information about the memory map and peripherals.

Chapter 2. System Overview

Chapter 2 shows the main components of Debug Support. Blocks shown in dotted lines are optional.

RISC-V Debug System Overview


linejoin="miter" fill="none" stroke="#000000" d="M5174.9 858.297H7299.5V3391.4268H5174.9Z"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M5023.14 1000.05H7147.7307V3543.1602H5023.14Z" fill="#ffffff" fill-rule="evenodd"/> <path transform="matrix(.1,0,0,-.1,0,796)" stroke-width="2.8346" stroke-linecap="butt" stroke-miterlimit="10" stroke-linejoin="miter" fill="none" stroke="#ffffff" d="M5023.14 1000.05H7147.7307V3543.1602H5023.14Z"/> <path transform="matrix(.1,0,0,-.1,0,796)" stroke-width="30.3515" stroke-linecap="butt" stroke-dasharray="60.7027" stroke-miterlimit="10" stroke-linejoin="miter" fill="none" stroke="#000000" d="M5023.14 1000.05H7147.7307V3543.1602H5023.14Z"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M4871.4 1141.82H6995.99V3694.9H4871.4Z" fill="#ffffff" fill-rule="evenodd"/> <path transform="matrix(.1,0,0,-.1,0,796)" stroke-width="2.8346" stroke-linecap="butt" stroke-miterlimit="10" stroke-linejoin="miter" fill="none" stroke="#ffffff" d="M4871.4 1141.82H6995.99V3694.9H4871.4Z"/> <path transform="matrix(.1,0,0,-.1,0,796)" stroke-width="30.3515" stroke-linecap="butt" stroke-miterlimit="10" stroke-linejoin="miter" fill="none" stroke="#000000" d="M4871.4 1141.82H6995.99V3694.9H4871.4Z"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M4949.86 4051.04C4953.65 4049.79 4957.34 4047.12 4960.94 4043.01 4964.55 4038.9 4968.17 4033.27 4971.79 4026.11L4988.73 3991.2H4970.73L4953.9 4023.94C4949.67 4032.5 4945.57 4038.17 4941.61 4040.96 4937.66 4043.77 4932.25 4045.17 4925.41 4045.17H4906.6V3991.2H4887.82V4120.27H4928.3C4943.09 4120.27 4954.12 4117.15 4961.38 4110.91 4968.66 4104.68 4972.3 4095.29 4972.3 4082.72 4972.3 4074.53 4970.39 4067.72 4966.55 4062.3 4962.73 4056.89 4957.17 4053.14 4949.86 4051.04M4906.6 4106.19V4059.25H4928.3C4936.64 4059.25 4942.92 4061.25 4947.15 4065.23 4951.41 4069.21 4953.53 4075.07 4953.53 4082.79 4953.53 4090.54 4951.41 4096.37 4947.15 4100.28 4942.92 4104.22 4936.64 4106.19 4928.3 4106.19H4906.6"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M5013.85 4120.27H5032.62V3991.2H5013.85V4120.27"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M5147.44 4115.57V4099.14C5140.79 4102.3 5134.52 4104.64 5128.63 4106.19 5122.74 4107.75 5117.04 4108.53 5111.54 4108.53 5102.01 4108.53 5094.65 4106.72 5089.47 4103.11 5084.31 4099.49 5081.73 4094.34 5081.73 4087.67 5081.73 4082.07 5083.41 4077.84 5086.76 4074.98 5090.13 4072.15 5096.51 4069.85 5105.89 4068.09L5116.23 4065.96C5129.31 4063.47 5138.96 4059.06 5145.16 4052.73 5151.38 4046.42 5154.48 4037.96 5154.48 4027.35 5154.48 4014.71 5150.23 4005.13 5141.72 3998.61 5133.24 3992.11 5120.8 3988.85 5104.39 3988.85 5098.21 3988.85 5091.62 3989.64 5084.63 3991.2 5077.66 3992.79 5070.44 3995.14 5062.96 3998.24V4017.01C5070.12 4012.34 5077.13 4008.82 5083.97 4006.45 5090.84 4004.11 5097.59 4002.93 5104.21 4002.93 5114.28 4002.93 5122.04 4004.95 5127.49 4008.98 5132.97 4013.02 5135.71 4018.76 5135.71 4026.21 5135.71 4032.72 5133.8 4037.8 5129.98 4041.47 5126.17 4045.16 5119.91 4047.92 5111.21 4049.76L5100.8 4051.77C5087.48 4054.32 5077.84 4058.3 5071.87 4063.73 5065.93 4069.18 5062.96 4076.74 5062.96 4086.42 5062.96 4097.64 5067.04 4106.48 5075.21 4112.93 5083.39 4119.39 5094.66 4122.61 5109.01 4122.61 5115.17 4122.61 5121.44 4122.03 5127.82 4120.85 5134.23 4119.68 5140.77 4117.92 5147.44 4115.57"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M5281.61 4110.88V4092.11C5275.65 4097.61 5269.29 4101.71 5262.55 4104.43 5255.8 4107.16 5248.64 4108.53 5241.06 4108.53 5226.1 4108.53 5214.65 4104 5206.71 4094.93 5198.76 4085.88 5194.79 4072.81 5194.79 4055.7 5194.79 4038.63 5198.76 4025.57 5206.71 4016.5 5214.65 4007.46 5226.1 4002.93 5241.06 4002.93 5248.64 4002.93 5255.8 4004.29 5262.55 4007 5269.29 4009.74 5275.65 4013.86 5281.61 4019.36V4000.59C5275.41 3996.68 5268.84 3993.74 5261.93 3991.79 5255.01 3989.83 5247.69 3988.85 5239.96 3988.85 5220.14 3988.85 5204.52 3994.82 5193.1 4006.75 5181.71 4018.7 5176.02 4035.02 5176.02 4055.7 5176.02 4076.43 5181.71 4092.75 5193.1 4104.68 5204.52 4116.64 5220.14 4122.61 5239.96 4122.61 5247.79 4122.61 5255.15 4121.63 5262.07 4119.68 5269.02 4117.72 5275.53 4114.79 5281.61 4110.88"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M5302.75 4047.52H5349.68V4033.44H5302.75V4047.52"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M5400.09 3991.2 5350.22 4120.27H5368.66L5410.06 4011.59 5451.53 4120.27H5469.9L5420.11 3991.2H5400.09"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M5644.1 4110.88V4092.11C5638.14 4097.61 5631.78 4101.71 5625.04 4104.43 5618.29 4107.16 5611.13 4108.53 5603.55 4108.53 5588.59

4108.53 5577.14 4104 5569.19 4094.93 5561.25 4085.88 5557.28 4072.81 5557.28 4055.7 5557.28 4038.63 5561.25 4025.57 5569.19 4016.5 5577.14 4007.46 5588.59 4002.93 5603.55 4002.93 5611.13 4002.93 5618.29 4004.29 5625.04 4007 5631.78 4009.74 5638.14 4013.86 5644.1 4019.36V4000.59C5637.89 3996.68 5631.33 3993.74 5624.41 3991.79 5617.5 3989.83 5610.18 3988.85 5602.45 3988.85 5582.63 3988.85 5567 3994.82 5555.59 4006.75 5544.2 4018.7 5538.5 4035.02 5538.5 4055.7 5538.5 4076.43 5544.2 4092.75 5555.59 4104.68 5567 4116.64 5582.63 4122.61 5602.45 4122.61 5610.27 4122.61 5617.64 4121.63 5624.56 4119.68 5631.5 4117.72 5638.02 4114.79 5644.1 4110.88"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M5709.86 4078.03C5701.15 4078.03 5694.27 4074.68 5689.21 4067.98 5684.18 4061.28 5681.66 4052.11 5681.66 4040.48 5681.66 4028.84 5684.16 4019.68 5689.18 4012.98 5694.21 4006.28 5701.11 4002.93 5709.86 4002.93 5718.51 4002.93 5725.35 4006.29 5730.39 4013.02 5735.45 4019.74 5737.98 4028.89 5737.98 4040.48 5737.98 4052.02 5735.45 4061.16 5730.39 4067.91 5725.35 4074.65 5718.51 4078.03 5709.86 4078.03M5709.82 4092.11C5723.7 4092.11 5734.61 4087.54 5742.52 4078.39 5750.45 4069.27 5754.41 4056.64 5754.41 4040.48 5754.41 4024.37 5750.45 4011.73 5742.52 4002.57 5734.61 3993.43 5723.7 3988.85 5709.82 3988.85 5695.89 3988.85 5684.97 3993.43 5677.07 4002.57 5669.18 4011.73 5665.23 4024.37 5665.23 4040.48 5665.23 4056.64 5669.18 4069.27 5677.07 4078.39 5684.97 4087.54 5695.89 4092.11 5709.82 4092.11"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M5839.75 4075.68C5837.98 4076.48 5836.08 4077.07 5834.02 4077.44 5831.97 4077.83 5829.7 4078.03 5827.21 4078.03 5818.41 4078.03 5811.65 4075.08 5806.93 4069.19 5802.21 4063.32 5799.85 4054.89 5799.85 4043.89V3991.2H5783.43V4089.76H5799.85V4075.68C5803.13 4081.23 5807.39 4085.35 5812.65 4088.04 5817.9 4090.75 5824.29 4092.11 5831.79 4092.11 5832.86 4092.11 5834.05 4092.11 5835.34 4092.11 5836.64 4092.11 5838.08 4092.11 5839.67 4092.11L5839.75 4075.68"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M5937.99 4045.46V4038.13H5862.9C5863.61 4026.67 5866.96 4017.93 5872.95 4011.92 5878.94 4005.93 5887.27 4002.93 5897.95 4002.93 5904.16 4002.93 5910.18 4003.71 5915.99 4005.28 5921.81 4006.84 5927.58 4009.19 5933.3 4012.32V3998.24C5927.53 3995.18 5921.62 3992.85 5915.55 3991.24 5909.52 3989.65 5903.39 3988.85 5897.18 3988.85 5881.59 3988.85 5869.23 3993.41 5860.11 4002.53 5851.02 4011.67 5846.47 4024.03 5846.47 4039.6 5846.47 4055.71 5850.84 4068.48 5859.56 4077.91 5868.29 4087.38 5880.06 4092.11 5894.88 4092.11 5908.17 4092.11 5918.68 4087.93 5926.41 4079.57 5934.13 4071.21 5937.99 4059.84 5937.99 4045.46M5921.57 4049.87C5921.45 4058.42 5918.94 4065.25 5914.05 4070.36 5909.19 4075.47 5902.75 4078.03 5894.73 4078.03 5885.63 4078.03 5878.35 4075.56 5872.88 4070.62 5867.42 4065.68 5864.28 4058.73 5863.45 4049.76L5921.57 4049.87"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M318.688 2170.12H2746.798V5508.77H318.688Z" fill="#ffffff" fill-rule="evenodd"/> <path transform="matrix(.1,0,0,-.1,0,796)" stroke-width="2.8346" stroke-linecap="butt" stroke-miterlimit="10" stroke-linejoin="miter" fill="none" stroke="#ffffff" d="M318.688 2170.12H2746.798V5508.77H318.688Z"/> <path transform="matrix(.1,0,0,-.1,0,796)" stroke-width="30.3515" stroke-linecap="butt" stroke-miterlimit="10" stroke-linejoin="miter" fill="none" stroke="#000000" d="M318.688 2170.12H2746.798V5508.77H318.688Z"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M657.402 5320.24V5219.34H678.523C696.367 5219.34 709.43 5223.39 717.719 5231.51 726.004 5239.63 730.148 5252.43 730.148 5269.94 730.148 5287.32 726.004 5300.04 717.719 5308.11 709.43 5316.2 696.367 5320.24 678.523 5320.24H657.402M638.629 5334.32H675.844C701.023 5334.32 719.492 5329.12 731.246 5318.7 743.031 5308.31 748.922 5292.06 748.922 5269.94 748.922 5247.67 743.004 5231.31 731.176 5220.88 719.344 5210.46 700.902 5205.26 675.844 5205.26H638.629V5334.32"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M862.578 5259.52V5252.19H787.488C788.195 5240.73 791.547 5231.99 797.535 5225.97 803.523 5219.98 811.859 5216.99 822.539 5216.99 828.75 5216.99 834.762 5217.77 840.582 5219.34 846.398 5220.9 852.168 5223.25 857.887 5226.38V5212.3C852.117 5209.24 846.203 5206.91 840.141 5205.29 834.102 5203.7 827.98 5202.91 821.77 5202.91 806.176 5202.91 793.82 5207.47 784.699 5216.59 775.609 5225.73 771.063 5238.09 771.063 5253.66 771.063 5269.77 775.426 5282.54 784.152 5291.97 792.879 5301.43 804.648 5306.16 819.461 5306.16 832.758

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1771.53 5895.82 1771.53 5904.38 1771.53 5911.01 1774.71 5915.73 1781.06 5920.47 1787.42 5922.84 1796.35 5922.84 1807.87M5939.27 1770.17C5939.27 1753.21 5935.59 1740.6 5928.23 1732.33 5920.9 1724.05 5909.67 1719.9 5894.54 1719.9 5888.91 1719.9 5883.62 1720.3 5878.66 1721.08 5873.7 1721.84 5868.87 1723.01 5864.18 1724.6V1741.02C5868.82 1738.63 5873.41 1736.86 5877.93 1735.71 5882.47 1734.56 5887.09 1733.98 5891.79 1733.98 5902.18 1733.98 5909.95 1736.73 5915.11 1742.23 5920.27 1747.73 5922.84 1756.03 5922.84 1767.13V1773.88C5919.57 1768.38 5915.38 1764.26 5910.27 1761.52 5905.16 1758.81 5899.04 1757.45 5891.9 1757.45 5880.07 1757.45 5870.53 1762.05 5863.3 1771.24 5856.06 1780.45 5852.45 1792.66 5852.45 1807.87 5852.45 1823.12 5856.06 1835.34 5863.3 1844.53 5870.53 1853.75 5880.07 1858.36 5891.9 1858.36 5899.04 1858.36 5905.16 1856.99 5910.27 1854.25 5915.38 1851.54 5919.57 1847.43 5922.84 1841.93V1856.01H5939.27V1770.17"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M6038.25 1807.87C6038.25 1819.43 6035.88 1828.39 6031.13 1834.74 6026.41 1841.1 6019.78 1844.28 6011.22 1844.28 6002.71 1844.28 5996.09 1841.1 5991.35 1834.74 5986.63 1828.39 5984.27 1819.43 5984.27 1807.87 5984.27 1796.35 5986.63 1787.42 5991.35 1781.06 5996.09 1774.71 6002.71 1771.53 6011.22 1771.53 6019.78 1771.53 6026.41 1774.71 6031.13 1781.06 6035.88 1787.42 6038.25 1796.35 6038.25 1807.87M6054.67 1770.17C6054.67 1753.21 6050.99 1740.6 6043.64 1732.33 6036.3 1724.05 6025.07 1719.9 6009.94 1719.9 6004.32 1719.9 5999.02 1720.3 5994.06 1721.08 5989.1 1721.84 5984.27 1723.01 5979.58 1724.6V1741.02C5984.22 1738.63 5988.81 1736.86 5993.33 1735.71 5997.88 1734.56 6002.5 1733.98 6007.19 1733.98 6017.58 1733.98 6025.35 1736.73 6030.51 1742.23 6035.67 1747.73 6038.25 1756.03 6038.25 1767.13V1773.88C6034.97 1768.38 6030.78 1764.26 6025.67 1761.52 6020.56 1758.81 6014.44 1757.45 6007.3 1757.45 5995.47 1757.45 5985.93 1762.05 5978.7 1771.24 5971.46 1780.45 5967.85 1792.66 5967.85 1807.87 5967.85 1823.12 5971.46 1835.34 5978.7 1844.53 5985.93 1853.75 5995.47 1858.36 6007.3 1858.36 6014.44 1858.36 6020.56 1856.99 6025.67 1854.25 6030.78 1851.54 6034.97 1847.43 6038.25 1841.93V1856.01H6054.67V1770.17"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M6174.77 1811.71V1804.38H6099.68C6100.38 1792.92 6103.73 1784.18 6109.72 1778.17 6115.71 1772.18 6124.05 1769.18 6134.73 1769.18 6140.94 1769.18 6146.95 1769.96 6152.77 1771.53 6158.59 1773.09 6164.36 1775.44 6170.07 1778.57V1764.49C6164.3 1761.43 6158.39 1759.1 6152.33 1757.49 6146.29 1755.9 6140.17 1755.11 6133.96 1755.11 6118.36 1755.11 6106 1759.66 6096.89 1768.78 6087.79 1777.92 6083.25 1790.28 6083.25 1805.85 6083.25 1821.96 6087.61 1834.73 6096.34 1844.17 6105.07 1853.63 6116.84 1858.36 6131.65 1858.36 6144.95 1858.36 6155.46 1854.18 6163.18 1845.82 6170.91 1837.46 6174.77 1826.09 6174.77 1811.71M6158.34 1816.12C6158.22 1824.67 6155.71 1831.5 6150.82 1836.61 6145.96 1841.72 6139.52 1844.28 6131.5 1844.28 6122.41 1844.28 6115.13 1841.81 6109.65 1836.87 6104.2 1831.93 6101.05 1824.98 6100.23 1816.01L6158.34 1816.12"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M6258.47 1841.93C6256.71 1842.73 6254.8 1843.32 6252.75 1843.69 6250.7 1844.08 6248.42 1844.28 6245.93 1844.28 6237.13 1844.28 6230.37 1841.33 6225.65 1835.44 6220.93 1829.57 6218.57 1821.14 6218.57 1810.14V1757.45H6202.15V1856.01H6218.57V1841.93C6221.85 1847.48 6226.12 1851.6 6231.37 1854.29 6236.63 1857 6243.01 1858.36 6250.51 1858.36 6251.59 1858.36 6252.77 1858.36 6254.07 1858.36 6255.36 1858.36 6256.8 1858.36 6258.39 1858.36L6258.47 1841.93"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M5633.98 1659.75H5661.62L5693.78 1572.77 5726.12 1659.75H5753.66V1530.68H5734.88V1644.16L5702.39 1556.5H5685.23L5652.75 1644.16V1530.68H5633.98V1659.75"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M5828.02 1617.51C5819.32 1617.51 5812.44 1614.16 5807.38 1607.46 5802.34 1600.76 5799.83 1591.6 5799.83 1579.96 5799.83 1568.32 5802.33 1559.16 5807.34 1552.46 5812.38 1545.77 5819.27 1542.41 5828.02 1542.41 5836.68 1542.41 5843.52 1545.78 5848.56 1552.5 5853.62 1559.22 5856.15 1568.38 5856.15 1579.96 5856.15 1591.5 5853.62 1600.64 5848.56 1607.39 5843.52 1614.13 5836.68 1617.51 5828.02 1617.51M5827.99 1631.59C5841.87 1631.59 5852.77 1627.02 5860.7 1617.88 5868.61 1608.76 5872.57 1596.12 5872.57 1579.96 5872.57 1563.85 5868.61 1551.21 5860.7 1542.05 5852.77 1532.91 5841.87 1528.34 5827.99 1528.34 5814.05 1528.34 5803.14 1532.91 5795.25 1542.05 5787.35 1551.21 5783.4 1563.85 5783.4 1579.96 5783.4 1596.12 5787.35 1608.76 5795.25 1617.88 5803.14 1627.02 5814.05 1631.59 5827.99 1631.59"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M5964.95 1615.16V1666.79H5981.38V1530.68H5964.95V1544.76C5961.63 1539.21 5957.43 1535.08 5952.34


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5824.02 695.93 5824.02 703.09 5825.38 709.836 5828.09 716.582 5830.82 722.938 5834.94 728.902 5840.44V5821.67C722.695 5817.76 716.133 5814.82 709.215 5812.87 702.297 5810.91 694.977 5809.94 687.25 5809.94 667.426 5809.94 651.805 5815.9 640.391 5827.83 629 5839.78 623.305 5856.1 623.305 5876.78 623.305 5897.51 629 5913.84 640.391 5925.77 651.805 5937.72 667.426 5943.7 687.25 5943.7 695.074 5943.7 702.441 5942.72 709.359 5940.76 716.301 5938.8 722.816 5935.88 728.902 5931.96"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M750.035 5868.6H796.969V5854.52H750.035V5868.6"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M847.375 5812.29 797.508 5941.35H815.953L857.348 5832.67 898.816 5941.35H917.188L867.395 5812.29H847.375"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1011.61 5927.27V5877.99H1033.31C1041.36 5877.99 1047.56 5880.13 1051.94 5884.41 1056.34 5888.68 1058.54 5894.77 1058.54 5902.66 1058.54 5910.51 1056.34 5916.57 1051.94 5920.85 1047.56 5925.13 1041.36 5927.27 1033.31 5927.27H1011.61M992.832 5941.35H1033.31C1047.81 5941.35 1058.76 5938.06 1066.16 5931.48 1073.6 5924.93 1077.31 5915.33 1077.31 5902.66 1077.31 5889.91 1073.6 5880.25 1066.16 5873.7 1058.76 5867.17 1047.81 5863.91 1033.31 5863.91H1011.61V5812.29H992.832V5941.35"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1101.86 5948.39H1118.29V5812.29H1101.86V5948.39"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1195.17 5861.56C1182.51 5861.56 1173.73 5860.11 1168.85 5857.2 1163.96 5854.29 1161.52 5849.32 1161.52 5842.28 1161.52 5836.68 1163.35 5832.23 1167.02 5828.93 1170.68 5825.66 1175.67 5824.02 1181.97 5824.02 1190.68 5824.02 1197.66 5827.1 1202.91 5833.26 1208.16 5839.44 1210.79 5847.65 1210.79 5857.89V5861.56H1195.17M1227.22 5867.76V5812.29H1210.79V5826.36C1207.18 5820.74 1202.66 5816.6 1197.27 5813.93 1191.86 5811.27 1185.25 5809.94 1177.43 5809.94 1167.53 5809.94 1159.66 5812.7 1153.81 5818.22 1148 5823.77 1145.09 5831.19 1145.09 5840.48 1145.09 5851.33 1148.74 5859.51 1156.05 5865.01 1163.36 5870.54 1174.27 5873.3 1188.79 5873.3H1210.79V5875.05C1210.79 5882.71 1208.39 5888.62 1203.57 5892.8 1198.78 5897.01 1192.04 5899.11 1183.37 5899.11 1177.84 5899.11 1172.46 5898.52 1167.23 5897.35 1162 5896.18 1156.97 5894.41 1152.13 5892.07V5906.15C1157.97 5908.5 1163.64 5910.25 1169.14 5911.43 1174.66 5912.6 1180.03 5913.19 1185.24 5913.19 1199.32 5913.19 1209.83 5909.43 1216.77 5901.89 1223.74 5894.39 1227.22 5883.01 1227.22 5867.76"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1279.71 5939V5910.84H1312.56V5899.11H1279.71V5845.36C1279.71 5837.29 1280.78 5832.11 1282.93 5829.81 1285.11 5827.51 1289.52 5826.36 1296.17 5826.36H1312.56V5812.29H1296.17C1283.73 5812.29 1275.14 5814.66 1270.39 5819.4 1265.65 5824.16 1263.28 5832.82 1263.28 5845.36V5899.11H1251.55V5910.84H1263.28V5939H1279.71"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1383.36 5948.39V5934.31H1367.85C1362.23 5934.31 1358.32 5933.2 1356.12 5930.97 1353.94 5928.77 1352.85 5924.8 1352.85 5919.05V5910.84H1378.66V5899.11H1352.85V5812.29H1336.43V5899.11H1320V5910.84H1336.43V5917.3C1336.43 5928.13 1338.95 5936.01 1343.98 5940.95 1349.04 5945.91 1357.06 5948.39 1368.03 5948.39H1383.36"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1435.38 5899.11C1426.68 5899.11 1419.8 5895.76 1414.74 5889.06 1409.7 5882.36 1407.18 5873.2 1407.18 5861.56 1407.18 5849.93 1409.69 5840.76 1414.7 5834.06 1419.74 5827.37 1426.63 5824.02 1435.38 5824.02 1444.04 5824.02 1450.88 5827.38 1455.91 5834.1 1460.97 5840.82 1463.5 5849.98 1463.5 5861.56 1463.5 5873.1 1460.97 5882.24 1455.91 5888.99 1450.88 5895.73 1444.04 5899.11 1435.38 5899.11M1435.34 5913.19C1449.23 5913.19 1460.13 5908.62 1468.05 5899.48 1475.97 5890.36 1479.93 5877.72 1479.93 5861.56 1479.93 5845.45 1475.97 5832.82 1468.05 5823.65 1460.13 5814.51 1449.23 5809.94 1435.34 5809.94 1421.41 5809.94 1410.5 5814.51 1402.6 5823.65 1394.71 5832.82 1390.76 5845.45 1390.76 5861.56 1390.76 5877.72 1394.71 5890.36 1402.6 5899.48 1410.5 5908.62 1421.41 5913.19 1435.34 5913.19"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1565.27 5896.76C1563.51 5897.57 1561.61 5898.16 1559.55 5898.52 1557.5 5898.91 1555.22 5899.11 1552.73 5899.11 1543.93 5899.11 1537.17 5896.16 1532.45 5890.27 1527.73 5884.41 1525.38 5875.97 1525.38 5864.97V5812.29H1508.95V5910.84H1525.38V5896.76C1528.65 5902.31 1532.92 5906.43 1538.17 5909.12 1543.43 5911.83 1549.81 5913.19 1557.31 5913.19 1558.39 5913.19 1559.57 5913.19 1560.87 5913.19 1562.16 5913.19 1563.61 5913.19 1565.2 5913.19L1565.27 5896.76"/> <path


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1003.91 1233.63 1006.62 1240.01 1007.98 1247.51 1007.98 1248.59 1007.98 1249.77 1007.98 1251.07 1007.98 1252.37 1007.98 1253.81 1007.98 1255.4 1007.98L1255.47 991.551"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1370.73 1043.18C1362.78 1029.75 1356.88 1016.48 1353.02 1003.36 1349.18 990.254 1347.26 976.957 1347.26 963.465 1347.26 949.996 1349.2 936.648 1353.09 923.422 1356.98 910.223 1362.86 896.949 1370.73 883.605H1356.5C1347.92 897.316 1341.49 910.785 1337.21 924.012 1332.96 937.258 1330.84 950.41 1330.84 963.465 1330.84 976.469 1332.95 989.559 1337.18 1002.73 1341.41 1015.93 1347.85 1029.41 1356.5 1043.18H1370.73"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1450.91 1020.85 1408.3 951.656H1450.91V1020.85M1447.87 1036.14H1469.69V951.656H1488.46V937.578H1469.69V907.07H1450.91V937.578H1394.59V954.406L1447.87 1036.14"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1535.81 970.43V921.148H1562.79C1571.96 921.148 1578.75 923.18 1583.14 927.238 1587.57 931.293 1589.78 937.492 1589.78 945.828 1589.78 954.234 1587.57 960.434 1583.14 964.418 1578.75 968.426 1571.96 970.43 1562.79 970.43H1535.81M1535.81 1022.05V984.508H1560.7C1568.92 984.508 1575.03 986.051 1579.04 989.129 1583.07 992.234 1585.09 996.953 1585.09 1003.28 1585.09 1009.57 1583.07 1014.26 1579.04 1017.36 1575.03 1020.49 1568.92 1022.05 1560.7 1022.05H1535.81M1517.04 1036.14H1561.95C1575.37 1036.14 1585.71 1033.45 1592.97 1028.07 1600.23 1022.69 1603.86 1015.04 1603.86 1005.12 1603.86 997.441 1601.93 991.328 1598.07 986.781 1594.21 982.262 1588.52 979.438 1581.02 978.313 1589.72 976.43 1596.48 972.496 1601.29 966.508 1606.13 960.52 1608.55 953.039 1608.55 944.066 1608.55 932.262 1604.66 923.141 1596.86 916.715 1589.06 910.285 1577.98 907.07 1563.6 907.07H1517.04V1036.14"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1634.6 963.391H1681.54V949.309H1634.6V963.391"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1747.84 979.816C1740.27 979.816 1734.26 977.09 1729.84 971.641 1725.41 966.215 1723.2 958.77 1723.2 949.309 1723.2 939.898 1725.41 932.457 1729.84 926.98 1734.26 921.527 1740.27 918.805 1747.84 918.805 1755.42 918.805 1761.42 921.527 1765.84 926.98 1770.27 932.457 1772.48 939.898 1772.48 949.309 1772.48 958.77 1770.27 966.215 1765.84 971.641 1761.42 977.09 1755.42 979.816 1747.84 979.816M1781.87 1033.79V1017.36C1777.64 1019.64 1773.38 1021.37 1769.07 1022.57 1764.79 1023.79 1760.54 1024.4 1756.31 1024.4 1745.21 1024.4 1736.73 1020.55 1730.86 1012.85 1725.02 1005.18 1721.69 993.578 1720.86 978.055 1724.18 983.164 1728.36 987.078 1733.39 989.789 1738.43 992.527 1743.98 993.895 1750.04 993.895 1762.75 993.895 1772.8 989.898 1780.18 981.906 1787.56 973.938 1791.25 963.07 1791.25 949.309 1791.25 935.84 1787.33 925.035 1779.48 916.898 1771.64 908.781 1761.2 904.723 1748.17 904.723 1733.23 904.723 1721.82 910.43 1713.93 921.848 1706.03 933.285 1702.08 949.859 1702.08 971.566 1702.08 991.953 1706.86 1008.2 1716.42 1020.3 1726 1032.42 1738.85 1038.48 1754.95 1038.48 1759.28 1038.48 1763.64 1038.09 1768.04 1037.31 1772.47 1036.53 1777.08 1035.36 1781.87 1033.79"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1871.46 1020.85 1828.85 951.656H1871.46V1020.85M1868.41 1036.14H1890.23V951.656H1909V937.578H1890.23V907.07H1871.46V937.578H1815.14V954.406L1868.41 1036.14"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1956.35 970.43V921.148H1983.34C1992.5 921.148 1999.29 923.18 2003.69 927.238 2008.11 931.293 2010.32 937.492 2010.32 945.828 2010.32 954.234 2008.11 960.434 2003.69 964.418 1999.29 968.426 1992.5 970.43 1983.34 970.43H1956.35M1956.35 1022.05V984.508H1981.25C1989.46 984.508 1995.57 986.051 1999.58 989.129 2003.62 992.234 2005.63 996.953 2005.63 1003.28 2005.63 1009.57 2003.62 1014.26 1999.58 1017.36 1995.57 1020.49 1989.46 1022.05 1981.25 1022.05H1956.35M1937.58 1036.14H1982.5C1995.91 1036.14 2006.25 1033.45 2013.52 1028.07 2020.77 1022.69 2024.41 1015.04 2024.41 1005.12 2024.41 997.441 2022.47 991.328 2018.61 986.781 2014.75 982.262 2009.07 979.438 2001.56 978.313 2010.27 976.43 2017.02 972.496 2021.84 966.508 2026.68 960.52 2029.1 953.039 2029.1 944.066 2029.1 932.262 2025.2 923.141 2017.4 916.715 2009.61 910.285 1998.52 907.07 1984.14 907.07H1937.58V1036.14"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M2059.84 1043.18H2074.07C2082.64 1029.41 2089.06 1015.93 2093.32 1002.73 2097.59 989.559 2099.73 976.469 2099.73 963.465 2099.73 950.41 2097.59 937.258 2093.32 924.012 2089.06 910.785 2082.64 897.316 2074.07 883.605H2059.84C2067.71 896.949 2073.59 910.223 2077.48 923.422 2081.36 936.648 2083.3

949.996 2083.3 963.465 2083.3 976.957 2081.36 990.254 2077.48 1003.36 2073.59 1016.48 2067.71 1029.75 2059.84 1043.18"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M622.203 4294.7H2443.283V4901.727H622.203Z" fill="#ffffff" fill-rule="evenodd"/> <path transform="matrix(.1,0,0,-.1,0,796)" stroke-width="2.8346" stroke-linecap="butt" stroke-miterlimit="10" stroke-linejoin="miter" fill="none" stroke="#ffffff" d="M622.203 4294.7H2443.283V4901.727H622.203Z"/> <path transform="matrix(.1,0,0,-.1,0,796)" stroke-width="30.3515" stroke-linecap="butt" stroke-miterlimit="10" stroke-linejoin="miter" fill="none" stroke="#000000" d="M622.203 4294.7H2443.283V4901.727H622.203Z"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1171.79 4727.1C1170.04 4727.91 1168.13 4728.49 1166.07 4728.86 1164.02 4729.25 1161.75 4729.45 1159.25 4729.45 1150.45 4729.45 1143.7 4726.5 1138.98 4720.61 1134.26 4714.74 1131.9 4706.31 1131.9 4695.31V4642.62H1115.47V4741.18H1131.9V4727.1C1135.18 4732.65 1139.44 4736.77 1144.7 4739.46 1149.95 4742.17 1156.33 4743.52 1163.84 4743.52 1164.91 4743.52 1166.1 4743.52 1167.39 4743.52 1168.69 4743.52 1170.13 4743.52 1171.72 4743.52L1171.79 4727.1"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1270.04 4696.89V4689.55H1194.95C1195.66 4678.09 1199.01 4669.35 1205 4663.34 1210.98 4657.35 1219.32 4654.35 1230 4654.35 1236.21 4654.35 1242.22 4655.14 1248.04 4656.7 1253.86 4658.27 1259.63 4660.61 1265.35 4663.74V4649.66C1259.58 4646.61 1253.66 4644.27 1247.6 4642.66 1241.56 4641.07 1235.44 4640.27 1229.23 4640.27 1213.64 4640.27 1201.28 4644.83 1192.16 4653.95 1183.07 4663.09 1178.52 4675.45 1178.52 4691.02 1178.52 4707.13 1182.89 4719.9 1191.61 4729.34 1200.34 4738.8 1212.11 4743.52 1226.92 4743.52 1240.22 4743.52 1250.73 4739.34 1258.45 4730.98 1266.18 4722.63 1270.04 4711.26 1270.04 4696.89M1253.61 4701.29C1253.49 4709.84 1250.99 4716.67 1246.1 4721.78 1241.23 4726.89 1234.79 4729.45 1226.77 4729.45 1217.68 4729.45 1210.4 4726.98 1204.92 4722.04 1199.47 4717.1 1196.33 4710.15 1195.5 4701.18L1253.61 4701.29"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1358.44 4736.48V4722.41C1354.04 4724.75 1349.46 4726.51 1344.72 4727.68 1339.98 4728.86 1335.07 4729.45 1329.98 4729.45 1322.26 4729.45 1316.46 4728.23 1312.6 4725.82 1308.74 4723.39 1306.81 4719.77 1306.81 4714.93 1306.81 4711.23 1308.15 4708.34 1310.84 4706.23 1313.55 4704.13 1319.01 4702.13 1327.2 4700.22L1332.44 4699.01C1343.54 4696.57 1351.42 4693.11 1356.09 4688.64 1360.78 4684.16 1363.13 4677.92 1363.13 4669.9 1363.13 4660.78 1359.63 4653.56 1352.64 4648.23 1345.65 4642.93 1336.03 4640.27 1323.79 4640.27 1318.68 4640.27 1313.36 4640.86 1307.84 4642.03 1302.31 4643.21 1296.5 4644.96 1290.38 4647.31V4663.74C1296.13 4660.61 1301.79 4658.27 1307.36 4656.7 1312.93 4655.14 1318.45 4654.35 1323.89 4654.35 1331.23 4654.35 1336.86 4655.64 1340.8 4658.2 1344.73 4660.79 1346.7 4664.42 1346.7 4669.09 1346.7 4673.45 1345.31 4676.77 1342.52 4679.07 1339.73 4681.39 1333.61 4683.63 1324.15 4685.78L1318.84 4687.06C1308.79 4689.16 1301.53 4692.39 1297.05 4696.74 1292.61 4701.09 1290.38 4707.05 1290.38 4714.63 1290.38 4723.85 1293.61 4730.96 1300.06 4735.97 1306.52 4741.01 1315.67 4743.52 1327.53 4743.52 1333.39 4743.52 1338.92 4742.94 1344.1 4741.77 1349.28 4740.59 1354.06 4738.83 1358.44 4736.48"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1476.06 4696.89V4689.55H1400.97C1401.68 4678.09 1405.03 4669.35 1411.02 4663.34 1417.01 4657.35 1425.34 4654.35 1436.02 4654.35 1442.23 4654.35 1448.25 4655.14 1454.06 4656.7 1459.88 4658.27 1465.65 4660.61 1471.37 4663.74V4649.66C1465.6 4646.61 1459.69 4644.27 1453.63 4642.66 1447.59 4641.07 1441.46 4640.27 1435.25 4640.27 1419.66 4640.27 1407.3 4644.83 1398.18 4653.95 1389.09 4663.09 1384.54 4675.45 1384.54 4691.02 1384.54 4707.13 1388.91 4719.9 1397.63 4729.34 1406.36 4738.8 1418.13 4743.52 1432.95 4743.52 1446.24 4743.52 1456.75 4739.34 1464.48 4730.98 1472.2 4722.63 1476.06 4711.26 1476.06 4696.89M1459.64 4701.29C1459.52 4709.84 1457.01 4716.67 1452.12 4721.78 1447.26 4726.89 1440.82 4729.45 1432.8 4729.45 1423.7 4729.45 1416.42 4726.98 1410.95 4722.04 1405.49 4717.1 1402.35 4710.15 1401.52 4701.18L1459.64 4701.29"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1519.87 4769.34V4741.18H1552.72V4729.45H1519.87V4675.69C1519.87 4667.63 1520.95 4662.45 1523.1 4660.14 1525.27 4657.85 1529.69 4656.7 1536.34 4656.7H1552.72V4642.62H1536.34C1523.89 4642.62 1515.3 4644.99 1510.56 4649.73 1505.82 4654.5 1503.45 4663.15 1503.45 4675.69V4729.45H1491.71V4741.18H1503.45V4769.34H1519.87"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1603.8 4771.68H1618.83L1572.85 4626.19H1557.82L1603.8 4771.68"/> <path

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4164.09 5305.99"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M4270.55 5344.38V5330.3C4265.95 5332.64 4261.35 5334.4 4256.73 5335.58 4252.13 5336.75 4247.49 5337.34 4242.79 5337.34 4232.26 5337.34 4224.08 5334.05 4218.26 5327.47 4212.45 5320.9 4209.54 5311.67 4209.54 5299.79 4209.54 5287.91 4212.45 5278.68 4218.26 5272.11 4224.08 5265.53 4232.26 5262.25 4242.79 5262.25 4247.49 5262.25 4252.13 5262.83 4256.73 5264 4261.35 5265.18 4265.95 5266.94 4270.55 5269.29V5255.2C4266.05 5252.86 4261.39 5251.1 4256.58 5249.93 4251.79 5248.75 4246.68 5248.16 4241.25 5248.16 4226.51 5248.16 4214.8 5252.81 4206.13 5262.1 4197.45 5271.41 4193.11 5283.98 4193.11 5299.79 4193.11 5315.82 4197.5 5328.44 4206.27 5337.63 4215.05 5346.82 4227.06 5351.42 4242.32 5351.42 4247.28 5351.42 4252.12 5350.83 4256.84 5349.66 4261.55 5348.48 4266.13 5346.72 4270.55 5344.38"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M4384.46 5304.78V5297.45H4309.36C4310.07 5285.98 4313.42 5277.24 4319.41 5271.23 4325.4 5265.24 4333.73 5262.25 4344.41 5262.25 4350.63 5262.25 4356.64 5263.03 4362.46 5264.59 4368.27 5266.16 4374.04 5268.5 4379.76 5271.63V5257.55C4373.99 5254.5 4368.08 5252.16 4362.02 5250.55 4355.98 5248.96 4349.86 5248.16 4343.64 5248.16 4328.05 5248.16 4315.7 5252.72 4306.57 5261.84 4297.48 5270.98 4292.94 5283.34 4292.94 5298.91 4292.94 5315.02 4297.3 5327.79 4306.03 5337.23 4314.75 5346.69 4326.52 5351.42 4341.34 5351.42 4354.63 5351.42 4365.14 5347.24 4372.87 5338.88 4380.59 5330.52 4384.46 5319.15 4384.46 5304.78M4368.03 5309.18C4367.91 5317.73 4365.4 5324.57 4360.51 5329.67 4355.65 5334.78 4349.21 5337.34 4341.19 5337.34 4332.1 5337.34 4324.81 5334.87 4319.34 5329.93 4313.88 5324.99 4310.74 5318.04 4309.91 5309.07L4368.03 5309.18"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M4509.07 5386.62C4501.13 5373.2 4495.23 5359.92 4491.37 5346.8 4487.53 5333.7 4485.61 5320.4 4485.61 5306.9 4485.61 5293.43 4487.55 5280.09 4491.44 5266.86 4495.33 5253.66 4501.2 5240.39 4509.07 5227.04H4494.85C4486.27 5240.76 4479.84 5254.23 4475.56 5267.45 4471.31 5280.7 4469.18 5293.85 4469.18 5306.9 4469.18 5319.91 4471.3 5333 4475.53 5346.17 4479.75 5359.38 4486.2 5372.86 4494.85 5386.62H4509.07"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M4558.75 5365.5V5264.59H4579.88C4597.72 5264.59 4610.79 5268.65 4619.07 5276.77 4627.36 5284.88 4631.5 5297.69 4631.5 5315.19 4631.5 5332.57 4627.36 5345.29 4619.07 5353.36 4610.79 5361.45 4597.72 5365.5 4579.88 5365.5H4558.75M4539.98 5379.58H4577.2C4602.38 5379.58 4620.84 5374.37 4632.6 5363.96 4644.38 5353.57 4650.27 5337.31 4650.27 5315.19 4650.27 5292.92 4644.36 5276.57 4632.53 5266.13 4620.7 5255.72 4602.25 5250.51 4577.2 5250.51H4539.98V5379.58"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M4679.45 5379.58H4707.1L4739.26 5292.61 4771.6 5379.58H4799.13V5250.51H4780.36V5363.99L4747.87 5276.32H4730.71L4698.23 5363.99V5250.51H4679.45V5379.58"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M4835.92 5379.58H4854.69V5250.51H4835.92V5379.58"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M4887.38 5386.62H4901.61C4910.18 5372.86 4916.6 5359.38 4920.86 5346.17 4925.13 5333 4927.27 5319.91 4927.27 5306.9 4927.27 5293.85 4925.13 5280.7 4920.86 5267.45 4916.6 5254.23 4910.18 5240.76 4901.61 5227.04H4887.38C4895.25 5240.39 4901.13 5253.66 4905.02 5266.86 4908.9 5280.09 4910.84 5293.43 4910.84 5306.9 4910.84 5320.4 4908.9 5333.7 4905.02 5346.8 4901.13 5359.92 4895.25 5373.2 4887.38 5386.62"/> <path transform="matrix(.1,0,0,-.1,0,796)" stroke-width="28.346" stroke-linecap="butt" stroke-miterlimit="10" stroke-linejoin="miter" fill="none" stroke="#000000" d="M3396.64 1225.42 2520.28 1128.9"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M2414.62 1117.27 2547.74 1203.22 2520.28 1128.9 2563.26 1062.34" fill-rule="evenodd"/> <path transform="matrix(.1,0,0,-.1,0,796)" stroke-width="28.346" stroke-linecap="butt" stroke-miterlimit="10" stroke-linejoin="miter" fill="none" stroke="#000000" d="M2414.62 1117.27 2547.74 1203.22 2520.28 1128.9 2563.26 1062.34Z"/> <path transform="matrix(.1,0,0,-.1,0,796)" stroke-width="28.346" stroke-linecap="butt" stroke-miterlimit="10" stroke-linejoin="miter" fill="none" stroke="#000000" d="M1532.74 2170.11 1483.57 1554.85"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M1475.11 1448.89 1415.76 1595.81 1483.57 1554.85 1557.04 1584.52" fill-rule="evenodd"/> <path transform="matrix(.1,0,0,-.1,0,796)" stroke-width="28.346" stroke-linecap="butt" stroke-miterlimit="10" stroke-linejoin="miter" fill="none" stroke="#000000" d="M1475.11 1448.89 1415.76 1595.81 1483.57 1554.85 1557.04 1584.52Z"/> <path transform="matrix(.1,0,0,-.1,0,796)" stroke-width="28.346" stroke-linecap="butt" stroke-miterlimit="10"

stroke-linejoin="miter" fill="none" stroke="#000000" d="M2443.28 2777.17 3324.41 1343"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M3380.05 1252.43 3245.48 1336.09 3324.41 1343 3366.24 1410.28" fill-rule="evenodd"/> <path transform="matrix(.1,0,0,-.1,0,796)" stroke-width="28.346" stroke-linecap="butt" stroke-miterlimit="10" stroke-linejoin="miter" fill="none" stroke="#000000" d="M3380.05 1252.43 3245.48 1336.09 3324.41 1343 3366.24 1410.28Z"/> <path transform="matrix(.1,0,0,-.1,0,796)" stroke-width="28.346" stroke-linecap="butt" stroke-miterlimit="10" stroke-linejoin="miter" fill="none" stroke="#000000" d="M4870.61 2257.28 4373.3 1346.54"/> <path transform="matrix(.1,0,0,-.1,0,796)" d="M4322.36 1253.24 4328.09 1411.59 4373.3 1346.54 4452.48 1343.67" fill-rule="evenodd"/> <path transform="matrix(.1,0,0,-.1,0,796)" stroke-width="28.346" stroke-linecap="butt" stroke-miterlimit="10" stroke-linejoin="miter" fill="none" stroke="#000000" d="M4322.36 1253.24 4328.09 1411.59 4373.3 1346.54 4452.48 1343.67Z"/> </svg>

The user interacts with the Debug Host (e.g. laptop), which is running a debugger (e.g. gdb). The debugger communicates with a Debug Translator (e.g. OpenOCD, which may include a hardware driver) to communicate with Debug Transport Hardware (e.g. Olimex USB-JTAG adapter). The Debug Transport Hardware connects the Debug Host to the hardware platform's Debug Transport Module (DTM). The DTM provides access to one or more Debug Modules (DMs) using the Debug Module Interface (DMI).

Each hart in the hardware platform is controlled by exactly one DM. Harts may be heterogeneous. There is no further limit on the hart-DM mapping, but usually all harts in a single core are controlled by the same DM. In most hardware platforms there will only be one DM that controls all the harts in the hardware platform.

DMs provide run control of their harts in the hardware platform. Abstract commands provide access to GPRs. Additional registers are accessible through abstract commands or by writing programs to the optional Program Buffer.

The Program Buffer allows the debugger to execute arbitrary instructions on a hart. This mechanism can also be used to access memory. An optional system bus access block allows memory accesses without using a RISC-V hart to perform the access.

Each RISC-V hart may implement a Trigger Module. When trigger conditions are met, harts will halt and inform the debug module that they have halted.

Chapter 3. Debug Module (DM) (non-ISA extension)

The Debug Module implements a translation interface between abstract debug operations and their specific implementation. It might support the following operations:

Give the debugger necessary information about the implementation. (Required)

Allow any individual hart to be halted and resumed. (Required)

Provide status on which harts are halted. (Required)

Provide abstract read and write access to a halted hart's GPRs. (Required)

Provide access to a reset signal that allows debugging from the very first instruction after reset. (Required)

Provide a mechanism to allow debugging harts immediately out of reset (regardless of the reset cause). (Optional)

Provide abstract access to non-GPR hart registers. (Optional)

Provide a Program Buffer to force the hart to execute arbitrary instructions. (Optional)

Allow multiple harts to be halted, resumed, and/or reset at the same time. (Optional)

Allow memory access from a hart's point of view. (Optional)

Allow direct System Bus Access. (Optional)

Group harts. When any hart in the group halts, they all halt. (Optional)

Respond to external triggers by halting each hart in a configured group. (Optional)

Signal an external trigger when a hart in a group halts. (Optional)

In order to be compatible with this specification an implementation must:

Implement all the required features listed above.

Implement at least one of Program Buffer, System Bus Access, or Abstract Access Memory command mechanisms.

Do at least one of:

Implement the Program Buffer.

Implement abstract access to all registers that are visible to software running on the hart including all the registers that are present on the hart and listed in Table #tab:regno.

Implement abstract access to at least all GPRs, , and , and advertise the implementation as conforming to the `Minimal RISC-V Debug Specification '', instead of the` RISC-V Debug Specification ".

A single DM can debug up to 2^{20} harts.

3.1. Debug Module Interface (DMI)

Debug Modules are subordinates on a bus called the Debug Module Interface (DMI). The bus manager is the Debug Transport Module(s). The Debug Module Interface can be a trivial bus with one manager and one subordinate (see [dmi_signals]), or use a more full-featured bus like TileLink or the AMBA Advanced Peripheral Bus. The details are left to the system designer.

The DMI uses between 7 and 32 address bits. Each address points at a single 32-bit register that can be read or written. The bottom of the address space is used for the first (and usually only) DM. Extra space can be used for custom debug devices, other cores, additional DMs, etc. If there are additional DMs on this DMI, the base address of the next DM in the DMI address space is given in .

The Debug Module is controlled via register accesses to its DMI address space.

3.2. Reset Control

There are two methods that allow a debugger to reset harts. resets all the harts in the hardware platform, as well as all other parts of the hardware platform except for the Debug Modules, Debug Transport Modules, and Debug Module Interface. Exactly what is affected by this reset is implementation dependent, but it must be possible to debug programs from the first instruction executed. resets all the currently selected harts. In this case an implementation may reset more harts than just the ones that are selected. The debugger can discover which other harts are reset (if any) by selecting them and checking and .

To perform either of these resets, the debugger first asserts the bit, and then clears it. The actual reset may start as soon as the bit is asserted, but may start an arbitrarily long time after the bit is deasserted. The reset itself may also take an arbitrarily long time. While the reset is on-going, harts are either in the running state, indicating it's possible to perform some abstract commands during this time, or in the unavailable state, indicating it's not possible to perform any abstract commands during this time. Once a hart's reset is complete, `havereset` becomes set. When a hart comes out of reset and or are set, the hart will immediately enter Debug Mode (halted state). Otherwise, if the hart was initially running it will execute normally (running state) and if the hart was initially halted it should now be running but may be halted.

There is no general, reliable way for the debugger to know when reset has actually begun.

The Debug Module's own state and registers should only be reset at power-up and while in is 0. If there is another mechanism to reset the DM, this mechanism must also reset all the harts accessible to the DM.

Due to clock and power domain crossing issues, it might not be possible to perform arbitrary DMI accesses across hardware platform reset. While or any external reset is asserted, the only supported DM operations are reading and writing . The behavior of other accesses is undefined.

When harts have been reset, they must set a sticky `havereset` state bit. The conceptual `havereset` state bits can be read for selected harts in and in . These bits must be set regardless of the cause of the reset. The `havereset` bits for the selected harts can be cleared by writing 1 to in . The `havereset` bits might or might not be cleared when is low.

3.3. Selecting Harts

Up to 2^{20} harts can be connected to a single DM. Commands issued to the DM only apply to the currently selected harts.

To enumerate all the harts, a debugger must first determine `HARTSELLEN` by writing all ones to (assuming the maximum size) and reading back the value to see which bits were actually set. Then it selects each hart starting from 0 until either in is 1, or the highest index (depending on `HARTSELLEN`) is reached.

The debugger can discover the mapping between hart indices and by using the interface to read , or by reading the hardware platform's configuration structure.

3.3.1. Selecting a Single Hart

All debug modules must support selecting a single hart. The debugger can select a hart by writing its index to . Hart indexes start at 0 and are contiguous until the final index.

3.3.2. Selecting Multiple Harts

Debug Modules may implement a Hart Array Mask register to allow selecting multiple harts at once. The nth bit in the Hart Array Mask register applies to the hart with index n. If the bit is 1 then the hart is selected. Usually a DM will have a Hart Array Mask register exactly wide enough to select all the harts it supports, but it's allowed to tie any of these bits to 0.

The debugger can set bits in the hart array mask register using and , then apply actions to all selected harts by setting . If this feature is supported, multiple harts can be halted, resumed, and reset simultaneously. The state of the hart array mask register is not affected by setting or clearing .

Execution of Abstract Commands ignores this mechanism and only applies to the hart selected by .

3.4. Hart DM States

Every hart that can be selected is in exactly one of the following four DM states: non-existent, unavailable, running, or halted. Which state the selected harts are in is reflected by , , , , , , , and .

Harts are nonexistent if they will never be part of this hardware platform, no matter how long a user waits. E.g. in a simple single-hart hardware platform only one hart exists, and all others are nonexistent. Debuggers may assume that a hardware platform has no harts with indexes higher than the first nonexistent one.

Harts are unavailable if they might exist/become available at a later time, or if there are other harts with higher indexes than this one. Harts may be unavailable for a variety of reasons including being reset, temporarily powered down, and not being plugged into the hardware platform. That means harts might become available or unavailable at any time, although these events should be rare in hardware platforms built to be easily debugged. There are no guarantees about the state of the hart when it becomes available.

Hardware platforms with very large number of harts may permanently disable some during manufacturing, leaving holes in the otherwise continuous hart index space. In order to let the debugger discover all harts, they must show up as unavailable even if there is no chance of them ever becoming available.

Harts are running when they are executing normally, as if no debugger was attached. This includes being in a low power mode or waiting for an interrupt, as long as a halt request will result in the hart being halted.

Harts are halted when they are in Debug Mode, only performing tasks on behalf of the debugger.

Which states a hart that is reset goes through is implementation dependent. Harts may be unavailable while reset is asserted, and some time after reset is deasserted. They might transition to running for some time after reset is deasserted. Finally they end up either running or halted, depending on and .

3.5. Run Control

For every hart, the Debug Module tracks 4 conceptual bits of state: halt request, resume ack, halt-on-reset request, and hart reset. (The hart reset and halt-on-reset request bits are optional.) These 4 bits reset to 0, except for resume ack, which may reset to either 0 or 1. The DM receives halted, running, and havereset signals from each hart. The debugger can observe the state of resume ack in and , and the state of halted, running, and havereset signals in , , , , , and . The state of the other bits cannot be observed directly.

When a debugger writes 1 to , each selected hart's halt request bit is set. When a running hart, or a hart just coming out of reset, sees its halt request bit high, it responds by halting, deasserting its running signal, and asserting its halted signal. Halted harts ignore their halt request bit.

When a debugger writes 1 to , each selected hart's resume ack bit is cleared and each selected, halted hart is sent a resume request. Harts respond by resuming, clearing their halted signal, and asserting their running signal. At the end of this process the resume ack bit is set. These status signals of all selected harts are reflected in , , , and . Resume requests are ignored by running harts.

When halt or resume is requested, a hart must respond in less than one second, unless it is unavailable. (How this is implemented is not further specified. A few clock cycles will be a more typical latency).

The DM can implement optional halt-on-reset bits for each hart, which it indicates by setting to 1. This means the DM implements the and bits. Writing 1 to sets the halt-on-reset request bit for each selected hart. When a hart's halt-on-reset request bit is set, the hart will immediately enter debug mode on the next deassertion of its reset. This is true regardless of the reset's cause. The hart's halt-on-reset request bit remains set until cleared by the debugger writing 1 to while the hart is selected, or by DM reset.

If the DM is reset while a hart is halted, it is whether that hart resumes. Debuggers should use to explicitly resume harts before clearing and disconnecting.

3.6. Halt Groups, Resume Groups, and External Triggers

An optional feature allows a debugger to place harts into two kinds of groups: halt groups and resume groups. It is also possible to add external triggers to a halt and resume groups. At any given time, each hart and each trigger is a member of exactly one halt group and exactly one resume group.

In both halt and resume groups, group 0 is special. Harts in group 0 halt/resume as if groups aren't implemented at all.

When any hart in a halt group halts:

That hart halts normally, with reflecting the original cause of the halt.

All the other harts in the halt group that are running will quickly halt. for those harts should be set to 6, but may be set to 3. Other harts in the halt group that are halted but have started the process of resuming must also quickly become halted, even if they do resume briefly.

Any external triggers in that group are notified.

Adding a hart to a halt group does not automatically halt that hart, even if other harts in the group are already halted.

When an external trigger that's a member of the halt group fires:

All the harts in the halt group that are running will quickly halt. for those harts should be set to 6, but may be set to 3. Other harts in the halt group that are halted but have started the process of resuming must also quickly become halted, even if they do resume briefly.

When any hart in a resume group resumes:

All the other harts in that group that are halted will quickly resume as soon as any currently executing abstract commands have completed. Each hart in the group sets its resume ack bit as soon as it has resumed. Harts that are in the process of halting should complete that process and stay halted.

Any external triggers in that group are notified.

Adding a hart to a resume group does not automatically resume that hart, even if other harts in the group are currently running.

When an external trigger that's a member of the resume group fires:

All the harts in that group that are halted will quickly resume as soon as any currently executing abstract commands have completed. Each hart in the group sets its resume ack bit as soon as it has resumed. Harts that are in the process of halting should complete that process and stay halted.

External triggers are abstract concepts that can signal the DM and/or receive signals from the DM. This configuration is done through , where external triggers are referred to by a number. Commonly, external triggers are capable of sending a signal from the hardware platform into the DM, as well as receiving a signal from the DM to take their own action on. It is also allowable for an external trigger to be input-only or output-only. By convention external triggers 0–7 are bidirectional, triggers 8–11 are input-only, and triggers 12–15 are output-only but this is not required.

External triggers could be used to implement near simultaneous halting/resuming of all cores in a hardware platform, when not all cores are RISC-V cores.

When the DM is reset, all harts must be placed in the lowest-numbered halt and resume groups that they can be in. (This will usually be group 0.)

Some designs may choose to hardcode hart groups to a group other than group 0, meaning it is never possible to halt or resume just a single hart. This is explicitly allowed. In that case it must be possible to discover the groups by using even if it's not possible to change the configuration.

3.7. Abstract Commands

The DM supports a set of abstract commands, most of which are optional. Depending on the implementation, the debugger may be able to perform some abstract commands even when the selected hart is not halted. Debuggers can only determine which abstract commands are supported by a given hart in a given state (running, halted, or held in reset) by attempting them and then looking at in to see if they were successful. Commands may be supported with some options set, but not with other options set. If a command has unsupported options set or if bits that are defined as 0 aren't 0, then the DM must set to 2 (not supported).

Example: Every DM must support the Access Register command, but might not support accessing CSRs. If the debugger requests to read a CSR in that case, the command will return `not supported."

Debuggers execute abstract commands by writing them to . They can determine whether an abstract command is complete by reading in . If the debugger starts a new command while is set, becomes 1 (busy), the currently executing command still gets to run to completion, but any error generated by the currently executing command is lost. After completion, indicates whether the command was successful or not. Commands may fail because a hart is not halted, not running, unavailable, or because they encounter an error during execution.

If the command takes arguments, the debugger must write them to the `data` registers before writing to . If a command returns results, the Debug Module must ensure they are placed in the `data` registers before is cleared. Which `data` registers are used for the arguments is described in Table #tab:datareg. In all cases the least-significant word is placed in the lowest-numbered `data` register. The argument width depends on the command being executed, and is DXLEN where not explicitly specified.

|r|l|l|l| Argument Width & arg0/return value & arg1 & arg2
& & `data1` & `data2`
& , `data1` & `data2`, `data3` & `data4`, `data5`
& –`data3` & `data4`–`data7` & `data8`–`data11`

The Abstract Command interface is designed to allow a debugger to write commands as fast as possible, and then later check whether they completed without error. In the common case the debugger will be much slower than the target and commands succeed, which allows for maximum throughput. If there is a failure, the interface ensures that no commands execute after the failing one. To discover which command failed, the debugger has to look at the state of the DM (e.g. contents of) or hart (e.g. contents of a register modified by a Program Buffer program) to determine which one failed.

Before starting an abstract command, a debugger must ensure that , , and are all 0.

While an abstract command is executing (in is high), a debugger must not change , and must not write 1 to , , , , or .

If an abstract command does not complete in the expected time and appears to be hung, the debugger can try to reset the hart (using or). If that doesn't clear , then it can try resetting the Debug Module (using).

If an abstract command is started while the selected hart is unavailable or if a hart becomes unavailable while executing an abstract command, then the Debug Module may terminate the abstract command, setting low, and to 4 (halt/resume). Alternatively, the command could just appear to be hung (never goes low).

3.7.1. Abstract Command Listing

This section describes each of the different abstract commands and how their fields should be interpreted when they are written to .

Each abstract command is a 32-bit value. The top 8 bits contain which determines the kind of command. Table #tab:cmdtype lists all commands.

|r|l|l|l| & Command & Page
& Access Register Command &
& Quick Access &
& Access Memory Command &

3.8. Program Buffer

To support executing arbitrary instructions on a halted hart, a Debug Module can include a Program Buffer that a debugger can write small programs to. DMs that support all necessary functionality using abstract commands only may choose to omit the Program Buffer.

A debugger can write a small program to the Program Buffer, and then execute it exactly once with the Access Register Abstract Command, setting the bit in . The debugger can write whatever program it likes (including jumps out of the Program Buffer), but the program must end with `ebreak` or `c.ebreak`. An implementation may support an implicit `ebreak` that is executed when a hart runs off the end of the Program Buffer. This is indicated by . With this feature, a Program Buffer of just 2 32-bit words can offer efficient debugging.

While these programs are executed, the hart does not leave Debug Mode (see Section [debugmode]). If an exception is encountered during execution of the Program Buffer, no more instructions are executed, the hart remains in Debug Mode, and is set to 3 (`exception error`). If the debugger executes a program that doesn't terminate with an `ebreak` instruction, the hart will remain in Debug Mode and the debugger will lose control of the hart.

If is 1 then the following apply:

must be 1.

If the debugger writes a compressed instruction into the Program Buffer, it must be placed into the lower 16 bits and accompanied by a compressed `nop` in the upper 16 bits.

This requirement on the debugger for the case of equal to 1 is to accommodate hardware designs that prefer to stuff instructions directly into the pipeline when halted, instead of having the Program Buffer exist in the address space somewhere.

The Program Buffer may be implemented as RAM which is accessible to the hart. A debugger can determine if this is the case by executing small programs that attempt to write and read back relative to while executing from the Program Buffer. If so, the debugger has more flexibility in what it can do with the program buffer.

3.9. Overview of Hart Debug States

Figure #fig:abstract_sm[1.1] shows a conceptual view of the states passed through by a hart during run/halt debugging as influenced by the different fields of , , , and .

[fig/abstract_commands] | *fig/abstract_commands.pdf*

Figure 1. Run/Halt Debug State Machine for single-hart hardware platforms. As only a small amount of state is visible to the debugger, the states and transitions are conceptual.

3.10. System Bus Access

A debugger can access memory from a hart's point of view using a Program Buffer or the Abstract Access Memory command. (Both these features are optional.) A Debug Module may also include a System Bus Access block to provide memory access without involving a hart, regardless of whether Program Buffer is implemented. The System Bus Access block uses physical addresses.

The System Bus Access block may support 8-, 16-, 32-, 64-, and 128-bit accesses. Table #tab:sbdatabits shows which bits in `sbdata` are used for each access size.

|r|l| Access Size & Data Bits
& bits 7:0
& bits 15:0
&
& ,
& , , ,

Depending on the microarchitecture, data accessed through System Bus Access might not always be coherent with that observed by each hart. It is up to the debugger to enforce coherency if the implementation does not. This specification does not define a standard way to do this. Possibilities may include writing to special memory-mapped locations, or executing special instructions via the Program Buffer.

Implementing a System Bus Access block has several benefits even when a Debug Module also implements a Program Buffer. First, it is possible to access memory in a running system with minimal impact. Second, it may improve performance when accessing memory. Third, it may provide access to devices that a hart does not have access to.

3.11. Minimally Intrusive Debugging

Depending on the task it is performing, some harts can only be halted very briefly. There are several mechanisms that allow accessing resources in such a running system with a minimal impact on the running hart.

First, an implementation may allow some abstract commands to execute without halting the hart.

Second, the Quick Access abstract command can be used to halt a hart, quickly execute the contents of the Program Buffer, and let the hart run again. Combined with instructions that allow Program Buffer code to access the `data` registers, as described in , this can be used to quickly perform a memory or register access. For some hardware platforms this will be too intrusive, but many hardware platforms that can't be halted can bear an occasional hiccup of a hundred or less cycles.

Third, if the System Bus Access block is implemented, it can be used while a hart is running to access system memory.

3.12. Security

To protect intellectual property it may be desirable to lock access to the Debug Module. To allow access during a manufacturing process and not afterwards, a reasonable solution could be to add a fuse bit to the Debug Module that can be used to be permanently disable it. Since this is technology specific, it is not further addressed in this spec.

Another option is to allow the DM to be unlocked only by users who have an access key. Between , , and arbitrarily complex authentication mechanism can be supported. When is clear, the DM must not interact with the rest of the hardware platform, nor expose details about the harts connected to the DM. All DM registers should read 0, while writes should be ignored, with the following mandatory exceptions:

in is readable.

in is readable.

in is readable.

in is readable and writable.

is readable and writable.

Implementations where it's not possible to unlock the DM by using should not implement that register.

3.13. Version Detection

To detect the version of the Debug Module with a minimum of side effects, use the following procedure:

Read .

If is 0 or is 1:

1. Write , preserving , , , and from the value that was read, setting , and clearing all the other bits.
2. Read until is high.

Read , which contains .

If it was necessary to clear , this might have the following unavoidable side effects:

is cleared, potentially preventing a halt request made by a previous debugger from taking effect.

is cleared, potentially preventing a resume request made by a previous debugger from taking effect.

is deasserted, releasing the hardware platform from reset if a previous debugger had set it.

is asserted, releasing the DM from reset. This in itself is not observable by any harts.

This procedure is guaranteed to work in future versions of this spec. The meaning of the bits where , , , and currently reside might change, but preserving them will have no side effects. Clearing the bits of not explicitly mentioned here will have no side effects beyond the ones mentioned above.

3.14. Debug Module Registers

The registers described in this section are accessed over the DMI bus. Each DM has a base address (which is 0 for the first DM). The register addresses below are offsets from this base address.

Debug Module DMI Registers that are unimplemented or not mentioned in the table below return 0 when read. Writing them has no effect.

Address	Name	Page
Continued on next page		
0x04	Abstract Data 0 (`data0`)	
0x05	Abstract Data 1 (`data1`)	
0x06	Abstract Data 2 (`data2`)	
0x07	Abstract Data 3 (`data3`)	
0x08	Abstract Data 4 (`data4`)	
0x09	Abstract Data 5 (`data5`)	
0x0a	Abstract Data 6 (`data6`)	
0x0b	Abstract Data 7 (`data7`)	
0x0c	Abstract Data 8 (`data8`)	
0x0d	Abstract Data 9 (`data9`)	
0x0e	Abstract Data 10 (`data10`)	
0x0f	Abstract Data 11 (`data11`)	
0x10	Debug Module Control (`dmcontrol`)	
0x11	Debug Module Status (`dmstatus`)	
0x12	Hart Info (`hartinfo`)	
0x13	Halt Summary 1 (`haltsum1`)	
0x14	Hart Array Window Select (`hawindowsel`)	
0x15	Hart Array Window (`hawindow`)	
0x16	Abstract Control and Status (`abstractcs`)	
0x17	Abstract Command (`command`)	
0x18	Abstract Command Autoexec (`abstractauto`)	
0x19	Configuration Structure Pointer 0 (`confstrptr0`)	
0x1a	Configuration Structure Pointer 1 (`confstrptr1`)	
0x1b	Configuration Structure Pointer 2 (`confstrptr2`)	
0x1c	Configuration Structure Pointer 3 (`confstrptr3`)	

Address	Name	Page
0x1d	Next Debug Module (`nextdm`)	
0x1f	Custom Features (`custom`)	
0x20	Program Buffer 0 (`progbuf0`)	
0x21	Program Buffer 1 (`progbuf1`)	
0x22	Program Buffer 2 (`progbuf2`)	
0x23	Program Buffer 3 (`progbuf3`)	
0x24	Program Buffer 4 (`progbuf4`)	
0x25	Program Buffer 5 (`progbuf5`)	
0x26	Program Buffer 6 (`progbuf6`)	
0x27	Program Buffer 7 (`progbuf7`)	
0x28	Program Buffer 8 (`progbuf8`)	
0x29	Program Buffer 9 (`progbuf9`)	
0x2a	Program Buffer 10 (`progbuf10`)	
0x2b	Program Buffer 11 (`progbuf11`)	
0x2c	Program Buffer 12 (`progbuf12`)	
0x2d	Program Buffer 13 (`progbuf13`)	
0x2e	Program Buffer 14 (`progbuf14`)	
0x2f	Program Buffer 15 (`progbuf15`)	
0x30	Authentication Data (`authdata`)	
0x32	Debug Module Control and Status 2 (`dmcs2`)	
0x34	Halt Summary 2 (`haltsum2`)	
0x35	Halt Summary 3 (`haltsum3`)	
0x37	System Bus Address 127:96 (`sbaddress3`)	
0x38	System Bus Access Control and Status (`sbcs`)	
0x39	System Bus Address 31:0 (`sbaddress0`)	
0x3a	System Bus Address 63:32 (`sbaddress1`)	
0x3b	System Bus Address 95:64 (`sbaddress2`)	
0x3c	System Bus Data 31:0 (`sbdata0`)	
0x3d	System Bus Data 63:32 (`sbdata1`)	
0x3e	System Bus Data 95:64 (`sbdata2`)	
0x3f	System Bus Data 127:96 (`sbdata3`)	
0x40	Halt Summary 0 (`haltsum0`)	
0x70	Custom Features 0 (`custom0`)	

Address	Name	Page
0x71	Custom Features 1 (`custom1`)	
0x72	Custom Features 2 (`custom2`)	
0x73	Custom Features 3 (`custom3`)	
0x74	Custom Features 4 (`custom4`)	
0x75	Custom Features 5 (`custom5`)	
0x76	Custom Features 6 (`custom6`)	
0x77	Custom Features 7 (`custom7`)	
0x78	Custom Features 8 (`custom8`)	
0x79	Custom Features 9 (`custom9`)	
0x7a	Custom Features 10 (`custom10`)	
0x7b	Custom Features 11 (`custom11`)	
0x7c	Custom Features 12 (`custom12`)	
0x7d	Custom Features 13 (`custom13`)	
0x7e	Custom Features 14 (`custom14`)	
0x7f	Custom Features 15 (`custom15`)	

Table 2. Debug Module Debug Bus Registers

3.14.1. Debug Module Status (`dmstatus`, at 0x11)

[dmDmstatus]# This register reports status for the overall Debug Module as well as the currently selected harts, as defined in . Its address will not change in the future, because it contains .

This entire register is read-only.

31	25	24		23		22		21	20	19	
latexmath:[$	0	$]		latexmath:[$	ndmresetpending	$]		latexmath:[$	stickyunavail	$]	
latexmath:[$	impebreak	$]		latexmath:[$	0	$]		latexmath:[$	allhavereset	$]	
7		1		1		1		2		1	

18		17		16		15		14		13	
latexmath:[$	anyhavereset	$]		latexmath:[$	allresumeack	$]		latexmath:[$	anyresumeack	$]	
latexmath:[$	allnonexistent	$]		latexmath:[$	anynonexistent	$]		latexmath:[$	allunavail	$]	
1		1		1		1		1		1	

12		11		10		9		8		7	
latexmath:[$	anyunavail	$]		latexmath:[$	allrunning	$]		latexmath:[$	anyrunning	$]	

12		11		10		9		8		7	
latexmath:[$	allhalted	$]		latexmath:[$	anyhalted	$]		latexmath:[$	authenticated	$]	
1		1		1		1		1		1	

6		5		4		3	0
latexmath:[$	authbusy	$]		latexmath:[$	hasresethaltreq	$]	
latexmath:[$	confstrptrvalid	$]		latexmath:[$	version	$]	
1		1		1		4	

Field	Description	Access	Reset
Continued on next page			
[dmDmstatusNdmresetpending]# |ndmresetpending|	0 (false): Unimplemented, or is zero and no ndmreset is currently in progress. 1 (true): is currently nonzero, or there is an ndmreset in progress.	R	-
[dmDmstatusStickyunavail]# |stickyunavail|	0 (current): The per-hart `unavail` bits reflect the current state of the hart. 1 (sticky): The per-hart `unavail` bits are sticky. Once they are set, they will not clear until the debugger acknowledges them using .	R	Preset
[dmDmstatusImpebreak]# |impebreak|	If 1, then there is an implicit `ebreak` instruction at the non-existent word immediately after the Program Buffer. This saves the debugger from having to write the `ebreak` itself, and allows the Program Buffer to be one word smaller. This must be 1 when is 1.	R	Preset
[dmDmstatusAllhavereset]# |allhavereset|	This field is 1 when all currently selected harts have been reset and reset has not been acknowledged for any of them.	R	-
[dmDmstatusAnyhavereset]# |anyhavereset|	This field is 1 when at least one currently selected hart has been reset and reset has not been acknowledged for that hart.	R	-

Field	Description	Access	Reset
[dmDmstatusAllresumeack]# |allresumeack|	This field is 1 when all currently selected harts have their resume ack bit set.	R	-
[dmDmstatusAnyresumeack]# |anyresumeack|	This field is 1 when any currently selected hart has its resume ack bit set.	R	-
[dmDmstatusAllnonexistent]# |allnonexistent|	This field is 1 when all currently selected harts do not exist in this hardware platform.	R	-
[dmDmstatusAnynonexistent]# |anynonexistent|	This field is 1 when any currently selected hart does not exist in this hardware platform.	R	-
[dmDmstatusAllunavail]# |allunavail|	This field is 1 when all currently selected harts are unavailable, or (if is 1) were unavailable without that being acknowledged.	R	-
[dmDmstatusAnyunavail]# |anyunavail|	This field is 1 when any currently selected hart is unavailable, or (if is 1) was unavailable without that being acknowledged.	R	-
[dmDmstatusAllrunning]# |allrunning|	This field is 1 when all currently selected harts are running.	R	-
[dmDmstatusAnyrunning]# |anyrunning|	This field is 1 when any currently selected hart is running.	R	-
[dmDmstatusAllhalted]# |allhalted|	This field is 1 when all currently selected harts are halted.	R	-
[dmDmstatusAnyhalted]# |anyhalted|	This field is 1 when any currently selected hart is halted.	R	-
[dmDmstatusAuthenticated]# |authenticated|	0 (false): Authentication is required before using the DM. 1 (true): The authentication check has passed. On components that don't implement authentication, this bit must be preset as 1.	R	Preset

Field	Description	Access	Reset
[dmDmstatusAuthbusy]# |authbusy|	0 (ready): The authentication module is ready to process the next read/write to . 1 (busy): The authentication module is busy. Accessing results in unspecified behavior. only becomes set in immediate response to an access to .	R	0
[dmDmstatusHasresethaltreq]# |hasresethaltreq|	1 if this Debug Module supports halt-on-reset functionality controllable by the and bits. 0 otherwise.	R	Preset
[dmDmstatusConfstrptrvalid]# |confstrptrvalid|	0 (invalid): –hold information which is not relevant to the configuration structure. 1 (valid): –hold the address of the configuration structure.	R	Preset
|version|	0 (none): There is no Debug Module present. 1 (0.11): There is a Debug Module and it conforms to version 0.11 of this specification. 2 (0.13): There is a Debug Module and it conforms to version 0.13 of this specification. 3 (1.0): There is a Debug Module and it conforms to version 1.0 of this specification. 15 (custom): There is a Debug Module but it does not conform to any available version of this spec.	R	3

3.14.2. Debug Module Control (`dmcontrol`, at 0x10)

[dmDmcontrol]# This register controls the overall Debug Module as well as the currently selected harts, as defined in .

[hartsel]# Throughout this document we refer to , which is combined with . While the spec allows for

20 bits, an implementation may choose to implement fewer than that. The actual width of is called HARTSELLEN. It must be at least 0 and at most 20. A debugger should discover HARTSELLEN by writing all ones to (assuming the maximum size) and reading back the value to see which bits were actually set. Debuggers must not change while an abstract command is executing.

There are separate and bits so that it is possible to write without changing the halt-on-reset request bit for each selected hart, when not all selected harts have the same configuration.

On any given write, a debugger may only write 1 to at most one of the following bits: , , , , and . The others must be written 0.

[resethaltreq]# is an optional internal bit of per-hart state that cannot be read, but can be written with and .

[keepalive]# is an optional internal bit of per-hart state. When it is set, it suggests that the hardware should attempt to keep the hart available for the debugger, e.g. by keeping it from entering a low-power state once powered on. Even if the bit is implemented, hardware might not be able to keep a hart available. The bit is written through and .

For forward compatibility, will always be readable when bit 1 () is 0 and bit 0 () is 1.

31		30		29		28		27	
latexmath:[$	haltreq	$]		latexmath:[$	resumereq	$]		latexmath:[$	hartreset
$]		latexmath:[$	ackhavereset	$]		latexmath:[$	ackunavail	$]	
1		1		1		1		1	

26		25	16	15	6	5		4	
latexmath:[$	hasel	$]		latexmath:[$	hartsello	$]		latexmath:[$	hartselhi
$]		latexmath:[$	setkeepalive	$]		latexmath:[$	clrkeepalive	$]	
1		10		10		1		1	

3		2		1		0	
latexmath:[$	setresethaltreq	$]		latexmath:[$	clrresethaltreq	$]	
latexmath:[$	ndmreset	$]		latexmath:[$	dmactive	$]	
1		1		1		1	

Field	Description	Access	Reset
Continued on next page			

Field	Description	Access	Reset
[dmDmcontrolHaltreq]# |haltreq|	Writing 0 clears the halt request bit for all currently selected harts. This may cancel outstanding halt requests for those harts. Writing 1 sets the halt request bit for all currently selected harts. Running harts will halt whenever their halt request bit is set. Writes apply to the new value of and .	WARZ	-
[dmDmcontrolResumereq]# |resumereq|	Writing 1 causes the currently selected harts to resume once, if they are halted when the write occurs. It also clears the resume ack bit for those harts. is ignored if is set. Writes apply to the new value of and .	W1	-
[dmDmcontrolHartreset]# |hartreset|	This optional field writes the reset bit for all the currently selected harts. To perform a reset the debugger writes 1, and then writes 0 to deassert the reset signal. While this bit is 1, the debugger must not change which harts are selected. If this feature is not implemented, the bit always stays 0, so after writing 1 the debugger can read the register back to see if the feature is supported. Writes apply to the new value of and .	WARL	0
[dmDmcontrolAckhavereset]# |ackhavereset|	0 (nop): No effect. 1 (ack): Clears `havereset` for any selected harts. Writes apply to the new value of and .	W1	-

Field	Description	Access	Reset
[dmDmcontrolAckunavail]# |ackunavail|	0 (nop): No effect. 1 (ack): Clears `unavail` for any selected harts that are currently available. Writes apply to the new value of and .	W1	-
[dmDmcontrolHasel]# |hasel|	Selects the definition of currently selected harts. 0 (single): There is a single currently selected hart, that is selected by . 1 (multiple): There may be multiple currently selected harts – the hart selected by , plus those selected by the hart array mask register. An implementation which does not implement the hart array mask register must tie this field to 0. A debugger which wishes to use the hart array mask register feature should set this bit and read back to see if the functionality is supported.	WARL	0
[dmDmcontrolHartsello]# |hartsello|	The low 10 bits of : the DM-specific index of the hart to select. This hart is always part of the currently selected harts.	WARL	0
[dmDmcontrolHartselhi]# |hartselhi|	The high 10 bits of : the DM-specific index of the hart to select. This hart is always part of the currently selected harts.	WARL	0
[dmDmcontrolSetkeepalive]# |setkeepalive|	This optional field sets for all currently selected harts, unless is simultaneously set to 1. Writes apply to the new value of and .	W1	-
[dmDmcontrolClrkeepalive]# |clrkeepalive|	This optional field clears for all currently selected harts. Writes apply to the new value of and .	W1	-

Field	Description	Access	Reset
[dmDmcontrolSetresethaltreq]# |setresethaltreq|	This optional field writes the halt-on-reset request bit for all currently selected harts, unless is simultaneously set to 1. When set to 1, each selected hart will halt upon the next deassertion of its reset. The halt-on-reset request bit is not automatically cleared. The debugger must write to to clear it. Writes apply to the new value of and . If is 0, this field is not implemented.	W1	-
[dmDmcontrolClrresethaltreq]# |clrresethaltreq|	This optional field clears the halt-on-reset request bit for all currently selected harts. Writes apply to the new value of and .	W1	-
[dmDmcontrolNdmreset]# |ndmreset|	This bit controls the reset signal from the DM to the rest of the hardware platform. The signal should reset every part of the hardware platform, including every hart, except for the DM and any logic required to access the DM. To perform a hardware platform reset the debugger writes 1, and then writes 0 to deassert the reset.	R/W	0

Field	Description	Access	Reset
|dmactive|	This bit serves as a reset signal for the Debug Module itself. After changing the value of this bit, the debugger must poll until has taken the requested value before performing any action that assumes the requested state change has completed. Hardware may take an arbitrarily long time to complete activation or deactivation and will indicate completion by setting to the requested value. 0 (inactive): The module's state, including authentication mechanism, takes its reset values (the bit is the only bit which can be written to something other than its reset value). Any accesses to the module may fail. Specifically, might not return correct data. 1 (active): The module functions normally. No other mechanism should exist that may result in resetting the Debug Module after power up. To place the Debug Module into a known state, a debugger may write 0 to , poll until is observed 0, write 1 to , and poll until is observed 1. Implementations may pay attention to this bit to further aid debugging, for example by preventing the Debug Module from being power gated while debugging is active.	R/W	0

3.14.3. Hart Info (`hartinfo`, at 0x12)

[dmHartinfo]# This register gives information about the hart currently selected by .

This register is optional. If it is not present it should read all-zero.

If this register is included, the debugger can do more with the Program Buffer by writing programs which explicitly access the `data` and/or `dscratch` registers.

This entire register is read-only.

31	24	23	20	19	17	16		15	12	11	0
latexmath:[$	0	$]		latexmath:[$	nscratch	$]		latexmath:[$	0	$]	
latexmath:[$	dataaccess	$]		latexmath:[$	datasize	$]		latexmath:[$	dataaddr	$]	
8		4		3		1		4		12	

Field	Description	Access	Reset
Continued on next page			
[dmHartinfoNscratch]# |nscratch|	Number of `dscratch` registers available for the debugger to use during program buffer execution, starting from . The debugger can make no assumptions about the contents of these registers between commands.	R	Preset
[dmHartinfoDataaccess]# |dataaccess|	0 (csr): The `data` registers are shadowed in the hart by CSRs. Each CSR is DXLEN bits in size, and corresponds to a single argument, per Table #tab:datareg. 1 (memory): The `data` registers are shadowed in the hart's memory map. Each register takes up 4 bytes in the memory map.	R	Preset
[dmHartinfoDatasize]# |datasize|	If is 0: Number of CSRs dedicated to shadowing the `data` registers. If is 1: Number of 32-bit words in the memory map dedicated to shadowing the `data` registers. If this value is non-zero, then the tt data registers must be traditional registers and not MRs. Since there are at most 12 `data` registers, the value in this register must be 12 or smaller.	R	Preset

Field	Description	Access	Reset
|dataaddr|	If is 0: The number of the first CSR dedicated to shadowing the `data` registers. If is 1: Address of RAM where the data registers are shadowed. This address is sign extended giving a range of -2048 to 2047, easily addressed with a load or store using as the address register.	R	Preset

3.14.4. Hart Array Window Select (`hawindowsel`, at 0x14)

[dmHawindowsel]# This register selects which of the 32-bit portion of the hart array mask register (see Section 1.3.2) is accessible in .

31	15	14	0
latexmath:[$	0	$]	
latexmath:[$	hawindowsel	$]	
17		15	

Field	Description	Access	Reset
Continued on next page			
|hawindowsel|	The high bits of this field may be tied to 0, depending on how large the array mask register is. E.g. on a hardware platform with 48 harts only bit 0 of this field may actually be writable.	WARL	0

3.14.5. Hart Array Window (`hawindow`, at 0x15)

[dmHawindow]# This register provides R/W access to a 32-bit portion of the hart array mask register (see Section 1.3.2). The position of the window is determined by . I.e. bit 0 refers to hart RdmHawindowsel * 32, while bit 31 refers to hart RdmHawindowsel * 32+31.

Since some bits in the hart array mask register may be constant 0, some bits in this register may be constant 0, depending on the current value of .

31	0
latexmath:[$	maskdata
$]	
32	

3.14.6. Abstract Control and Status (`abstractcs`, at 0x16)

[dmAbstractcs]# Writing this register while an abstract command is executing causes to become 1 (busy) once the command completes (busy becomes 0).

must be at least 1 to support RV32 harts, 2 to support RV64 harts, or 4 to support RV128 harts.

31	29	28	24	23	13	12	
latexmath:[$	0	$]		latexmath:[$	progbufsize	$]	
latexmath:[$	0	$]		latexmath:[$	busy	$]	
3		5		11		1	

11		10	8	7	4	3	0
latexmath:[$	relaxedpriv	$]		latexmath:[$	cmderr	$]	
latexmath:[$	0	$]		latexmath:[$	datacount	$]	
1		3		4		4	

Field	Description	Access	Reset
Continued on next page			
[dmAbstractcsProgbufsize]# |progbufsize|	Size of the Program Buffer, in 32-bit words. Valid sizes are 0 - 16.	R	Preset
[dmAbstractcsBusy]# |busy|	0 (ready): There is no abstract command currently being executed. 1 (busy): An abstract command is currently being executed. This bit is set as soon as is written, and is not cleared until that command has completed.	R	0

Field	Description	Access	Reset
[dmAbstractcsRelaxedpriv] # |relaxedpriv|	This optional bit controls whether program buffer and abstract memory accesses are performed with the exact and full set of permission checks that apply based on the current architectural state of the hart performing the access, or with a relaxed set of permission checks (e.g. PMP restrictions are ignored). The details of the latter are implementation-specific. 0 (full checks): Full permission checks apply. 1 (relaxed checks): Relaxed permission checks apply.	WARL	Preset

Field	Description	Access	Reset
[dmAbstractcsCmderr]# |cmderr|	Gets set if an abstract command fails. The bits in this field remain set until they are cleared by writing 1 to them. No abstract command is started until the value is reset to 0. This field only contains a valid value if is 0. 0 (none): No error. 1 (busy): An abstract command was executing while , , or was written, or when one of the `data` or `progbuf` registers was read or written. This status is only written if contains 0. 2 (not supported): The command in is not supported. It may be supported with different options set, but it will not be supported at a later time when the hart or system state are different. 3 (exception): An exception occurred while executing the command (e.g. while executing the Program Buffer). 4 (halt/resume): The abstract command couldn't execute because the hart wasn't in the required state (running/halted), or unavailable. 5 (bus): The abstract command failed due to a bus error (e.g. alignment, access size, or timeout). 6 (reserved): Reserved for future use. 7 (other): The command failed for another reason.	R/W1C	0

Field	Description	Access	Reset
|datacount|	Number of `data` registers that are implemented as part of the abstract command interface. Valid sizes are 1 – 12.	R	Preset

3.14.7. Abstract Command (`command`, at 0x17)

[dmCommand]# Writes to this register cause the corresponding abstract command to be executed.

Writing this register while an abstract command is executing causes to become 1 (busy) once the command completes (busy becomes 0).

If is non-zero, writes to this register are ignored.

inhibits starting a new command to accommodate debuggers that, for performance reasons, send several commands to be executed in a row without checking in between. They can safely do so and check at the end without worrying that one command failed but then a later command (which might have depended on the previous one succeeding) passed.

31	24	23	0
latexmath:[$	cmdtype	$]	
latexmath:[$	control	$]	
8		24	

Field	Description	Access	Reset
Continued on next page			
[dmCommandCmdtype]# |cmdtype|	The type determines the overall functionality of this abstract command.	WARZ	0
|control|	This field is interpreted in a command-specific manner, described for each abstract command.	WARZ	0

3.14.8. Abstract Command Autoexec (`abstractauto`, at 0x18)

[dmAbstractauto]# This register is optional. Including it allows more efficient burst accesses. A debugger can detect whether it is supported by setting bits and reading them back.

If this register is implemented then bits corresponding to implemented progbuf and data registers must be writable. Other bits must be hard-wired to 0.

If this register is written while an abstract command is executing then the write is ignored and becomes 1 (busy) once the command completes (busy becomes 0).

31	16	15	12	11	0
latexmath:[$	autoexecprogbuf	$]		latexmath:[$	0
$]		latexmath:[$	autoexecdata	$]	

31	16	15	12	11	0
16		4		12	

Field	Description	Access	Reset
Continued on next page			
[dmAbstractautoAutoexecprogbuf]# |autoexecprogbuf|	When a bit in this field is 1, read or write accesses to the corresponding `progbuf` word cause the DM to act as if the current value in was written there again after the access to `progbuf` completes.	WARL	0
|autoexecdata|	When a bit in this field is 1, read or write accesses to the corresponding `data` word cause the DM to act as if the current value in was written there again after the access to `data` completes.	WARL	0

3.14.9. Configuration Structure Pointer 0 (`confstrptr0`, at 0x19)

[dmConfstrptrZero]# When is set, reading this register returns bits 31:0 of the configuration structure pointer. Reading the other `confstrptr` registers returns the upper bits of the address.

When system bus access is implemented, this must be an address that can be used with the System Bus Access module. Otherwise, this must be an address that can be used to access the configuration structure from the hart with ID 0.

If is 0, then the `confstrptr` registers hold identifier information which is not further specified in this document.

The configuration structure itself is a data structure of the same format as the data structure pointed to by mconfigptr as described in the Privileged Spec.

This entire register is read-only.

31	0
latexmath:[$	addr
$]	
32	

3.14.10. Configuration Structure Pointer 1 (`confstrptr1`, at 0x1a)

[dmConfstrptrOne]# When is set, reading this register returns bits 63:32 of the configuration structure pointer. See for more details.

This entire register is read-only.

31	0
latexmath:[$	addr
$]	
32	

3.14.11. Configuration Structure Pointer 2 (`confstrptr2`, at 0x1b)

[dmConfstrptrTwo]# When is set, reading this register returns bits 95:64 of the configuration structure pointer. See for more details.

This entire register is read-only.

31	0
latexmath:[$	addr
$]	
32	

3.14.12. Configuration Structure Pointer 3 (`confstrptr3`, at 0x1c)

[dmConfstrptrThree]# When is set, reading this register returns bits 127:96 of the configuration structure pointer. See for more details.

This entire register is read-only.

31	0
latexmath:[$	addr
$]	
32	

3.14.13. Next Debug Module (`nextdm`, at 0x1d)

[dmNextdm]# If there is more than one DM accessible on this DMI, this register contains the base address of the next one in the chain, or 0 if this is the last one in the chain.

This entire register is read-only.

31	0
latexmath:[$	addr
$]	
32	

3.14.14. Abstract Data 0 (`data0`, at 0x04)

[dmDataZero]# through may be Message Registers, whose behavior is described in Section #sec:mr. These registers may be read or changed by abstract commands. indicates how many of them are implemented, starting at , counting up. Table #tab:datareg shows how abstract commands use these registers.

Accessing these registers while an abstract command is executing causes to be set to 1 (busy) if it is 0.

Attempts to write them while is set does not change their value.

The values in these registers might not be preserved after an abstract command is executed. The only guarantees on their contents are the ones offered by the command in question. If the command fails, no assumptions can be made about the contents of these registers.

31	0
latexmath:[$	data
$]	
32	

3.14.15. Program Buffer 0 (`progbuf0`, at 0x20)

[dmProgbufZero]# through must provide write access to the optional program buffer. It may also be possible for the debugger to read from the program buffer through these registers. If reading is not supported, then all reads return 0.

indicates how many `progbuf` registers are implemented starting at , counting up.

Accessing these registers while an abstract command is executing causes to be set to 1 (busy) if it is 0.

Attempts to write them while is set does not change their value.

31	0
latexmath:[$	data
$]	
32	

3.14.16. Authentication Data (`authdata`, at 0x30)

[dmAuthdata]# This register serves as a 32-bit serial port to/from the authentication module.

When is clear, the debugger can communicate with the authentication module by reading or writing this register. There is no separate mechanism to signal overflow/underflow.

31	0
latexmath:[$	data
$]	
32	

3.14.17. Debug Module Control and Status 2 (`dmcs2`, at 0x32)

[dmDmcsTwo]# This register contains DM control and status bits that didn't easily fit in and . All are optional.

If halt groups are not implemented, then will always be 0 when is 0.

If resume groups are not implemented, then will remain 0 even after 1 is written there.

The DM external triggers available to add to halt groups may be the same as or distinct from the DM external triggers available to add to resume groups.

31	12	11		10	7	6	2	1		0	
latexmath:[$	0	$]		latexmath:[$	grouptype	$]		latexmath:[$	dmexttrigger	$]	
latexmath:[$	group	$]		latexmath:[$	hgwrite	$]		latexmath:[$	hgselect	$]	
20		1		4		5		1		1	

Field	Description	Access	Reset
Continued on next page			
[dmDmcsTwoGrouptype]# |grouptype|	0 (halt): The remaining fields in this register configure halt groups. 1 (resume): The remaining fields in this register configure resume groups.	WARL	0
[dmDmcsTwoDmexttrigger]# |dmexttrigger|	This field contains the currently selected DM external trigger. If a non-existent trigger value is written here, the hardware will change it to a valid one or 0 if no DM external triggers exist.	WARL	0
[dmDmcsTwoGroup]# |group|	When is 0, contains the group of the hart specified by . When is 1, contains the group of the DM external trigger selected by . The value written to this field is ignored unless is also written 1. Group numbers are contiguous starting at 0, with the highest number being implementation-dependent, and possibly different between different group types. Debuggers should read back this field after writing to confirm they are using a hart group that is supported. If groups aren't implemented, then this entire field is 0.	WARL	preset

Field	Description	Access	Reset
[dmDmcsTwoHgwrite]# |hgwrite|	When 1 is written and is 0, for every selected hart the DM will change its group to the value written to , if the hardware supports that group for that hart. Implementations may also change the group of a minimal set of unselected harts in the same way, if that is necessary due to a hardware limitation. When 1 is written and is 1, the DM will change the group of the DM external trigger selected by to the value written to , if the hardware supports that group for that trigger. Writing 0 has no effect.	W1	-
|hgselect|	0 (harts): Operate on harts. 1 (triggers): Operate on DM external triggers. If there are no DM external triggers, this field must be tied to 0.	WARL	0

3.14.18. Halt Summary 0 (`haltsum0`, at 0x40)

[dmHaltsumZero]# Each bit in this read-only register indicates whether one specific hart is halted or not. Unavailable/nonexistent harts are not considered to be halted.

This register might not be present if fewer than 2 harts are connected to this DM.

The LSB reflects the halt status of hart \{hartsel[19:5],5'h0}, and the MSB reflects halt status of hart \{hartsel[19:5],5'h1f}.

This entire register is read-only.

31	0
latexmath:[$	haltsum0
$]	
32	

3.14.19. Halt Summary 1 (`haltsum1`, at 0x13)

[dmHaltsumOne]# Each bit in this read-only register indicates whether any of a group of harts is halted or not. Unavailable/nonexistent harts are not considered to be halted.

This register might not be present if fewer than 33 harts are connected to this DM.

The LSB reflects the halt status of harts \{hartsel[19:10],10'h0} through \{hartsel[19:10],10'h1f}. The MSB reflects the halt status of harts \{hartsel[19:10],10'h3e0} through \{hartsel[19:10],10'h3ff}.

This entire register is read-only.

31	0
latexmath:[$	haltsum1
$]	
32	

3.14.20. Halt Summary 2 (`haltsum2`, at 0x34)

[dmHaltsumTwo]# Each bit in this read-only register indicates whether any of a group of harts is halted or not. Unavailable/nonexistent harts are not considered to be halted.

This register might not be present if fewer than 1025 harts are connected to this DM.

The LSB reflects the halt status of harts \{hartsel[19:15],15'h0} through \{hartsel[19:15],15'h3ff}. The MSB reflects the halt status of harts \{hartsel[19:15],15'h7c00} through \{hartsel[19:15],15'h7fff}.

This entire register is read-only.

31	0
latexmath:[$	haltsum2
$]	
32	

3.14.21. Halt Summary 3 (`haltsum3`, at 0x35)

[dmHaltsumThree]# Each bit in this read-only register indicates whether any of a group of harts is halted or not. Unavailable/nonexistent harts are not considered to be halted.

This register might not be present if fewer than 32769 harts are connected to this DM.

The LSB reflects the halt status of harts 20'h0 through 20'h7fff. The MSB reflects the halt status of harts 20'hf8000 through 20'hfffff.

This entire register is read-only.

31	0
latexmath:[$	haltsum3
$]	
32	

3.14.22. System Bus Access Control and Status (`sbcs`, at 0x38)

[dmSbcs]#

31	29	28	23	22		21		20	
latexmath :[$	sbversion	$]		latexmath :[$	0	$]		latexmath :[$	sbbusyerr or
$]		latexmath :[$	sbbusy	$]		latexmath :[$	sbreadona ddr	$]	
3		6		1		1		1	

19	17	16		15		14	12	11	5
latexmath :[$	sbaccess	$]		latexmath :[$	sbautoinc rement	$]		latexmath :[$	sbreadond ata
$]		latexmath :[$	sberror	$]		latexmath :[$	sbasize	$]	
3		1		1		3		7	

4		3		2		1		0	
latexmath :[$	sbaccess12 8	$]		latexmath :[$	sbaccess6 4	$]		latexmath :[$	sbaccess3 2
$]		latexmath :[$	sbaccess1 6	$]		latexmath :[$	sbaccess8	$]	
1		1		1		1		1	

Field	Description	Access	Reset
Continued on next page			
[dmSbcsSbversion]# |sbversion|	0 (legacy): The System Bus interface conforms to mainline drafts of this spec older than 1 January, 2018. 1 (1.0): The System Bus interface conforms to this version of the spec. Other values are reserved for future versions.	R	1
[dmSbcsSbbusyerror]# |sbbusyerror|	Set when the debugger attempts to read data while a read is in progress, or when the debugger initiates a new access while one is already in progress (while is set). It remains set until it's explicitly cleared by the debugger. While this field is set, no more system bus accesses can be initiated by the Debug Module.	R/W1C	0

Field	Description	Access	Reset
[dmSbcsSbbusy]# |sbbusy|	When 1, indicates the system bus manager is busy. (Whether the system bus itself is busy is related, but not the same thing.) This bit goes high immediately when a read or write is requested for any reason, and does not go low until the access is fully completed. Writes to while is high result in undefined behavior. A debugger must not write to until it reads as 0.	R	0
[dmSbcsSbreadonaddr]# |sbreadonaddr|	When 1, every write to automatically triggers a system bus read at the new address.	R/W	0
[dmSbcsSbaccess]# |sbaccess|	Select the access size to use for system bus accesses. 0 (8bit): 8-bit 1 (16bit): 16-bit 2 (32bit): 32-bit 3 (64bit): 64-bit 4 (128bit): 128-bit If has an unsupported value when the DM starts a bus access, the access is not performed and is set to 4.	R/W	2
[dmSbcsSbautoincrement]# |sbautoincrement|	When 1, `sbaddress` is incremented by the access size (in bytes) selected in after every system bus access.	R/W	0
[dmSbcsSbreadondata]# |sbreadondata|	When 1, every read from automatically triggers a system bus read at the (possibly auto-incremented) address.	R/W	0

Field	Description	Access	Reset
[dmSbcsSberror]# |sberror|	When the Debug Module's system bus manager encounters an error, this field gets set. The bits in this field remain set until they are cleared by writing 1 to them. While this field is non-zero, no more system bus accesses can be initiated by the Debug Module. An implementation may report `Other" (7) for any error condition. 0 (none): There was no bus error. 1 (timeout): There was a timeout. 2 (address): A bad address was accessed. 3 (alignment): There was an alignment error. 4 (size): An access of unsupported size was requested. 7 (other): Other.	R/W1C	0
[dmSbcsSbasize]# |sbasize|	Width of system bus addresses in bits. (0 indicates there is no bus access support.)	R	Preset
[dmSbcsSbaccessOneTwentyeight]# |sbaccess128|	1 when 128-bit system bus accesses are supported.	R	Preset
[dmSbcsSbaccessSixtyfour]# |sbaccess64|	1 when 64-bit system bus accesses are supported.	R	Preset
[dmSbcsSbaccessThirtytwo]# |sbaccess32|	1 when 32-bit system bus accesses are supported.	R	Preset
[dmSbcsSbaccessSixteen]# |sbaccess16|	1 when 16-bit system bus accesses are supported.	R	Preset
|sbaccess8|	1 when 8-bit system bus accesses are supported.	R	Preset

3.14.23. System Bus Address 31:0 (`sbaddress0`, at 0x39)

[dmSbaddressZero]# If is 0, then this register is not present.

When the system bus manager is busy, writes to this register will set and don't do anything else.

If is 0, is 0, and is set then writes to this register start the following:

Set .

Perform a bus read from the new value of `sbaddress`.

If the read succeeded and is set, increment `sbaddress`.

Clear .

31	0
latexmath:[$	address
$]	
32	

Field	Description	Access	Reset
Continued on next page			
|address|	Accesses bits 31:0 of the physical address in `sbaddress`.	R/W	0

3.14.24. System Bus Address 63:32 (`sbaddress1`, at 0x3a)

[dmSbaddressOne]# If is less than 33, then this register is not present.

When the system bus manager is busy, writes to this register will set and don't do anything else.

31	0
latexmath:[$	address
$]	
32	

Field	Description	Access	Reset
Continued on next page			
|address|	Accesses bits 63:32 of the physical address in `sbaddress` (if the system address bus is that wide).	R/W	0

3.14.25. System Bus Address 95:64 (`sbaddress2`, at 0x3b)

[dmSbaddressTwo]# If is less than 65, then this register is not present.

When the system bus manager is busy, writes to this register will set and don't do anything else.

31	0
latexmath:[$	address
$]	
32	

Field	Description	Access	Reset
Continued on next page			
|address|	Accesses bits 95:64 of the physical address in `sbaddress` (if the system address bus is that wide).	R/W	0

3.14.26. System Bus Address 127:96 (`sbaddress3`, at 0x37)

[dmSbaddressThree]# If is less than 97, then this register is not present.

When the system bus manager is busy, writes to this register will set and don't do anything else.

31	0
latexmath:[$	address
$]	
32	

Field	Description	Access	Reset
Continued on next page			
|address|	Accesses bits 127:96 of the physical address in `sbaddress` (if the system address bus is that wide).	R/W	0

3.14.27. System Bus Data 31:0 (`sbdata0`, at 0x3c)

[dmSbdataZero]# If all of the `sbaccess` bits in are 0, then this register is not present.

Any successful system bus read updates `sbdata`. If the width of the read access is less than the width of `sbdata`, the contents of the remaining high bits may take on any value.

If either or isn't 0 then accesses do nothing.

If the bus manager is busy then accesses set , and don't do anything else.

Writes to this register start the following:

Set .

Perform a bus write of the new value of `sbdata` to `sbaddress`.

If the write succeeded and is set, increment `sbaddress`.

Clear .

Reads from this register start the following:

``Return'' the data.

Set .

If is set:

Perform a system bus read from the address contained in `sbaddress`, placing the result in `sbdata`.

If is set and the read was successful, increment `sbaddress`.

Clear .

Only has this behavior. The other `sbdata` registers have no side effects. On systems that have buses wider than 32 bits, a debugger should access after accessing the other `sbdata` registers.

31	0
latexmath:[$	data
$]	
32	

Field	Description	Access	Reset
Continued on next page			
|data|	Accesses bits 31:0 of `sbdata`.	R/W	0

3.14.28. System Bus Data 63:32 (`sbdata1`, at 0x3d)

[dmSbdataOne]# If and are 0, then this register is not present.

If the bus manager is busy then accesses set , and don't do anything else.

31	0
latexmath:[$	data
$]	
32	

Field	Description	Access	Reset
Continued on next page			
|data|	Accesses bits 63:32 of `sbdata` (if the system bus is that wide).	R/W	0

3.14.29. System Bus Data 95:64 (`sbdata2`, at 0x3e)

[dmSbdataTwo]# This register only exists if is 1.

If the bus manager is busy then accesses set , and don't do anything else.

31	0
latexmath:[$	data
$]	
32	

Field	Description	Access	Reset
Continued on next page			
|data|	Accesses bits 95:64 of `sbdata` (if the system bus is that wide).	R/W	0

3.14.30. System Bus Data 127:96 (`sbdata3`, at 0x3f)

[dmSbdataThree]# This register only exists if is 1.

If the bus manager is busy then accesses set , and don't do anything else.

31	0
latexmath:[$	data
$]	
32	

Field	Description	Access	Reset
Continued on next page			
|data|	Accesses bits 127:96 of `sbdata` (if the system bus is that wide).	R/W	0

3.14.31. Custom Features (`custom`, at 0x1f)

[dmCustom]# This optional register may be used for non-standard features. Future version of the debug spec will not use this address.

3.14.32. Custom Features 0 (`custom0`, at 0x70)

[dmCustomZero]# The optional through registers may be used for non-standard features. Future versions of the debug spec will not use these addresses.

Chapter 4. Sdext (ISA Extension)

This chapter describes the Sdext ISA extension. It must be implemented to make external debug work, and is only useful in conjunction with external debug.

Modifications to the RISC-V core to support debug are kept to a minimum. There is a special execution mode (Debug Mode) and a few extra CSRs. The DM takes care of the rest.

In order to be compatible with this specification an implementation must implement everything described in this chapter that is not explicitly listed as optional.

If Sdext is implemented and Sdtrig is not implemented, then accessing any of the Sdtrig CSRs must raise an illegal instruction exception.

4.1. Debug Mode

Debug Mode is a special processor mode used only when a hart is halted for external debugging. Because the hart is halted, there is no forward progress in the normal instruction stream. How Debug Mode is implemented is not specified here.

When executing code due to an abstract command, the hart stays in Debug Mode and the following apply:

All implemented instructions operate just as they do in M-mode, unless an exception is mentioned in this list.

All operations are executed with machine mode privilege, except that additional Debug Mode CSRs are accessible and in may be ignored according to . Full permission checks, or a relaxed set of permission checks, will apply according to .

All interrupts (including NMI) are masked.

Traps don't take place. Instead, they end execution of the program buffer and the hart remains in Debug Mode. Because they do not trap to M-mode, they do not update registers such as , `mepc`, `mcause`, ` mtval`, `mtval2`, and `mtinst`. The same is true for the equivalent privileged registers that are updated when trapping to other modes. Registers that may be updated as part of execution before the exception are allowed to be updated. For example, vector load/store instructions which raise exceptions may partially update the destination register and set `vstart` appropriately.

Triggers don't match or fire.

If is 0 then counters continue. If it is 1 then counters are stopped.

If is 0 then continues to update. If it is 1 then will not update. It will resynchronize with after leaving Debug Mode.

Instructions that place the hart into a stalled state act as a `nop`. This includes `wfi`, `wrs.sto`, and `wrs.nto`.

Almost all instructions that change the privilege mode have behavior. This includes `ecall`, `mret`, `sret`, and `uret`. (To change the privilege mode, the debugger can write and in). The only exception is `ebreak`, which ends execution of the Program Buffer when executed.

All control transfer instructions may act as illegal instructions if their destination is in the Program Buffer. If one such instruction acts as an illegal instruction, all such instructions must act as illegal instructions.

All control transfer instructions may act as illegal instructions if their destination is outside the Program Buffer. If one such instruction acts as an illegal instruction, all such instructions must act as illegal instructions.

Instructions that depend on the value of the PC (e.g. `auipc`) may act as illegal instructions.

Effective XLEN is DXLEN.

Forward progress is guaranteed.

When , the external debugger can set MPRV and MPP appropriately to have hardware perform memory accesses with the appropriate endianness, address translation, permission checks, and PMP/PMA checks (subject to). This is also the only way to access all of physical memory when 34-bit physical addresses are supported on a Sv32 hart. If hardware ties to 0 then the external debugger is expected to simulate all the effects of MPRV, including any extensions that affect memory accesses. For these reasons it is recommended to tie to 1.

4.2. Load-Reserved/Store-Conditional Instructions

The reservation registered by an `lr` instruction on a memory address may be lost when entering Debug Mode or while in Debug Mode. This means that there may be no forward progress if Debug Mode is entered between `lr` and `sc` pairs.

This is a behavior that debug users must be aware of. If they have a breakpoint set between a `lr` and `sc` pair, or are stepping through such code, the `sc` may never succeed. Fortunately in general use there will be very few instructions in such a sequence, and anybody debugging it will quickly notice that the reservation is not occurring. The solution in that case is to set a breakpoint on the first instruction after the `sc` and run to it. A higher level debugger may choose to automate this.

4.3. Wait for Interrupt Instruction

If halt is requested while `wfi` is executing, then the hart must leave the stalled state, completing this instruction's execution, and then enter Debug Mode.

4.4. Wait-on-Reservation-Set Instructions

If halt is requested while `wrs.sto` or `wrs.nto` is executing, then the hart must leave the stalled state, completing this instruction's execution, and then enter Debug Mode.

4.5. Single Step

4.5.1. Step Bit In Dcsr

This method is only available to external debuggers, and is the preferred way to single step.

An external debugger can cause a halted hart to execute a single instruction or trap and then re-enter

Debug Mode by setting before resuming. If is set when a hart resumes then it will single step, regardless of the reason for resuming.

If control is transferred to a trap handler while executing the instruction, then Debug Mode is re-entered immediately after the PC is changed to the trap handler, and the appropriate `tval` and `cause` registers are updated. In this case none of the trap handler is executed, and if the cause was a pending interrupt no instructions might be executed at all.

If executing or fetching the instruction causes a trigger to fire with action=1, Debug Mode is re-entered immediately after that trigger has fired. In that case is set to 2 (trigger) instead of 4 (single step). Whether the instruction is executed or not depends on the specific configuration of the trigger.

If the instruction that is executed causes the PC to change to an address where an instruction fetch causes an exception, that exception does not occur until the next time the hart is resumed. Similarly, a trigger at the new address does not fire until the hart actually attempts to execute that instruction.

If the instruction being stepped over would normally stall the hart, then instead the instruction is treated as a `nop`. This includes `wfi`, `wrs.sto`, and `wrs.nto`.

4.5.2. Icount Trigger

Native debuggers won't have access to , but can use the trigger by setting to 1.

This approach does have some limitations:

Interrupts will fire as usual. Debuggers that want to disable interrupts while stepping must disable them by changing , and specially handle instructions that read .

`wfi` instructions are not treated specially and might take a very long time to complete.

This mechanism cleanly supports a system which supports multiple privilege levels, where the OS or a debug stub runs in M-Mode while the program being debugged runs in a less privileged mode. Systems that only support M-Mode can use as well, but count must be able to count several instructions (depending on the software implementation). See Section [nativestep].

4.6. Reset

If the halt signal (driven by the hart's halt request bit in the Debug Module) or are asserted when a hart comes out of reset, the hart must enter Debug Mode before executing any instructions, but after performing any initialization that would usually happen before the first instruction is executed.

4.7. Halt

When a hart halts:

is updated.

and are set to reflect current privilege mode.

is set to the next instruction that should be executed.

If the current instruction can be partially executed and should be restarted to complete, then the

relevant state for that is updated. E.g. if a halt occurs during a partially executed vector instruction, then `vstart` is updated, and is updated to the address of the partially executed instruction. This is analogous to how vector instructions behave for exceptions.

The hart enters Debug Mode.

4.8. Resume

When a hart resumes:

changes to the value stored in .

The current privilege mode and virtualization mode are changed to that specified by and .

If the new privilege mode is less privileged than M-mode, in is cleared.

The hart is no longer in debug mode.

4.9. XLEN

While in Debug Mode, XLEN is DXLEN. It is up to the debugger to determine the XLEN during normal program execution (by looking at) and to clearly communicate this to the user.

4.10. Core Debug Registers

The supported Core Debug Registers must be implemented for each hart that can be debugged. They are CSRs, accessible using the RISC-V `csr` opcodes and optionally also using abstract debug commands.

Attempts to access an unimplemented Core Debug Register raise an illegal instruction exception.

4.11. Virtual Debug Registers

Chapter 5. Sdtrig (ISA Extension)

This chapter describes the Sdtrig ISA extension, which can be implemented independently of functionality described in the other chapters. It consists exclusively of the Trigger Module ™.

Triggers can cause a breakpoint exception, entry into Debug Mode, or a trace action without having to execute a special instruction. This makes them invaluable when debugging code from ROM. They can trigger on execution of instructions at a given memory address, or on the address/data in loads/stores.

If Sdtrig is implemented, the Trigger Module must support at least one trigger. Accessing trigger CSRs that are not used by any of the implemented triggers must result in an illegal instruction exception. M-Mode and Debug Mode accesses to trigger CSRs that are used by any of the implemented triggers must succeed, regardless of the current type of the currently selected trigger.

A trigger matches when the conditions that it specifies (e.g. a load from a specific address) are met. A trigger fires when a trigger that matches performs the action configured for that trigger.

Triggers do not fire while in Debug Mode.

5.1. Enumeration

Each trigger may support a variety of features. A debugger can build a list of all triggers and their features as follows:

Write 0 to . If this results in an illegal instruction exception, then there are no triggers implemented.

Read back and check that it contains the written value. If not, exit the loop.

Read .

If that caused an exception, the debugger must read to discover the type. (If is 0, this trigger doesn't exist. Exit the loop.)

If is 1, this trigger doesn't exist. Exit the loop.

Otherwise, the selected trigger supports the types discovered in .

Repeat, incrementing the value in .

The above algorithm reads back so that implementations which have 2^n triggers only need to implement n bits of .

The algorithm checks and in case the implementation has m bits of but fewer than 2^m triggers.

5.2. Actions

Triggers can be configured to take one of several actions when they fire. Table #tab:action lists all options.

|r|L| Value & Description
& Raise a breakpoint exception. (Used when software wants to use the trigger module without an external debugger attached.) must contain the virtual address of the next instruction that must be

executed to preserve the program flow.
& Enter Debug Mode. must contain the virtual address of the next instruction that must be executed to preserve the program flow.

This action is only legal when the trigger's is 1. Since the `tdata` registers are WARL, hardware should clear the action field whenever the action field is 1, the new value of would be 0, and the new value of the action field would be 1.

This action can only be supported if Sdext is implemented on the hart.
& Trace on, described in the trace specification.
& Trace off, described in the trace specification.
& Trace notify, described in the trace specification.
& Reserved for use by the trace specification.
– 9 & Send a signal to TM external trigger output 0 or 1 (respectively).
other & Reserved for future use.

Actions 8 and 9 are intended to increment custom event counters, but these signals could also be brought to outputs for use by external logic.

5.3. Priority

Table #tab:priority lists the synchronous exceptions from the Privileged Spec, and where the various types of triggers fit in. The first 3 columns come from the Privileged Spec, and the final column shows where triggers fit in. Priorities in the table are separated by horizontal lines, so e.g. etrigger and itrigger have the same priority. If this table contradicts the table in the Privileged Spec, then the latter takes precedence.

This table only applies if triggers are precise. Otherwise triggers will fire some indeterminate time after the event, and the priority is irrelevant. When triggers are chained, the priority is the lowest priority of the triggers in the chain.

|l|p.7in|p2.3in|p2.5in| Priority & Exception Code & Description & Trigger
Highest & 3 & & etrigger
& 3 & & icount
& 3 & & itrigger
& 3 & & mcontrol/mcontrol6 after (on previous instruction)
& 3 & Instruction address breakpoint & mcontrol/mcontrol6 execute address before
& 12, 20, 1 & During instruction address translation: First encountered page fault, guest-page fault, or access fault &
& 1 & With physical address for instruction: Instruction access fault &
& 3 & & mcontrol/mcontrol6 execute data before
& 2 & Illegal instruction &
& 22 & Virtual instruction &
& 0 & Instruction address misaligned &
& 8, 9, 10, 11 & Environment call &
& 3 & Environment break &
& 3 & Load/Store/AMO address breakpoint & mcontrol/mcontrol6 load/store address/data before
& 4, 6 & Optionally: Load/Store/AMO address misaligned &
& 13, 15, 21, 23, 5, 7 & During address translation for an explicit memory access: First encountered page fault, guest-page fault, or access fault &
& 5, 7 & With physical address for an explicit memory access: Load/store/AMO access fault &
& 4, 6 & If not higher priority: Load/store/AMO address misaligned &

Lowest & 3 & & mcontrol/mcontrol6 load data before

When multiple triggers in the same priority fire at once, (if implemented) is set for all of them. If more than one of these triggers has then `tval` is updated in accordance with one of them, but which one is . If one of these triggers has the `enter Debug Mode'' action (1) and another trigger has the` raise a breakpoint exception" action (0), the preferred behavior is to have both actions take place. It is implementation-dependent which of the two happens first. This ensures both that the presence of an external debugger doesn't affect execution and that a trigger set by user code doesn't affect the external debugger. If this is not implemented, then the hart must enter Debug Mode and ignore the breakpoint exception. In the latter case, of the trigger whose action is 0 must still be set, giving a debugger an opportunity to handle this case. What happens with trace actions when triggers with different actions are also firing is left to the trace specification.

5.4. Native Triggers

Triggers can be used for native debugging when . If supported by the hart and desired by the debugger, triggers will often be programmed to have so that when they fire they cause a breakpoint exception to trap to a more privileged mode. That breakpoint exception can either be taken in M-mode or it can be delegated to a less privileged mode. However, it is possible for triggers to fire in the same mode that the resulting exception will be handled in.

In these cases such a trigger may cause a breakpoint exception while already in a trap handler. This might leave the hart unable to resume normal execution because state such as and would be overwritten.

In particular, when :

mcontrol and mcontrol6 triggers with can cause a breakpoint exception that is taken from M-mode to M-mode (regardless of delegation).

mcontrol and mcontrol6 triggers with can cause a breakpoint exception that is taken from S-mode to S-mode if .

mcontrol6 triggers with can cause a breakpoint exception that is taken from VS-mode to VS-mode if and .

icount triggers with can cause a breakpoint exception that is taken from M-mode to M-mode (regardless of delegation).

icount triggers with can cause a breakpoint exception that is taken from S-mode to S-mode if .

icount triggers with can cause a breakpoint exception that is taken from VS-mode to VS-mode if and .

etrigger and itrigger triggers will always be taken from a trap handler before the first instruction of the handler. If etrigger/itrigger is set to trigger on exception/interrupt X and if X is delegated to mode Y then the trigger will cause a breakpoint exception that is taken from mode Y to mode Y unless breakpoint exceptions are delegated to a more privileged mode than Y.

tmexttrigger triggers are asynchronous and may occur in any mode and at any time.

Harts that support triggers with should implement one of the following two solutions to solve the problem of reentrancy:

The hardware prevents triggers with from matching or firing while in M-mode and while in is 0. If then it prevents triggers with from matching or firing while in S-mode and while in is 0. If and then it prevents triggers with from matching or firing while in VS-mode and while in is 0.

and in is implemented. is hard-wired to 0.

The first option has the limitation that interrupts might be disabled at times when a user still might want triggers to fire. It has the benefit that breakpoints are not required to be handled in M-mode.

The second option has the benefit that it only disables triggers during the trap handler, though it requires specific software support for this debug feature in the M-mode trap handlers. It can only work if breakpoints are not delegated to less privileged modes and therefore targets primarily implementations without S-mode.

Because is not accessible to S-mode, the second option can not be extended to accommodate delegation without adding additional S-mode and VS-mode CSRs.

Both options prevent etrigger and itrigger from having any effect on exceptions and interrupts that are handled in M-mode. They also prevent triggering during some initial portion of each handler. Debuggers should use other mechanisms to debug these cases, such as patching the handler or setting a breakpoint on the instruction after is cleared.

5.5. Memory Access Triggers

and both enable triggers on memory accesses. This section describes for both of them how certain corner cases are treated.

5.5.1. A Extension

If the A extension is supported, then triggers on loads/stores treat them as follows:

`lr` instructions are loads.

Successful `sc` instructions are stores.

It is whether failing `sc` instructions are stores or not.

Each AMO instruction is a load for the read portion of the operation. The address is always available to trigger on, although the value loaded might not be, depending on the hardware implementation.

Each AMO instruction is a store for the write portion of the operation. The address is always available to trigger on, although the value stored might not be, depending on the hardware implementation.

If the destination register of any load or AMO is then it is whether a data load trigger will match. Whether data store triggers match on AMOs is .

5.5.2. Combined Accesses

Some instructions lead a hart to perform multiple memory accesses. This includes vector loads and stores, as well as `cm.push` and `cm.pop` instructions. The Trigger Module should match such accesses as if they all happened individually. E.g. a vector load should be treated as if it performed multiple loads of size SEW (selected element width), and `cm.push` should be treated as if it performed multiple stores of size XLEN.

5.5.3. Cache Operations

Cache operations are infrequently performed, and code that uses them can have hard-to-find bugs. For the purposes of debug triggers, two classes of cache operations must match as stores:

Cache operations that enable software to maintain coherence between otherwise non-coherent implicit and explicit memory accesses.

Cache operations that perform block writes of constant data.

Only triggers with and will match. Since cache operations affect multiple addresses, there are multiple possible values to compare against. Implementations must implement one of the following options. From most desirable to least desirable, they are:

Every address from the effective address rounded down to the nearest cache block boundary (inclusive) to the effective address rounded up to the nearest cache block boundary (exclusive) is a compare value.

The effective address rounded down to the nearest cache block boundary is a compare value.

The effective address of the instruction is a compare value.

Cache operations encoded as HINTs do not match debug triggers.

The above language intends to capture the trigger behavior with respect to the cache operations to be introduced in a forthcoming I/D consistency extension.

For RISC-V Base Cache Management Operation ISA Extensions 1.0.1, this means the following:

, , and match as if they are stores because they affect consistency.

matches as if it is a store because it performs a block write of constant data.

The prefetch instructions don't match at all.

5.6. Multiple State Change Instructions

An instruction that performs multiple architectural state changes (e.g., register updates and/or memory accesses) might cause a trigger to fire at an intermediate point in its execution. As a result, architectural state changes up to that point might have been performed, while subsequent state changes, starting from the event that activated the trigger, might not have been. The definition of such an instruction will specify the order in which architectural state changes take place. Alternatively, it may state that partial execution is not allowed, implying that a mid-execution trigger must prevent any architectural state changes from occurring.

Debuggers won't be aware if an instruction has been partially executed. When they resume execution, they will execute the same instruction once more. Therefore, it's crucial that partially executing the instruction and then executing it again leaves the hart in a state closely resembling the state it would have been in if the instruction had only been executed once.

5.7. Trigger Registers

These registers are CSRs, accessible using the RISC-V `csr` opcodes and optionally also using abstract debug commands.

Almost all trigger functionality is optional. All `tdata` registers follow write-any-read-legal semantics. If a debugger writes an unsupported configuration, the register will read back a value that is supported (which may simply be a disabled trigger). This means that a debugger must always read back values it writes to `tdata` registers, unless it already knows already what is supported. Writes to one `tdata` register must not modify the contents of other `tdata` registers, nor the configuration of any trigger besides the one that is currently selected.

The combination of these rules means that a debugger cannot simply set a trigger by writing , then , etc. The current value of might not be legal with the new value of . To help with this situation, it is guaranteed that writing 0 to disables the trigger, and leaves it in a state where and can be written with any value that makes sense for any trigger type supported by this trigger.

As a result, a debugger can write any supported trigger as follows:

Write 0 to . (This will result in containing a non-zero value, since the register is .)

Write desired values to and .

Write desired value to .

Code that restores CSR context of triggers that might be configured to fire in the current privilege mode must use this same sequence to restore the triggers. This avoids the problem of a partially written trigger firing at a different time than is expected.

Attempts to access an unimplemented Trigger Register raise an illegal instruction exception.

Chapter 6. JTAG Debug Transport Module

This Debug Transport Module is based around a normal JTAG Test Access Port (TAP). The JTAG TAP allows access to arbitrary JTAG registers by first selecting one using the JTAG instruction register (IR), and then accessing it through the JTAG data register (DR).

6.1. JTAG Background

JTAG refers to IEEE Std 1149.1-2013. It is a standard that defines test logic that can be included in an integrated circuit to test the interconnections between integrated circuits, test the integrated circuit itself, and observe or modify circuit activity during the component's normal operation. This specification uses the latter functionality. The JTAG standard defines a Test Access Port (TAP) that can be used to read and write a few custom registers, which can be used to communicate with debug hardware in a component.

6.2. JTAG DTM Registers

JTAG TAPs used as a DTM must have an IR of at least 5 bits. When the TAP is reset, IR must default to 00001, selecting the IDCODE instruction. A full list of JTAG registers along with their encoding is in Table #dtmTable:jtagregisters. If the IR actually has more than 5 bits, then the encodings in Table #dtmTable:jtagregisters should be extended with 0's in their most significant bits, except for the 0x1f encoding of BYPASS, which must be extended with 1's in the most significant bits. The only regular JTAG registers a debugger might use are BYPASS and IDCODE, but this specification leaves IR space for many other standard JTAG instructions. Unimplemented instructions must select the BYPASS register.

6.3. JTAG Connector

6.3.1. Recommended JTAG Connector

To make it easy to acquire debug hardware, this spec recommends a connector that is compatible with the MIPI-10 .05 inch connector specification, as described in MIPI Debug & Trace Connector Recommendations, Version 1.20, 2 July 2021.

The connector has .05 inch spacing, gold-plated male header with .016 inch thick hardened copper or beryllium bronze square posts (SAMTEC FTSH or equivalent). Female connectors are compatible $20\mu m$ gold connectors.

Viewing the male header from above (the pins pointing at your eye), a target's connector looks as it does in Table #tab:mipiten[1]. The function of each pin is described in Table #tab:pinout.

VREF DEBUG	1	2	TMS
GND	3	4	TCK
GND	5	6	TDO
GND or KEY	7	8	TDI
GND	9	10	nRESET

Table 3. MIPI 10-pin JTAG + nRESET Connector Diagram

|l|c|L| Essential & GND & Connected to ground.
& TCK & JTAG TCK signal, driven by the debug adapter.
& TDI & JTAG TDI signal, driven by the debug adapter.
& TDO & JTAG TDO signal, driven by the target.
& TMS & JTAG TMS signal, driven by the debug adapter.
& VREF DEBUG & Reference voltage for logic high.
Recommended & nRESET & Open drain active low reset signal, usually driven by the debug adapter. The signal may be used bi-directional to drive or sense the target reset signal.

Asserting reset should reset any RISC-V cores as well as any other peripherals on the PCB. It should not reset the debug logic. This pin is optional but strongly encouraged.

nRESET should never be connected to the TAP reset, otherwise the debugger might not be able to debug through a reset to discover the cause of a crash or to maintain execution control after the reset.
& KEY & This pin may be cut on the male and plugged on the female header to ensure the header is always plugged in correctly. It is, however, recommended to use this pin as an additional ground, to allow for fastest TCK speeds. A shrouded connector should be used to prevent the cable from being plugged in incorrectly.
Advanced & EXT & Reserved for custom use. Could be an input or an output.
& TRIGIN & Not used by this specification, to be driven by debug adapter. (Can be used for extended functions like UART or boot mode selection by some debug adapters).
& TRIGOUT & Not used by this specification, driven by the target.
Specialized & nTRST & Test reset, driven by the debug adapter. Asserting nTRST initializes the JTAG DTM asynchronously. It is used in systems where the JTAG DTM is not ready to be used after a normal power up. This signal is sometimes called TRST*.
Legacy & RTCK & Return test clock, driven by the target. A target may relay the TCK signal here once it has processed it, allowing a debugger to adjust its TCK frequency in response.

This signal should only be used to support legacy components that rely on this functionality.
& nTRST_PD & Test reset pull-down, driven by the debug adapter. Same function as nTRST, but with pull-down resistor on target.

This signal should only be used to support legacy components that rely on this functionality.

If a hardware platform requires nTRST then it is permissible to reuse the nRESET pin as the nTRST signal, resulting in a MIPI 10-pin JTAG
nTRST connector.

6.3.2. Alternate JTAG Connector

The MIPI-10 connector should provide plenty of signals for all modern hardware. If a design does need legacy JTAG signals, then the MIPI-20 connector should be used. Pins whose functionality isn't needed may be left unconnected.

Its physical connector is virtually identical to MIPI-10, except that it's twice as long, supporting twice as many pins. Its pinout is shown in Table #tab:mipitwenty[2]. The function of each pin is described in Table #tab:pinout.

VREF DEBUG	1	2	TMS
GND	3	4	TCK
GND	5	6	TDO

VREF DEBUG	1	2	TMS
GND or KEY	7	8	TDI
GND	9	10	nRESET
GND	11	12	GND or RTCK
GND	13	14	NC or nTRST_PD
GND	15	16	nTRST or NC
GND	17	18	TRIGIN or NC
GND	19	20	TRIGOUT or GND

Table 4. MIPI 20-pin JTAG Connector Diagram

6.4. cJTAG

This spec does not have specific recommendations on how to use the cJTAG protocol.

When implementing cJTAG access to a JTAG DTM, the MIPI 10-pin Narrow JTAG connector should be used. Pins whose functionality isn't needed may be left unconnected.

Viewing the male header from above (the pins pointing at your eye), a target's connector looks as it does in Table #tab:mipicjtag[3].

VREF DEBUG	1	2	TMSC
GND	3	4	TCKC
GND	5	6	EXT or NC
GND or KEY	7	8	NC or nTRST_PD
GND	9	10	nRESET

Table 5. MIPI 10-pin Narrow JTAG Connector Diagram

Chapter 7. Hardware Implementations

Below are two possible implementations. A designer could choose one, mix and match, or come up with their own design.

7.1. Abstract Command Based

Halting happens by stalling the hart execution pipeline.

Muxes on the register file(s) allow for accessing GPRs and CSRs using the Access Register abstract command.

Memory is accessed using the Abstract Access Memory command or through System Bus Access.

This implementation could allow a debugger to collect information from the hart even when that hart is unable to execute instructions.

7.2. Execution Based

This implementation only implements the Access Register abstract command for GPRs on a halted hart, and relies on the Program Buffer for all other operations. It uses the hart's existing pipeline and ability to execute from arbitrary memory locations to avoid modifications to a hart's datapath.

When the halt request bit is set, the Debug Module raises a special interrupt to the selected harts. This interrupt causes each hart to enter Debug Mode and jump to a defined memory region that is serviced by the DM and is only accessible to the harts in Debug Mode. Accesses to this memory should be uncached to avoid side effects from debugging operations. When taking this jump, is saved to and is updated in . This jump is similar to a trap but it is not architecturally considered a trap, so for instance doesn't count as a trap for trigger behavior.

The code in the Debug Module causes the hart to execute a `park loop." In the park loop the hart writes its to a memory location within the Debug Module to indicate that it is halted. To allow the DM to individually control one out of several halted harts, each hart polls for flags in a DM-controlled memory location to determine whether the debugger wants it to execute the Program Buffer or perform a resume.

To execute an abstract command, the DM first populates some internal words of program buffer according to . When is set, the DM populates these words with `lw <gpr>, 0x400(zero)` or `sw 0x400(zero), <gpr>`. 64- and 128-bit accesses use `ld`/`sd` and `lq`/`sq` respectively. If is not set, the DM populates these instructions as `nop`s. If is set, execution continues to the debugger-controlled Program Buffer, otherwise the DM causes a `ebreak` to execute immediately.

When `ebreak` is executed (indicating the end of the Program Buffer code) the hart returns to its park loop. If an exception is encountered, the hart jumps to an address within the Debug Module. The code there causes the hart to write to the Debug Module indicating an exception. Then the hart jumps back to the park loop. The DM infers from the write that there was an exception, and sets appropriately. Typically the hart will execute a `fence` instruction before entering the park loop, to ensure that any effects from the abstract command, such as a write to , take effect before the DM returns to 0.

To resume execution, the debug module sets a flag which causes the hart to execute a `dret`. `dret` is an instruction that only has meaning while in Debug Mode and not executing from the Program Buffer.

Its recommended encoding is 0x7b200073. When `dret` is executed, is restored from and normal execution resumes at the privilege set by and .

etc. are mapped into regular memory at an address relative to with only a 12-bit `imm`. The exact address is an implementation detail that a debugger must not rely on. For example, the `data` registers might be mapped to `0x400`.

For additional flexibility, , etc. are mapped into regular memory immediately preceding , in order to form a contiguous region of memory which can be used for either program execution or data transfer.

The PMP must not disallow fetches, loads, or stores in the address range associated with the Debug Module when the hart is in Debug Mode, regardless of how the PMP is configured. The same is true of PMA. Without this guarantee, the park loop would enter an infinite loop of traps and debug would not be possible.

7.3. Debug Module Interface Signals

As stated in section [dmi] the details of the DMI are left to the system designer. It is quite often the case that only one DTM and one DM is implemented. In this case it might be useful to comply with the signals suggested in table #tab:dmi_signals[1.1], which is the implementation used in the open-source rocket-chip RISC-V core.

The DTM can start a request when the DM sets REQ_READY to 1. When this is the case REQ_OP can be set to 1 for a read or 2 for a write request. The desired address is driven with the REQ_ADDRESS signal. Finally REQ_VALID is set high, indicating to the DM that a valid request is pending.

The DM must respond to a request from the DTM when RSP_READY is high. The status of the response is indicated by the RSP_OP signal (see). The data of the response is driven to RSP_DATA. A pending response is signalled by setting RSP_VALID.

Signal	Width	Source	Description
REQ_VALID	1	DTM	Indicates that a valid request is pending
REQ_READY	1	DM	Indicates that the DM is able to process a request
REQ_ADDRESS		DTM	Requested address
REQ_DATA	32	DTM	Requested data
REQ_OP	2	DTM	Same meaning as the field
RSP_VALID	1	DM	Indicates that a valid respond is pending
RSP_READY	1	DTM	Indicates that the DTM is able to process a respond
RSP_DATA	32	DM	Response data
RSP_OP	2	DM	Same meaning as the field

Table 6. Signals for the suggested DMI between one DTM and one DM

Chapter 8. Debugger Implementation

8.1. C Header File

github.com/riscv/riscv-debug-spec contains instructions for generating a C header file that defines macros for every field in every register/abstract command mentioned in this document.

8.2. External Debugger Implementation

This section details how an external debugger might use the described debug interface to perform some common operations on RISC-V cores using the JTAG DTM described in Section #sec:jtagdtm. All these examples assume a 32-bit core but it should be easy to adapt the examples to 64- or 128-bit cores.

To keep the examples readable, they all assume that everything succeeds, and that they complete faster than the debugger can perform the next access. This will be the case in a typical JTAG setup. However, the debugger must always check the sticky error status bits after performing a sequence of actions. If it sees any that are set, then it should attempt the same actions again, possibly while adding in some delay, or explicit checks for status bits.

8.2.1. Debug Module Interface Access

To read an arbitrary Debug Module register, select , and scan in a value with set to 1, and set to the desired register address. In Update-DR the operation will start, and in Capture-DR its results will be captured into . If the operation didn't complete in time, will be 3 and the value in must be ignored. The busy condition must be cleared by writing in , and then the second scan scan must be performed again. This process must be repeated until returns 0. In later operations the debugger should allow for more time between Update-DR and Capture-DR.

To write an arbitrary Debug Bus register, select , and scan in a value with set to 2, and and set to the desired register address and data respectively. From then on everything happens exactly as with a read, except that a write is performed instead of the read.

It should almost never be necessary to scan IR, avoiding a big part of the inefficiency in typical JTAG use.

8.2.2. Checking for Halted Harts

A user will want to know as quickly as possible when a hart is halted (e.g. due to a breakpoint). To efficiently determine which harts are halted when there are many harts, the debugger uses the `haltsum` registers. Assuming the maximum number of harts exist, first it checks . For each bit set there, it writes , and checks . This process repeats through and . Depending on how many harts exist, the process should start at one of the lower `haltsum` registers.

8.2.3. Halting

To halt one or more harts, the debugger selects them, sets , and then waits for to indicate the harts are halted. Then it can clear to 0, or leave it high to catch a hart that resets while halted.

8.2.4. Running

First, the debugger should restore any registers that it has overwritten. Then it can let the selected harts run by setting . Once is set, the debugger knows the selected harts have resumed. Harts might halt very quickly after resuming (e.g. by hitting a software breakpoint) so the debugger cannot use /to check whether the hart resumed.

8.2.5. Single Step

Using the hardware single step feature is almost the same as regular running. The debugger just sets in before letting the hart run. The hart behaves exactly as in the running case, except that interrupts may be disabled (depending on) and it only fetches and executes a single instruction before re-entering Debug Mode.

8.2.6. Accessing Registers

8.2.6.1. Using Abstract Command

Read using abstract command:

Op	Address	Value	Comment
Write		= 2, , = 0x1008	Read
Read		-	Returns value that was in

Write using abstract command:

Op	Address	Value	Comment
Write		new value	
Write		= 2, , , = 0x300	Write

8.2.6.2. Using Program Buffer

Abstract commands are used to exchange data with GPRs. Using this mechanism, other registers can be accessed by moving their value into/out of GPRs.

Write using program buffer:

Op	Address	Value	Comment
Write		`csrw s0, MSTATUS`	
Write	`progbuf1`	`ebreak`	
Write		new value	
Write		= 2, , , , = 0x1008	Write , then execute program buffer

Read using program buffer:

Op	Address	Value	Comment
Write		`fmv.x.s s0, f1`	
Write	`progbuf1`	`ebreak`	

Op	Address	Value	Comment
Write			Execute program buffer
Write		, = 0x1008	read
Read		-	Returns the value that was in

8.2.7. Reading Memory

8.2.7.1. Using System Bus Access

With system bus access, addresses are physical system bus addresses.

Read a word from memory using system bus access:

Op	Address	Value	Comment
Write		= 2,	Setup
Write		address	
Read		-	Value read from memory

Read block of memory using system bus access:

Op	Address	Value	Comment
Write		= 2, , ,	Turn on autoread and autoincrement
Write		address	Writing address triggers read and increment
Read		-	Value read from memory
Read		-	Next value read from memory
...	...	...	...
Write		0	Disable autoread
Read		-	Get last value read from memory.

8.2.7.2. Using Program Buffer

Through the Program Buffer, the hart performs the memory accesses. Addresses are physical or virtual (depending on and other system configuration).

Read a word from memory using program buffer:

Op	Address	Value	Comment
Write		`lw s0, 0(s0)`	
Write	`progbuf1`	`ebreak`	
Write		address	
Write		, , , = 0x1008	Write , then execute program buffer

Op	Address	Value	Comment
Write		= 0x1008	Read
Read		-	Value read from memory

Read block of memory using program buffer:

Op	Address	Value	Comment
Write		`lw s1, 0(s0)`	
Write	`progbuf1`	`addi s0, s0, 4`	
Write	`progbuf2`	`ebreak`	
Write		address	
Write		, , , = 0x1008	Write , then execute program buffer
Write		, = 0x1009	Read , then execute program buffer
Write			Set
Read		-	Get value read from memory, then execute program buffer
Read		-	Get next value read from memory, then execute program buffer
...	...	...	...
Write		0	Clear
Read		-	Get last value read from memory.

8.2.7.3. Using Abstract Memory Access

Abstract memory accesses act as if they are performed by the hart, although the actual implementation may differ.

Read a word from memory using abstract memory access:

Op	Address	Value	Comment
Write		address	
Write		cmdtype=2,	
Read		-	Value read from memory

Read block of memory using abstract memory access:

Op	Address	Value	Comment
Write		1	Re-execute the command when is accessed
Write		address	
Write		cmdtype=2, ,	

Op	Address	Value	Comment
Read		-	Read value, and trigger reading of next address
...	...	...	...
Write		0	Disable auto-exec
Read		-	Get last value read from memory.

8.2.8. Writing Memory

8.2.8.1. Using System Bus Access

With system bus access, addresses are physical system bus addresses.

Write a word to memory using system bus access:

Op	Address	Value	Comment
Write		= 2	Configure access size
Write		address	
Write		value	

Write a block of memory using system bus access:

Op	Address	Value	Comment
Write		= 2,	Turn on autoincrement
Write		address	
Write		value0	
Write		value1	
...	...	...	...
Write		valueN	

8.2.8.2. Using Program Buffer

Through the Program Buffer, the hart performs the memory accesses. Addresses are physical or virtual (depending on and other system configuration).

Write a word to memory using program buffer:

Op	Address	Value	Comment
Write		`sw s1, 0(s0)`	
Write	`progbuf1`	`ebreak`	
Write		address	
Write		, , = 0x1008	Write
Write		value	
Write		, , , = 0x1009	Write , then execute program buffer

Write block of memory using program buffer:

Op	Address	Value	Comment
Write		`sw s1, 0(s0)`	
Write	`progbuf1`	`addi s0, s0, 4`	
Write	`progbuf2`	`ebreak`	
Write		address	
Write		, , = 0x1008	Write
Write		value0	
Write		, , , = 0x1009	Write , then execute program buffer
Write			Set
Write		value1	
...	...	...	...
Write		valueN	
Write		0	Clear

8.2.8.3. Using Abstract Memory Access

Abstract memory accesses act as if they are performed by the hart, although the actual implementation may differ.

Write a word to memory using abstract memory access:

Op	Address	Value	Comment
Write		address	
Write		value	
Write		cmdtype=2, , write=1	

Write a block of memory using abstract memory access:

Op	Address	Value	Comment
Write		address	
Write		value0	
Write		cmdtype=2, , write=1,	
Write		1	Re-execute the command when is accessed
Write		value1	
Write		value2	
...	...	...	...
Write		valueN	
Write		0	Disable auto-exec

8.2.9. Triggers

A debugger can use hardware triggers to halt a hart when a certain event occurs. Below are some examples, but as there is no requirement on the number of features of the triggers implemented by a hart, these examples might not be applicable to all implementations. When a debugger wants to set a trigger, it writes the desired configuration, and then reads back to see if that configuration is supported. All examples assume XLEN=32.

Enter Debug Mode when the instruction at 0x80001234 is executed, to be used as an instruction breakpoint in ROM:

|r|r|L| & 0x6980105c & type=6, dmode=1, action=1, select=0, match=0, m=1, s=1, u=1, vs=1, vu=1, execute=1
& 0x80001234 & address

Enter Debug Mode when performing a load at address 0x80007f80 in M-mode or S-mode or U-mode:

|r|r|L| & 0x68001059 & type=6, dmode=1, action=1, select=0, match=0, m=1, s=1, u=1, load=1
& 0x80007f80 & address

Enter Debug Mode when storing to an address between 0x80007c80 and 0x80007cef (inclusive) in VS-mode or VU-mode when hgatp.VMID=1:

|r|r|L| & 0x69801902 & type=6, dmode=1, action=1, chain=1, select=0, match=2, vs=1, vu=1, store=1
& 0x80007c80 & start address (inclusive)
& 0x03000000 & mhselect=6, mhvalue=0
& 0x69801182 & type=6, dmode=1, action=1, select=0, match=3, vs=1, vu=1, store=1
& 0x80007cf0 & end address (exclusive)
& 0x03000000 & mhselect=6, mhvalue=0

Enter Debug Mode when storing to an address between 0x81230000 and 0x8123ffff (inclusive):

|r|r|L| & 0x698010da & type=6, dmode=1, action=1, select=0, match=1, m=1, s=1, u=1, vs=1, vu=1, store=1
& 0x81237fff & 16 upper bits to match exactly, then 0, then all ones.

Enter Debug Mode when loading from an address between 0x86753090 and 0x8675309f or between 0x96753090 and 0x9675309f (inclusive):

|r|r|L| & 0x69801a59 & type=6, dmode=1, action=1, chain=1, match=4, m=1, s=1, u=1, vs=1, vu=1, load=1
& 0xfff03090 & Mask for low half, then match for low half
& 0x698012d9 & type=6, dmode=1, action=1, match=5, m=1, s=1, u=1, vs=1, vu=1, load=1
& 0xefff8675 & Mask for high half, then match for high half

8.2.10. Handling Exceptions

Generally the debugger can avoid exceptions by being careful with the programs it writes. Sometimes they are unavoidable though, e.g. if the user asks to access memory or a CSR that is not implemented. A typical debugger will not know enough about the hardware platform to know what's going to happen, and must attempt the access to determine the outcome.

When an exception occurs while executing the Program Buffer, becomes set. The debugger can check this field to see whether a program encountered an exception. If there was an exception, it's left to the

debugger to know what must have caused it.

8.2.11. Quick Access

There are a variety of instructions to transfer data between GPRs and the ` data` registers. They are either loads/stores or CSR reads/writes. The specific addresses also vary. This is all specified in . The examples here use the pseudo-op `transfer dest, src` to represent all these options.

Halt the hart for a minimum amount of time to perform a single memory write:

Op	Address	Value	Comment
Write		`transfer arg2, s0`	Save
Write	`progbuf1`	`transfer s0, arg0`	Read first argument (address)
Write	`progbuf2`	`transfer arg0, s1`	Save
Write	`progbuf3`	`transfer s1, arg1`	Read second argument (data)
Write	`progbuf4`	`sw s1, 0(s0)`	
Write	`progbuf5`	`transfer s1, arg0`	Restore
Write	`progbuf6`	`transfer s0, arg2`	Restore
Write	`progbuf7`	`ebreak`	
Write		address	
Write	`data1`	data	
Write		0x10000000	Perform quick access

This shows an example of setting the bit in to enable a hardware breakpoint in M-mode. Similar quick access instructions could have been used previously to configure the trigger that is being enabled here:

Op	Address	Value	Comment
Write		`transfer arg0, s0`	Save
Write	`progbuf1`	`li s0, (1 << 6)`	Form the mask for bit
Write	`progbuf2`	`csrrs x0, , s0`	Apply the mask to
Write	`progbuf3`	`transfer s0, arg2`	Restore
Write	`progbuf4`	`ebreak`	
Write		0x10000000	Perform quick access

8.3. Native Debugger Implementation

The spec contains a few features to aid in writing a native debugger. This section describes how some common tasks might be achieved.

8.3.1. Single Step

Single step is straightforward if the OS or a debug stub runs in M-Mode while the program being debugged runs in a less privileged mode. When a step is required, the OS or debug stub writes , , before

returning control to the lower user program with an `mret` instruction.

Stepping code running in the same privilege mode as the debugger is more complicated, depending on what other debug features are implemented.

If hardware implements and , then stepping through non-trap code which doesn't allow for nested interrupts is also straightforward.

If hardware automatically prevents triggers from matching when entering a trap handler as described in Section #sec:nativetrigger, then a carefully written trap handler can ensure that interrupts are disabled whenever the icount trigger must not match.

If neither of these features exist, then single step is doable, but tricky to get right. To single step, the debug stub would execute something like:

```
li    t0, \FcsrIcountCount=4, \FcsrIcountAction=0, \FcsrIcountM=1
csrw  tdata1, t0    /* Write the trigger. */
lw    t0, 8(sp)     /* Restore t0, count decrements to 3 */
lw    sp, 0(sp)     /* Restore sp, count decrements to 2 */
mret                /* Return to program being debugged. count decrements to 1 */
```

There is an additional problem with using to single step. An instruction may cause an exception into a more privileged mode where the trigger is not enabled. The exception handler might address the cause of the exception, and then restart the instruction. Examples of this include page faults, FPU instructions when the FPU is not yet enabled, and interrupts. When a user is single stepping through such code, they will have to step twice to get past the restarted instruction. The first time the exception handler runs, and the second time the instruction actually executes. That is confusing and usually undesirable.

To help users out, debuggers should detect when a single step restarted an instruction, and then step again. This way the users see the expected behavior of stepping over the instruction. Ideally the debugger would notify the user that an exception handler executed the first time.

The debugger should perform this extra step when the PC doesn't change during a regular step.

It is safe to perform an extra step when the PC changes, because every RISC-V instruction either changes the PC or has side effects when repeated, but never both.

To avoid an infinite loop if the exception handler does not address the cause of the exception, the debugger must execute no more than a single extra step. = RISC-V Debug Specification
Version 1.0-
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RISC-V Debug Specification Version 1.0-

Chapter 9. Preface

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Chapter 10. Introduction

When a design progresses from simulation to hardware implementation, a user's control and understanding of the system's current state drops dramatically. To help bring up and debug low level software and hardware, it is critical to have good debugging support built into the hardware. When a robust OS is running on a core, software can handle many debugging tasks. However, in many scenarios, hardware support is essential.

This document outlines a standard architecture for debug support on RISC-V hardware platforms. This architecture allows a variety of implementations and tradeoffs, which is complementary to the wide range of RISC-V implementations. At the same time, this specification defines common interfaces to allow debugging tools and components to target a variety of hardware platforms based on the RISC-V ISA.

System designers may choose to add additional hardware debug support, but this specification defines a standard interface for common functionality.

10.1. Terminology

An advanced feature for advanced users. Most users will not be able to take advantage of it.

Atomic Memory Operation.

JTAG instruction that selects a single bit data register, also called BYPASS.

A RISC-V core, or other part of a hardware platform. Typically all components will be connected to a single system bus.

Control and Status Register.

Debug Module (see Chapter #chap:dm[4]).

Debug Module Interface (see Section 4.1).

JTAG Data Register.

Debug Transport Module (see Section 7).

Debug XLEN, which is the widest XLEN a hart supports, ignoring the current value of $|MXL|$ in `misa`.

An essential feature must be present in order for debug to work correctly.

General Purpose Register.

A single system consisting of one or more *components*.

A hardware thread in a RISC-V core.

32-bit Identification CODE, and a JTAG instruction that returns the IDCODE value.

JTAG Instruction Register.

Refers to work done by IEEE's Joint Test Action Group, described in IEEE 1149.1.

A legacy feature should only be implemented to support legacy hardware that is present in a system.

A subset of the full Debug Specification that allows for very small implementations. See Chapter #chap:dm[4].

Naturally Aligned Power-Of-Two.

Non-Maskable Interrupt.

An address that is directly usable on the system bus.

A recommended feature is not required for debug to work correctly, but it is so useful that it should not be omitted without good reason.

System Bus Access (see Section 4.10).

A specialized feature, that only makes sense in the context of some specific hardware.

Test Access Port, defined in IEEE 1149.1.

Trigger Module (see Section #sec:trigger[6]).

An address as a hart sees it. If the hart is using address translation this may be different from the physical address. If there is no translation then it will be the same.

The exception program counter CSR (e.g. `mepc`) that is appropriate for the mode being trapped to.

10.2. Context

This specification attempts to support all RISC-V ISA extensions that have, roughly, been ratified through the first half of 2023. In particular, though, this specification specifically addresses features in the following extensions:

1. A
2. C
3. D
4. F
5. H
6. Sm1p13
7. Ss1p13
8. Smstateen
9. V
10. Zawrs
11. Zcmp
12. Zicbom
13. Zicboz
14. Zicbop

10.2.1. Versions

Version 0.13 of this document was ratified by the RISC-V Foundation's board. Versions 0.13.x are bug fix releases to that ratified specification.

Version 0.14 was a working version that was never officially ratified.

Version 1.0 is almost entirely forwards and backwards compatible with Version 0.13.

10.2.1.1. Bugfixes from 0.13 to 1.0

Changes that fix a bug in the spec:

1. Fix order of operations described in . #392
2. Resume ack is set after resume, in Section 4.5. #400
3. applies to . #402
4. only applies when action=0. #411
5. does not affect Argument Width. #420
6. Clarify that harts halt out of reset if . #419

10.2.1.2. Incompatible Changes from 0.13 to 1.0

Changes that are not backwards-compatible. Debuggers or hardware implementations that implement 0.13 will have to change something in order to implement 1.0:

1. Make haltsum0 optional if there is only one hart. #505
2. System bus autoincrement only happens if an access actually takes place. () #507
3. Bump to 3. #512
4. Require debugger to poll after lowering it. #566
5. Add to . #574
6. When a selected trigger is disabled, and can be written with any value supported by any of the types this trigger supports. #721
7. fields only apply to breakpoint traps, not any trap. #723
8. If is greater than 0, then (previously called .|hit|) now contains 0 when a trigger fires more than one instruction after the instruction that matched. (This information is now reflected in .) #795
9. If is greater than 0, then bit 20 of is no longer used for timing information. (Previously the bit was called .|$timing$|.) #807
10. If is greater than 0, then the encodings of for sizes greater than 64 bit have changed. #807

10.2.1.3. Minor Changes from 0.13 to 1.0

Changes that slightly modify defined behavior. Technically backwards incompatible, but unlikely to be noticeable:

1. only applies to hart-local counters. #405
2. may be invalid when . #414

3. Address triggers () may fire on any accessed address. #421
4. All trigger registers (Section [csrTrigger]) are optional. #431
5. When extending IR, still is all ones. #437
6. and are WARL. #458
7. NMIs are disabled by . #465
8. R/W1C fields should be cleared by writing every bit high. #472
9. Specify trigger priorities in Table #tab:priority relative to exceptions. #478
10. Time may pass before becomes high. #500
11. Clear MPRV when resuming into lower privilege mode. #503
12. Halt state may not be preserved across reset. #504
13. Hardware should clear trigger action when is cleared and action is 1. #501
14. Change quick access exceptions to halt the target in Section [acQuickaccess]. #585
15. Writing 0 to forces a state where and are writable. #598
16. Solutions to deal with reentrancy in Section #sec:nativetrigger[6.4] prevent triggers from *matching*, not merely *firing*. This primarily affects behavior. #722
17. Attempts to access an unimplemented CSR raise an illegal instruction exception. #791

10.2.1.4. New Features from 0.13 to 1.0

New backwards-compatible feature that did not exist before:

1. Add halt groups and external triggers in Section 4.6. #404
2. Reserve some DMI space for non-standard use. See , and through . #406
3. Reserve trigger values for non-standard use. #417
4. Add bit to . #408 and #709
5. Recommend matching on every accessed address. #449
6. Add resume groups in Section 4.6. #506
7. Add . #536
8. Move , renaming original to , and create . #535
9. Add , deprecating . #538
10. Add hypervisor support: , , , , , , and . #549
11. Optionally make and sticky, controlled by . #520
12. Add to support trigger module external trigger inputs. #543
13. Describe and behavior with atomic instructions. #561
14. Trigger hit bits must be set on fire, may be set on match. #593
15. Add and to and . #588
16. Allow debugger to request harts stay alive with keepalive bit in Section [keepalive]. #592
17. Add to allow a debugger to determine when ndmreset is complete. #594
18. Add to support triggers from an interrupt controller. #599

10.2.1.5. Incompatible Changes During 1.0 Stable

Backwards-incompatible changes between two versions that are both called 1.0 stable.

1. was moved from to , and is now subject to the mode bits in that trigger.
2. #728 introduced Message Registers, which were later removed in #878.
3. It may not be possible to read the contents of the Program Buffer using the `progbuf` registers. #731
4. fields apply to all traps, not just breakpoint traps. This reverts #723. #880

10.3. About This Document

10.3.1. Structure

This document contains two parts. The main part of the document is the specification, which is given in the numbered chapters. The second part of the document is a set of appendices. The information in the appendices is intended to clarify and provide examples, but is not part of the actual specification.

10.3.2. ISA vs. non-ISA

This specification contains both ISA and non-ISA parts. The ISA parts define self-contained ISA extensions. The other parts of the document describe the non-ISA external debug extension. Chapters whose contents are solely one or the other are labeled as such in their title. Chapters without such a label apply to both ISA and non-ISA.

10.3.3. Register Definition Format

All register definitions in this document follow the format shown below. A simple graphic shows which fields are in the register. The upper and lower bit indices are shown to the top left and top right of each field. The total number of bits in the field are shown below it.

After the graphic follows a table which for each field lists its name, description, allowed accesses, and reset value. The allowed accesses are listed in Table #tab:access. The reset value is either a constant or ``Preset." The latter means it is an implementation-specific legal value.

Parts of the register which are currently unused are labeled with the number 0. Software must only write 0 to those fields, and ignore their value while reading. Hardware must return 0 when those fields are read, and ignore the value written to them.

> – –
>
> ```
>  +
> This behavior enables us to use those fields later without having to
> increase the values in the version fields.
> ```

Names of registers and their fields are hyperlinks to their definition, and are also listed in the index on page .

|l|L| R & Read-only.

R/W & Read/Write.
R/W1C & Read/Write Ones to Clear. Writing 0 to every bit has no effect. Writing 1 to every bit clears the field. The result of other writes is undefined.
WARZ & Write any, read zero. A debugger may write any value. When read this field returns 0.
W1 & Write-only. Only writing 1 has an effect. When read the returned value should be 0.
WARL & Write any, read legal. A debugger may write any value. If a value is unsupported, the implementation converts the value to one that is supported.

10.4. Background

There are several use cases for dedicated debugging hardware, both in native debug and external debug. Native debug (sometimes called self-hosted debug) refers to debug software running on a RISC-V platform which debugs the same platform. The optional Trigger Module provides features that are useful for native debug. External debug refers to debug software running somewhere else, debugging the RISC-V platform via a debug transport like JTAG. The entire document provides features that are useful for external debug.

This specification addresses the use cases listed below. Implementations can choose not to implement every feature, which means some use cases might not be supported.

- Accessing hardware on a hardware platform without a working CPU. (External debug.)
- Bootstrapping a hardware platform to test, configure, and program components before there is any executable code path in the hardware platform. (External debug.)
- Debugging low-level software in the absence of an OS or other software. (External debug.)
- Debugging issues in the OS itself. (External or native debug.)
- Debugging processes running on an OS. (Native or external debug.)

10.5. Supported Features

The debug interface described in this specification supports the following features:

1. All hart registers (including CSRs) can be read/written.
2. Memory can be accessed either from the hart's point of view, through the system bus directly, or both.
3. RV32, RV64, and future RV128 are all supported.
4. Any hart in the hardware platform can be independently debugged.
5. A debugger can discover almost[1] everything it needs to know itself, without user configuration.
6. Each hart can be debugged from the very first instruction executed.
7. A RISC-V hart can be halted when a software breakpoint instruction is executed.
8. Hardware single-step can execute one instruction at a time.
9. Debug functionality is independent of the debug transport used.
10. The debugger does not need to know anything about the microarchitecture of the harts it is debugging.
11. Arbitrary subsets of harts can be halted and resumed simultaneously. (Optional)
12. Arbitrary instructions can be executed on a halted hart. That means no new debug functionality is

needed when a core has additional or custom instructions or state, as long as there exist programs that can move that state into GPRs. (Optional)

13. Registers can be accessed without halting. (Optional)
14. A running hart can be directed to execute a short sequence of instructions, with little overhead. (Optional)
15. A system bus manager allows memory access without involving any hart. (Optional)
16. A RISC-V hart can be halted when a trigger matches the PC, read/write address/data, or an instruction opcode. (Optional)
17. Harts can be grouped, and harts in the same group will all halt when any of them halts. These groups can also react to or notify external triggers. (Optional)

This document does not suggest a strategy or implementation for hardware test, debugging or error detection techniques. Scan, built-in self test (BIST), etc. are out of scope of this specification, but this specification does not intend to limit their use in RISC-V systems.

It is possible to debug code that uses software threads, but there is no special debug support for it.

[1] Notable exceptions include information about the memory map and peripherals.

Chapter 11. System Overview

Figure #fig:overview[3.1] shows the main components of Debug Support. Blocks shown in dotted lines are optional.

[fig/overview-eps-converted-to] | *fig/overview-eps-converted-to.pdf*

Figure 2. RISC-V Debug System Overview

The user interacts with the Debug Host (e.g. laptop), which is running a debugger (e.g. gdb). The debugger communicates with a Debug Translator (e.g. OpenOCD, which may include a hardware driver) to communicate with Debug Transport Hardware (e.g. Olimex USB-JTAG adapter). The Debug Transport Hardware connects the Debug Host to the hardware platform's Debug Transport Module (DTM). The DTM provides access to one or more Debug Modules (DMs) using the Debug Module Interface (DMI).

Each hart in the hardware platform is controlled by exactly one DM. Harts may be heterogeneous. There is no further limit on the hart-DM mapping, but usually all harts in a single core are controlled by the same DM. In most hardware platforms there will only be one DM that controls all the harts in the hardware platform.

DMs provide run control of their harts in the hardware platform. Abstract commands provide access to GPRs. Additional registers are accessible through abstract commands or by writing programs to the optional Program Buffer.

The Program Buffer allows the debugger to execute arbitrary instructions on a hart. This mechanism can also be used to access memory. An optional system bus access block allows memory accesses without using a RISC-V hart to perform the access.

Each RISC-V hart may implement a Trigger Module. When trigger conditions are met, harts will halt and inform the debug module that they have halted.

Chapter 12. Debug Module (DM) (non-ISA extension)

The Debug Module implements a translation interface between abstract debug operations and their specific implementation. It might support the following operations:

1. Give the debugger necessary information about the implementation. (Required)
2. Allow any individual hart to be halted and resumed. (Required)
3. Provide status on which harts are halted. (Required)
4. Provide abstract read and write access to a halted hart's GPRs. (Required)
5. Provide access to a reset signal that allows debugging from the very first instruction after reset. (Required)
6. Provide a mechanism to allow debugging harts immediately out of reset (regardless of the reset cause). (Optional)
7. Provide abstract access to non-GPR hart registers. (Optional)
8. Provide a Program Buffer to force the hart to execute arbitrary instructions. (Optional)
9. Allow multiple harts to be halted, resumed, and/or reset at the same time. (Optional)
10. Allow memory access from a hart's point of view. (Optional)
11. Allow direct System Bus Access. (Optional)
12. Group harts. When any hart in the group halts, they all halt. (Optional)
13. Respond to external triggers by halting each hart in a configured group. (Optional)
14. Signal an external trigger when a hart in a group halts. (Optional)

In order to be compatible with this specification an implementation must:

1. Implement all the required features listed above.
2. Implement at least one of Program Buffer, System Bus Access, or Abstract Access Memory command mechanisms.
3. Do at least one of:
    a. Implement the Program Buffer.
    b. Implement abstract access to all registers that are visible to software running on the hart including all the registers that are present on the hart and listed in Table #tab:regno.
    c. Implement abstract access to at least all GPRs, , and , and advertise the implementation as conforming to the `Minimal RISC-V Debug Specification 1.0-'', instead of the` RISC-V Debug Specification 1.0-".

A single DM can debug up to 2^{20} harts.

12.1. Debug Module Interface (DMI)

Debug Modules are subordinates on a bus called the Debug Module Interface (DMI). The bus manager is the Debug Transport Module(s). The Debug Module Interface can be a trivial bus with one manager

and one subordinate (see 8.3), or use a more full-featured bus like TileLink or the AMBA Advanced Peripheral Bus. The details are left to the system designer.

The DMI uses between 7 and 32 address bits. Each address points at a single 32-bit register that can be read or written. The bottom of the address space is used for the first (and usually only) DM. Extra space can be used for custom debug devices, other cores, additional DMs, etc. If there are additional DMs on this DMI, the base address of the next DM in the DMI address space is given in .

The Debug Module is controlled via register accesses to its DMI address space.

12.2. Reset Control

There are two methods that allow a debugger to reset harts. resets all the harts in the hardware platform, as well as all other parts of the hardware platform except for the Debug Modules, Debug Transport Modules, and Debug Module Interface. Exactly what is affected by this reset is implementation dependent, but it must be possible to debug programs from the first instruction executed. resets all the currently selected harts. In this case an implementation may reset more harts than just the ones that are selected. The debugger can discover which other harts are reset (if any) by selecting them and checking and .

To perform either of these resets, the debugger first asserts the bit, and then clears it. The actual reset may start as soon as the bit is asserted, but may start an arbitrarily long time after the bit is deasserted. The reset itself may also take an arbitrarily long time. While the reset is on-going, harts are either in the running state, indicating it's possible to perform some abstract commands during this time, or in the unavailable state, indicating it's not possible to perform any abstract commands during this time. Once a hart's reset is complete, `havereset` becomes set. When a hart comes out of reset and or |hyperref [*resethaltreq*{resethaltreq}|$] are set, the hart will immediately enter Debug Mode (halted state). Otherwise, if the hart was initially running it will execute normally (running state) and if the hart was initially halted it should now be running but may be halted.

> — —
>
> ```
>  +
> There is no general, reliable way for the debugger to know when reset
> has actually begun.
> ```

The Debug Module's own state and registers should only be reset at power-up and while in is 0. If there is another mechanism to reset the DM, this mechanism must also reset all the harts accessible to the DM.

Due to clock and power domain crossing issues, it might not be possible to perform arbitrary DMI accesses across hardware platform reset. While or any external reset is asserted, the only supported DM operations are reading and writing . The behavior of other accesses is undefined.

When harts have been reset, they must set a sticky `havereset` state bit. The conceptual `havereset` state bits can be read for selected harts in and in . These bits must be set regardless of the cause of the reset. The `havereset` bits for the selected harts can be cleared by writing 1 to in . The `havereset` bits might or might not be cleared when is low.

12.3. Selecting Harts

Up to 2^{20} harts can be connected to a single DM. Commands issued to the DM only apply to the currently selected harts.

To enumerate all the harts, a debugger must first determine `HARTSELLEN` by writing all ones to |hyperref [*hartsel*{hartsel}|$](assuming the maximum size) and reading back the value to see which bits were actually set. Then it selects each hart starting from 0 until either in is 1, or the highest index (depending on `HARTSELLEN`) is reached.

The debugger can discover the mapping between hart indices and `mhartid` by using the interface to read `mhartid`, or by reading the hardware platform's configuration structure.

12.3.1. Selecting a Single Hart

All debug modules must support selecting a single hart. The debugger can select a hart by writing its index to |hyperref [*hartsel*{hartsel}|$]. Hart indexes start at 0 and are contiguous until the final index.

12.3.2. Selecting Multiple Harts

Debug Modules may implement a Hart Array Mask register to allow selecting multiple harts at once. The nth bit in the Hart Array Mask register applies to the hart with index n. If the bit is 1 then the hart is selected. Usually a DM will have a Hart Array Mask register exactly wide enough to select all the harts it supports, but it's allowed to tie any of these bits to 0.

The debugger can set bits in the hart array mask register using and , then apply actions to all selected harts by setting . If this feature is supported, multiple harts can be halted, resumed, and reset simultaneously. The state of the hart array mask register is not affected by setting or clearing .

Execution of Abstract Commands ignores this mechanism and only applies to the hart selected by |hyperref [*hartsel*{hartsel}|$].

12.4. Hart DM States

Every hart that can be selected is in exactly one of the following four DM states: non-existent, unavailable, running, or halted. Which state the selected harts are in is reflected by , , , , , , , and .

Harts are nonexistent if they will never be part of this hardware platform, no matter how long a user waits. E.g. in a simple single-hart hardware platform only one hart exists, and all others are nonexistent. Debuggers may assume that a hardware platform has no harts with indexes higher than the first nonexistent one.

Harts are unavailable if they might exist/become available at a later time, or if there are other harts with higher indexes than this one. Harts may be unavailable for a variety of reasons including being reset, temporarily powered down, and not being plugged into the hardware platform. That means harts might become available or unavailable at any time, although these events should be rare in hardware platforms built to be easily debugged. There are no guarantees about the state of the hart when it becomes available.

Hardware platforms with very large number of harts may permanently disable some during manufacturing, leaving holes in the otherwise continuous hart index space. In order to let the debugger discover all harts, they must show up as unavailable even if there is no chance of them ever

becoming available.

Harts are running when they are executing normally, as if no debugger was attached. This includes being in a low power mode or waiting for an interrupt, as long as a halt request will result in the hart being halted.

Harts are halted when they are in Debug Mode, only performing tasks on behalf of the debugger.

Which states a hart that is reset goes through is implementation dependent. Harts may be unavailable while reset is asserted, and some time after reset is deasserted. They might transition to running for some time after reset is deasserted. Finally they end up either running or halted, depending on and |hyperref [*resethaltreq*{resethaltreq}|$].

12.5. Run Control

For every hart, the Debug Module tracks 4 conceptual bits of state: halt request, resume ack, halt-on-reset request, and hart reset. (The hart reset and halt-on-reset request bits are optional.) These 4 bits reset to 0, except for resume ack, which may reset to either 0 or 1. The DM receives halted, running, and havereset signals from each hart. The debugger can observe the state of resume ack in and , and the state of halted, running, and havereset signals in , , , , , and . The state of the other bits cannot be observed directly.

When a debugger writes 1 to , each selected hart's halt request bit is set. When a running hart, or a hart just coming out of reset, sees its halt request bit high, it responds by halting, deasserting its running signal, and asserting its halted signal. Halted harts ignore their halt request bit.

When a debugger writes 1 to , each selected hart's resume ack bit is cleared and each selected, halted hart is sent a resume request. Harts respond by resuming, clearing their halted signal, and asserting their running signal. At the end of this process the resume ack bit is set. These status signals of all selected harts are reflected in , , , and . Resume requests are ignored by running harts.

When halt or resume is requested, a hart must respond in less than one second, unless it is unavailable. (How this is implemented is not further specified. A few clock cycles will be a more typical latency).

The DM can implement optional halt-on-reset bits for each hart, which it indicates by setting to 1. This means the DM implements the and bits. Writing 1 to sets the halt-on-reset request bit for each selected hart. When a hart's halt-on-reset request bit is set, the hart will immediately enter debug mode on the next deassertion of its reset. This is true regardless of the reset's cause. The hart's halt-on-reset request bit remains set until cleared by the debugger writing 1 to while the hart is selected, or by DM reset.

If the DM is reset while a hart is halted, it is unspecified whether that hart resumes. Debuggers should use to explicitly resume harts before clearing and disconnecting.

12.6. Halt Groups, Resume Groups, and External Triggers

An optional feature allows a debugger to place harts into two kinds of groups: halt groups and resume groups. It is also possible to add external triggers to a halt and resume groups. At any given time, each hart and each trigger is a member of exactly one halt group and exactly one resume group.

In both halt and resume groups, group 0 is special. Harts in group 0 halt/resume as if groups aren't implemented at all.

When any hart in a halt group halts:

1. That hart halts normally, with reflecting the original cause of the halt.
2. All the other harts in the halt group that are running will quickly halt. for those harts should be set to 6, but may be set to 3. Other harts in the halt group that are halted but have started the process of resuming must also quickly become halted, even if they do resume briefly.
3. Any external triggers in that group are notified.

Adding a hart to a halt group does not automatically halt that hart, even if other harts in the group are already halted.

When an external trigger that's a member of the halt group fires:

1. All the harts in the halt group that are running will quickly halt. for those harts should be set to 6, but may be set to 3. Other harts in the halt group that are halted but have started the process of resuming must also quickly become halted, even if they do resume briefly.

When any hart in a resume group resumes:

1. All the other harts in that group that are halted will quickly resume as soon as any currently executing abstract commands have completed. Each hart in the group sets its resume ack bit as soon as it has resumed. Harts that are in the process of halting should complete that process and stay halted.
2. Any external triggers in that group are notified.

Adding a hart to a resume group does not automatically resume that hart, even if other harts in the group are currently running.

When an external trigger that's a member of the resume group fires:

1. All the harts in that group that are halted will quickly resume as soon as any currently executing abstract commands have completed. Each hart in the group sets its resume ack bit as soon as it has resumed. Harts that are in the process of halting should complete that process and stay halted.

External triggers are abstract concepts that can signal the DM and/or receive signals from the DM. This configuration is done through , where external triggers are referred to by a number. Commonly, external triggers are capable of sending a signal from the hardware platform into the DM, as well as receiving a signal from the DM to take their own action on. It is also allowable for an external trigger to be input-only or output-only. By convention external triggers 0–7 are bidirectional, triggers 8–11 are input-only, and triggers 12–15 are output-only but this is not required.

> — —
>
> ```
>  +
> External triggers could be used to implement near simultaneous
> halting/resuming of all cores in a hardware platform, when not all cores
> are RISC-V cores.
> ```

When the DM is reset, all harts must be placed in the lowest-numbered halt and resume groups that they can be in. (This will usually be group 0.)

Some designs may choose to hardcode hart groups to a group other than group 0, meaning it is never possible to halt or resume just a single hart. This is explicitly allowed. In that case it must be possible to discover the groups by using even if it's not possible to change the configuration.

12.7. Abstract Commands

The DM supports a set of abstract commands, most of which are optional. Depending on the implementation, the debugger may be able to perform some abstract commands even when the selected hart is not halted. Debuggers can only determine which abstract commands are supported by a given hart in a given state (running, halted, or held in reset) by attempting them and then looking at in to see if they were successful. Commands may be supported with some options set, but not with other options set. If a command has unsupported options set or if bits that are defined as 0 aren't 0, then the DM must set to 2 (not supported).

> – –
>
> ```
>  +
> Example: Every DM must support the Access Register command, but might
> not support accessing CSRs. If the debugger requests to read a CSR in
> that case, the command will return ``not supported.''
> ```

Debuggers execute abstract commands by writing them to . They can determine whether an abstract command is complete by reading in . If the debugger starts a new command while is set, becomes 1 (busy), the currently executing command still gets to run to completion, but any error generated by the currently executing command is lost. After completion, indicates whether the command was successful or not. Commands may fail because a hart is not halted, not running, unavailable, or because they encounter an error during execution.

If the command takes arguments, the debugger must write them to the `data` registers before writing to . If a command returns results, the Debug Module must ensure they are placed in the `data` registers before is cleared. Which `data` registers are used for the arguments is described in Table #tab:datareg. In all cases the least-significant word is placed in the lowest-numbered `data` register. The argument width depends on the command being executed, and is DXLEN where not explicitly specified.

|r|l|l|l| Argument Width & arg0/return value & arg1 & arg2
& & `data1` & `data2`
& , `data1` & `data2`, `data3` & `data4`, `data5`
& –`data3` & `data4`–`data7` & `data8`–`data11`

> – –
>
> ```
>  +
> The Abstract Command interface is designed to allow a debugger to write
> commands as fast as possible, and then later check whether they
> completed without error. In the common case the debugger will be much
> ```

```
slower than the target and commands succeed, which allows for maximum
throughput. If there is a failure, the interface ensures that no
commands execute after the failing one. To discover which command
failed, the debugger has to look at the state of the DM (e.g. contents
of ) or hart (e.g. contents of a register modified by a Program Buffer
program) to determine which one failed.
```

Before starting an abstract command, a debugger must ensure that , , and are all 0.

While an abstract command is executing (in is high), a debugger must not change |hyperref [*hartsel*{hartsel}|$], and must not write 1 to , , , , or .

If an abstract command does not complete in the expected time and appears to be hung, the debugger can try to reset the hart (using or). If that doesn't clear , then it can try resetting the Debug Module (using).

If an abstract command is started while the selected hart is unavailable or if a hart becomes unavailable while executing an abstract command, then the Debug Module may terminate the abstract command, setting low, and to 4 (halt/resume). Alternatively, the command could just appear to be hung (never goes low).

12.7.1. Abstract Command Listing

This section describes each of the different abstract commands and how their fields should be interpreted when they are written to .

Each abstract command is a 32-bit value. The top 8 bits contain which determines the kind of command. Table #tab:cmdtype lists all commands.

|r|l|l|l| & Command & Page
& Access Register Command &
& Quick Access &
& Access Memory Command &

12.8. Program Buffer

To support executing arbitrary instructions on a halted hart, a Debug Module can include a Program Buffer that a debugger can write small programs to. DMs that support all necessary functionality using abstract commands only may choose to omit the Program Buffer.

A debugger can write a small program to the Program Buffer, and then execute it exactly once with the Access Register Abstract Command, setting the bit in . The debugger can write whatever program it likes (including jumps out of the Program Buffer), but the program must end with `ebreak` or `c.ebreak`. An implementation may support an implicit `ebreak` that is executed when a hart runs off the end of the Program Buffer. This is indicated by . With this feature, a Program Buffer of just 2 32-bit words can offer efficient debugging.

While these programs are executed, the hart does not leave Debug Mode (see Section 5.1). If an exception is encountered during execution of the Program Buffer, no more instructions are executed, the hart remains in Debug Mode, and is set to 3 (`exception error`). If the debugger executes a program that doesn't terminate with an `ebreak` instruction, the hart will remain in Debug Mode and the debugger will lose control of the hart.

If is 1 then the following apply:

1. must be 1.
2. If the debugger writes a compressed instruction into the Program Buffer, it must be placed into the lower 16 bits and accompanied by a compressed `nop` in the upper 16 bits.

> _ _
>
> ```
>  +
> This requirement on the debugger for the case of equal to 1 is to
> accommodate hardware designs that prefer to stuff instructions directly
> into the pipeline when halted, instead of having the Program Buffer
> exist in the address space somewhere.
> ```

The Program Buffer may be implemented as RAM which is accessible to the hart. A debugger can determine if this is the case by executing small programs that attempt to write and read back relative to `pc` while executing from the Program Buffer. If so, the debugger has more flexibility in what it can do with the program buffer.

12.9. Overview of Hart Debug States

Figure #fig:abstract_sm[4.1] shows a conceptual view of the states passed through by a hart during run/halt debugging as influenced by the different fields of , , , and .

[fig/abstract_commands] | *fig/abstract_commands.pdf*

Figure 3. Run/Halt Debug State Machine for single-hart hardware platforms. As only a small amount of state is visible to the debugger, the states and transitions are conceptual.

12.10. System Bus Access

A debugger can access memory from a hart's point of view using a Program Buffer or the Abstract Access Memory command. (Both these features are optional.) A Debug Module may also include a System Bus Access block to provide memory access without involving a hart, regardless of whether Program Buffer is implemented. The System Bus Access block uses physical addresses.

The System Bus Access block may support 8-, 16-, 32-, 64-, and 128-bit accesses. Table #tab:sbdatabits shows which bits in `sbdata` are used for each access size.

|r|l| Access Size & Data Bits
& bits 7:0
& bits 15:0
&
& ,
& , , ,

Depending on the microarchitecture, data accessed through System Bus Access might not always be coherent with that observed by each hart. It is up to the debugger to enforce coherency if the implementation does not. This specification does not define a standard way to do this. Possibilities may include writing to special memory-mapped locations, or executing special instructions via the

Program Buffer.

> — —
>
> ```
>  +
> Implementing a System Bus Access block has several benefits even when a
> Debug Module also implements a Program Buffer. First, it is possible to
> access memory in a running system with minimal impact. Second, it may
> improve performance when accessing memory. Third, it may provide access
> to devices that a hart does not have access to.
> ```

12.11. Minimally Intrusive Debugging

Depending on the task it is performing, some harts can only be halted very briefly. There are several mechanisms that allow accessing resources in such a running system with a minimal impact on the running hart.

First, an implementation may allow some abstract commands to execute without halting the hart.

Second, the Quick Access abstract command can be used to halt a hart, quickly execute the contents of the Program Buffer, and let the hart run again. Combined with instructions that allow Program Buffer code to access the `data` registers, as described in , this can be used to quickly perform a memory or register access. For some hardware platforms this will be too intrusive, but many hardware platforms that can't be halted can bear an occasional hiccup of a hundred or less cycles.

Third, if the System Bus Access block is implemented, it can be used while a hart is running to access system memory.

12.12. Security

To protect intellectual property it may be desirable to lock access to the Debug Module. To allow access during a manufacturing process and not afterwards, a reasonable solution could be to add a fuse bit to the Debug Module that can be used to be permanently disable it. Since this is technology specific, it is not further addressed in this spec.

Another option is to allow the DM to be unlocked only by users who have an access key. Between , , and arbitrarily complex authentication mechanism can be supported. When is clear, the DM must not interact with the rest of the hardware platform, nor expose details about the harts connected to the DM. All DM registers should read 0, while writes should be ignored, with the following mandatory exceptions:

1. in is readable.
2. in is readable.
3. in is readable.
4. in is readable and writable.
5. is readable and writable.

Implementations where it's not possible to unlock the DM by using should not implement that

register.

12.13. Version Detection

To detect the version of the Debug Module with a minimum of side effects, use the following procedure:

1. Read .
2. If is 0 or is 1:
   a. Write , preserving , , , and from the value that was read, setting , and clearing all the other bits.
   b. Read until is high.
3. Read , which contains .

If it was necessary to clear , this might have the following unavoidable side effects:

1. is cleared, potentially preventing a halt request made by a previous debugger from taking effect.
2. is cleared, potentially preventing a resume request made by a previous debugger from taking effect.
3. is deasserted, releasing the hardware platform from reset if a previous debugger had set it.
4. is asserted, releasing the DM from reset. This in itself is not observable by any harts.

This procedure is guaranteed to work in future versions of this spec. The meaning of the bits where , , , and currently reside might change, but preserving them will have no side effects. Clearing the bits of not explicitly mentioned here will have no side effects beyond the ones mentioned above.

12.14. Debug Module Registers

The registers described in this section are accessed over the DMI bus. Each DM has a base address (which is 0 for the first DM). The register addresses below are offsets from this base address.

Debug Module DMI Registers that are unimplemented or not mentioned in the table below return 0 when read. Writing them has no effect.

Address	Name	Page
Continued on next page		
0x04	Abstract Data 0 (`data0`)	
0x05	Abstract Data 1 (`data1`)	
0x06	Abstract Data 2 (`data2`)	
0x07	Abstract Data 3 (`data3`)	
0x08	Abstract Data 4 (`data4`)	
0x09	Abstract Data 5 (`data5`)	
0x0a	Abstract Data 6 (`data6`)	
0x0b	Abstract Data 7 (`data7`)	
0x0c	Abstract Data 8 (`data8`)	

Address	Name	Page
0x0d	Abstract Data 9 (`data9`)	
0x0e	Abstract Data 10 (`data10`)	
0x0f	Abstract Data 11 (`data11`)	
0x10	Debug Module Control (`dmcontrol`)	
0x11	Debug Module Status (`dmstatus`)	
0x12	Hart Info (`hartinfo`)	
0x13	Halt Summary 1 (`haltsum1`)	
0x14	Hart Array Window Select (`hawindowsel`)	
0x15	Hart Array Window (`hawindow`)	
0x16	Abstract Control and Status (`abstractcs`)	
0x17	Abstract Command (`command`)	
0x18	Abstract Command Autoexec (`abstractauto`)	
0x19	Configuration Structure Pointer 0 (`confstrptr0`)	
0x1a	Configuration Structure Pointer 1 (`confstrptr1`)	
0x1b	Configuration Structure Pointer 2 (`confstrptr2`)	
0x1c	Configuration Structure Pointer 3 (`confstrptr3`)	
0x1d	Next Debug Module (`nextdm`)	
0x1f	Custom Features (`custom`)	
0x20	Program Buffer 0 (`progbuf0`)	
0x21	Program Buffer 1 (`progbuf1`)	
0x22	Program Buffer 2 (`progbuf2`)	
0x23	Program Buffer 3 (`progbuf3`)	
0x24	Program Buffer 4 (`progbuf4`)	
0x25	Program Buffer 5 (`progbuf5`)	
0x26	Program Buffer 6 (`progbuf6`)	
0x27	Program Buffer 7 (`progbuf7`)	
0x28	Program Buffer 8 (`progbuf8`)	
0x29	Program Buffer 9 (`progbuf9`)	
0x2a	Program Buffer 10 (`progbuf10`)	
0x2b	Program Buffer 11 (`progbuf11`)	
0x2c	Program Buffer 12 (`progbuf12`)	
0x2d	Program Buffer 13 (`progbuf13`)	

Address	Name	Page
0x2e	Program Buffer 14 (progbuf14)	
0x2f	Program Buffer 15 (progbuf15)	
0x30	Authentication Data (authdata)	
0x32	Debug Module Control and Status 2 (dmcs2)	
0x34	Halt Summary 2 (haltsum2)	
0x35	Halt Summary 3 (haltsum3)	
0x37	System Bus Address 127:96 (sbaddress3)	
0x38	System Bus Access Control and Status (sbcs)	
0x39	System Bus Address 31:0 (sbaddress0)	
0x3a	System Bus Address 63:32 (sbaddress1)	
0x3b	System Bus Address 95:64 (sbaddress2)	
0x3c	System Bus Data 31:0 (sbdata0)	
0x3d	System Bus Data 63:32 (sbdata1)	
0x3e	System Bus Data 95:64 (sbdata2)	
0x3f	System Bus Data 127:96 (sbdata3)	
0x40	Halt Summary 0 (haltsum0)	
0x70	Custom Features 0 (custom0)	
0x71	Custom Features 1 (custom1)	
0x72	Custom Features 2 (custom2)	
0x73	Custom Features 3 (custom3)	
0x74	Custom Features 4 (custom4)	
0x75	Custom Features 5 (custom5)	
0x76	Custom Features 6 (custom6)	
0x77	Custom Features 7 (custom7)	
0x78	Custom Features 8 (custom8)	
0x79	Custom Features 9 (custom9)	
0x7a	Custom Features 10 (custom10)	
0x7b	Custom Features 11 (custom11)	
0x7c	Custom Features 12 (custom12)	
0x7d	Custom Features 13 (custom13)	
0x7e	Custom Features 14 (custom14)	
0x7f	Custom Features 15 (custom15)	

Table 7. Debug Module Debug Bus Registers

12.14.1. Debug Module Status (`dmstatus`, at 0x11)

[dmDmstatus]# This register reports status for the overall Debug Module as well as the currently selected harts, as defined in . Its address will not change in the future, because it contains .

This entire register is read-only.

p3.5 exp3.5 exp7.5 exp7.5 exp6.5 exp6.5 exp4.5 exp4.5 exp2.4 exp2.4 exp6.0 exp6.0 ex 31 & & & & & 21 & &
& & & & &
& & & & &

p6.0 exp6.0 exp6.0 exp6.0 exp6.0 exp6.0 exp7.0 exp7.0 exp7.0 exp7.0 exp5.0 exp5.0 ex & & & & & & & & & &
& & & & &

p5.0 exp5.0 exp5.0 exp5.0 exp5.0 exp5.0 exp4.5 exp4.5 exp4.5 exp4.5 exp6.5 exp6.5 ex & & & & & & & & & &
& & & & &

p4.0 exp4.0 exp7.5 exp7.5 exp7.5 exp7.5 exp3.5 exp3.5 ex & & & 3 & & & &
& & &

|l|p0.5|c|l| Field & Description & Access & Reset

[dmDmstatusNdmresetpending]# |ndmresetpending| &

0 (false): Unimplemented, or is zero and no ndmreset is currently in progress.

1 (true): is currently nonzero, or there is an ndmreset in progress. & R & -
[dmDmstatusStickyunavail]# |stickyunavail| &

0 (current): The per-hart `unavail` bits reflect the current state of the hart.

1 (sticky): The per-hart `unavail` bits are sticky. Once they are set, they will not clear until the debugger acknowledges them using . & R & Preset
[dmDmstatusImpebreak]# |impebreak| & If 1, then there is an implicit `ebreak` instruction at the non-existent word immediately after the Program Buffer. This saves the debugger from having to write the `ebreak` itself, and allows the Program Buffer to be one word smaller.

This must be 1 when is 1. & R & Preset
|allhavereset| & This field is 1 when all currently selected harts have been reset and reset has not been acknowledged for any of them. & R & -
[dmDmstatusAnyhavereset] |anyhavereset| & This field is 1 when at least one currently selected hart has been reset and reset has not been acknowledged for that hart. & R & -
|allresumeack| & This field is 1 when all currently selected harts have their resume ack bit set. & R & -
[#dmDmstatusAnyresumeack] |anyresumeack| & This field is 1 when any currently selected hart has its resume ack bit set. & R & -
|allnonexistent| & This field is 1 when all currently selected harts do not exist in this hardware platform. & R & -
[#dmDmstatusAnynonexistent] |anynonexistent| & This field is 1 when any currently selected hart

does not exist in this hardware platform. & R & -
|allunavail| & This field is 1 when all currently selected harts are unavailable, or (if is 1) were unavailable without that being acknowledged. & R & -
[#dmDmstatusAnyunavail] |anyunavail| & This field is 1 when any currently selected hart is unavailable, or (if is 1) was unavailable without that being acknowledged. & R & -
|allrunning| & This field is 1 when all currently selected harts are running. & R & -
[#dmDmstatusAnyrunning] |anyrunning| & This field is 1 when any currently selected hart is running. & R & -
|allhalted| & This field is 1 when all currently selected harts are halted. & R & -
[#dmDmstatusAnyhalted] |anyhalted| & This field is 1 when any currently selected hart is halted. & R & -
[#dmDmstatusAuthenticated]# |authenticated| &

0 (false): Authentication is required before using the DM.

1 (true): The authentication check has passed.

On components that don't implement authentication, this bit must be preset as 1. & R & Preset
[dmDmstatusAuthbusy]# |authbusy| &

0 (ready): The authentication module is ready to process the next read/write to .

1 (busy): The authentication module is busy. Accessing results in unspecified behavior.

only becomes set in immediate response to an access to . & R & 0
|hasresethaltreq| & 1 if this Debug Module supports halt-on-reset functionality controllable by the and bits. 0 otherwise. & R & Preset
[#dmDmstatusConfstrptrvalid] |confstrptrvalid| &

0 (invalid): –hold information which is not relevant to the configuration structure.

1 (valid): –hold the address of the configuration structure. & R & Preset
[dmDmstatusVersion]# |version| &

0 (none): There is no Debug Module present.

1 (0.11): There is a Debug Module and it conforms to version 0.11 of this specification.

2 (0.13): There is a Debug Module and it conforms to version 0.13 of this specification.

3 (1.0): There is a Debug Module and it conforms to version 1.0 of this specification.

15 (custom): There is a Debug Module but it does not conform to any available version of this spec. & R & 3

12.14.2. Debug Module Control (`dmcontrol`, at 0x10)

[dmDmcontrol]# This register controls the overall Debug Module as well as the currently selected harts, as defined in .

[hartsel]# Throughout this document we refer to |hyperref [*hartsel*{hartsel}|$], which is combined with . While the spec allows for 20 |hyperref [*hartsel*{hartsel}|$] bits, an implementation may choose to implement fewer than that. The actual width of |hyperref [*hartsel*{hartsel}|$] is called `HARTSELLEN`. It must be at least 0 and at most 20. A debugger should discover `HARTSELLEN` by writing all ones to

|hyperref [*hartsel*{hartsel}|$](assuming the maximum size) and reading back the value to see which bits were actually set. Debuggers must not change |hyperref [*hartsel*{hartsel}|$] while an abstract command is executing.

> – –
>
> ```
>  +
> There are separate and bits so that it is possible to write without
> changing the halt-on-reset request bit for each selected hart, when not
> all selected harts have the same configuration.
> ```

On any given write, a debugger may only write 1 to at most one of the following bits: , , , , and . The others must be written 0.

is an optional internal bit of per-hart state that cannot be read, but can be written with and .

[keepalive]# |hyperref [*keepalive*{keepalive}|$] is an optional internal bit of per-hart state. When it is set, it suggests that the hardware should attempt to keep the hart available for the debugger, e.g. by keeping it from entering a low-power state once powered on. Even if the bit is implemented, hardware might not be able to keep a hart available. The bit is written through and .

For forward compatibility, will always be readable when bit 1 () is 0 and bit 0 () is 1.

p3.5 exp3.5 exp4.5 exp4.5 exp4.5 exp4.5 exp6.0 exp6.0 exp5.0 exp5.0 ex & & & &
& & & &
& & & &

p2.5 exp2.5 exp5.0 exp5.0 exp6.7 exp3.3 exp6.0 exp6.0 exp6.0 exp6.0 ex & 25 & & 15 & & &
& & & &
& & & &

p7.5 exp7.5 exp7.5 exp7.5 exp4.0 exp4.0 exp4.0 exp4.0 ex & & &
& & &
& & &

|l|p0.5|c|l| Field & Description & Access & Reset

[dmDmcontrolHaltreq]# |haltreq| & Writing 0 clears the halt request bit for all currently selected harts. This may cancel outstanding halt requests for those harts.

Writing 1 sets the halt request bit for all currently selected harts. Running harts will halt whenever their halt request bit is set.

Writes apply to the new value of |hyperref [*hartsel*{hartsel}|$] and . & WARZ & -
[dmDmcontrolResumereq]# |resumereq| & Writing 1 causes the currently selected harts to resume once, if they are halted when the write occurs. It also clears the resume ack bit for those harts.

is ignored if is set.

Writes apply to the new value of |hyperref [*hartsel*{hartsel}|$] and . & W1 & -
[dmDmcontrolHartreset]# |hartreset| & This optional field writes the reset bit for all the currently

selected harts. To perform a reset the debugger writes 1, and then writes 0 to deassert the reset signal.

While this bit is 1, the debugger must not change which harts are selected.

If this feature is not implemented, the bit always stays 0, so after writing 1 the debugger can read the register back to see if the feature is supported.

Writes apply to the new value of |hyperref [*hartsel*{hartsel}|$] and . & WARL & 0 [dmDmcontrolAckhavereset]# |ackhavereset| &

0 (nop): No effect.

1 (ack): Clears `havereset` for any selected harts.

Writes apply to the new value of |hyperref [*hartsel*{hartsel}|$] and . & W1 & - [dmDmcontrolAckunavail]# |ackunavail| &

0 (nop): No effect.

1 (ack): Clears `unavail` for any selected harts that are currently available.

Writes apply to the new value of |hyperref [*hartsel*{hartsel}|$] and . & W1 & - [dmDmcontrolHasel]# |hasel| & Selects the definition of currently selected harts.

0 (single): There is a single currently selected hart, that is selected by |hyperref [*hartsel*{hartsel}|$].

1 (multiple): There may be multiple currently selected harts — the hart selected by |hyperref [*hartsel*{hartsel}|$], plus those selected by the hart array mask register.

An implementation which does not implement the hart array mask register must tie this field to 0. A debugger which wishes to use the hart array mask register feature should set this bit and read back to see if the functionality is supported. & WARL & 0
|hartsello| & The low 10 bits of |hyperref [*hartsel*{hartsel}|$]: the DM-specific index of the hart to select. This hart is always part of the currently selected harts. & WARL & 0
[dmDmcontrolHartselhi] |hartselhi| & The high 10 bits of |hyperref [*hartsel*{hartsel}|$]: the DM-specific index of the hart to select. This hart is always part of the currently selected harts. & WARL & 0
[#dmDmcontrolSetkeepalive]# |setkeepalive| & This optional field sets |hyperref [*keepalive*{keepalive}|$] for all currently selected harts, unless is simultaneously set to 1.

Writes apply to the new value of |hyperref [*hartsel*{hartsel}|$] and . & W1 & - [dmDmcontrolClrkeepalive]# |clrkeepalive| & This optional field clears |hyperref [*keepalive*{keepalive}|$] for all currently selected harts.

Writes apply to the new value of |hyperref [*hartsel*{hartsel}|$] and . & W1 & - [dmDmcontrolSetresethaltreq]# |setresethaltreq| & This optional field writes the halt-on-reset request bit for all currently selected harts, unless is simultaneously set to 1. When set to 1, each selected hart will halt upon the next deassertion of its reset. The halt-on-reset request bit is not automatically cleared. The debugger must write to to clear it.

Writes apply to the new value of |hyperref [*hartsel*{hartsel}|$] and .

If is 0, this field is not implemented. & W1 & - [dmDmcontrolClrresethaltreq]# |clrresethaltreq| & This optional field clears the halt-on-reset request bit for all currently selected harts.

Writes apply to the new value of |hyperref [*hartsel*{hartsel}|$] and . & W1 & -
|ndmreset| & This bit controls the reset signal from the DM to the rest of the hardware platform. The signal should reset every part of the hardware platform, including every hart, except for the DM and any logic required to access the DM. To perform a hardware platform reset the debugger writes 1, and then writes 0 to deassert the reset. & R/W & 0
[#dmDmcontrolDmactive] |dmactive| & This bit serves as a reset signal for the Debug Module itself. After changing the value of this bit, the debugger must poll until has taken the requested value before performing any action that assumes the requested state change has completed. Hardware may take an arbitrarily long time to complete activation or deactivation and will indicate completion by setting to the requested value.

0 (inactive): The module's state, including authentication mechanism, takes its reset values (the bit is the only bit which can be written to something other than its reset value). Any accesses to the module may fail. Specifically, might not return correct data.

1 (active): The module functions normally.

No other mechanism should exist that may result in resetting the Debug Module after power up.

To place the Debug Module into a known state, a debugger may write 0 to , poll until is observed 0, write 1 to , and poll until is observed 1.

Implementations may pay attention to this bit to further aid debugging, for example by preventing the Debug Module from being power gated while debugging is active. & R/W & 0

12.14.3. Hart Info (`hartinfo`, at 0x12)

[dmHartinfo]# This register gives information about the hart currently selected by |hyperref [*hartsel*{hartsel}|$].

This register is optional. If it is not present it should read all-zero.

If this register is included, the debugger can do more with the Program Buffer by writing programs which explicitly access the `data` and/or `dscratch` registers.

This entire register is read-only.

p4.0 exp4.0 exp4.0 exp4.0 exp2.4 exp2.4 exp5.0 exp5.0 exp4.0 exp4.0 exp8.0 exp4.0 ex 31 & & 23 & & 19 & & & 15 & & 11 &
& & & & &
& & & & &

|l|p0.5|c|l| Field & Description & Access & Reset

|nscratch| & Number of `dscratch` registers available for the debugger to use during program buffer execution, starting from . The debugger can make no assumptions about the contents of these registers between commands. & R & Preset
[#dmHartinfoDataaccess] |dataaccess| &

0 (csr): The `data` registers are shadowed in the hart by CSRs. Each CSR is DXLEN bits in size, and corresponds to a single argument, per Table #tab:datareg.

1 (memory): The `data` registers are shadowed in the hart's memory map. Each register takes up 4 bytes

in the memory map. & R & Preset
[dmHartinfoDatasize]# |datasize| & If is 0: Number of CSRs dedicated to shadowing the `data` registers.

If is 1: Number of 32-bit words in the memory map dedicated to shadowing the `data` registers.

If this value is non-zero, then the tt data registers must be traditional registers and not MRs.

Since there are at most 12 `data` registers, the value in this register must be 12 or smaller. & R & Preset
[dmHartinfoDataaddr]# |dataaddr| & If is 0: The number of the first CSR dedicated to shadowing the `data` registers.

If is 1: Address of RAM where the data registers are shadowed. This address is sign extended giving a range of -2048 to 2047, easily addressed with a load or store using `x0` as the address register. & R & Preset

12.14.4. Hart Array Window Select (`hawindowsel`, at 0x14)

[dmHawindowsel]# This register selects which of the 32-bit portion of the hart array mask register (see Section 4.3.2) is accessible in .

p8.5 exp8.5 exp10.0 exp5.0 ex 31 & & 14 &
&
&

|l|p0.5|c|l| Field & Description & Access & Reset

[dmHawindowselHawindowsel]# |hawindowsel| & The high bits of this field may be tied to 0, depending on how large the array mask register is. E.g. on a hardware platform with 48 harts only bit 0 of this field may actually be writable. & WARL & 0

12.14.5. Hart Array Window (`hawindow`, at 0x15)

[dmHawindow]# This register provides R/W access to a 32-bit portion of the hart array mask register (see Section 4.3.2). The position of the window is determined by . I.e. bit 0 refers to hart RdmHawindowsel * 32, while bit 31 refers to hart RdmHawindowsel * 32+31.

Since some bits in the hart array mask register may be constant 0, some bits in this register may be constant 0, depending on the current value of .

p21.3 exp10.7 ex 31 &

12.14.6. Abstract Control and Status (`abstractcs`, at 0x16)

[dmAbstractcs]# Writing this register while an abstract command is executing causes to become 1 (busy) once the command completes (busy becomes 0).

> — —
>
> +

```
must be at least 1 to support RV32 harts, 2 to support RV64 harts, or 4
to support RV128 harts.
```

p2.4 exp2.4 exp5.5 exp5.5 exp5.5 exp5.5 exp2.4 exp2.4 ex 31 & & 28 & & 23 & &
& & &
& & &

p5.5 exp5.5 exp4.0 exp2.0 exp2.0 exp2.0 exp4.5 exp4.5 ex & 10 & & 7 & & 3 &
& & &
& & &

|l|p0.5|c|l| Field & Description & Access & Reset

|progbufsize| & Size of the Program Buffer, in 32-bit words. Valid sizes are 0 - 16. & R & Preset
[#dmAbstractcsBusy] |busy| &

0 (ready): There is no abstract command currently being executed.

1 (busy): An abstract command is currently being executed.

This bit is set as soon as is written, and is not cleared until that command has completed. & R & 0
[dmAbstractcsRelaxedpriv]# |relaxedpriv| & This optional bit controls whether program buffer and abstract memory accesses are performed with the exact and full set of permission checks that apply based on the current architectural state of the hart performing the access, or with a relaxed set of permission checks (e.g. PMP restrictions are ignored). The details of the latter are implementation-specific.

0 (full checks): Full permission checks apply.

1 (relaxed checks): Relaxed permission checks apply. & WARL & Preset
[dmAbstractcsCmderr]# |cmderr| & Gets set if an abstract command fails. The bits in this field remain set until they are cleared by writing 1 to them. No abstract command is started until the value is reset to 0.

This field only contains a valid value if is 0.

0 (none): No error.

1 (busy): An abstract command was executing while , , or was written, or when one of the `data` or `progbuf` registers was read or written. This status is only written if contains 0.

2 (not supported): The command in is not supported. It may be supported with different options set, but it will not be supported at a later time when the hart or system state are different.

3 (exception): An exception occurred while executing the command (e.g. while executing the Program Buffer).

4 (halt/resume): The abstract command couldn't execute because the hart wasn't in the required state (running/halted), or unavailable.

5 (bus): The abstract command failed due to a bus error (e.g. alignment, access size, or timeout).

6 (reserved): Reserved for future use.

7 (other): The command failed for another reason. & R/W1C & 0
[dmAbstractcsDatacount]# |datacount| & Number of `data` registers that are implemented as part of the abstract command interface. Valid sizes are 1 – 12. & R & Preset

12.14.7. Abstract Command (`command`, at 0x17)

[dmCommand]# Writes to this register cause the corresponding abstract command to be executed.

Writing this register while an abstract command is executing causes to become 1 (busy) once the command completes (busy becomes 0).

If is non-zero, writes to this register are ignored.

> – –
>
> ```
>  +
> inhibits starting a new command to accommodate debuggers that, for
> performance reasons, send several commands to be executed in a row
> without checking in between. They can safely do so and check at the end
> without worrying that one command failed but then a later command (which
> might have depended on the previous one succeeding) passed.
> ```

31	24	23	0
latexmath:[$	cmdtype	$]	
latexmath:[$	control	$]	
8		24	

Field	Description	Access	Reset
Continued on next page			
[dmCommandCmdtype]# |cmdtype|	The type determines the overall functionality of this abstract command.	WARZ	0
|control|	This field is interpreted in a command-specific manner, described for each abstract command.	WARZ	0

12.14.8. Abstract Command Autoexec (`abstractauto`, at 0x18)

[dmAbstractauto]# This register is optional. Including it allows more efficient burst accesses. A debugger can detect whether it is supported by setting bits and reading them back.

If this register is implemented then bits corresponding to implemented progbuf and data registers must be writable. Other bits must be hard-wired to 0.

If this register is written while an abstract command is executing then the write is ignored and becomes 1 (busy) once the command completes (busy becomes 0).

31	16	15	12	11	0
latexmath:[$	autoexecprogbuf	$]		latexmath:[$	0
$]		latexmath:[$	autoexecdata	$]	
16		4		12	

Field	Description	Access	Reset
Continued on next page			
[dmAbstractautoAutoexecprogbuf]# |autoexecprogbuf|	When a bit in this field is 1, read or write accesses to the corresponding `progbuf` word cause the DM to act as if the current value in was written there again after the access to `progbuf` completes.	WARL	0
|autoexecdata|	When a bit in this field is 1, read or write accesses to the corresponding `data` word cause the DM to act as if the current value in was written there again after the access to `data` completes.	WARL	0

12.14.9. Configuration Structure Pointer 0 (`confstrptr0`, at 0x19)

[dmConfstrptrZero]# When is set, reading this register returns bits 31:0 of the configuration structure pointer. Reading the other `confstrptr` registers returns the upper bits of the address.

When system bus access is implemented, this must be an address that can be used with the System Bus Access module. Otherwise, this must be an address that can be used to access the configuration structure from the hart with ID 0.

If is 0, then the `confstrptr` registers hold identifier information which is not further specified in this document.

The configuration structure itself is a data structure of the same format as the data structure pointed to by mconfigptr as described in the Privileged Spec.

This entire register is read-only.

31	0
latexmath:[$	addr
$]	
32	

12.14.10. Configuration Structure Pointer 1 (`confstrptr1`, at 0x1a)

[dmConfstrptrOne]# When is set, reading this register returns bits 63:32 of the configuration structure pointer. See for more details.

This entire register is read-only.

31	0
latexmath:[$	addr
$]	
32	

12.14.11. Configuration Structure Pointer 2 (confstrptr2, at 0x1b)

[dmConfstrptrTwo]# When is set, reading this register returns bits 95:64 of the configuration structure pointer. See for more details.

This entire register is read-only.

31	0
latexmath:[$	addr
$]	
32	

12.14.12. Configuration Structure Pointer 3 (confstrptr3, at 0x1c)

[dmConfstrptrThree]# When is set, reading this register returns bits 127:96 of the configuration structure pointer. See for more details.

This entire register is read-only.

31	0
latexmath:[$	addr
$]	
32	

12.14.13. Next Debug Module (nextdm, at 0x1d)

[dmNextdm]# If there is more than one DM accessible on this DMI, this register contains the base address of the next one in the chain, or 0 if this is the last one in the chain.

This entire register is read-only.

31	0
latexmath:[$	addr
$]	
32	

12.14.14. Abstract Data 0 (data0, at 0x04)

[dmDataZero]# through may be Message Registers, whose behavior is described in Section #sec:mr. These registers may be read or changed by abstract commands. indicates how many of them are implemented, starting at , counting up. Table #tab:datareg shows how abstract commands use these registers.

Accessing these registers while an abstract command is executing causes to be set to 1 (busy) if it is 0.

Attempts to write them while is set does not change their value.

The values in these registers might not be preserved after an abstract command is executed. The only guarantees on their contents are the ones offered by the command in question. If the command fails, no assumptions can be made about the contents of these registers.

31	0
latexmath:[$	data
$]	
32	

12.14.15. Program Buffer 0 (`progbuf0`, at 0x20)

[dmProgbufZero]# through must provide write access to the optional program buffer. It may also be possible for the debugger to read from the program buffer through these registers. If reading is not supported, then all reads return 0.

indicates how many `progbuf` registers are implemented starting at , counting up.

Accessing these registers while an abstract command is executing causes to be set to 1 (busy) if it is 0.

Attempts to write them while is set does not change their value.

31	0
latexmath:[$	data
$]	
32	

12.14.16. Authentication Data (`authdata`, at 0x30)

[dmAuthdata]# This register serves as a 32-bit serial port to/from the authentication module.

When is clear, the debugger can communicate with the authentication module by reading or writing this register. There is no separate mechanism to signal overflow/underflow.

31	0
latexmath:[$	data
$]	
32	

12.14.17. Debug Module Control and Status 2 (`dmcs2`, at 0x32)

[dmDmcsTwo]# This register contains DM control and status bits that didn't easily fit in and . All are optional.

If halt groups are not implemented, then will always be 0 when is 0.

If resume groups are not implemented, then will remain 0 even after 1 is written there.

The DM external triggers available to add to halt groups may be the same as or distinct from the DM external triggers available to add to resume groups.

31	12	11		10	7	6	2	1		0	
latexmath:[$	0	$]		latexmath:[$	grouptype	$]		latexmath:[$	dmexttrigger	$]	
latexmath:[$	group	$]		latexmath:[$	hgwrite	$]		latexmath:[$	hgselect	$]	
20		1		4		5		1		1	

Field	Description	Access	Reset
Continued on next page			
[dmDmcsTwoGrouptype]# |grouptype|	0 (halt): The remaining fields in this register configure halt groups. 1 (resume): The remaining fields in this register configure resume groups.	WARL	0
[dmDmcsTwoDmexttrigger]# |dmexttrigger|	This field contains the currently selected DM external trigger. If a non-existent trigger value is written here, the hardware will change it to a valid one or 0 if no DM external triggers exist.	WARL	0
[dmDmcsTwoGroup]# |group|	When is 0, contains the group of the hart specified by latexmath:[$	\hyperref[hartsel]{hartsel}	$]. When is 1, contains the group of the DM external trigger selected by . The value written to this field is ignored unless is also written 1. Group numbers are contiguous starting at 0, with the highest number being implementation-dependent, and possibly different between different group types. Debuggers should read back this field after writing to confirm they are using a hart group that is supported. If groups aren't implemented, then this entire field is 0.

Field	Description	Access	Reset
WARL	preset	[dmDmcsTwoHgwrite]# |hgwrite|	When 1 is written and is 0, for every selected hart the DM will change its group to the value written to , if the hardware supports that group for that hart. Implementations may also change the group of a minimal set of unselected harts in the same way, if that is necessary due to a hardware limitation. When 1 is written and is 1, the DM will change the group of the DM external trigger selected by to the value written to , if the hardware supports that group for that trigger. Writing 0 has no effect.
W1	-	|hgselect|	0 (harts): Operate on harts. 1 (triggers): Operate on DM external triggers. If there are no DM external triggers, this field must be tied to 0.

12.14.18. Halt Summary 0 (`haltsum0`, at 0x40)

[dmHaltsumZero]# Each bit in this read-only register indicates whether one specific hart is halted or not. Unavailable/nonexistent harts are not considered to be halted.

This register might not be present if fewer than 2 harts are connected to this DM.

The LSB reflects the halt status of hart \{hartsel[19:5],5'h0}, and the MSB reflects halt status of hart \{hartsel[19:5],5'h1f}.

This entire register is read-only.

31	0
latexmath:[$	haltsum0
$]	
32	

12.14.19. Halt Summary 1 (`haltsum1`, at 0x13)

[dmHaltsumOne]# Each bit in this read-only register indicates whether any of a group of harts is halted or not. Unavailable/nonexistent harts are not considered to be halted.

This register might not be present if fewer than 33 harts are connected to this DM.

The LSB reflects the halt status of harts \{hartsel[19:10],10'h0} through \{hartsel[19:10],10'h1f}. The MSB reflects the halt status of harts \{hartsel[19:10],10'h3e0} through \{hartsel[19:10],10'h3ff}.

This entire register is read-only.

31	0
latexmath:[$	haltsum1
$]	
32	

12.14.20. Halt Summary 2 (`haltsum2`, at 0x34)

[dmHaltsumTwo]# Each bit in this read-only register indicates whether any of a group of harts is halted or not. Unavailable/nonexistent harts are not considered to be halted.

This register might not be present if fewer than 1025 harts are connected to this DM.

The LSB reflects the halt status of harts \{hartsel[19:15],15'h0} through \{hartsel[19:15],15'h3ff}. The MSB reflects the halt status of harts \{hartsel[19:15],15'h7c00} through \{hartsel[19:15],15'h7fff}.

This entire register is read-only.

31	0
latexmath:[$	haltsum2
$]	
32	

12.14.21. Halt Summary 3 (`haltsum3`, at 0x35)

[dmHaltsumThree]# Each bit in this read-only register indicates whether any of a group of harts is halted or not. Unavailable/nonexistent harts are not considered to be halted.

This register might not be present if fewer than 32769 harts are connected to this DM.

The LSB reflects the halt status of harts 20'h0 through 20'h7fff. The MSB reflects the halt status of harts 20'hf8000 through 20'hfffff.

This entire register is read-only.

31	0
latexmath:[$	haltsum3
$]	
32	

12.14.22. System Bus Access Control and Status (`sbcs`, at 0x38)

[dmSbcs]#

31	29	28	23	22		21		20	
latexmath :[$	sbversion	$]		latexmath :[$	0	$]		latexmath :[$	sbbusyerr or
$]		latexmath :[$	sbbusy	$]		latexmath :[$	sbreadona ddr	$]	
3		6		1		1		1	

19	17	16		15		14	12	11	5
latexmath :[$	sbaccess	$]		latexmath :[$	sbautoinc rement	$]		latexmath :[$	sbreadond ata
$]		latexmath :[$	sberror	$]		latexmath :[$	sbasize	$]	
3		1		1		3		7	

4		3		2		1		0	
latexmath :[$	sbaccess12 8	$]		latexmath :[$	sbaccess6 4	$]		latexmath :[$	sbaccess3 2
$]		latexmath :[$	sbaccess1 6	$]		latexmath :[$	sbaccess8	$]	
1		1		1		1		1	

Field	Description	Access	Reset
Continued on next page			
[dmSbcsSbversion]# |sbversion|	0 (legacy): The System Bus interface conforms to mainline drafts of this spec older than 1 January, 2018. 1 (1.0): The System Bus interface conforms to this version of the spec. Other values are reserved for future versions.	R	1
[dmSbcsSbbusyerror]# |sbbusyerror|	Set when the debugger attempts to read data while a read is in progress, or when the debugger initiates a new access while one is already in progress (while is set). It remains set until it's explicitly cleared by the debugger. While this field is set, no more system bus accesses can be initiated by the Debug Module.	R/W1C	0

Field	Description	Access	Reset
[dmSbcsSbbusy]# |sbbusy|	When 1, indicates the system bus manager is busy. (Whether the system bus itself is busy is related, but not the same thing.) This bit goes high immediately when a read or write is requested for any reason, and does not go low until the access is fully completed. Writes to while is high result in undefined behavior. A debugger must not write to until it reads as 0.	R	0
[dmSbcsSbreadonaddr]# |sbreadonaddr|	When 1, every write to automatically triggers a system bus read at the new address.	R/W	0
[dmSbcsSbaccess]# |sbaccess|	Select the access size to use for system bus accesses. 0 (8bit): 8-bit 1 (16bit): 16-bit 2 (32bit): 32-bit 3 (64bit): 64-bit 4 (128bit): 128-bit If has an unsupported value when the DM starts a bus access, the access is not performed and is set to 4.	R/W	2
[dmSbcsSbautoincrement]# |sbautoincrement|	When 1, `sbaddress` is incremented by the access size (in bytes) selected in after every system bus access.	R/W	0
[dmSbcsSbreadondata]# |sbreadondata|	When 1, every read from automatically triggers a system bus read at the (possibly auto-incremented) address.	R/W	0

Field	Description	Access	Reset
[dmSbcsSberror]# |sberror|	When the Debug Module's system bus manager encounters an error, this field gets set. The bits in this field remain set until they are cleared by writing 1 to them. While this field is non-zero, no more system bus accesses can be initiated by the Debug Module. An implementation may report `Other" (7) for any error condition. 0 (none): There was no bus error. 1 (timeout): There was a timeout. 2 (address): A bad address was accessed. 3 (alignment): There was an alignment error. 4 (size): An access of unsupported size was requested. 7 (other): Other.	R/W1C	0
[dmSbcsSbasize]# |sbasize|	Width of system bus addresses in bits. (0 indicates there is no bus access support.)	R	Preset
[dmSbcsSbaccessOneTwentyeight]# |sbaccess128|	1 when 128-bit system bus accesses are supported.	R	Preset
[dmSbcsSbaccessSixtyfour]# |sbaccess64|	1 when 64-bit system bus accesses are supported.	R	Preset
[dmSbcsSbaccessThirtytwo]# |sbaccess32|	1 when 32-bit system bus accesses are supported.	R	Preset
[dmSbcsSbaccessSixteen]# |sbaccess16|	1 when 16-bit system bus accesses are supported.	R	Preset
|sbaccess8|	1 when 8-bit system bus accesses are supported.	R	Preset

12.14.23. System Bus Address 31:0 (`sbaddress0`, at 0x39)

[dmSbaddressZero]# If is 0, then this register is not present.

When the system bus manager is busy, writes to this register will set and don't do anything else.

If is 0, is 0, and is set then writes to this register start the following:

1. Set .
2. Perform a bus read from the new value of `sbaddress`.
3. If the read succeeded and is set, increment `sbaddress`.
4. Clear .

31	0
latexmath:[$	address
$]	
32	

Field	Description	Access	Reset
Continued on next page			
|address|	Accesses bits 31:0 of the physical address in `sbaddress`.	R/W	0

12.14.24. System Bus Address 63:32 (`sbaddress1`, at 0x3a)

[dmSbaddressOne]# If is less than 33, then this register is not present.

When the system bus manager is busy, writes to this register will set and don't do anything else.

31	0
latexmath:[$	address
$]	
32	

Field	Description	Access	Reset
Continued on next page			
|address|	Accesses bits 63:32 of the physical address in `sbaddress` (if the system address bus is that wide).	R/W	0

12.14.25. System Bus Address 95:64 (`sbaddress2`, at 0x3b)

[dmSbaddressTwo]# If is less than 65, then this register is not present.

When the system bus manager is busy, writes to this register will set and don't do anything else.

31	0
latexmath:[$	address
$]	
32	

Field	Description	Access	Reset
Continued on next page			
|address|	Accesses bits 95:64 of the physical address in `sbaddress` (if the system address bus is that wide).	R/W	0

12.14.26. System Bus Address 127:96 (`sbaddress3`, at 0x37)

[dmSbaddressThree]# If is less than 97, then this register is not present.

When the system bus manager is busy, writes to this register will set and don't do anything else.

31	0
latexmath:[$	address
$]	
32	

Field	Description	Access	Reset
Continued on next page			
|address|	Accesses bits 127:96 of the physical address in `sbaddress` (if the system address bus is that wide).	R/W	0

12.14.27. System Bus Data 31:0 (`sbdata0`, at 0x3c)

[dmSbdataZero]# If all of the `sbaccess` bits in are 0, then this register is not present.

Any successful system bus read updates `sbdata`. If the width of the read access is less than the width of `sbdata`, the contents of the remaining high bits may take on any value.

If either or isn't 0 then accesses do nothing.

If the bus manager is busy then accesses set , and don't do anything else.

Writes to this register start the following:

1. Set .
2. Perform a bus write of the new value of `sbdata` to `sbaddress`.
3. If the write succeeded and is set, increment `sbaddress`.
4. Clear .

Reads from this register start the following:

1. ``Return" the data.
2. Set .
3. If is set:

a. Perform a system bus read from the address contained in `sbaddress`, placing the result in `sbdata`.

b. If is set and the read was successful, increment `sbaddress`.

4. Clear .

Only has this behavior. The other `sbdata` registers have no side effects. On systems that have buses wider than 32 bits, a debugger should access after accessing the other `sbdata` registers.

31	0
latexmath:[$	data
$]	
32	

Field	Description	Access	Reset
Continued on next page			
|data|	Accesses bits 31:0 of `sbdata`.	R/W	0

12.14.28. System Bus Data 63:32 (`sbdata1`, at 0x3d)

[dmSbdataOne]# If and are 0, then this register is not present.

If the bus manager is busy then accesses set , and don't do anything else.

31	0
latexmath:[$	data
$]	
32	

Field	Description	Access	Reset
Continued on next page			
|data|	Accesses bits 63:32 of `sbdata` (if the system bus is that wide).	R/W	0

12.14.29. System Bus Data 95:64 (`sbdata2`, at 0x3e)

[dmSbdataTwo]# This register only exists if is 1.

If the bus manager is busy then accesses set , and don't do anything else.

31	0
latexmath:[$	data
$]	
32	

Field	Description	Access	Reset
Continued on next page			
|data|	Accesses bits 95:64 of `sbdata` (if the system bus is that wide).	R/W	0

12.14.30. System Bus Data 127:96 (`sbdata3`, at 0x3f)

[dmSbdataThree]# This register only exists if is 1.

If the bus manager is busy then accesses set , and don't do anything else.

31	0
latexmath:[$	data
$]	
32	

Field	Description	Access	Reset
Continued on next page			
|data|	Accesses bits 127:96 of `sbdata` (if the system bus is that wide).	R/W	0

12.14.31. Custom Features (`custom`, at 0x1f)

[dmCustom]# This optional register may be used for non-standard features. Future version of the debug spec will not use this address.

12.14.32. Custom Features 0 (`custom0`, at 0x70)

[dmCustomZero]# The optional through registers may be used for non-standard features. Future versions of the debug spec will not use these addresses.

Chapter 13. Sdext (ISA Extension)

This chapter describes the Sdext ISA extension. It must be implemented to make external debug work, and is only useful in conjunction with external debug.

Modifications to the RISC-V core to support debug are kept to a minimum. There is a special execution mode (Debug Mode) and a few extra CSRs. The DM takes care of the rest.

In order to be compatible with this specification an implementation must implement everything described in this chapter that is not explicitly listed as optional.

If Sdext is implemented and Sdtrig is not implemented, then accessing any of the Sdtrig CSRs must raise an illegal instruction exception.

13.1. Debug Mode

Debug Mode is a special processor mode used only when a hart is halted for external debugging. Because the hart is halted, there is no forward progress in the normal instruction stream. How Debug Mode is implemented is not specified here.

When executing code due to an abstract command, the hart stays in Debug Mode and the following apply:

1. All implemented instructions operate just as they do in M-mode, unless an exception is mentioned in this list.
2. All operations are executed with machine mode privilege, except that additional Debug Mode CSRs are accessible and $|MPRV|$ in `mstatus` may be ignored according to . Full permission checks, or a relaxed set of permission checks, will apply according to .
3. All interrupts (including NMI) are masked.
4. Traps don't take place. Instead, they end execution of the program buffer and the hart remains in Debug Mode. Because they do not trap to M-mode, they do not update registers such as `mstatus`, `mepc`, `mcause`, `` mtval`, `mtval2`, and `mtinst`. The same is true for the equivalent privileged registers that are updated when trapping to other modes. Registers that may be updated as part of execution before the exception are allowed to be updated. For example, vector load/store instructions which raise exceptions may partially update the destination register and set `vstart` appropriately.
5. Triggers don't match or fire.
6. If is 0 then counters continue. If it is 1 then counters are stopped.
7. If is 0 then `time` continues to update. If it is 1 then `time` will not update. It will resynchronize with `mtime` after leaving Debug Mode.
8. Instructions that place the hart into a stalled state act as a `nop`. This includes `wfi`, `wrs.sto`, and `wrs.nto`.
9. Almost all instructions that change the privilege mode have unspecified behavior. This includes `ecall`, `mret`, `sret`, and `uret`. (To change the privilege mode, the debugger can write and in). The only exception is `ebreak`, which ends execution of the Program Buffer when executed.
10. All control transfer instructions may act as illegal instructions if their destination is in the Program Buffer. If one such instruction acts as an illegal instruction, all such instructions must act as illegal instructions.

11. All control transfer instructions may act as illegal instructions if their destination is outside the Program Buffer. If one such instruction acts as an illegal instruction, all such instructions must act as illegal instructions.
12. Instructions that depend on the value of the PC (e.g. `auipc`) may act as illegal instructions.
13. Effective XLEN is DXLEN.
14. Forward progress is guaranteed.

> — —
>
> ```
>  +
> When , the external debugger can set MPRV and MPP appropriately to have
> hardware perform memory accesses with the appropriate endianness,
> address translation, permission checks, and PMP/PMA checks (subject to
> ). This is also the only way to access all of physical memory when
> 34-bit physical addresses are supported on a Sv32 hart. If hardware ties
> to 0 then the external debugger is expected to simulate all the effects
> of MPRV, including any extensions that affect memory accesses. For these
> reasons it is recommended to tie to 1.
> ```

13.2. Load-Reserved/Store-Conditional Instructions

The reservation registered by an `lr` instruction on a memory address may be lost when entering Debug Mode or while in Debug Mode. This means that there may be no forward progress if Debug Mode is entered between `lr` and `sc` pairs.

> — —
>
> ```
>  +
> This is a behavior that debug users must be aware of. If they have a
> breakpoint set between a `lr` and `sc` pair, or are stepping through
> such code, the `sc` may never succeed. Fortunately in general use there
> will be very few instructions in such a sequence, and anybody debugging
> it will quickly notice that the reservation is not occurring. The
> solution in that case is to set a breakpoint on the first instruction
> after the `sc` and run to it. A higher level debugger may choose to
> automate this.
> ```

13.3. Wait for Interrupt Instruction

If halt is requested while `wfi` is executing, then the hart must leave the stalled state, completing this instruction's execution, and then enter Debug Mode.

13.4. Wait-on-Reservation-Set Instructions

If halt is requested while `wrs.sto` or `wrs.nto` is executing, then the hart must leave the stalled state, completing this instruction's execution, and then enter Debug Mode.

13.5. Single Step

13.5.1. Step Bit In Dcsr

This method is only available to external debuggers, and is the preferred way to single step.

An external debugger can cause a halted hart to execute a single instruction or trap and then re-enter Debug Mode by setting before resuming. If is set when a hart resumes then it will single step, regardless of the reason for resuming.

If control is transferred to a trap handler while executing the instruction, then Debug Mode is re-entered immediately after the PC is changed to the trap handler, and the appropriate `tval` and `cause` registers are updated. In this case none of the trap handler is executed, and if the cause was a pending interrupt no instructions might be executed at all.

If executing or fetching the instruction causes a trigger to fire with action=1, Debug Mode is re-entered immediately after that trigger has fired. In that case is set to 2 (trigger) instead of 4 (single step). Whether the instruction is executed or not depends on the specific configuration of the trigger.

If the instruction that is executed causes the PC to change to an address where an instruction fetch causes an exception, that exception does not occur until the next time the hart is resumed. Similarly, a trigger at the new address does not fire until the hart actually attempts to execute that instruction.

If the instruction being stepped over would normally stall the hart, then instead the instruction is treated as a `nop`. This includes `wfi`, `wrs.sto`, and `wrs.nto`.

13.5.2. Icount Trigger

Native debuggers won't have access to , but can use the trigger by setting to 1.

This approach does have some limitations:

1. Interrupts will fire as usual. Debuggers that want to disable interrupts while stepping must disable them by changing `mstatus`, and specially handle instructions that read `mstatus`.
2. `wfi` instructions are not treated specially and might take a very long time to complete.

This mechanism cleanly supports a system which supports multiple privilege levels, where the OS or a debug stub runs in M-Mode while the program being debugged runs in a less privileged mode. Systems that only support M-Mode can use as well, but count must be able to count several instructions (depending on the software implementation). See Section 9.3.1.

13.6. Reset

If the halt signal (driven by the hart's halt request bit in the Debug Module) or |hyperref [*resethaltreq*{resethaltreq}|$] are asserted when a hart comes out of reset, the hart must enter Debug Mode before executing any instructions, but after performing any initialization that would usually happen before the first instruction is executed.

13.7. Halt

When a hart halts:

1. is updated.
2. and are set to reflect current privilege mode.
3. is set to the next instruction that should be executed.
4. If the current instruction can be partially executed and should be restarted to complete, then the relevant state for that is updated. E.g. if a halt occurs during a partially executed vector instruction, then `vstart` is updated, and is updated to the address of the partially executed instruction. This is analogous to how vector instructions behave for exceptions.
5. The hart enters Debug Mode.

13.8. Resume

When a hart resumes:

1. `pc` changes to the value stored in .
2. The current privilege mode and virtualization mode are changed to that specified by and .
3. If the new privilege mode is less privileged than M-mode, $|MPRV|$ in `mstatus` is cleared.
4. The hart is no longer in debug mode.

13.9. XLEN

While in Debug Mode, XLEN is DXLEN. It is up to the debugger to determine the XLEN during normal program execution (by looking at `misa`) and to clearly communicate this to the user.

13.10. Core Debug Registers

The supported Core Debug Registers must be implemented for each hart that can be debugged. They are CSRs, accessible using the RISC-V `csr` opcodes and optionally also using abstract debug commands.

Attempts to access an unimplemented Core Debug Register raise an illegal instruction exception.

13.11. Virtual Debug Registers

Chapter 14. Sdtrig (ISA Extension)

This chapter describes the Sdtrig ISA extension, which can be implemented independently of functionality described in the other chapters. It consists exclusively of the Trigger Module ™.

Triggers can cause a breakpoint exception, entry into Debug Mode, or a trace action without having to execute a special instruction. This makes them invaluable when debugging code from ROM. They can trigger on execution of instructions at a given memory address, or on the address/data in loads/stores.

If Sdtrig is implemented, the Trigger Module must support at least one trigger. Accessing trigger CSRs that are not used by any of the implemented triggers must result in an illegal instruction exception. M-Mode and Debug Mode accesses to trigger CSRs that are used by any of the implemented triggers must succeed, regardless of the current type of the currently selected trigger.

A trigger matches when the conditions that it specifies (e.g. a load from a specific address) are met. A trigger fires when a trigger that matches performs the action configured for that trigger.

Triggers do not fire while in Debug Mode.

14.1. Enumeration

Each trigger may support a variety of features. A debugger can build a list of all triggers and their features as follows:

1. Write 0 to . If this results in an illegal instruction exception, then there are no triggers implemented.
2. Read back and check that it contains the written value. If not, exit the loop.
3. Read .
4. If that caused an exception, the debugger must read to discover the type. (If is 0, this trigger doesn't exist. Exit the loop.)
5. If is 1, this trigger doesn't exist. Exit the loop.
6. Otherwise, the selected trigger supports the types discovered in .
7. Repeat, incrementing the value in .

> – –
>
> ---
>
> ```
>  +
> The above algorithm reads back so that implementations which have
> latexmath:[$2^n$] triggers only need to implement latexmath:[$n$] bits
> of .
> ```
>
> The algorithm checks and in case the implementation has m bits of but fewer than 2^m triggers.

14.2. Actions

Triggers can be configured to take one of several actions when they fire. Table #tab:action lists all options.

|r|L| Value & Description
& Raise a breakpoint exception. (Used when software wants to use the trigger module without an external debugger attached.) `xepc` must contain the virtual address of the next instruction that must be executed to preserve the program flow.
& Enter Debug Mode. must contain the virtual address of the next instruction that must be executed to preserve the program flow.

This action is only legal when the trigger's is 1. Since the `tdata` registers are WARL, hardware should clear the action field whenever the action field is 1, the new value of would be 0, and the new value of the action field would be 1.

This action can only be supported if Sdext is implemented on the hart.
& Trace on, described in the trace specification.
& Trace off, described in the trace specification.
& Trace notify, described in the trace specification.
& Reserved for use by the trace specification.
– 9 & Send a signal to TM external trigger output 0 or 1 (respectively).
other & Reserved for future use.

> – –
>
> ```
>  +
> Actions 8 and 9 are intended to increment custom event counters, but
> these signals could also be brought to outputs for use by external
> logic.
> ```

14.3. Priority

Table #tab:priority lists the synchronous exceptions from the Privileged Spec, and where the various types of triggers fit in. The first 3 columns come from the Privileged Spec, and the final column shows where triggers fit in. Priorities in the table are separated by horizontal lines, so e.g. etrigger and itrigger have the same priority. If this table contradicts the table in the Privileged Spec, then the latter takes precedence.

This table only applies if triggers are precise. Otherwise triggers will fire some indeterminate time after the event, and the priority is irrelevant. When triggers are chained, the priority is the lowest priority of the triggers in the chain.

|l|p.7in|p2.3in|p2.5in| Priority & Exception Code & Description & Trigger
Highest & 3 & & etrigger
& 3 & & icount
& 3 & & itrigger
& 3 & & mcontrol/mcontrol6 after (on previous instruction)
& 3 & Instruction address breakpoint & mcontrol/mcontrol6 execute address before

& 12, 20, 1 & During instruction address translation: First encountered page fault, guest-page fault, or access fault &
& 1 & With physical address for instruction: Instruction access fault &
& 3 & & mcontrol/mcontrol6 execute data before
& 2 & Illegal instruction &
& 22 & Virtual instruction &
& 0 & Instruction address misaligned &
& 8, 9, 10, 11 & Environment call &
& 3 & Environment break &
& 3 & Load/Store/AMO address breakpoint & mcontrol/mcontrol6 load/store address/data before
& 4, 6 & Optionally: Load/Store/AMO address misaligned &
& 13, 15, 21, 23, 5, 7 & During address translation for an explicit memory access: First encountered page fault, guest-page fault, or access fault &
& 5, 7 & With physical address for an explicit memory access: Load/store/AMO access fault &
& 4, 6 & If not higher priority: Load/store/AMO address misaligned &
Lowest & 3 & & mcontrol/mcontrol6 load data before

When multiple triggers in the same priority fire at once, (if implemented) is set for all of them. If more than one of these triggers has then `tval` is updated in accordance with one of them, but which one is unspecified. If one of these triggers has the `enter Debug Mode'' action (1) and another trigger has the` raise a breakpoint exception" action (0), the preferred behavior is to have both actions take place. It is implementation-dependent which of the two happens first. This ensures both that the presence of an external debugger doesn't affect execution and that a trigger set by user code doesn't affect the external debugger. If this is not implemented, then the hart must enter Debug Mode and ignore the breakpoint exception. In the latter case, of the trigger whose action is 0 must still be set, giving a debugger an opportunity to handle this case. What happens with trace actions when triggers with different actions are also firing is left to the trace specification.

14.4. Native Triggers

Triggers can be used for native debugging when . If supported by the hart and desired by the debugger, triggers will often be programmed to have so that when they fire they cause a breakpoint exception to trap to a more privileged mode. That breakpoint exception can either be taken in M-mode or it can be delegated to a less privileged mode. However, it is possible for triggers to fire in the same mode that the resulting exception will be handled in.

In these cases such a trigger may cause a breakpoint exception while already in a trap handler. This might leave the hart unable to resume normal execution because state such as `mcause` and `mepc` would be overwritten.

> – –
>
> ```
>  +
> In particular, when :
> ```
>
> 1. mcontrol and mcontrol6 triggers with can cause a breakpoint exception that is taken from M-mode to M-mode (regardless of delegation).
> 2. mcontrol and mcontrol6 triggers with can cause a breakpoint exception that is

taken from S-mode to S-mode if `medeleg`[3]=1.

3. mcontrol6 triggers with can cause a breakpoint exception that is taken from VS-mode to VS-mode if `medeleg`[3]=1 and `hedeleg`[3]=1.
4. icount triggers with can cause a breakpoint exception that is taken from M-mode to M-mode (regardless of delegation).
5. icount triggers with can cause a breakpoint exception that is taken from S-mode to S-mode if `medeleg`[3]=1.
6. icount triggers with can cause a breakpoint exception that is taken from VS-mode to VS-mode if `medeleg`[3]=1 and `hedeleg`[3]=1.
7. etrigger and itrigger triggers will always be taken from a trap handler before the first instruction of the handler. If etrigger/itrigger is set to trigger on exception/interrupt X and if X is delegated to mode Y then the trigger will cause a breakpoint exception that is taken from mode Y to mode Y unless breakpoint exceptions are delegated to a more privileged mode than Y.
8. tmexttrigger triggers are asynchronous and may occur in any mode and at any time.

Harts that support triggers with should implement one of the following two solutions to solve the problem of reentrancy:

1. The hardware prevents triggers with from matching or firing while in M-mode and while $|MIE|$ in `mstatus` is 0. If `medeleg`[3]=1 then it prevents triggers with from matching or firing while in S-mode and while $|SIE|$ in `sstatus` is 0. If `medeleg`[3]=1 and `hedeleg`[3]=1 then it prevents triggers with from matching or firing while in VS-mode and while $|SIE|$ in `vsstatus` is 0.
2. and in is implemented. `medeleg`[3] is hard-wired to 0.

– –

```
 +
The first option has the limitation that interrupts might be disabled at
times when a user still might want triggers to fire. It has the benefit
that breakpoints are not required to be handled in M-mode.
```

The second option has the benefit that it only disables triggers during the trap handler, though it requires specific software support for this debug feature in the M-mode trap handlers. It can only work if breakpoints are not delegated to less privileged modes and therefore targets primarily implementations without S-mode.

Because is not accessible to S-mode, the second option can not be extended to accommodate delegation without adding additional S-mode and VS-mode CSRs.

Both options prevent etrigger and itrigger from having any effect on exceptions and interrupts that are handled in M-mode. They also prevent triggering during some initial portion of each handler. Debuggers should use other mechanisms to debug

> these cases, such as patching the handler or setting a breakpoint on the instruction after $|MIE|$ is cleared.

14.5. Memory Access Triggers

and both enable triggers on memory accesses. This section describes for both of them how certain corner cases are treated.

14.5.1. A Extension

If the A extension is supported, then triggers on loads/stores treat them as follows:

1. `lr` instructions are loads.
2. Successful `sc` instructions are stores.
3. It is unspecified whether failing `sc` instructions are stores or not.
4. Each AMO instruction is a load for the read portion of the operation. The address is always available to trigger on, although the value loaded might not be, depending on the hardware implementation.
5. Each AMO instruction is a store for the write portion of the operation. The address is always available to trigger on, although the value stored might not be, depending on the hardware implementation.

If the destination register of any load or AMO is `zero` then it is unspecified whether a data load trigger will match. Whether data store triggers match on AMOs is unspecified.

14.5.2. Combined Accesses

Some instructions lead a hart to perform multiple memory accesses. This includes vector loads and stores, as well as `cm.push` and `cm.pop` instructions. The Trigger Module should match such accesses as if they all happened individually. E.g. a vector load should be treated as if it performed multiple loads of size SEW (selected element width), and `cm.push` should be treated as if it performed multiple stores of size XLEN.

14.5.3. Cache Operations

Cache operations are infrequently performed, and code that uses them can have hard-to-find bugs. For the purposes of debug triggers, two classes of cache operations must match as stores:

1. Cache operations that enable software to maintain coherence between otherwise non-coherent implicit and explicit memory accesses.
2. Cache operations that perform block writes of constant data.

Only triggers with and will match. Since cache operations affect multiple addresses, there are multiple possible values to compare against. Implementations must implement one of the following options. From most desirable to least desirable, they are:

1. Every address from the effective address rounded down to the nearest cache block boundary (inclusive) to the effective address rounded up to the nearest cache block boundary (exclusive) is a compare value.

2. The effective address rounded down to the nearest cache block boundary is a compare value.
3. The effective address of the instruction is a compare value.

Cache operations encoded as HINTs do not match debug triggers.

> — —
>
> ```
>  +
> The above language intends to capture the trigger behavior with respect
> to the cache operations to be introduced in a forthcoming I/D
> consistency extension.
> ```
>
> For RISC-V Base Cache Management Operation ISA Extensions 1.0.1, this means the following:
>
> 1. `cbo.clean`, `cbo.flush`, and `cbo.inval` match as if they are stores because they affect consistency.
> 2. `cbo.zero` matches as if it is a store because it performs a block write of constant data.
> 3. The prefetch instructions don't match at all.

14.6. Multiple State Change Instructions

An instruction that performs multiple architectural state changes (e.g., register updates and/or memory accesses) might cause a trigger to fire at an intermediate point in its execution. As a result, architectural state changes up to that point might have been performed, while subsequent state changes, starting from the event that activated the trigger, might not have been. The definition of such an instruction will specify the order in which architectural state changes take place. Alternatively, it may state that partial execution is not allowed, implying that a mid-execution trigger must prevent any architectural state changes from occurring.

Debuggers won't be aware if an instruction has been partially executed. When they resume execution, they will execute the same instruction once more. Therefore, it's crucial that partially executing the instruction and then executing it again leaves the hart in a state closely resembling the state it would have been in if the instruction had only been executed once.

14.7. Trigger Registers

These registers are CSRs, accessible using the RISC-V `csr` opcodes and optionally also using abstract debug commands.

Almost all trigger functionality is optional. All `tdata` registers follow write-any-read-legal semantics. If a debugger writes an unsupported configuration, the register will read back a value that is supported (which may simply be a disabled trigger). This means that a debugger must always read back values it writes to `tdata` registers, unless it already knows already what is supported. Writes to one `tdata` register must not modify the contents of other `tdata` registers, nor the configuration of any trigger besides the one that is currently selected.

The combination of these rules means that a debugger cannot simply set a trigger by writing , then , etc. The current value of might not be legal with the new value of . To help with this situation, it is guaranteed that writing 0 to disables the trigger, and leaves it in a state where and can be written with any value that makes sense for any trigger type supported by this trigger.

As a result, a debugger can write any supported trigger as follows:

1. Write 0 to . (This will result in containing a non-zero value, since the register is **WARL**.)
2. Write desired values to and .
3. Write desired value to .

Code that restores CSR context of triggers that might be configured to fire in the current privilege mode must use this same sequence to restore the triggers. This avoids the problem of a partially written trigger firing at a different time than is expected.

Attempts to access an unimplemented Trigger Register raise an illegal instruction exception.

Chapter 15. Debug Transport Module (DTM) (non-ISA extension)

Debug Transport Modules provide access to the DM over one or more transports (e.g. JTAG or USB).

There may be multiple DTMs in a single hardware platform. Ideally every component that communicates with the outside world includes a DTM, allowing a hardware platform to be debugged through every transport it supports. For instance a USB component could include a DTM. This would trivially allow any hardware platform to be debugged over USB. All that is required is that the USB module already in use also has access to the Debug Module Interface.

Using multiple DTMs at the same time is not supported. It is left to the user to ensure this does not happen.

This specification defines a JTAG DTM in Section #sec:jtagdtm[7.1]. Additional DTMs may be added in future versions of this specification.

An implementation can be compatible with this specification without implementing any of this section. In that case it must be advertised as conforming to `RISC-V Debug Specification 1.0-, with custom DTM.'' If the JTAG DTM described here is implemented, it must be advertised as conforming to the` RISC-V Debug Specification 1.0-, with JTAG DTM."

15.1. JTAG Debug Transport Module

This Debug Transport Module is based around a normal JTAG Test Access Port (TAP). The JTAG TAP allows access to arbitrary JTAG registers by first selecting one using the JTAG instruction register (IR), and then accessing it through the JTAG data register (DR).

15.1.1. JTAG Background

JTAG refers to IEEE Std 1149.1-2013. It is a standard that defines test logic that can be included in an integrated circuit to test the interconnections between integrated circuits, test the integrated circuit itself, and observe or modify circuit activity during the component's normal operation. This specification uses the latter functionality. The JTAG standard defines a Test Access Port (TAP) that can be used to read and write a few custom registers, which can be used to communicate with debug hardware in a component.

15.1.2. JTAG DTM Registers

JTAG TAPs used as a DTM must have an IR of at least 5 bits. When the TAP is reset, IR must default to 00001, selecting the IDCODE instruction. A full list of JTAG registers along with their encoding is in Table #dtmTable:jtagregisters. If the IR actually has more than 5 bits, then the encodings in Table #dtmTable:jtagregisters should be extended with 0's in their most significant bits, except for the 0x1f encoding of BYPASS, which must be extended with 1's in the most significant bits. The only regular JTAG registers a debugger might use are BYPASS and IDCODE, but this specification leaves IR space for many other standard JTAG instructions. Unimplemented instructions must select the BYPASS register.

15.1.3. JTAG Connector

15.1.3.1. Recommended JTAG Connector

To make it easy to acquire debug hardware, this spec recommends a connector that is compatible with the MIPI-10 .05 inch connector specification, as described in MIPI Debug & Trace Connector Recommendations, Version 1.20, 2 July 2021.

The connector has .05 inch spacing, gold-plated male header with .016 inch thick hardened copper or beryllium bronze square posts (SAMTEC FTSH or equivalent). Female connectors are compatible $20\mu m$ gold connectors.

Viewing the male header from above (the pins pointing at your eye), a target's connector looks as it does in Table #tab:mipiten[7.1]. The function of each pin is described in Table #tab:pinout.

VREF DEBUG	1	2	TMS
GND	3	4	TCK
GND	5	6	TDO
GND or KEY	7	8	TDI
GND	9	10	nRESET

Table 8. MIPI 10-pin JTAG + nRESET Connector Diagram

|l|c|L| Essential & GND & Connected to ground.
& TCK & JTAG TCK signal, driven by the debug adapter.
& TDI & JTAG TDI signal, driven by the debug adapter.
& TDO & JTAG TDO signal, driven by the target.
& TMS & JTAG TMS signal, driven by the debug adapter.
& VREF DEBUG & Reference voltage for logic high.
Recommended & nRESET & Open drain active low reset signal, usually driven by the debug adapter. The signal may be used bi-directional to drive or sense the target reset signal.

Asserting reset should reset any RISC-V cores as well as any other peripherals on the PCB. It should not reset the debug logic. This pin is optional but strongly encouraged.

nRESET should never be connected to the TAP reset, otherwise the debugger might not be able to debug through a reset to discover the cause of a crash or to maintain execution control after the reset.
& KEY & This pin may be cut on the male and plugged on the female header to ensure the header is always plugged in correctly. It is, however, recommended to use this pin as an additional ground, to allow for fastest TCK speeds. A shrouded connector should be used to prevent the cable from being plugged in incorrectly.
Advanced & EXT & Reserved for custom use. Could be an input or an output.
& TRIGIN & Not used by this specification, to be driven by debug adapter. (Can be used for extended functions like UART or boot mode selection by some debug adapters).
& TRIGOUT & Not used by this specification, driven by the target.
Specialized & nTRST & Test reset, driven by the debug adapter. Asserting nTRST initializes the JTAG DTM asynchronously. It is used in systems where the JTAG DTM is not ready to be used after a normal power up. This signal is sometimes called TRST*.
Legacy & RTCK & Return test clock, driven by the target. A target may relay the TCK signal here once it has processed it, allowing a debugger to adjust its TCK frequency in response.

This signal should only be used to support legacy components that rely on this functionality.

& nTRST_PD & Test reset pull-down, driven by the debug adapter. Same function as nTRST, but with pull-down resistor on target.

This signal should only be used to support legacy components that rely on this functionality.

If a hardware platform requires nTRST then it is permissible to reuse the nRESET pin as the nTRST signal, resulting in a MIPI 10-pin JTAG
nTRST connector.

15.1.3.2. Alternate JTAG Connector

The MIPI-10 connector should provide plenty of signals for all modern hardware. If a design does need legacy JTAG signals, then the MIPI-20 connector should be used. Pins whose functionality isn't needed may be left unconnected.

Its physical connector is virtually identical to MIPI-10, except that it's twice as long, supporting twice as many pins. Its pinout is shown in Table #tab:mipitwenty[7.2]. The function of each pin is described in Table #tab:pinout.

VREF DEBUG	1	2	TMS
GND	3	4	TCK
GND	5	6	TDO
GND or KEY	7	8	TDI
GND	9	10	nRESET
GND	11	12	GND or RTCK
GND	13	14	NC or nTRST_PD
GND	15	16	nTRST or NC
GND	17	18	TRIGIN or NC
GND	19	20	TRIGOUT or GND

Table 9. MIPI 20-pin JTAG Connector Diagram

15.1.4. cJTAG

This spec does not have specific recommendations on how to use the cJTAG protocol.

When implementing cJTAG access to a JTAG DTM, the MIPI 10-pin Narrow JTAG connector should be used. Pins whose functionality isn't needed may be left unconnected.

Viewing the male header from above (the pins pointing at your eye), a target's connector looks as it does in Table #tab:mipicjtag[7.3].

VREF DEBUG	1	2	TMSC
GND	3	4	TCKC
GND	5	6	EXT or NC
GND or KEY	7	8	NC or nTRST_PD
GND	9	10	nRESET

Table 10. MIPI 10-pin Narrow JTAG Connector Diagram

Chapter 16. Hardware Implementations

Below are two possible implementations. A designer could choose one, mix and match, or come up with their own design.

16.1. Abstract Command Based

Halting happens by stalling the hart execution pipeline.

Muxes on the register file(s) allow for accessing GPRs and CSRs using the Access Register abstract command.

Memory is accessed using the Abstract Access Memory command or through System Bus Access.

This implementation could allow a debugger to collect information from the hart even when that hart is unable to execute instructions.

16.2. Execution Based

This implementation only implements the Access Register abstract command for GPRs on a halted hart, and relies on the Program Buffer for all other operations. It uses the hart's existing pipeline and ability to execute from arbitrary memory locations to avoid modifications to a hart's datapath.

When the halt request bit is set, the Debug Module raises a special interrupt to the selected harts. This interrupt causes each hart to enter Debug Mode and jump to a defined memory region that is serviced by the DM and is only accessible to the harts in Debug Mode. Accesses to this memory should be uncached to avoid side effects from debugging operations. When taking this jump, `pc` is saved to and is updated in . This jump is similar to a trap but it is not architecturally considered a trap, so for instance doesn't count as a trap for trigger behavior.

The code in the Debug Module causes the hart to execute a `` `park loop.'' In the park loop the hart writes its `mhartid `` to a memory location within the Debug Module to indicate that it is halted. To allow the DM to individually control one out of several halted harts, each hart polls for flags in a DM-controlled memory location to determine whether the debugger wants it to execute the Program Buffer or perform a resume.

To execute an abstract command, the DM first populates some internal words of program buffer according to . When is set, the DM populates these words with `lw <gpr>, 0x400(zero)` or `sw 0x400(zero), <gpr>`. 64- and 128-bit accesses use `ld`/`sd` and `lq`/`sq` respectively. If is not set, the DM populates these instructions as `nop`s. If is set, execution continues to the debugger-controlled Program Buffer, otherwise the DM causes a `ebreak` to execute immediately.

When `ebreak` is executed (indicating the end of the Program Buffer code) the hart returns to its park loop. If an exception is encountered, the hart jumps to an address within the Debug Module. The code there causes the hart to write to the Debug Module indicating an exception. Then the hart jumps back to the park loop. The DM infers from the write that there was an exception, and sets appropriately. Typically the hart will execute a `fence` instruction before entering the park loop, to ensure that any effects from the abstract command, such as a write to , take effect before the DM returns to 0.

To resume execution, the debug module sets a flag which causes the hart to execute a `dret`. `dret` is an instruction that only has meaning while in Debug Mode and not executing from the Program Buffer.

Its recommended encoding is 0x7b200073. When `dret` is executed, `pc` is restored from and normal execution resumes at the privilege set by and .

etc. are mapped into regular memory at an address relative to `zero` with only a 12-bit `imm`. The exact address is an implementation detail that a debugger must not rely on. For example, the `data` registers might be mapped to `0x400`.

For additional flexibility, , etc. are mapped into regular memory immediately preceding , in order to form a contiguous region of memory which can be used for either program execution or data transfer.

The PMP must not disallow fetches, loads, or stores in the address range associated with the Debug Module when the hart is in Debug Mode, regardless of how the PMP is configured. The same is true of PMA. Without this guarantee, the park loop would enter an infinite loop of traps and debug would not be possible.

16.3. Debug Module Interface Signals

As stated in section 4.1 the details of the DMI are left to the system designer. It is quite often the case that only one DTM and one DM is implemented. In this case it might be useful to comply with the signals suggested in table #tab:dmi_signals[8.1], which is the implementation used in the open-source rocket-chip RISC-V core.

The DTM can start a request when the DM sets REQ_READY to 1. When this is the case REQ_OP can be set to 1 for a read or 2 for a write request. The desired address is driven with the REQ_ADDRESS signal. Finally REQ_VALID is set high, indicating to the DM that a valid request is pending.

The DM must respond to a request from the DTM when RSP_READY is high. The status of the response is indicated by the RSP_OP signal (see). The data of the response is driven to RSP_DATA. A pending response is signalled by setting RSP_VALID.

Signal	Width	Source	Description
REQ_VALID	1	DTM	Indicates that a valid request is pending
REQ_READY	1	DM	Indicates that the DM is able to process a request
REQ_ADDRESS		DTM	Requested address
REQ_DATA	32	DTM	Requested data
REQ_OP	2	DTM	Same meaning as the field
RSP_VALID	1	DM	Indicates that a valid respond is pending
RSP_READY	1	DTM	Indicates that the DTM is able to process a respond
RSP_DATA	32	DM	Response data
RSP_OP	2	DM	Same meaning as the field

Table 11. Signals for the suggested DMI between one DTM and one DM

Chapter 17. Debugger Implementation

17.1. C Header File

github.com/riscv/riscv-debug-spec contains instructions for generating a C header file that defines macros for every field in every register/abstract command mentioned in this document.

17.2. External Debugger Implementation

This section details how an external debugger might use the described debug interface to perform some common operations on RISC-V cores using the JTAG DTM described in Section #sec:jtagdtm[7.1]. All these examples assume a 32-bit core but it should be easy to adapt the examples to 64- or 128-bit cores.

To keep the examples readable, they all assume that everything succeeds, and that they complete faster than the debugger can perform the next access. This will be the case in a typical JTAG setup. However, the debugger must always check the sticky error status bits after performing a sequence of actions. If it sees any that are set, then it should attempt the same actions again, possibly while adding in some delay, or explicit checks for status bits.

17.2.1. Debug Module Interface Access

To read an arbitrary Debug Module register, select , and scan in a value with set to 1, and set to the desired register address. In Update-DR the operation will start, and in Capture-DR its results will be captured into . If the operation didn't complete in time, will be 3 and the value in must be ignored. The busy condition must be cleared by writing in , and then the second scan scan must be performed again. This process must be repeated until returns 0. In later operations the debugger should allow for more time between Update-DR and Capture-DR.

To write an arbitrary Debug Bus register, select , and scan in a value with set to 2, and and set to the desired register address and data respectively. From then on everything happens exactly as with a read, except that a write is performed instead of the read.

It should almost never be necessary to scan IR, avoiding a big part of the inefficiency in typical JTAG use.

17.2.2. Checking for Halted Harts

A user will want to know as quickly as possible when a hart is halted (e.g. due to a breakpoint). To efficiently determine which harts are halted when there are many harts, the debugger uses the `haltsum` registers. Assuming the maximum number of harts exist, first it checks . For each bit set there, it writes |hyperref [*hartsel*{hartsel}|$], and checks . This process repeats through and . Depending on how many harts exist, the process should start at one of the lower `haltsum` registers.

17.2.3. Halting

To halt one or more harts, the debugger selects them, sets , and then waits for to indicate the harts are halted. Then it can clear to 0, or leave it high to catch a hart that resets while halted.

17.2.4. Running

First, the debugger should restore any registers that it has overwritten. Then it can let the selected harts run by setting . Once is set, the debugger knows the selected harts have resumed. Harts might halt very quickly after resuming (e.g. by hitting a software breakpoint) so the debugger cannot use /to check whether the hart resumed.

17.2.5. Single Step

Using the hardware single step feature is almost the same as regular running. The debugger just sets in before letting the hart run. The hart behaves exactly as in the running case, except that interrupts may be disabled (depending on) and it only fetches and executes a single instruction before re-entering Debug Mode.

17.2.6. Accessing Registers

17.2.6.1. Using Abstract Command

Read `s0` using abstract command:

|c|r|p0.3|p0.3| Op & Address & Value & Comment
Write & & = 2, , = 0x1008 & Read `s0`
Read & & - & Returns value that was in `s0`

Write `mstatus` using abstract command:

|c|r|p0.3|p0.3| Op & Address & Value & Comment
Write & & new value &
Write & & = 2, , , = 0x300 & Write `mstatus`

17.2.6.2. Using Program Buffer

Abstract commands are used to exchange data with GPRs. Using this mechanism, other registers can be accessed by moving their value into/out of GPRs.

Write `mstatus` using program buffer:

|c|r|p0.3|p0.3| Op & Address & Value & Comment
Write & & `csrw s0, MSTATUS` &
Write & `progbuf1` & `ebreak` &
Write & & new value &
Write & & = 2, , , , = 0x1008 & Write `s0`, then execute program buffer

Read `f1` using program buffer:

|c|r|p0.3|p0.3| Op & Address & Value & Comment
Write & & `fmv.x.s s0, f1` &
Write & `progbuf1` & `ebreak` &
Write & & & Execute program buffer
Write & & , = 0x1008 & read `s0`
Read & & - & Returns the value that was in `f1`

17.2.7. Reading Memory

17.2.7.1. Using System Bus Access

With system bus access, addresses are physical system bus addresses.

Read a word from memory using system bus access:

|c|r|p0.3|p0.3| Op & Address & Value & Comment
Write & & = 2, & Setup
Write & & address &
Read & & - & Value read from memory

Read block of memory using system bus access:

|r|r|p13em|l| Op & Address & Value & Comment
Write & & = 2, , , & Turn on autoread and autoincrement
Write & & address & Writing address triggers read and increment
Read & & - & Value read from memory
Read & & - & Next value read from memory
... & ... & ... & ...
Write & & 0 & Disable autoread
Read & & - & Get last value read from memory.

17.2.7.2. Using Program Buffer

Through the Program Buffer, the hart performs the memory accesses. Addresses are physical or virtual (depending on and other system configuration).

Read a word from memory using program buffer:

|c|r|p0.3|p0.3| Op & Address & Value & Comment
Write & & `lw s0, 0(s0)` &
Write & `progbuf1` & `ebreak` &
Write & & address &
Write & & , , , = 0x1008 & Write `s0`, then execute program buffer
Write & & = 0x1008 & Read `s0`
Read & & - & Value read from memory

Read block of memory using program buffer:

|c|r|p0.3|p0.3| Op & Address & Value & Comment
Write & & `lw s1, 0(s0)` &
Write & `progbuf1` & `addi s0, s0, 4` &
Write & `progbuf2` & `ebreak` &
Write & & address &
Write & & , , , = 0x1008 & Write `s0`, then execute program buffer
Write & & , = 0x1009 & Read `s1`, then execute program buffer
Write & & & Set
Read & & - & Get value read from memory, then execute program buffer
Read & & - & Get next value read from memory, then execute program buffer
... & ... & ... & ...
Write & & 0 & Clear

Read & & - & Get last value read from memory.

17.2.7.3. Using Abstract Memory Access

Abstract memory accesses act as if they are performed by the hart, although the actual implementation may differ.

Read a word from memory using abstract memory access:

|c|r|p0.3|p0.3| Op & Address & Value & Comment
Write & `data1`& address &
Write & & cmdtype=2, &
Read & & - & Value read from memory

Read block of memory using abstract memory access:

|c|r|p0.3|p0.3| Op & Address & Value & Comment
Write & & 1 & Re-execute the command when is accessed
Write & `data1`& address &
Write & & cmdtype=2, , &
Read & & - & Read value, and trigger reading of next address
... & ... & ... & ...
Write & & 0 & Disable auto-exec
Read & & - & Get last value read from memory.

17.2.8. Writing Memory

17.2.8.1. Using System Bus Access

With system bus access, addresses are physical system bus addresses.

Write a word to memory using system bus access:

|c|r|p0.3|p0.3| Op & Address & Value & Comment
Write & & = 2 & Configure access size
Write & & address &
Write & & value &

Write a block of memory using system bus access:

|c|r|p0.3|p0.3| Op & Address & Value & Comment
Write & & = 2, & Turn on autoincrement
Write & & address &
Write & & value0 &
Write & & value1 &
... & ... & ... & ...
Write & & valueN &

17.2.8.2. Using Program Buffer

Through the Program Buffer, the hart performs the memory accesses. Addresses are physical or virtual (depending on and other system configuration).

Write a word to memory using program buffer:

|c|r|p0.3|p0.3| Op & Address & Value & Comment
Write & & `sw s1, 0(s0)` &
Write & `progbuf1` & `ebreak` &
Write & & address &
Write & & , , = 0x1008 & Write `s0`
Write & & value &
Write & & , , , = 0x1009 & Write `s1`, then execute program buffer

Write block of memory using program buffer:

|c|r|p0.3|p0.3| Op & Address & Value & Comment
Write & & `sw s1, 0(s0)` &
Write & `progbuf1` & `addi s0, s0, 4` &
Write & `progbuf2` & `ebreak` &
Write & & address &
Write & & , , = 0x1008 & Write `s0`
Write & & value0 &
Write & & , , , = 0x1009 & Write `s1`, then execute program buffer
Write & & & Set
Write & & value1 &
... & ... & ... & ...
Write & & valueN &
Write & & 0 & Clear

17.2.8.3. Using Abstract Memory Access

Abstract memory accesses act as if they are performed by the hart, although the actual implementation may differ.

Write a word to memory using abstract memory access:

|c|r|p0.3|p0.3| Op & Address & Value & Comment
Write & `data1`& address &
Write & & value &
Write & & cmdtype=2, , write=1 &

Write a block of memory using abstract memory access:

|c|r|p0.3|p0.3| Op & Address & Value & Comment
Write & `data1`& address &
Write & & value0 &
Write & & cmdtype=2, , write=1, &
Write & & 1 & Re-execute the command when is accessed
Write & & value1 &
Write & & value2 &
... & ... & ... & ...
Write & & valueN &
Write & & 0 & Disable auto-exec

17.2.9. Triggers

A debugger can use hardware triggers to halt a hart when a certain event occurs. Below are some examples, but as there is no requirement on the number of features of the triggers implemented by a hart, these examples might not be applicable to all implementations. When a debugger wants to set a trigger, it writes the desired configuration, and then reads back to see if that configuration is supported. All examples assume XLEN=32.

Enter Debug Mode when the instruction at 0x80001234 is executed, to be used as an instruction breakpoint in ROM:

|r|r|L| & 0x6980105c & type=6, dmode=1, action=1, select=0, match=0, m=1, s=1, u=1, vs=1, vu=1, execute=1
& 0x80001234 & address

Enter Debug Mode when performing a load at address 0x80007f80 in M-mode or S-mode or U-mode:

|r|r|L| & 0x68001059 & type=6, dmode=1, action=1, select=0, match=0, m=1, s=1, u=1, load=1
& 0x80007f80 & address

Enter Debug Mode when storing to an address between 0x80007c80 and 0x80007cef (inclusive) in VS-mode or VU-mode when hgatp.VMID=1:

|r|r|L| & 0x69801902 & type=6, dmode=1, action=1, chain=1, select=0, match=2, vs=1, vu=1, store=1
& 0x80007c80 & start address (inclusive)
& 0x03000000 & mhselect=6, mhvalue=0
& 0x69801182 & type=6, dmode=1, action=1, select=0, match=3, vs=1, vu=1, store=1
& 0x80007cf0 & end address (exclusive)
& 0x03000000 & mhselect=6, mhvalue=0

Enter Debug Mode when storing to an address between 0x81230000 and 0x8123ffff (inclusive):

|r|r|L| & 0x698010da & type=6, dmode=1, action=1, select=0, match=1, m=1, s=1, u=1, vs=1, vu=1, store=1
& 0x81237fff & 16 upper bits to match exactly, then 0, then all ones.

Enter Debug Mode when loading from an address between 0x86753090 and 0x8675309f or between 0x96753090 and 0x9675309f (inclusive):

|r|r|L| & 0x69801a59 & type=6, dmode=1, action=1, chain=1, match=4, m=1, s=1, u=1, vs=1, vu=1, load=1
& 0xfff03090 & Mask for low half, then match for low half
& 0x698012d9 & type=6, dmode=1, action=1, match=5, m=1, s=1, u=1, vs=1, vu=1, load=1
& 0xefff8675 & Mask for high half, then match for high half

17.2.10. Handling Exceptions

Generally the debugger can avoid exceptions by being careful with the programs it writes. Sometimes they are unavoidable though, e.g. if the user asks to access memory or a CSR that is not implemented. A typical debugger will not know enough about the hardware platform to know what's going to happen, and must attempt the access to determine the outcome.

When an exception occurs while executing the Program Buffer, becomes set. The debugger can check this field to see whether a program encountered an exception. If there was an exception, it's left to the

debugger to know what must have caused it.

17.2.11. Quick Access

There are a variety of instructions to transfer data between GPRs and the ` data` registers. They are either loads/stores or CSR reads/writes. The specific addresses also vary. This is all specified in . The examples here use the pseudo-op `transfer dest, src` to represent all these options.

Halt the hart for a minimum amount of time to perform a single memory write:

|c|r|p0.3|p0.3| Op & Address & Value & Comment
Write & & `transfer arg2, s0` & Save `s0`
Write & `progbuf1` & `transfer s0, arg0` & Read first argument (address)
Write & `progbuf2` & `transfer arg0, s1` & Save `s1`
Write & `progbuf3` & `transfer s1, arg1` & Read second argument (data)
Write & `progbuf4` & `sw s1, 0(s0)` &
Write & `progbuf5` & `transfer s1, arg0` & Restore `s1`
Write & `progbuf6` & `transfer s0, arg2` & Restore `s0`
Write & `progbuf7` & `ebreak` &
Write & & address &
Write & `data1` & data &
Write & & 0x10000000 & Perform quick access

This shows an example of setting the bit in to enable a hardware breakpoint in M-mode. Similar quick access instructions could have been used previously to configure the trigger that is being enabled here:

|c|r|p0.3|p0.3| Op & Address & Value & Comment
Write & & `transfer arg0, s0` & Save `s0`
Write & `progbuf1` & `li s0, (1 << 6)` & Form the mask for bit
Write & `progbuf2` & `csrrs x0, , s0` & Apply the mask to
Write & `progbuf3` & `transfer s0, arg2` & Restore `s0`
Write & `progbuf4` & `ebreak` &
Write & & 0x10000000 & Perform quick access

17.3. Native Debugger Implementation

The spec contains a few features to aid in writing a native debugger. This section describes how some common tasks might be achieved.

17.3.1. Single Step

Single step is straightforward if the OS or a debug stub runs in M-Mode while the program being debugged runs in a less privileged mode. When a step is required, the OS or debug stub writes , , before returning control to the lower user program with an `mret` instruction.

Stepping code running in the same privilege mode as the debugger is more complicated, depending on what other debug features are implemented.

If hardware implements and , then stepping through non-trap code which doesn't allow for nested interrupts is also straightforward.

If hardware automatically prevents triggers from matching when entering a trap handler as described

in Section #sec:nativetrigger[6.4], then a carefully written trap handler can ensure that interrupts are disabled whenever the icount trigger must not match.

If neither of these features exist, then single step is doable, but tricky to get right. To single step, the debug stub would execute something like:

```
    li    t0, \FcsrIcountCount=4, \FcsrIcountAction=0, \FcsrIcountM=1
    csrw  tdata1, t0    /* Write the trigger. */
    lw    t0, 8(sp)     /* Restore t0, count decrements to 3 */
    lw    sp, 0(sp)     /* Restore sp, count decrements to 2 */
    mret                /* Return to program being debugged. count decrements to 1 */
```

There is an additional problem with using to single step. An instruction may cause an exception into a more privileged mode where the trigger is not enabled. The exception handler might address the cause of the exception, and then restart the instruction. Examples of this include page faults, FPU instructions when the FPU is not yet enabled, and interrupts. When a user is single stepping through such code, they will have to step twice to get past the restarted instruction. The first time the exception handler runs, and the second time the instruction actually executes. That is confusing and usually undesirable.

To help users out, debuggers should detect when a single step restarted an instruction, and then step again. This way the users see the expected behavior of stepping over the instruction. Ideally the debugger would notify the user that an exception handler executed the first time.

The debugger should perform this extra step when the PC doesn't change during a regular step.

> — —
>
> ```
>  +
> It is safe to perform an extra step when the PC changes, because every
> RISC-V instruction either changes the PC or has side effects when
> repeated, but never both.
> ```

To avoid an infinite loop if the exception handler does not address the cause of the exception, the debugger must execute no more than a single extra step.

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Chapter 18. Change Log

Chapter 19. Future Ideas

All items in this section are future ideas and should not be considered part of the specification.

Some future version of this spec may implement some of the following features.

1. The spec defines several additions to the Device Tree which enable a debugger to discover hart IDs and supported triggers for all the harts in the system.
2. DTMs can function as general bus subordinates, so they would look like regular RAM to bus managers.
3. Harts can be divided into groups. All the harts in the same group can be halted/run/stepped simultaneously. When a hart hits a breakpoint, all the other harts in the same group also halt within a few clock cycles.
4. DTMs are specified for protocols like USB, I2C, SPI, and SWD.
5. The debugger can communicate with the power manager to power cores up or down, and to query their status.
6. Serial ports can raise an interrupt when a send/receive queue becomes full/empty.
7. The debug interrupt can be masked by running code. If the interrupt is asserted, then deasserted, and then asserted again the debug interrupt happens anyway. This mechanism can be used to e.g. read/write memory with minimal interruption, making sure never to interrupt during a critical piece of code.
8. The Debug Module can include a serial interface for re-using the DTM interface as a generic communication interface.

19.1. Serial Ports

The Debug Module may implement up to 8 serial ports. They support basic flow control and full duplex data transfer between a component and the debugger, essentially allowing the Debug Transport to be used to communicate with a debug monitor running on a hart, or more generally emulate devices which aren't present. All these uses require software support, and are not further specified here. Only the DMI side of the Debug Module serial registers are defined in this specification as the core side interface should look like a peripheral device.